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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XE

Betano	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit Dual-Core
Speed	180MHz, 200MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	39
Program Memory Size	152KB (152K x 8)
Program Memory Type	FLASH, PRAM
EEPROM Size	
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 31x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ch128mp505-i-pt

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin #	Master Core	Slave Core
1	RP46/PWM1H/RB14	S1RP46/S1RB14
2	RP47/PWM1L/RB15	S1RP47 /S1RB15
3	RP60/PWM4H/RC12	S1RP60 /S1RC12
4	RP61/PWM4L/RC13	S1RP61 /S1RC13
5	RP62/RC14	S1RP62/S1PWM7H/S1RC14
6	RP63/RC15	S1RP63/S1PWM7L/S1RC15
7	MCLR	_
8	PCI22/RD15	S1PCI22/S1RD15
9	Vss	Vss
10	VDD	VDD
11	PCI21/RD14	S1ANN1/S1PGA2N2/S1PCI21/S1RD14
12	RD13	S1ANN0/S1PGA1N2/S1RD13
13	AN12/IBIAS3/RP48/RC0	S1AN10/ S1RP48 /S1RC0
14	AN0/CMP1A/RA0	S1RA0
15	AN1/RA1	S1AN15/S1RA1
16	AN2/RA2	S1AN16/S1RA2
17	AN3/IBIAS0/RA3	S1AN0/S1CMP1A/S1PGA1P1/S1RA3
18	AN4/IBIAS1/RA4	S1MCLR3/S1AN1/S1CMP2A/S1PGA2P1/S1PGA3P2/S1RA4
19	AVDD	AVDD
20	AVss	AVss
21	RD12	S1AN14/S1PGA2P2/S1RD12
22	AN13/ISRC0/ RP49 /RC1	S1ANA1/ S1RP49 /S1RC1
23	AN14/ISRC1/ RP50 /RC2	S1ANA0/ S1RP50 /S1RC2
24	RP54 /RC6	S1AN11/S1CMP1B/ S1RP54 /S1RC6
25	Vdd	VDD
26	Vss	Vss
27	CMP1B/ RP51 /RC3	S1AN8/S1CMP3B/ S1RP51 /S1RC3
28	OSCI/CLKI/AN5/RP32/RB0	S1AN5/ S1RP32 /S1RB0
29	OSCO/CLKO/AN6/IBIAS2/RP33/RB1	S1AN4/ S1RP33 /S1RB1
30	RD11	S1AN17/S1PGA1P2/S1RD11
31	ISRC3/RD10	S1AN13/S1CMP2B/S1RD10
32	AN15/ISRC2/ RP55 /RC7	S1AN12/ S1RP55 /S1RC7
33	DACOUT/AN7/CMP1D/ RP34 /INT0/RB2	S1MCLR2/S1AN3/S1ANC0/S1ANC1/S1CMP1D/S1CMP2D/S1CMP3D/S1RP34/ S1INT0/S1RB2
34	PGD2/AN8/ RP35 /RB3	S1PGD2/S1AN18/S1CMP3A/S1PGA3P1/S1RP35/S1RB3
35	PGC2/ RP36 /RB4	S1PGC2/S1AN9/S1RP36/S1PWM5L/S1RB4
36	RP56/ASDA1/SCK2/RC8	S1RP56/S1ASDA1/S1SCK1/S1RC8
37	RP57/ASCL1/SDI2/RC9	S1RP57/S1ASCL1/S1SDI1/S1RC9
38	PCI20/RD9	S1PCI20/S1RD9
39	SDO2/PCI19/RD8	S1SDO1/S1PCI19/S1RD8
40	Vss	Vss
41	VDD	VDD
42	RP71 /RD7	S1RP71 /S1PWM8H/S1RD7
43	RP70 /RD6	S1RP70 /S1PWM6H/S1RD6
44	RP69/RD5	S1RP69/S1PWM6L/S1RD5
45	PGD3/ RP37 /SDA2/RB5	S1PGD3/ S1RP37 /S1RB5
46	PGC3/RP38/SCL2/RB6	S1PGC3/ S1RP38 /S1RB6
47	TDO/AN9/ RP39 /RB7	S1MCLR1/S1AN6/S1RP39/S1PWM5H/S1RB7
48	PGD1/AN10/ RP40 /SCL1/RB8	S1PGD1/S1AN7/S1RP40/S1SCL1/S1RB8
49	PGC1/AN11/ RP41 /SDA1/RB9	S1PGC1/ S1RP41 /S1SDA1/S1RB9
50	RP52 /RC4	S1RP52 /S1PWM2H/S1RC4

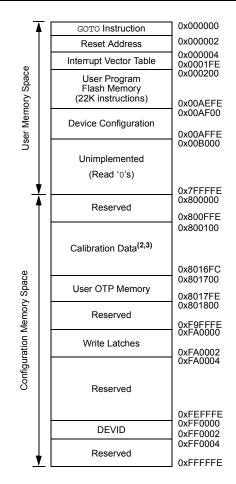
TABLE 8: 64-PIN TQFP/QFN

Legend: RPn and S1RPn represent remappable pins for Peripheral Pin Select functions.

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Note 1: Memory areas are not shown to scale.

- 2: Calibration data area must be maintained during programming.
- 3: Calibration data area includes UDID locations.

3.3.3.1 ECC Fault Injection

To test Fault handling, an EEC error can be generated. Both single and double-bit errors can be generated in both the read and write data paths. Read path Fault injection first reads the Flash data and then modifies it prior to entering the ECC logic. Write path Fault injection modifies the actual data prior to it being written into the target Flash and will cause an EEC error on subsequent Flash read. The following procedure is used to inject a Fault:

- 1. Load Flash target address into the ECCADDR register.
- Select 1st Fault bit determined by FLT1PTRx (ECCCONH<7:0>). The target bit is inverted to create the Fault.
- If a double Fault is desired, select the 2nd Fault bit determined by FLT2PTRx (ECCCONH<15:8>), otherwise set to all '1's.
- 4. Write the NVMKEY unlock sequence.
- 5. Enable the ECC Fault injection logic by setting the FLTINJ bit (ECCCONL<0>)
- 6. Perform a read or write to the Flash target address.

3.3.4 CONTROL REGISTERS

Five SFRs are used to write and erase the Program Flash Memory: NVMCON, NVMKEY, NVMADR, NVMADRU and NVMSRCADRL/H.

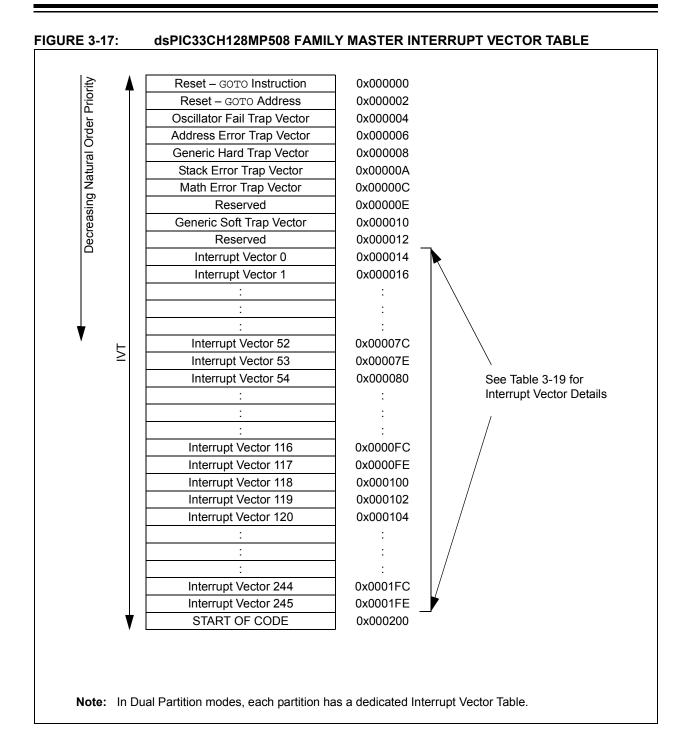
The NVMCON register (Register 3-4) selects the operation to be performed (page erase, word/row program, Inactive Partition erase) and initiates the program or erase cycle.

NVMKEY (Register 3-7) is a write-only register that is used for write protection. To start a programming or erase sequence, the user application must consecutively write 0x55 and 0xAA to the NVMKEY register.

There are two NVM Address registers: NVMADR and NVMADRU. These two registers, when concatenated, form the 24-bit Effective Address (EA) of the selected word/row for programming operations, or the selected page for erase operations. The NVMADRU register is used to hold the upper 8 bits of the EA, while the NVMADR register is used to hold the lower 16 bits of the EA.

For row programming operation, data to be written to Program Flash Memory is written into data memory space (RAM) at an address defined by the NVMSRCADRL/H register (location of first element in row programming data).

dsPIC33CH128MP508 FAMILY



| R/W-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| ICM3R7 | ICM3R6 | ICM3R5 | ICM3R4 | ICM3R3 | ICM3R2 | ICM3R1 | ICM3R0 |
| bit 15 | | • | | | | • | bit 8 |
| | | | | | | | |
| R/W-0 |
TCKI3R7	TCKI3R6	TCKI3R5	TCKI3R4	TCKI3R3	TCKI3R2	TCKI3R1	TCKI3R0
bit 7			•	•			bit 0
Legend:							

REGISTER 3-41: RPINR5: PERIPHERAL PIN SELECT INPUT REGISTER 5

Legena:			
R = Readable bit	W = Writable bit	U = Unimplemented bit,	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 ICM3R<7:0>: Assign SCCP Capture 3 (ICM3) Input to the Corresponding RPn Pin bits See Table 3-30.

bit 7-0 **TCKI3R<7:0>:** Assign SCCP Timer3 (TCKI3) Input to the Corresponding RPn Pin bits See Table 3-30.

REGISTER 3-42: RPINR6: PERIPHERAL PIN SELECT INPUT REGISTER 6

| R/W-0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| ICM4R7 | ICM4R6 | ICM4R5 | ICM4R4 | ICM4R3 | ICM4R2 | ICM4R1 | ICM4R0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| TCKI4R7 | TCKI4R6 | TCKI4R5 | TCKI4R4 | TCKI4R3 | TCKI4R2 | TCKI4R1 | TCKI4R0 |
| bit 7 | | | | | | | bit 0 |

Legend:					
R = Readable bit	W = Writable bit	U = Unimplemented bit,	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-8 ICM4R<7:0>: Assign SCCP Capture 4 (ICM4) Input to the Corresponding RPn Pin bits See Table 3-30.

bit 7-0 **TCKI4R<7:0>:** Assign SCCP Timer4 (TCKI4) Input to the Corresponding RPn Pin bits See Table 3-30.

| R/W-0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| OCFBR7 | OCFBR6 | OCFBR5 | OCFBR4 | OCFBR3 | OCFBR2 | OCFBR1 | OCFBR0 |
| bit 15 | | | | | | | bit 8 |
| | | | | | | | |

REGISTER 3-47: RPINR11: PERIPHERAL PIN SELECT INPUT REGISTER 11

| R/W-0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| OCFAR7 | OCFAR6 | OCFAR5 | OCFAR4 | OCFAR3 | OCFAR2 | OCFAR1 | OCFAR0 |
| bit 7 | | | | | | | bit 0 |

Legend:					
R = Readable bit	W = Writable bit	U = Unimplemented bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-8 **OCFBR<7:0>:** Assign SCCP Fault B (OCFB) Input to the Corresponding RPn Pin bits See Table 3-30.

bit 7-0 **OCFAR<7:0>:** Assign SCCP Fault A (OCFA) Input to the Corresponding RPn Pin bits See Table 3-30.

REGISTER 3-48: RPINR12: PERIPHERAL PIN SELECT INPUT REGISTER 12

| R/W-0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| PCI9R7 | PCI9R6 | PCI9R5 | PCI9R4 | PCI9R3 | PCI9R2 | PCI9R1 | PCI9R0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| PCI8R7 | PCI8R6 | PCI8R5 | PCI8R4 | PCI8R3 | PCI8R2 | PCI8R1 | PCI8R0 |
| bit 7 | | | | | | | bit 0 |

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	1 as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **PCI9R<7:0>:** Assign PWM Input 9 (PCI9) to the Corresponding RPn Pin bits See Table 3-30.

bit 7-0 **PCI8R<7:0>:** Assign PWM Input 8 (PCI8) to the Corresponding RPn Pin bits See Table 3-30.

U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
_	—	—	TXQCI4 ⁽¹⁾	TXQCI3 ⁽¹⁾	TXQCI2 ⁽¹⁾	TXQCI1 ⁽¹⁾	TXQCI0 ⁽¹
bit 15			·				bit
R-0	R-0	R-0	HS/C-0	U-0	R-1	U-0	R-1
TXABT ⁽²⁾	TXLARB	TXERR	TXATIF		TXQEIF	—	TXQNIF
bit 7							bit
Legend:		HS = Hardwar	e Settable bit	C = Clearable	hit		
R = Readable	≏ hit	W = Writable b			nented bit, read	1 as '0'	
-n = Value at		'1' = Bit is set		'0' = Bit is cle		x = Bit is unkr	NOWD
ii valao at							
bit 15-13	Unimplemer	nted: Read as 'o)'				
bit 12-8	-	: Transmit Mess		dex bits ⁽¹⁾			
		s register will ret			that the FIFO v	vill next attemp	t to transmi
bit 7		sage Aborted S				· · · · ·	
	1 = Message						
		was aborted					
	Ų	e completed such	cessfully				
bit 6	0 = Message		•	bit			
bit 6	0 = Message TXLARB: Me 1 = Message	e completed such essage Lost Arb e lost arbitration	itration Status while being se	nt			
bit 6	0 = Message TXLARB: Me 1 = Message 0 = Message	e completed suce essage Lost Arb e lost arbitration e did not lose arb	itration Status while being se pitration while I	nt peing sent			
	0 = Message TXLARB: Me 1 = Message 0 = Message TXERR: Erro	e completed suce essage Lost Arb e lost arbitration e did not lose arb or Detected Duri	itration Status while being se pitration while t ng Transmissio	nt peing sent on bit			
	0 = Message TXLARB: Me 1 = Message 0 = Message TXERR: Erro 1 = A bus err	e completed suce essage Lost Arb e lost arbitration e did not lose arb or Detected Duri ror occurred whi	itration Status while being se pitration while t ng Transmission le the message	nt being sent on bit e was being se			
bit 5	0 = Message TXLARB: Me 1 = Message 0 = Message TXERR: Error 1 = A bus err 0 = A bus err	e completed succ essage Lost Arb e lost arbitration e did not lose arb or Detected Duri ror occurred whi ror did not occur	itration Status while being se pitration while b ng Transmissio le the messag while the mes	nt being sent on bit e was being se ssage was beir	ig sent		
bit 5	0 = Message TXLARB: Me 1 = Message 0 = Message TXERR: Erro 1 = A bus err 0 = A bus err TXATIF: Tran	e completed suce essage Lost Arb e lost arbitration e did not lose arb or Detected Duri ror occurred whi ror did not occur nsmit Attempts E	itration Status while being se pitration while b ng Transmissio le the messag while the mes	nt being sent on bit e was being se ssage was beir	ig sent		
bit 5	0 = Message TXLARB: Me 1 = Message 0 = Message TXERR: Erro 1 = A bus err 0 = A bus err TXATIF: Trar 1 = Interrupt	e completed suce essage Lost Arb e lost arbitration e did not lose arb or Detected Duri ror occurred whi ror did not occur nsmit Attempts E is pending	itration Status while being se pitration while b ng Transmissio le the messag while the mes	nt being sent on bit e was being se ssage was beir	ig sent		
bit 5 bit 4	0 = Message TXLARB: Me 1 = Message 0 = Message TXERR: Erro 1 = A bus err 0 = A bus err TXATIF: Tran 1 = Interrupt 0 = Interrupt	e completed suce essage Lost Arb e lost arbitration e did not lose arb or Detected Duri for occurred whi for did not occur nsmit Attempts E is pending is not pending	itration Status while being se pitration while I ng Transmissio le the messag while the mess Exhausted Inte	nt being sent on bit e was being se ssage was beir	ig sent		
bit 5 bit 4 bit 3	0 = Message TXLARB: Me 1 = Message 0 = Message TXERR: Error 1 = A bus err 0 = A bus err TXATIF: Trar 1 = Interrupt 0 = Interrupt Unimplemer	e completed succ essage Lost Arb e lost arbitration e did not lose arb or Detected Duri ror occurred whi ror did not occur nsmit Attempts B is pending is not pending nted: Read as '0	itration Status while being se pitration while I ng Transmission le the message while the mess Exhausted Inte	nt being sent on bit e was being se sage was bein rrupt Pending	ig sent		
bit 5 bit 4 bit 3	0 = Message TXLARB: Me 1 = Message 0 = Message TXERR: Erro 1 = A bus err 0 = A bus err TXATIF: Trar 1 = Interrupt 0 = Interrupt Unimplemer TXQEIF: Tra	e completed succ essage Lost Arb e lost arbitration e did not lose arb or Detected Duri for occurred whi for did not occur hsmit Attempts B is pending is not pending nted: Read as '0 nsmit Queue Er	itration Status while being se pitration while I ng Transmission le the message while the mess Exhausted Inte	nt being sent on bit e was being se sage was bein rrupt Pending	ig sent		
bit 5 bit 4 bit 3	0 = Message TXLARB: Me 1 = Message 0 = Message TXERR: Erro 1 = A bus err 0 = A bus err TXATIF: Trar 1 = Interrupt 0 = Interrupt Unimplemer TXQEIF: Tra 1 = TXQ is er	e completed succ essage Lost Arb e lost arbitration e did not lose arb or Detected Duri ror occurred whi ror did not occur nsmit Attempts E is pending is not pending nted: Read as '0 nsmit Queue Er mpty	itration Status while being se bitration while I ng Transmissio le the messag while the mess Exhausted Inte o' npty Interrupt I	nt being sent on bit e was being se sage was bein rrrupt Pending	ıg sent bit		
bit 5 bit 4 bit 3 bit 2	0 = Message TXLARB: Me 1 = Message 0 = Message TXERR: Error 1 = A bus err 0 = A bus err TXATIF: Trar 1 = Interrupt 0 = Interrupt Unimplemen TXQEIF: Tra 1 = TXQ is en 0 = TXQ is m	e completed succ essage Lost Arb e lost arbitration e did not lose arb or Detected Duri for occurred whi for did not occur hsmit Attempts B is pending is not pending nted: Read as '0 nsmit Queue Er	itration Status while being se pitration while b ng Transmissio le the messag while the mess Exhausted Inte by npty Interrupt P st one messag	nt being sent on bit e was being se sage was bein rrrupt Pending	ıg sent bit		
bit 5 bit 4 bit 3 bit 2 bit 1	0 = Message TXLARB: Me 1 = Message 0 = Message TXERR: Error 1 = A bus err 0 = A bus err TXATIF: Trar 1 = Interrupt 0 = Interrupt Unimplemer TXQEIF: Tra 1 = TXQ is er 0 = TXQ is not	e completed succ essage Lost Arb e lost arbitration e did not lose arb or Detected Duri for occurred whi for did not occur nsmit Attempts E is pending is not pending nted: Read as '0 nsmit Queue Er mpty ot empty, at lease	itration Status while being se pitration while I ng Transmission le the message while the mess Exhausted Inte p ⁷ npty Interrupt I st one messag	nt being sent on bit e was being se sage was bein rrupt Pending Flag bit e is queued to	ıg sent bit		
bit 6 bit 5 bit 4 bit 3 bit 2 bit 1 bit 1 bit 0	0 = Message TXLARB: Me 1 = Message 0 = Message TXERR: Error 1 = A bus err 0 = A bus err TXATIF: Trar 1 = Interrupt 0 = Interrupt Unimplemer TXQEIF: Tra 1 = TXQ is er 0 = TXQ is not	e completed succ essage Lost Arb e lost arbitration e did not lose arb or Detected Duri for occurred whi for did not occur nsmit Attempts B is pending is not pending nted: Read as '0 nsmit Queue Er mpty ot empty, at leas nted: Read as '0 nsmit Queue No	itration Status while being se pitration while I ng Transmission le the message while the mess Exhausted Inte p ⁷ npty Interrupt I st one messag	nt being sent on bit e was being se sage was bein rrupt Pending Flag bit e is queued to	ıg sent bit		

REGISTER 3-132: C1TXQSTA: CAN TRANSMIT QUEUE STATUS REGISTER

deep (FSIZE<4:0> = 3), TXQCIx will take on a value of 0 to 3, depending on the state of the TXQ.

2: This bit is updated when a message completes (or aborts) or when the TXQ is reset.

REGISTER 3-178: ADTRIGNL AND ADTRIGNH: ADC CHANNEL TRIGGER n(x) SELECTION REGISTERS LOW AND HIGH (x = 0 TO 19; n = 0 TO 4) (CONTINUED)

bit 4-0 TRGSRCx<4:0>: Common Interrupt Enable for Corresponding Analog Input bits (TRGSRCx0 to TRGSRCx20 - Even) 11111 = ADTRG31 (PPS input) 11110 = Master PTG 11101 = Slave CLC1 11100 = Master CLC1 11011 = Slave PWM8 Trigger 2 11010 = Slave PWM5 Trigger 2 11001 = Slave PWM3 Trigger 2 11000 = Slave PWM1 Trigger 2 10111 = Master SCCP4 PWM interrupt 10110 = Master SCCP3 PWM interrupt 10101 = Master SCCP2 PWM interrupt 10100 = Master SCCP2 PWM interrupt 10011 = Reserved 10010 = Reserved 10001 = Reserved 10000 = Reserved 01111 = Reserved 01110 = Reserved 01101 = Reserved 01100 = Reserved 01011 = Master PWM4 Trigger 2 01010 = Master PWM4 Trigger 1 01001 = Master PWM3 Trigger 2 01000 = Master PWM3 Trigger 1 00111 = Master PWM2 Trigger 2 00110 = Master PWM2 Trigger 1 00101 = Master PWM1 Trigger 2 00100 = Master PWM1 Trigger 1 00011 = Reserved 00010 = Level software trigger 00001 = Common software trigger 00000 = No trigger is enabled

REGISTER 3-189: PTGT1LIM: PTG TIMER1 LIMIT REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGT1L	-IM<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGT1	LIM<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable bit		U = Unimpleme	ented bit, rea	d as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is clear	red	x = Bit is unk	nown

bit 15-0 **PTGT1LIM<15:0>:** PTG Timer1 Limit Register bits General Purpose Timer1 Limit register.

Note 1: These bits are read-only when the module is executing Step commands.

REGISTER 3-190: PTGSDLIM: PTG STEP DELAY LIMIT REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGSDI	_IM<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGSD	LIM<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable bit		U = Unimpler	nented bit, read	l as '0'	

bit 15-0 **PTGSDLIM<15:0>:** PTG Step Delay Limit Register bits This register holds a PTG Step delay value representing the number of additional PTG clocks between the start of a Step command and the completion of a Step command.

'0' = Bit is cleared

Note 1: These bits are read-only when the module is executing Step commands.

'1' = Bit is set

-n = Value at POR

x = Bit is unknown

4.2.2 DATA ADDRESS SPACE (SLAVE)

The dsPIC33CH128MP508S1 family CPU has a separate 16-bit wide data memory space. The Data Space is accessed using separate Address Generation Units (AGUs) for read and write operations. The data memory map is shown in Figure 4-5.

All Effective Addresses (EAs) in the data memory space are 16 bits wide and point to bytes within the Data Space. This arrangement gives a base Data Space address range of 64 Kbytes or 32K words.

The lower half of the data memory space (i.e., when EA<15> = 0) is used for implemented memory addresses, while the upper half (EA<15> = 1) is reserved for the Program Space Visibility (PSV).

The dsPIC33CH128MP508S1 family devices implement up to 4 Kbytes of data memory. If an EA points to a location outside of this area, an all-zero word or byte is returned.

4.2.2.1 Data Space Width

The data memory space is organized in byteaddressable, 16-bit wide blocks. Data is aligned in data memory and registers as 16-bit words, but all Data Space EAs resolve to bytes. The Least Significant Bytes (LSBs) of each word have even addresses, while the Most Significant Bytes (MSBs) have odd addresses.

4.2.2.2 Data Memory Organization and Alignment

To maintain backward compatibility with PIC[®] MCU devices and improve Data Space memory usage efficiency, the dsPIC33CH128MP508S1 family instruction set supports both word and byte operations. As a consequence of byte accessibility, all Effective Address calculations are internally scaled to step through wordaligned memory. For example, the core recognizes that Post-Modified Register Indirect Addressing mode [Ws++] results in a value of Ws + 1 for byte operations and Ws + 2 for word operations.

A data byte read, reads the complete word that contains the byte, using the LSb of any EA to determine which byte to select. The selected byte is placed onto the LSB of the data path. That is, data memory and registers are organized as two parallel, byte-wide entities with shared (word) address decode, but separate write lines. Data byte writes only write to the corresponding side of the array or register that matches the byte address. All word accesses must be aligned to an even address. Misaligned word data fetches are not supported, so care must be taken when mixing byte and word operations, or translating from 8-bit MCU code. If a misaligned read or write is attempted, an address error trap is generated. If the error occurred on a read, the instruction underway is completed. If the error occurred on a write, the instruction is executed but the write does not occur. In either case, a trap is then executed, allowing the system and/or user application to examine the machine state prior to execution of the address Fault.

All byte loads into any W register are loaded into the LSB; the MSB is not modified.

A Sign-Extend (SE) instruction is provided to allow user applications to translate 8-bit signed data to 16-bit signed values. Alternatively, for 16-bit unsigned data, user applications can clear the MSB of any W register by executing a Zero-Extend (ZE) instruction on the appropriate address.

4.2.2.3 SFR Space

The first 4 Kbytes of the Near Data Space, from 0x0000 to 0x0FFF, is primarily occupied by Special Function Registers (SFRs). These are used by the dsPIC33CH128MP508S1 family core and peripheral modules for controlling the operation of the device.

SFRs are distributed among the modules that they control and are generally grouped together by module. Much of the SFR space contains unused addresses; these are read as '0'.

Note: The actual set of peripheral features and interrupts varies by the device. Refer to the corresponding device tables and pinout diagrams for device-specific information.

4.2.2.4 Near Data Space

The 8-Kbyte area, between 0x0000 and 0x1FFF, is referred to as the Near Data Space. Locations in this space are directly addressable through a 13-bit absolute address field within all memory direct instructions. Additionally, the whole Data Space is addressable using MOV instructions, which support Memory Direct Addressing mode with a 16-bit address field, or by using Indirect Addressing mode using a Working register as an Address Pointer.

4.2.5.3 Move and Accumulator Instructions

Move instructions, and the DSP accumulator class of instructions, provide a greater degree of addressing flexibility than other instructions. In addition to the addressing modes supported by most MCU instructions, move and accumulator instructions also support Register Indirect with Register Offset Addressing mode, also referred to as Register Indexed mode.

Note:	For the MOV instructions, the addressing mode specified in the instruction can differ for the source and destination EA. How- ever, the 4-bit Wb (Register Offset) field is
	shared by both source and destination (but
	typically only used by one).

In summary, the following addressing modes are supported by move and accumulator instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- Register Indirect with Register Offset (Indexed)
- Register Indirect with Literal Offset
- 8-Bit Literal
- 16-Bit Literal
- Note: Not all instructions support all the addressing modes given above. Individual instructions may support different subsets of these addressing modes.

4.2.5.4 MAC Instructions

The dual source operand DSP instructions (CLR, ED, EDAC, MAC, MPY, MPY. N, MOVSAC and MSC), also referred to as MAC instructions, use a simplified set of addressing modes to allow the user application to effectively manipulate the Data Pointers through register indirect tables.

The two-source operand prefetch registers must be members of the set {W8, W9, W10, W11}. For data reads, W8 and W9 are always directed to the X RAGU, and W10 and W11 are always directed to the Y AGU. The Effective Addresses generated (before and after modification) must therefore, be valid addresses within X Data Space for W8 and W9, and Y Data Space for W10 and W11.

Note: Register Indirect with Register Offset Addressing mode is available only for W9 (in X space) and W11 (in Y space).

In summary, the following addressing modes are supported by the ${\tt MAC}$ class of instructions:

- Register Indirect
- Register Indirect Post-Modified by 2
- Register Indirect Post-Modified by 4
- Register Indirect Post-Modified by 6
- Register Indirect with Register Offset (Indexed)

4.2.5.5 Other Instructions

Besides the addressing modes outlined previously, some instructions use literal constants of various sizes. For example, BRA (branch) instructions use 16-bit signed literals to specify the branch destination directly, whereas the DISI instruction uses a 14-bit unsigned literal field. In some instructions, such as ULNK, the source of an operand or result is implied by the opcode itself. Certain operations, such as a NOP, do not have any operands.

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	—	RP33R5	RP33R4	RP33R3	RP33R2	RP33R1	RP33R0
bit 15							bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP32R5	RP32R4	RP32R3	RP32R2	RP32R1	RP32R0
bit 7							bit 0
Legend:							
R = Readable I	hit	W = Writable	hit	II = I Inimpler	mented hit read	as '0'	

REGISTER 4-60: RPOR0: PERIPHERAL PIN SELECT OUTPUT REGISTER 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit,	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14	Unimplemented: Read as '0'
bit 13-8	RP33R<5:0>: Peripheral Output Function is Assigned to S1RP33 Output Pin bits (see Table 4-31 for peripheral function numbers)
bit 7-6	Unimplemented: Read as '0'
bit 5-0	RP32R<5:0>: Peripheral Output Function is Assigned to S1RP32 Output Pin bits (see Table 4-31 for peripheral function numbers)

REGISTER 4-61: RPOR1: PERIPHERAL PIN SELECT OUTPUT REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP35R5	RP35R4	RP35R3	RP35R2	RP35R1	RP35R0
bit 15							bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP34R5	RP34R4	RP34R3	RP34R2	RP34R1	RP34R0
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	nented bit, read	as '0'	

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-14 Unimplemented: Read as '0'

- bit 13-8 **RP35R<5:0>:** Peripheral Output Function is Assigned to S1RP35 Output Pin bits (see Table 4-31 for peripheral function numbers)
- bit 7-6 Unimplemented: Read as '0'
- bit 5-0 **RP34R<5:0>:** Peripheral Output Function is Assigned to S1RP34 Output Pin bits (see Table 4-31 for peripheral function numbers)

4.8.3 PGA CONTROL REGISTERS

REGISTER 4-112: PGAxCON: PGAx CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PGAEN	PGAOEN	SELPI2	SELPI1	SELPI0	SELNI2	SELNI1	SELNI0
bit 15	·				•		bit 8
U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	HIGAIN		GAIN2	GAIN1	GAIN0
bit 7							bit 0
Legend:							
R = Readable		W = Writable		-	mented bit, read		
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	IOWN
bit 15	PGAEN: PGA						
		dule is enableo dule is disable		wer consumpti	ion)		
bit 14		GAx Output En					
		tput is connected		OUT pin			
		put is not conn					
bit 13-11	SELPI<2:0>:	PGAx Positive	Input Selecti	on bits			
	111 = Reserv	ved					
	110 = Reserv						
	101 = Reserv 100 = Reserv						
	011 = Ground						
	010 = Ground	b					
	001 = S1PGA						
hit 10 0	000 = S1PGA		a Input Salaa	tion hito			
bit 10-8	111 = Reserv	PGAx Negativ	e input Selec	LION DILS			
	110 = Reserv						
	101 = Reserv	ved					
	100 = Reserv						
	011 = Ground 010 = Reserv	d (Single-Ende	d mode)				
	001 = S1PGA						
	000 = Ground	d (Single-Ende	d mode)				
bit 7-5	Unimplemen	ted: Read as '	0'				
bit 4	HIGAIN: High	n-Gain Select b	it				
	This bit, wher	n asserted, ena	bles a 50% in	crease in gain	as specified by	the GAIN<2:0>	> bits.
bit 3	Unimplemen	ted: Read as '	0'				
bit 2-0	GAIN<2:0>: F	PGAx Gain Sel	ection bits				
	111 = Reserv						
	110 = Reserv						
	101 = Gain o 100 = Gain o						
	011 = Gain of						
	010 = Gain o t						
	001 = Reserv						
	000 = Reserv	ed					

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—		—	—	—	—	—	—
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTB8EN	CTB7EN	CTB6EN	CTB5EN	CTB4EN	CTB3EN	CTB2EN	CTB1EN
bit 7							bit 0
Legend:	. 1.4		1.11			(0)	
R = Readable		W = Writable		-	mented bit, read		
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unk	nown
bit 15-8	Unimplomon	ited: Read as '	· ^ '				
bit 7	-			M Concreter t	#8 as Source for	Combinations	l Trigger P bit
			•		Combinatorial Ti		
	0 = Disabled		Si Signal to be				
hit 6						~ · · · ·	
bit 6	CIB/EN: EN	able Trigger O	utput from PW	/M Generator #	#7 as Source for	Combinationa	I Trigger B bit
טונ ס			-		#7 as Source for Combinatorial Ti		
טון ס	1 = Enables 0 = Disabled	specified trigge	er signal to be	OR'd into the	Combinatorial Ti	rigger B signal	
bit 5	1 = Enables 0 = Disabled CTB6EN: En	specified trigge able Trigger O	er signal to be utput from PW	OR'd into the /M Generator #	Combinatorial Tr #6 as Source for	rigger B signal Combinationa	l Trigger B bit
	1 = Enables 0 = Disabled CTB6EN: En 1 = Enables	specified trigge able Trigger O specified trigge	er signal to be utput from PW	OR'd into the /M Generator #	Combinatorial Ti	rigger B signal Combinationa	l Trigger B bit
bit 5	1 = Enables 0 = Disabled CTB6EN: En 1 = Enables 0 = Disabled	specified trigge able Trigger O specified trigge	er signal to be utput from PW er signal to be	OR'd into the /M Generator # OR'd into the	Combinatorial Tr #6 as Source for Combinatorial Tr	rigger B signal Combinationa rigger B signal	l Trigger B bit
	1 = Enables 0 = Disabled CTB6EN: En 1 = Enables 0 = Disabled CTB5EN: En	specified trigge able Trigger O specified trigge able Trigger O	er signal to be utput from PW er signal to be utput from PW	OR'd into the /M Generator # OR'd into the /M Generator #	Combinatorial Ti #6 as Source for Combinatorial Ti #5 as Source for	rigger B signal Combinationa rigger B signal Combinationa	l Trigger B bit I Trigger B bit
bit 5	1 = Enables 0 = Disabled CTB6EN: En 1 = Enables 0 = Disabled CTB5EN: En	specified trigge able Trigger O specified trigge able Trigger O specified trigge	er signal to be utput from PW er signal to be utput from PW	OR'd into the /M Generator # OR'd into the /M Generator #	Combinatorial Tr #6 as Source for Combinatorial Tr	rigger B signal Combinationa rigger B signal Combinationa	l Trigger B bit I Trigger B bit
bit 5	1 = Enables 0 = Disabled CTB6EN: En 1 = Enables 0 = Disabled CTB5EN: En 1 = Enables 0 = Disabled	specified trigge able Trigger O specified trigge able Trigger O specified trigge	er signal to be utput from PW er signal to be utput from PW er signal to be	OR'd into the /M Generator # OR'd into the /M Generator # OR'd into the	Combinatorial Ti #6 as Source for Combinatorial Ti #5 as Source for	rigger B signal Combinationa rigger B signal Combinationa rigger B signal	l Trigger B bit I Trigger B bit
bit 5 bit 4	 1 = Enables 0 = Disabled CTB6EN: En 1 = Enables 0 = Disabled CTB5EN: En 1 = Enables 0 = Disabled CTB4EN: En 	specified trigge able Trigger O specified trigge able Trigger O specified trigge able Trigger O	er signal to be utput from PW er signal to be utput from PW er signal to be utput from PW	OR'd into the /M Generator # OR'd into the /M Generator # OR'd into the /M Generator #	Combinatorial Ti #6 as Source for Combinatorial Ti #5 as Source for Combinatorial Ti	rigger B signal Combinationa rigger B signal Combinationa rigger B signal Combinationa	I Trigger B bit I Trigger B bit I Trigger B bit
bit 5 bit 4	 1 = Enables 0 = Disabled CTB6EN: En 1 = Enables 0 = Disabled CTB5EN: En 1 = Enables 0 = Disabled CTB4EN: En 	specified trigge able Trigger O specified trigge able Trigger O specified trigge able Trigger O specified trigge	er signal to be utput from PW er signal to be utput from PW er signal to be utput from PW	OR'd into the /M Generator # OR'd into the /M Generator # OR'd into the /M Generator #	Combinatorial Tr #6 as Source for Combinatorial Tr #5 as Source for Combinatorial Tr #4 as Source for	rigger B signal Combinationa rigger B signal Combinationa rigger B signal Combinationa	I Trigger B bit I Trigger B bit I Trigger B bit
bit 5 bit 4	 1 = Enables 0 = Disabled CTB6EN: En 1 = Enables 0 = Disabled CTB5EN: En 1 = Enables 0 = Disabled CTB4EN: En 1 = Enables 0 = Disabled CTB3EN: En 	specified trigge able Trigger O specified trigge able Trigger O specified trigge able Trigger O specified trigge able Trigger O	er signal to be utput from PW er signal to be utput from PW er signal to be utput from PW er signal to be utput from PW	OR'd into the /M Generator # OR'd into the /M Generator # OR'd into the /M Generator # OR'd into the	Combinatorial Ti #6 as Source for Combinatorial Ti #5 as Source for Combinatorial Ti #4 as Source for Combinatorial Ti	rigger B signal Combinationa rigger B signal Combinationa rigger B signal Combinationa rigger B signal	I Trigger B bit I Trigger B bit I Trigger B bit I Trigger B bit
bit 5 bit 4 bit 3	 1 = Enables 0 = Disabled CTB6EN: En 1 = Enables 0 = Disabled CTB5EN: En 1 = Enables 0 = Disabled CTB4EN: En 1 = Enables 0 = Disabled CTB3EN: En 1 = Enables 	specified trigge able Trigger O specified trigge able Trigger O specified trigge able Trigger O specified trigge able Trigger O specified trigge	er signal to be utput from PW er signal to be utput from PW er signal to be utput from PW er signal to be utput from PW	OR'd into the /M Generator # OR'd into the /M Generator # OR'd into the /M Generator # OR'd into the	Combinatorial Ti #6 as Source for Combinatorial Ti #5 as Source for Combinatorial Ti #4 as Source for Combinatorial Ti	rigger B signal Combinationa rigger B signal Combinationa rigger B signal Combinationa rigger B signal	I Trigger B bit I Trigger B bit I Trigger B bit I Trigger B bit
bit 5 bit 4 bit 3 bit 2	 1 = Enables 0 = Disabled CTB6EN: En 1 = Enables 0 = Disabled CTB5EN: En 1 = Enables 0 = Disabled CTB4EN: En 1 = Enables 0 = Disabled CTB3EN: En 1 = Enables 0 = Disabled 	specified trigge able Trigger O specified trigge able Trigger O specified trigge able Trigger O specified trigge able Trigger O specified trigge	er signal to be utput from PW er signal to be	OR'd into the /M Generator # OR'd into the /M Generator # OR'd into the /M Generator # OR'd into the /M Generator # OR'd into the	Combinatorial Tr #6 as Source for Combinatorial Tr #5 as Source for Combinatorial Tr #4 as Source for Combinatorial Tr #3 as Source for Combinatorial Tr	rigger B signal Combinationa rigger B signal Combinationa rigger B signal Combinationa rigger B signal Combinationa	I Trigger B bit I Trigger B bit I Trigger B bit I Trigger B bit
bit 5 bit 4 bit 3	 1 = Enables 0 = Disabled CTB6EN: En 1 = Enables 0 = Disabled CTB5EN: En 1 = Enables 0 = Disabled CTB4EN: En 1 = Enables 0 = Disabled CTB3EN: En 1 = Enables 0 = Disabled CTB2EN: En 	specified trigge able Trigger O specified trigge able Trigger O specified trigge able Trigger O specified trigge able Trigger O specified trigge	er signal to be utput from PW er signal to be	OR'd into the /M Generator # OR'd into the /M Generator # OR'd into the /M Generator # OR'd into the /M Generator #	Combinatorial Ti #6 as Source for Combinatorial Ti #5 as Source for Combinatorial Ti #4 as Source for Combinatorial Ti #3 as Source for Combinatorial Ti	rigger B signal Combinationa rigger B signal Combinationa rigger B signal Combinationa rigger B signal Combinationa rigger B signal	I Trigger B bit I Trigger B bit I Trigger B bit I Trigger B bit I Trigger B bit
bit 5 bit 4 bit 3 bit 2	 1 = Enables 0 = Disabled CTB6EN: En 1 = Enables 0 = Disabled CTB5EN: En 1 = Enables 0 = Disabled CTB4EN: En 1 = Enables 0 = Disabled CTB3EN: En 1 = Enables 0 = Disabled CTB2EN: En 	specified trigge able Trigger O specified trigge able Trigger O specified trigge able Trigger O specified trigge able Trigger O specified trigge	er signal to be utput from PW er signal to be	OR'd into the /M Generator # OR'd into the /M Generator # OR'd into the /M Generator # OR'd into the /M Generator #	Combinatorial Tr #6 as Source for Combinatorial Tr #5 as Source for Combinatorial Tr #4 as Source for Combinatorial Tr #3 as Source for Combinatorial Tr	rigger B signal Combinationa rigger B signal Combinationa rigger B signal Combinationa rigger B signal Combinationa rigger B signal	I Trigger B bit I Trigger B bit I Trigger B bit I Trigger B bit I Trigger B bit
bit 5 bit 4 bit 3 bit 2	 1 = Enables 0 = Disabled CTB6EN: En 1 = Enables 0 = Disabled CTB5EN: En 1 = Enables 0 = Disabled CTB4EN: En 1 = Enables 0 = Disabled CTB3EN: En 1 = Enables 0 = Disabled CTB2EN: En 1 = Enables 0 = Disabled 	specified trigge able Trigger O specified trigge able Trigger O specified trigge able Trigger O specified trigge able Trigger O specified trigge able Trigger O	er signal to be utput from PW er signal to be	OR'd into the /M Generator # OR'd into the /M Generator # OR'd into the /M Generator # OR'd into the /M Generator # OR'd into the /M Generator #	Combinatorial Ti #6 as Source for Combinatorial Ti #5 as Source for Combinatorial Ti #4 as Source for Combinatorial Ti #3 as Source for Combinatorial Ti #2 as Source for Combinatorial Ti	rigger B signal Combinationa rigger B signal Combinationa rigger B signal Combinationa rigger B signal Combinationa rigger B signal	I Trigger B bit I Trigger B bit I Trigger B bit I Trigger B bit I Trigger B bit
bit 5 bit 4 bit 3 bit 2 bit 1	 1 = Enables 0 = Disabled CTB6EN: En 1 = Enables 0 = Disabled CTB5EN: En 1 = Enables 0 = Disabled CTB4EN: En 1 = Enables 0 = Disabled CTB3EN: En 1 = Enables 0 = Disabled CTB2EN: En 1 = Enables 0 = Disabled CTB2EN: En 1 = Enables 0 = Disabled CTB1EN: En 	specified trigge able Trigger O specified trigge	er signal to be utput from PW er signal to be	OR'd into the /M Generator # OR'd into the /M Generator # OR'd into the /M Generator # OR'd into the /M Generator # OR'd into the /M Generator #	Combinatorial Ti #6 as Source for Combinatorial Ti #5 as Source for Combinatorial Ti #4 as Source for Combinatorial Ti #3 as Source for Combinatorial Ti	rigger B signal Combinationa rigger B signal Combinationa rigger B signal Combinationa rigger B signal Combinationa rigger B signal Combinationa	I Trigger B bit I Trigger B bit I Trigger B bit I Trigger B bit I Trigger B bit

REGISTER 9-8: CMBTRIGH: COMBINATIONAL TRIGGER REGISTER HIGH

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0			
_	—	_	—	—	—	_	P1<8>			
bit 15							bit 8			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
			P1<	7:0>						
bit 7							bit 0			
Legend:										
R = Readable bit V		W = Writable bit		U = Unimplemented bit, read		d as '0'				
-n = Value at POR		'1' = Bit is set	'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown			
bit 15-9	Unimplemen	ted: Read as '0	3							
bit 8-0	P1<8:0>: Par	ameter 1 bits								
	DMX TX:									
	Number of Bytes to Transmit – 1 (not including Start code).									
	LIN Master TX:									
PID to transmit (bits<5:0>).										
		Asynchronous TX with Address Detect:								
	Address to transmit. A '1' is automatically inserted into bit 9 (bits<7:0>). Smart Card Mode:									
		Guard Time Counter bits. This counter is operated on the bit clock whose period is always equal to one								
	ETU (bits<8:0									
	Other Modes:	<u>.</u>								
	Not used.									

REGISTER 13-9: UxP1: UARTx TIMING PARAMETER 1 REGISTER

U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0			
_		—	FRMERREN	BUSYEN	_	_	SPITUREN			
bit 15							bit 8			
R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0			
SRMTEN	SPIROVEN	SPIRBEN	—	SPITBEN	—	SPITBFEN	SPIRBFEN			
bit 7							bit C			
Legend:										
R = Readabl		W = Writable bit		U = Unimplem						
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ired	x = Bit is unkr	iown			
bit 15-13	Unimplomon	ted: Read as '	o'							
bit 12	-			RMERR hit						
	FRMERREN: Enable Interrupt Events via FRMERR bit 1 = Frame error generates an interrupt event									
			nerate an interr							
bit 11	BUSYEN: Enable Interrupt Events via SPIBUSY bit									
	1 = SPIBUSY generates an interrupt event									
		•	erate an interrup	ot event						
bit 10-9	-	ted: Read as '								
bit 8	SPITUREN: Enable Interrupt Events via SPITUR bit									
			R) generates an not generate a							
bit 7	SRMTEN: Enable Interrupt Events via SRMT bit									
			RMT) generates es not generate							
bit 6	SPIROVEN: Enable Interrupt Events via SPIROV bit									
			(ROV) generate	•						
bit 5			Events via SPIF							
			enerates an inte bes not generate		vent					
bit 4	Unimplement	ted: Read as '	0'							
bit 3	SPITBEN: Enable Interrupt Events via SPITBE bit									
			oty generates ar oty does not ger	•						
bit 2	Unimplement	ted: Read as '	0'							
bit 1	SPITBFEN: Enable Interrupt Events via SPITBF bit									
			generates an in does not genera		event					
bit 0			t Events via SP	•						
		-	enerates an inte							
	0 = SPIx rece									

REGISTER 14-6: SPIxIMSKL: SPIx INTERRUPT MASK REGISTER LOW

REGISTER 21-23: FCFGPRD0: PORTD CONFIGURATION REGISTER

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16
R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
			CPRE	0<15:8>			
bit 15							bit 8
R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
			CPR	D<7:0>			
bit 7							bit 0
Legend: P		PO = Program Once bit					
R = Readable bit		W = Writable bit		U = Unimplemented bit, read as '0'			
-n = Value at POR		'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown	

bit 23-16 Unimplemented: Read as '1'

bit 15-0 CPRD<15:0>: Configure PORTD Ownership bits

1 = Master core owns pin

0 = Slave core owns pin

REGISTER 21-24: FCFGPRE0: PORTE CONFIGURATION REGISTER

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
_	_	_	—	—	_	—	
bit 23							bit 16
R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
			CPRE	=<15:8>			
bit 15							bit 8
R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
			CPR	E<7:0>			
bit 7							bit C
Legend:		PO = Progran	n Once bit				
R = Readable bit		W = Writable bit		U = Unimplemented bit, rea		ad as '0'	
-n = Value at POR		'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown	
bit 23-16	Unimplemer	nted: Read as ':	1'				
	•						

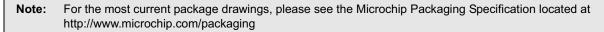
bit 15-0 CPRE<15:0>: Configure PORTE Ownership bits

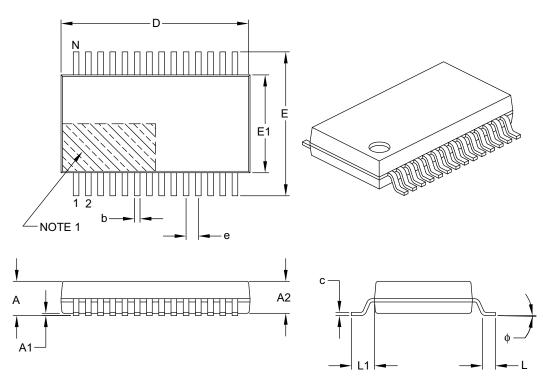
1 = Master core owns pin

0 = Slave core owns pin

25.2 Package Details

28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]





	Units		MILLIMETERS	3	
Dimer	Dimension Limits			MAX	
Number of Pins	Ν	28			
Pitch	е	0.65 BSC			
Overall Height	Α	-	-	2.00	
Molded Package Thickness	A2	1.65	1.75	1.85	
Standoff	A1	0.05	-	-	
Overall Width	E	7.40	7.80	8.20	
Molded Package Width	E1	5.00	5.30	5.60	
Overall Length	D	9.90	10.20	10.50	
Foot Length	L	0.55	0.75	0.95	
Footprint L1		1.25 REF			
Lead Thickness	С	0.09	-	0.25	
Foot Angle	φ	0°	4°	8°	
Lead Width	b	0.22	-	0.38	

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
 Dimensioning and tolerancing per ASME Y14.5M.
- BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

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