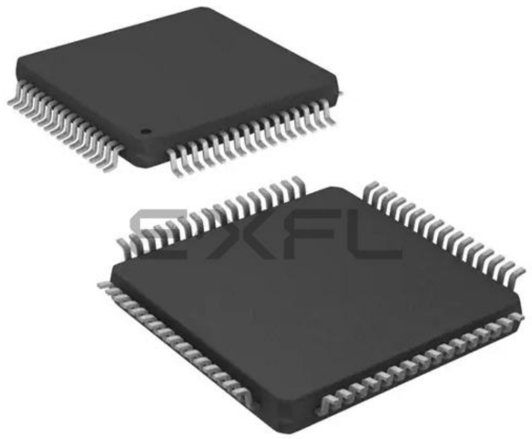

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Details	
Product Status	Active
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Speed	180MHz, 200MHz
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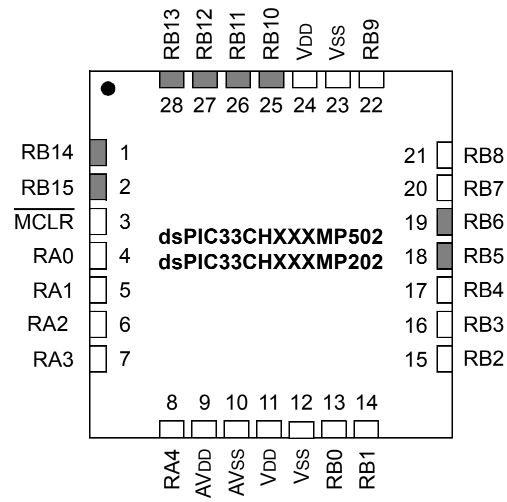
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	53
Program Memory Size	152KB (152K x 8)
Program Memory Type	FLASH, PRAM
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 34x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ch128mp506-e-pt

Pin Diagrams (Continued)

28-Pin UQFN[1,2]



Note 1: **Shaded pins** are up to 5.5 VDC tolerant (refer to Table 3-28 and Table 4-25). For the list of analog ports, refer to Table 3-27 and Table 4-24.

2: The large center pad on the bottom of the package may be left floating or connected to VSS. The four-corner anchor pads are internally connected to the large bottom pad, and therefore, must be connected to the same net as the large center pad.

TABLE 5: 28-PIN UQFN

Pin #	Master Core	Slave Core
1	**RP46**/PWM1H/RB14	**S1RP46**/S1PWM1H/S1RB14
2	**RP47**/PWM1L/RB15	**S1RP47**/S1PWM6H/S1PWM1L/S1RB15
3	$\overline{\text{MCLR}}$	—
4	AN0/CMP1A/RA0	S1RA0
5	AN1/RA1	S1AN15/S1RA1
6	AN2/RA2	S1AN16/S1RA2
7	AN3/IBIAS0/RA3	S1AN0/S1CMP1A/S1PGA1P1/S1RA3
8	AN4/IBIAS1/RA4	$\overline{\text{S1MCLR3}}$/S1AN1/S1CMP2A/S1PGA2P1/S1PGA3P2/S1RA4
9	AVDD	AVDD
10	AVSS	AVSS
11	VDD	VDD
12	VSS	VSS
13	OSCI/CLKI/AN5/**RP32**/RB0	S1AN5/**S1RP32**/S1RB0
14	OSCO/CLKO/AN6/IBIAS2/**RP33**/RB1	S1AN4/**S1RP33**/S1RB1
15	DACOUT/AN7/CMP1D/**RP34**/INT0/RB2	$\overline{\text{S1MCLR2}}$/S1AN3/S1ANC0/S1ANC1/S1CMP1D/S1CMP2D/S1CMP3D/**S1RP34**/S1INT0/S1RB2
16	PGD2/AN8/**RP35**/RB3	S1PGD2/S1AN18/S1CMP3A/S1PGA3P1/**S1RP35**/S1RB3
17	PGC2/**RP36**/RB4	S1PGC2/S1AN9/**S1RP36**/S1PWM5L/S1RB4
18	PGD3/**RP37**/SDA2/RB5	S1PGD3/**S1RP37**/S1RB5
19	PGC3/**RP38**/SCL2/RB6	S1PGC3/**S1RP38**/S1RB6
20	TDO/AN9/**RP39**/RB7	$\overline{\text{S1MCLR1}}$/S1AN6/**S1RP39**/S1PWM5H/S1RB7
21	PGD1/AN10/**RP40**/SCL1/RB8	S1PGD1/S1AN7/**S1RP40**/S1SCL1/S1RB8
22	PGC1/AN11/**RP41**/SDA1/RB9	S1PGC1/**S1RP41**/S1SDA1/S1RB9
23	VSS	VSS
24	VDD	VDD
25	TMS/**RP42**/PWM3H/RB10	**S1RP42**/S1PWM3H/S1RB10
26	TCK/**RP43**/PWM3L/RB11	**S1RP43**/S1PWM8H/S1PWM3L/S1RB11
27	TDI/**RP44**/PWM2H/RB12	**S1RP44**/S1PWM2H/S1RB12
28	**RP45**/PWM2L/RB13	**S1RP45**/S1PWM7H/S1PWM2L/S1RB13

Legend: **RPn** and **S1RPn** represent remappable pins for Peripheral Pin Select functions.

REGISTER 3-7: NVMKEY: NONVOLATILE MEMORY KEY REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
NVMKEY<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **NVMKEY<7:0>:** NVM Key Register bits (write-only)

REGISTER 3-8: NVMSRCADR: NVM SOURCE DATA ADDRESS REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NVMSRCADR<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NVMSRCADR<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

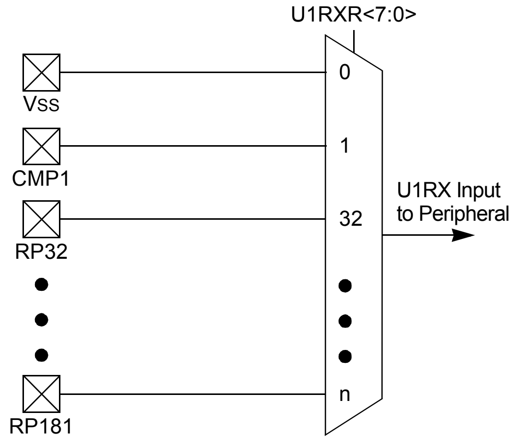
bit 15-0 **NVMSRCADR<15:0>:** NVM Source Data Address bits
The RAM address of the data to be programmed into Flash when the NVMOP<3:0> bits are set to row programming.

TABLE 3-26: MASTER INTERRUPT PRIORITY REGISTERS (CONTINUED)

Register	Address	Bit 15	Bit14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IPC35	886h	—	—	—	—	—	—	—	—	—	S1SRSTIP2	S1SRSTIP1	S1SRSTIP0	—	MSIFLTIP2	MSIFLTIP1	MSIFLTIP0
IPC36	888h	—	—	—	—	—	S1BRKIP2	S1BRKIP1	S1BRKIP0	—	—	—	—	—	—	—	—
IPC37	88Ah	—	—	—	—	—	CCT7IP2	CCT7IP1	CCT7IP0	—	CCP7IP2	CCP7IP1	CCP7IP0	—	—	—	—
IPC38	88Ch	—	—	—	—	—	—	—	—	—	CCT8IP2	CCT8IP1	CCT8IP0	—	CCP8IP2	CCP8IP1	CCP8IP0
IPC39	88Eh	—	—	—	—	—	—	—	—	—	S1CLKFIP2	S1CLKFIP1	S1CLKFIP0	—	—	—	—
IPC40	890h	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
IPC41	892h	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
IPC42	894h	—	PEVTCIP2	PEVTCIP1	PEVTCIP0	—	PEVTBIP2	PEVTBIP1	PEVTBIP0	—	PEVTAIP2	PEVTAIP1	PEVTAIP0	—	ADFIFOIP2	ADFIFOIP1	ADFIFOIP0
IPC43	896h	—	CLC3PIP2	CLC3PIP1	CLC3PIP0	—	PEVTFIP2	PEVTFIP1	PEVTFIP0	—	PEVTEIP2	PEVTEIP1	PEVTEIP0	—	PEVTDIP2	PEVTDIP1	PEVTDIP0
IPC44	898h	—	CLC3NIP2	CLC3NIP1	CLC3NIP0	—	CLC2NIP2	CLC2NIP1	CLC2NIP0	—	CLC1NIP2	CLC1NIP1	CLC1NIP0	—	CLC4PIP2	CLC4PIP1	CLC4PIP0
IPC45	89Ah	—	—	—	—	—	—	—	—	—	—	—	—	—	CLC4NIP2	CLC4NIP1	CLC4NIP0
IPC46	89Ch	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
IPC47	89Eh	—	—	—	—	—	U2EVTIP2	U2EVTIP1	U2EVTIP0	—	U1EVTIP2	U1EVTIP1	U1EVTIP0	—	—	—	—

Legend: — = Unimplemented.

FIGURE 3-20: REMAPPABLE INPUT FOR U1RX



Note: For input only, Peripheral Pin Select functionality does not have priority over TRISx settings. Therefore, when configuring an RPn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to '1'). Physical connection to a pin can be made through RP32 through RP71. There are internal signals and virtual pins that can be connected to an input. Table 3-30 shows the details of the input assignment.

Example 3-2 provides a configuration for bidirectional communication with flow control using UART1. The following input and output functions are used:

- Input Functions: U1RX, $\overline{\text{U1CTS}}$
- Output Functions: U1TX, $\overline{\text{U1RTS}}$

EXAMPLE 3-2: CONFIGURING UART1 INPUT AND OUTPUT FUNCTIONS

```
//
*******************************************
// Unlock Registers
//*****************************************
__builtin_write_RPCON(0x0000);
//*****************************************
// Configure Input Functions (See Table 3-31)
// Assign U1Rx To Pin RP35
//***************************
_U1RXR = 35;
// Assign U1CTS To Pin RP36
//***************************
_U1CTSR = 36;
//*****************************************
// Configure Output Functions (See Table 3-33)
//*****************************************
// Assign U1Tx To Pin RP37
//***************************
_RP37 = 1;
//***************************
// Assign U1RTS To Pin RP38
//***************************
_RP38 = 2;
//*****************************************
// Lock Registers
//*****************************************
__builtin_write_RPCON(0x0800);
```

REGISTER 3-80: RPOR12: PERIPHERAL PIN SELECT OUTPUT REGISTER 12

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP57R5	RP57R4	RP57R3	RP57R2	RP57R1	RP57R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP56R5	RP56R4	RP56R3	RP56R2	RP56R1	RP56R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14	**Unimplemented:** Read as ‘0’
bit 13-8	**RP57R<5:0>:** Peripheral Output Function is Assigned to RP57 Output Pin bits (see Table 3-33 for peripheral function numbers)
bit 7-6	**Unimplemented:** Read as ‘0’
bit 5-0	**RP56R<5:0>:** Peripheral Output Function is Assigned to RP56 Output Pin bits (see Table 3-33 for peripheral function numbers)

REGISTER 3-81: RPOR13: PERIPHERAL PIN SELECT OUTPUT REGISTER 13

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP59R5	RP59R4	RP59R3	RP59R2	RP59R1	RP59R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP58R5	RP58R4	RP58R3	RP58R2	RP58R1	RP58R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14	**Unimplemented:** Read as ‘0’
bit 13-8	**RP59R<5:0>:** Peripheral Output Function is Assigned to RP59 Output Pin bits (see Table 3-33 for peripheral function numbers)
bit 7-6	**Unimplemented:** Read as ‘0’
bit 5-0	**RP58R<5:0>:** Peripheral Output Function is Assigned to RP58 Output Pin bits (see Table 3-33 for peripheral function numbers)

REGISTER 3-126: C1TXREQH: CAN TRANSMIT REQUEST REGISTER HIGH

S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0
TXREQ<31:24>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	S/HC-0
TXREQ<23:16>							
bit 7							bit 0

Legend:	S = Settable bit	HC = Hardware Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **TXREQ<31:16>:** Unimplemented

REGISTER 3-127: C1TXREQL: CAN TRANSMIT REQUEST REGISTER LOW

S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0
TXREQ<15:8>							
bit 15							bit 8

S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0s
TXREQ<7:1>							TXREQ0
bit 7							bit 0

Legend:	S = Settable bit	HC = Hardware Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **TXREQ<15:8>:** Unimplemented

bit 7-1 **TXREQ<7:1>:** Message Send Request bits

TXEN = 1 (object configured as a transmit object):
Setting this bit to ‘1’ requests sending a message. The bit will automatically clear when the message(s) queued in the object is (are) successfully sent. This bit can NOT be used for aborting a transmission.

TXEN = 0 (object configured as a receive object):
This bit has no effect.

bit 0 **TXREQ0:** Transmit Queue Message Send Request bit

Setting this bit to ‘1’ requests sending a message. The bit will automatically clear when the message(s) queued in the object is (are) successfully sent. This bit can NOT be used for aborting a transmission.

REGISTER 3-162: ADCON3H: ADC CONTROL REGISTER 3 HIGH

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CLKSEL1	CLKSEL0	CLKDIV5	CLKDIV4	CLKDIV3	CLKDIV2	CLKDIV1	CLKDIV0
bit 15							bit 8

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
SHREN	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **CLKSEL<1:0>:** ADC Module Clock Source Selection bits
11 = FVCO/4
10 = AFVCODIV
01 = FOSC
00 = FP (FOSC/2)

bit 13-8 **CLKDIV<5:0>:** ADC Module Clock Source Divider bits
The divider forms a TCORESRC clock used by all ADC cores (shared and dedicated), from the TSRC ADC module clock source, selected by the CLKSEL<1:0> bits. Then, each ADC core individually divides the TCORESRC clock to get a core-specific TADCORE clock using the ADCS<6:0> bits in the ADCORExH register or the SHRADCS<6:0> bits in the ADCON2L register.
111111 = 64 Source Clock Periods
...
000011 = 4 Source Clock Periods
000010 = 3 Source Clock Periods
000001 = 2 Source Clock Periods
000000 = 1 Source Clock Period

bit 7 **SHREN:** Shared ADC Core Enable bit
1 = Shared ADC core is enabled
0 = Shared ADC core is disabled

bit 6-0 **Unimplemented:** Read as ‘0’

4.1.6 CPU RESOURCES

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

4.1.6.1 Key Resources

- **"dsPIC33E Enhanced CPU"** (DS70005158) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

FIGURE 4-21: ADC SHARED CORE BLOCK DIAGRAM

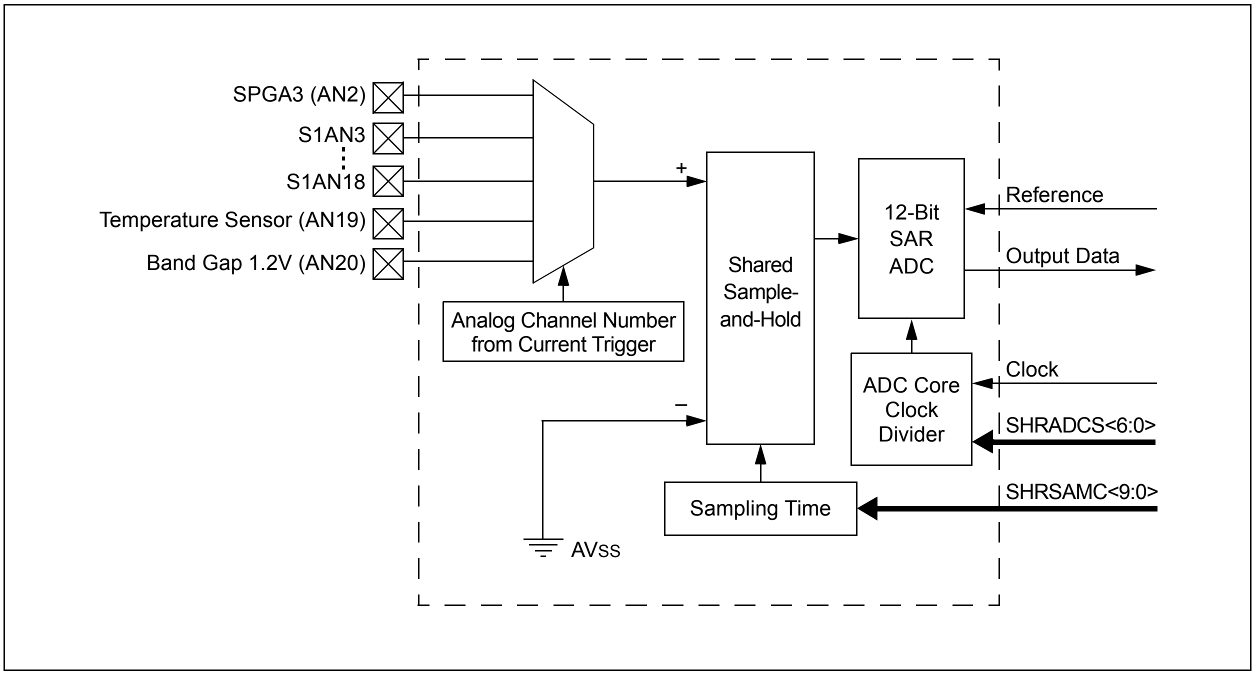
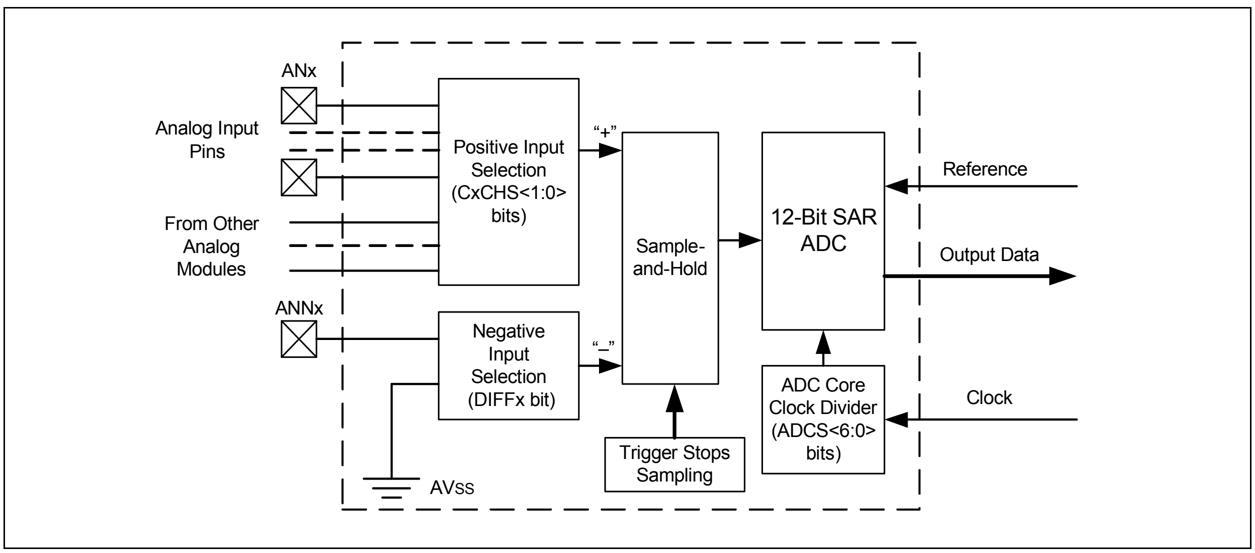


FIGURE 4-22: DEDICATED ADC CORE



4.8 Programmable Gain Amplifier (PGA) Slave

Note 1: This data sheet summarizes the features of the dsPIC33CH128MP508 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Programmable Gain Amplifier (PGA)"** (DS70005146) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

The dsPIC33CH128MP508S1 family devices have three Programmable Gain Amplifiers (PGA1, PGA2, PGA3). The PGA is an op amp-based, non-inverting amplifier with user-programmable gains. The output of the PGA can be connected to a number of dedicated Sample-and-Hold inputs of the Analog-to-Digital Converter and/or to the high-speed analog comparator module. The PGA has four selectable gains and may be used as a ground referenced amplifier (single-ended) or used with an independent ground reference point.

Key features of the PGA module include:

- Single-Ended or Independent Ground Reference
- Selectable Gains: 4x, 8x, 16x and 32x (and 6x,12x, 24x and 48x with the 1.5 gain)
- High-Gain Bandwidth
- Rail-to-Rail Output Voltage
- Wide Input Voltage Range

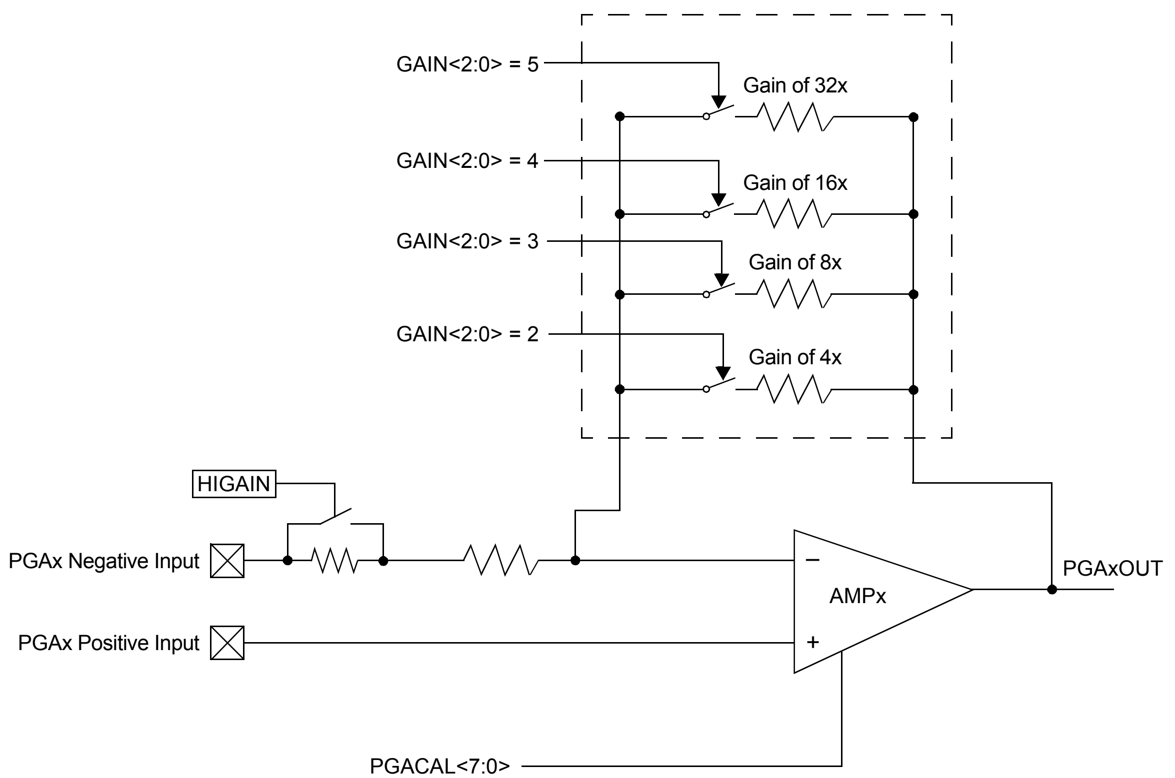
Table 4-38 shows an overview of the PGA module.

TABLE 4-38: PGA MODULE OVERVIEW(1)

	Number of PGA Modules	Identical (Modules)
Master	—	—
Slave	3	—

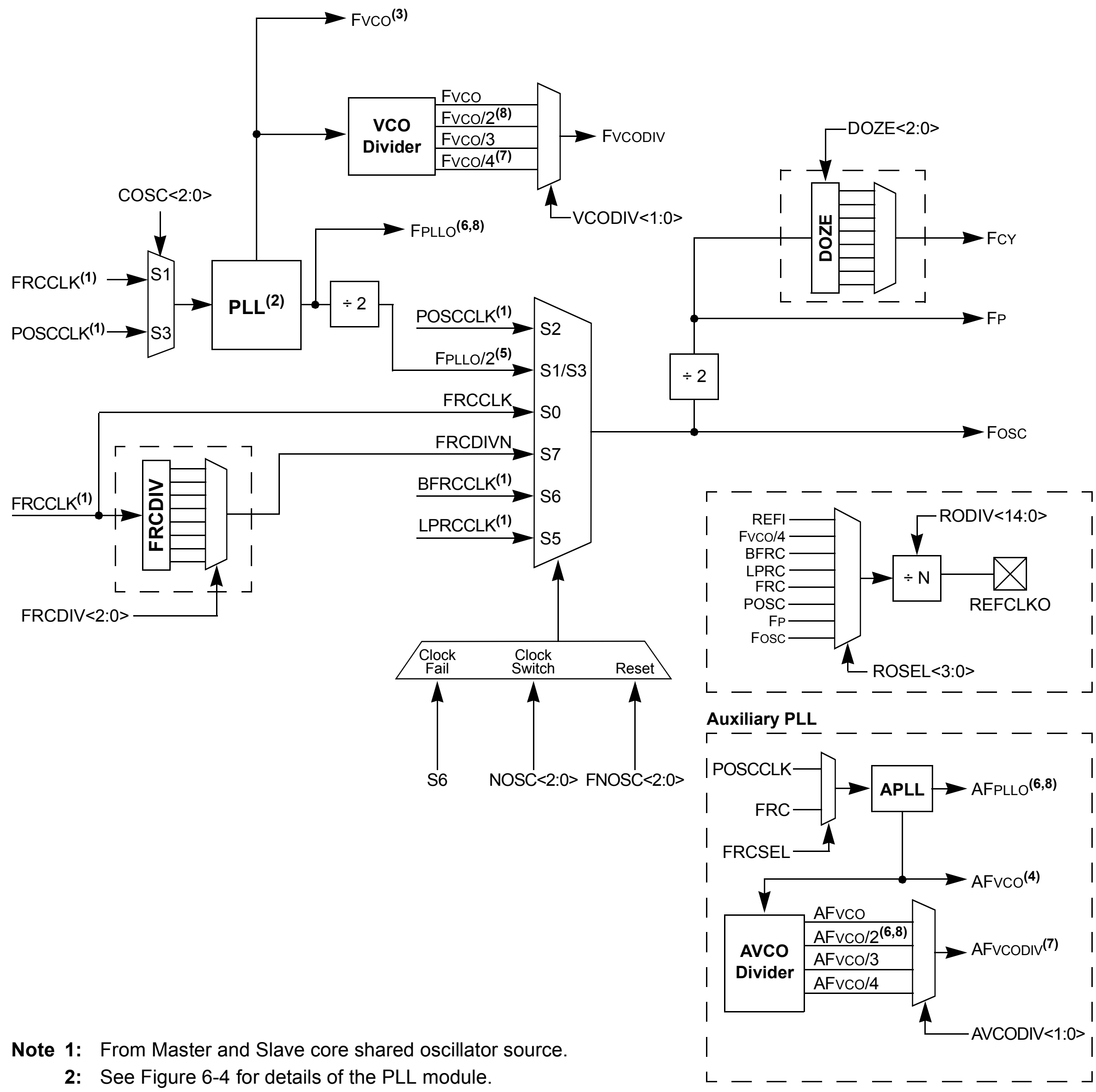
Note 1: The Slave owns the PGA module, but it is shared with the Master.

FIGURE 4-23: PGAx MODULE BLOCK DIAGRAM



Note 1: x = 1, 2 and 3.

FIGURE 6-3: SLAVE CORE OSCILLATOR SUBSYSTEM



Note 1: From Master and Slave core shared oscillator source.
2: See Figure 6-4 for details of the PLL module.
3: See Figure 6-4 for the source of FVCO.
4: See Figure 6-4 for the source of AVCO.
5: XTPLL, HSPLL, ECPLL, FRCPLL (FPLLO).
6: Clock option for PWM.
7: Clock option for ADC.
8: Clock option for DAC.

6.2 Master Oscillator Configuration Registers

Table 6-1 lists the configuration settings that select the device's Master core oscillator source and operating mode at a POR.

TABLE 6-1: CONFIGURATION BIT VALUES FOR CLOCK SELECTION FOR THE MASTER

Oscillator Source	Oscillator Mode	FNOSC<2:0> Value	POSCMD<1:0> Value(3)	Notes
S0	Fast RC Oscillator (FRC)	000	xx	**1**
S1	Fast RC Oscillator with PLL (FRCPLL)	001	xx	**1**
S2	Primary Oscillator (EC)	010	00	**1**
S2	Primary Oscillator (XT)	010	01	
S2	Primary Oscillator (HS)	010	10	
S3	Primary Oscillator with PLL (ECPLL)	011	00	**1**
S3	Primary Oscillator with PLL (XTPLL)	011	01	
S3	Primary Oscillator with PLL (HSPLL)	011	10	
S4	Reserved	100	xx	
S5	Low-Power RC Oscillator (LPRC)	101	xx	**1**
S6	Backup FRC (BFRC)	110	xx	**1**
S7	Fast RC Oscillator with ÷ N Divider (FRCDIVN)	111	xx	**1, 2**

Note 1: The OSCO pin function is determined by the OSCIOFNC Configuration bit.

2: This is the default oscillator mode for an unprogrammed (erased) device.

3: The POSCMDx bits are only available in the Master FOSC Configuration register.

REGISTER 6-5: PLLDIV: PLL OUTPUT DIVIDER REGISTER (MASTER)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	VCODIV1	VCODIV0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-1
—	POST1DIV2(1,2)	POST1DIV1(1,2)	POST1DIV0(1,2)	—	POST2DIV2(1,2)	POST2DIV1(1,2)	POST2DIV0(1,2)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-10 **Unimplemented:** Read as ‘0’

bit 9-8 **VCODIV<1:0>:** PLL VCO Output Divider Select bits
11 = FVCO
10 = FVCO/2
01 = FVCO/3
00 = FVCO/4

bit 7 **Unimplemented:** Read as ‘0’

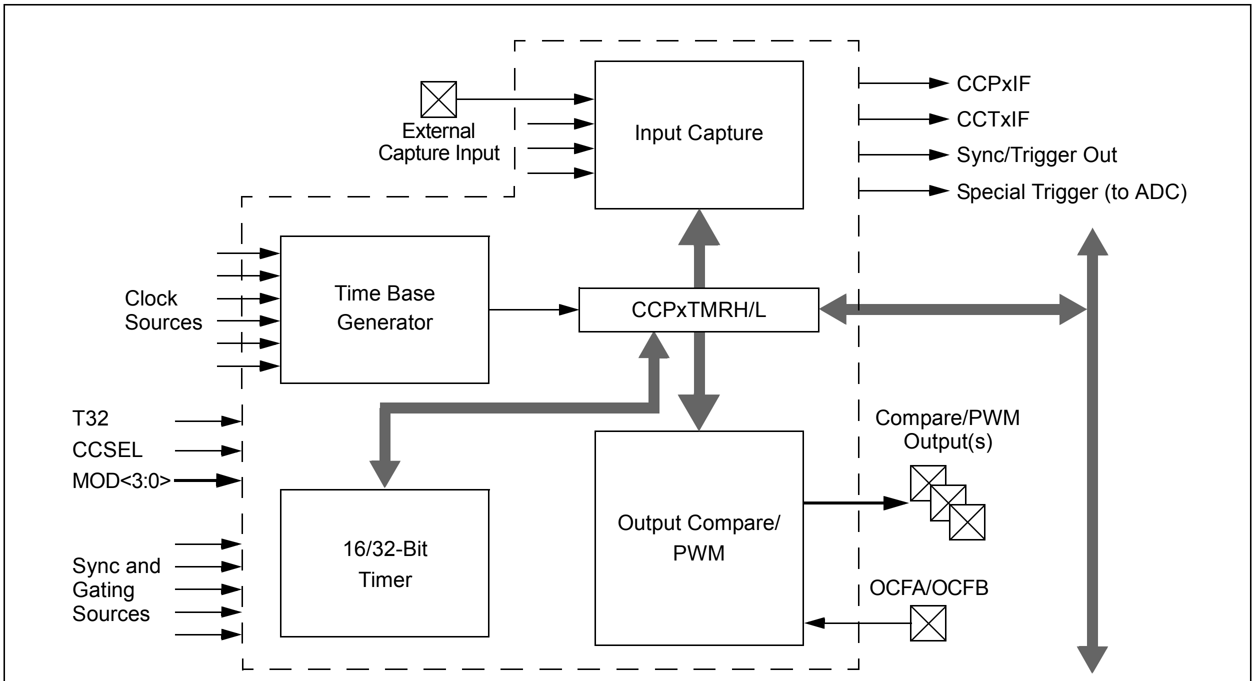
bit 6-4 **POST1DIV<2:0>:** PLL Output Divider #1 Ratio bits(1,2)
POST1DIV<2:0> can have a valid value, from 1 to 7 (POST1DIVx value should be greater than or equal to the POST2DIVx value). The POST1DIVx divider is designed to operate at higher clock rates than the POST2DIVx divider.

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **POST2DIV<2:0>:** PLL Output Divider #2 Ratio bits(1,2)
POST2DIV<2:0> can have a valid value, from 1 to 7 (POST2DIVx value should be less than or equal to the POST1DIVx value). The POST1DIVx divider is designed to operate at higher clock rates than the POST2DIVx divider.

Note 1: The POST1DIVx and POST2DIVx divider values must not be changed while the PLL is operating.
2: The default values for POST1DIVx and POST2DIVx are 4 and 1, respectively, yielding a 150 MHz system source clock.

FIGURE 10-1: SCCPx CONCEPTUAL BLOCK DIAGRAM

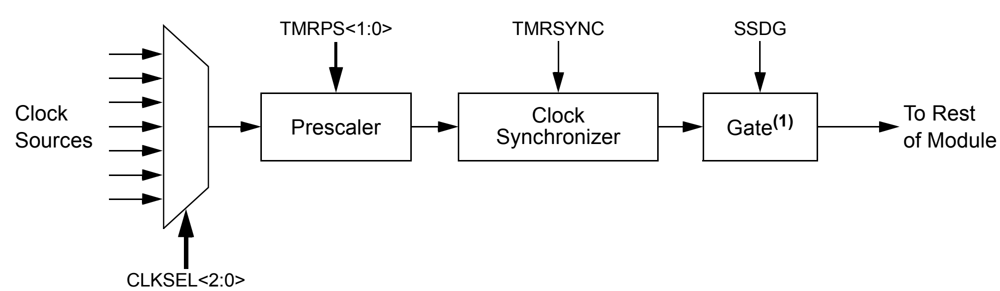


10.1 Time Base Generator

The Timer Clock Generator (TCG) generates a clock for the module's internal time base, using one of the clock signals already available on the microcontroller. This is used as the time reference for the module in its three major modes. The internal time base is shown in Figure 10-2.

There are eight inputs available to the clock generator, which are selected using the CLKSEL<2:0> bits (CCPxCON1L<10:8>). Available sources include the FRC and LPRC, the Secondary Oscillator and the TCLKI External Clock inputs. The system clock is the default source (CLKSEL<2:0> = `000`).

FIGURE 10-2: TIMER CLOCK GENERATOR



Note 1: Gating is available in Timer modes only.

REGISTER 13-14: UxRXCHK: UARTx RECEIVE CHECKSUM REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RXCHK<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **RXCHK<7:0>:** Receive Checksum bits (calculated from RX words)

<u>LIN Modes:</u>
C0EN = 1: Sum of all received data + addition carries, including PID.
C0EN = 0: Sum of all received data + addition carries, excluding PID.

<u>LIN Slave:</u>
Cleared when Break is detected.

<u>LIN Master/Slave:</u>
Cleared when Break is detected.

<u>Other Modes:</u>
C0EN = 1: Sum of every byte received + addition carries.
C0EN = 0: Value remains unchanged.

REGISTER 14-3: SPIxCON2L: SPIx CONTROL REGISTER 2 LOW

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	WLENGTH<4:0>(1,2)				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as ‘0’

bit 4-0 **WLENGTH<4:0>:** Variable Word Length bits(1,2)

11111 = 32-bit data
11110 = 31-bit data
11101 = 30-bit data
11100 = 29-bit data
11011 = 28-bit data
11010 = 27-bit data
11001 = 26-bit data
11000 = 25-bit data
10111 = 24-bit data
10110 = 23-bit data
10101 = 22-bit data
10100 = 21-bit data
10011 = 20-bit data
10010 = 19-bit data
10001 = 18-bit data
10000 = 17-bit data
01111 = 16-bit data
01110 = 15-bit data
01101 = 14-bit data
01100 = 13-bit data
01011 = 12-bit data
01010 = 11-bit data
01001 = 10-bit data
01000 = 9-bit data
00111 = 8-bit data
00110 = 7-bit data
00101 = 6-bit data
00100 = 5-bit data
00011 = 4-bit data
00010 = 3-bit data
00001 = 2-bit data
00000 = See MODE<32,16> bits in SPIxCON1L<11:10>

Note 1: These bits are effective when AUDEN = 0 only.
2: Varying the length by changing these bits does not affect the depth of the TX/RX FIFO.

NOTES:

REGISTER 21-8: FICD CONFIGURATION REGISTER

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 15							bit 8

r-1	U-1	R/PO-1	U-1	U-1	U-1	R/PO-1	R/PO-1
—	—	JTAGEN	—	—	—	ICS1	ICS0
bit 7							bit 0

Legend:	PO = Program Once bit	r = Reserved bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-8 **Unimplemented:** Read as ‘1’

bit 7 **Reserved:** Maintain as ‘1’

bit 6 **Unimplemented:** Read as ‘1’

bit 5 **JTAGEN:** JTAG Enable bit
1 = JTAG port is enabled
0 = JTAG port is disabled

bit 4-2 **Unimplemented:** Read as ‘1’

bit 1-0 **ICS<1:0>:** ICD Communication Channel Select bits
11 = Master communicates on PGC1 and PGD1
10 = Master communicates on PGC2 and PGD2
01 = Master communicates on PGC3 and PGD3
00 = Reserved, do not use

TABLE 24-11: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD})

DC CHARACTERISTICS	Master Sleep + Slave Sleep		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended		
Parameter No.	**Typ.**	**Max.**	**Units**	**Conditions**	
Power-Down Current (I_{PD})(1)					
DC60	3.2	4.8	mA	-40°C	3.3V
	3.4	8.2	mA	+25°C	
	3.7	14.3	mA	+85°C	
	7.6	21.5	mA	+125°C	

Note 1: I_{PD} (Sleep) current is measured as follows:
- CPU core is off, oscillator is configured in EC mode and External Clock is active; OSCI is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as output low
- $\overline{\text{MCLR}}$ = V_{DD}, WDT and FSCM are disabled
- All peripheral modules are disabled (PMDx bits are all set)
- The VREGS bit (RCON<8>) = 0 (i.e., core regulator is set to standby while the device is in Sleep mode)
- JTAG is disabled

TABLE 24-12: DC CHARACTERISTICS: WATCHDOG TIMER DELTA CURRENT (ΔI_{WDT})(1)

DC CHARACTERISTICS	Master and Slave		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended		
Parameter No.	**Typ.**	**Max.**	**Units**	**Conditions**	
DC61d	2.9	—	µA	-40°C	3.3V
DC61a	2.7	—	µA	+25°C	
DC61b	3.9	—	µA	+85°C	
DC61c	5.5	—	µA	+125°C	

Note 1: The ΔI_{WDT} current is the additional current consumed when the module is enabled. This current should be added to the base I_{PD} current. All parameters are characterized but not tested during manufacturing.

FIGURE 24-17: UARTx MODULE I/O TIMING CHARACTERISTICS

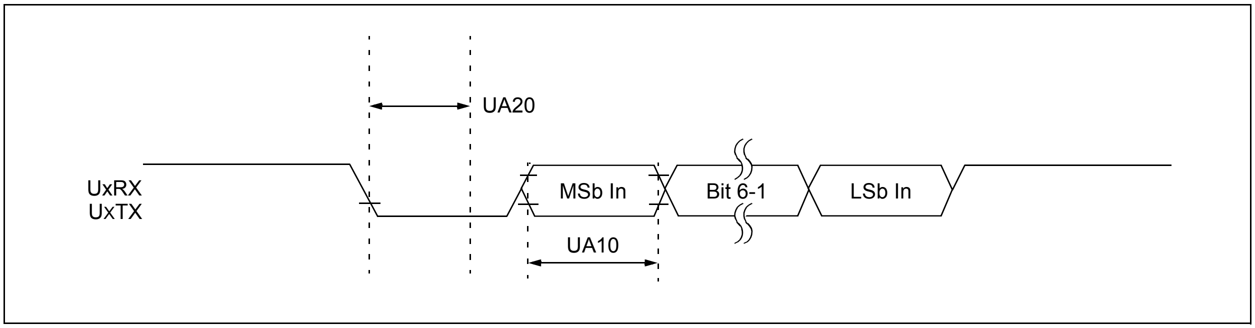


TABLE 24-42: UARTx MODULE I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
UA10	TUABAUD	UARTx Baud Time	66.67	—	—	ns	
UA11	FBAUD	UARTx Baud Frequency	—	—	15	Mbps	
UA20	TCWF	Start Bit Pulse Width to Trigger UARTx Wake-up	500	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in “Typ.” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

