Microchip Technology - DSPIC33CH64MP202-E/2N Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit Dual-Core
Speed	180MHz, 200MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	21
Program Memory Size	88KB (88K x 8)
Program Memory Type	FLASH, PRAM
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 23x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UQFN Exposed Pad
Supplier Device Package	28-UQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ch64mp202-e-2n

TABLE 6: 36-PIN UQFN

Pin #	Master Core	Slave Core
1	**RP46**/PWM1H/RB14	**S1RP46**/S1PWM1H/S1RB14
2	**RP47**/PWM1L/RB15	**S1RP47**/S1PWM6H/S1PWM1L/S1RB15
3	$\overline{\text{MCLR}}$	—
4	AN12/IBIAS3/**RP48**/RC0	S1AN10/**S1RP48**/S1RC0
5	AN0/CMP1A/RA0	S1RA0
6	AN1/RA1	S1AN15/S1RA1
7	AN2/RA2	S1AN16/S1RA2
8	AN3/IBIAS0/RA3	S1AN0/S1CMP1A/S1PGA1P1/S1RA3
9	AN4/IBIAS1/RA4	$\overline{\text{S1MCLR3}}$/S1AN1/S1CMP2A/S1PGA2P1/S1PGA3P2/S1RA4
10	AVDD	AVDD
11	AVSS	AVSS
12	AN13/ISRC0/**RP49**/RC1	S1ANA1/**S1RP49**/S1RC1
13	AN14/ISRC1/**RP50**/RC2	S1ANA0/**S1RP50**/S1RC2
14	VDD	VDD
15	VSS	VSS
16	CMP1B/**RP51**/RC3	S1AN8/S1CMP3B/**S1RP51**/S1RC3
17	OSCI/CLKI/AN5/**RP32**/RB0	S1AN5/**S1RP32**/S1RB0
18	OSCO/CLKO/AN6/IBIAS2/**RP33**/RB1	S1AN4/**S1RP33**/S1RB1
19	DACOUT/AN7/CMP1D/**RP34**/INT0/RB2	$\overline{\text{S1MCLR2}}$/S1AN3/S1ANC0/S1ANC1/S1CMP1D/S1CMP2D/S1CMP3D/**S1RP34**/S1INT0/S1RB2
20	PGD2/AN8/**RP35**/RB3	S1PGD2/S1AN18/S1CMP3A/S1PGA3P1/**S1RP35**/S1RB3
21	PGC2/**RP36**/RB4	S1PGC2/S1AN9/**S1RP36**/S1PWM5L/S1RB4
22	VSS	VSS
23	VDD	VDD
24	PGD3/**RP37**/SDA2/RB5	S1PGD3/**S1RP37**/S1RB5
25	PGC3/**RP38**/SCL2/RB6	S1PGC3/**S1RP38**/S1RB6
26	TDO/AN9/**RP39**/RB7	$\overline{\text{S1MCLR1}}$/S1AN6/**S1RP39**/S1PWM5H/S1RB7
27	PGD1/AN10/**RP40**/SCL1/RB8	S1PGD1/S1AN7/**S1RP40**/S1SCL1/S1RB8
28	PGC1/AN11/**RP41**/SDA1/RB9	S1PGC1/**S1RP41**/S1SDA1/S1RB9
29	**RP52**/RC4	**S1RP52**/S1PWM2H/S1RC4
30	**RP53**/RC5	**S1RP53**/S1PWM2L/S1RC5
31	VSS	VSS
32	VDD	VDD
33	TMS/**RP42**/PWM3H/RB10	**S1RP42**/S1PWM3H/S1RB10
34	TCK/**RP43**/PWM3L/RB11	**S1RP43**/S1PWM8H/S1PWM3L/S1RB11
35	TDI/**RP44**/PWM2H/RB12	**S1RP44**/S1PWM7L/S1RB12
36	**RP45**/PWM2L/RB13	**S1RP45**/S1PWM7H/S1RB13

Legend: **RPn** and **S1RPn** represent remappable pins for Peripheral Pin Select functions.

TABLE 3-17: MASTER SFR BLOCK E00h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
I/O Ports (Continued)			CNCONB	E2A	0---0----------	LATD	E5A	xxxxxxxxxxxxxxxx
ANSELA	E00	----------11111	CNEN0B	E2C	0000000000000000	ODCD	E5C	0000000000000000
TRISA	E02	----------11111	CNSTATB	E2E	0000000000000000	CNPUD	E5E	0000000000000000
PORTA	E04	----------xxxxx	CNEN1B	E30	0000000000000000	CNPDD	E60	0000000000000000
LATA	E06	----------xxxxx	CNFB	E32	0000000000000000	CNCOND	E62	0---0----------
ODCA	E08	----------00000	ANSELC	E38	--------1---1111	CNEN0D	E64	0000000000000000
CNPUA	E0A	----------00000	TRISC	E3A	1111111111111111	CNSTATD	E66	0000000000000000
CNPDA	E0C	----------00000	PORTC	E3C	xxxxxxxxxxxxxxxx	CNEN1D	E68	0000000000000000
CNCONA	E0E	0---0----------	LATC	E3E	xxxxxxxxxxxxxxxx	CNFD	E6A	0000000000000000
CNEN0A	E10	----------00000	ODCC	E40	0000000000000000	TRISE	E72	1111111111111111
CNSTATA	E12	----------00000	CNPUC	E42	0000000000000000	PORTE	E74	xxxxxxxxxxxxxxxx
CNEN1A	E14	----------00000	CNPDC	E44	0000000000000000	LATE	E76	xxxxxxxxxxxxxxxx
CNFA	E16	----------00000	CNCONC	E46	0---0----------	ODCE	E78	0000000000000000
ANSELB	E1C	------111---1111	CNEN0C	E48	0000000000000000	CNPUE	E7A	0000000000000000
TRISB	E1E	1111111111111111	CNSTATC	E4A	0000000000000000	CNPDE	E7C	0000000000000000
PORTB	E20	xxxxxxxxxxxxxxxx	CNEN1C	E4C	0000000000000000	CNCONE	E7E	0---0----------
LATB	E22	xxxxxxxxxxxxxxxx	CNFC	E4E	0000000000000000	CNEN0E	E80	0000000000000000
ODCB	E24	0000000000000000	ANSELD	E54	-----1----------	CNSTATE	E82	0000000000000000
CNPUB	E26	0000000000000000	TRISD	E56	1111111111111111	CNEN1E	E84	0000000000000000
CNPDB	E28	0000000000000000	PORTD	E58	xxxxxxxxxxxxxxxx	CNFE	E86	0000000000000000

Legend: x = unknown or indeterminate value; "-" = unimplemented bits. Address and Reset values are in hexadecimal and binary, respectively.

3.3.2 RTSP OPERATION

RTSP allows the user application to program one double instruction word or one row at a time.The double instruction word write blocks and single row write blocks are edge-aligned, from the beginning of program memory, on boundaries of one double instruction word and 64 double instruction words, respectively.

The basic sequence for RTSP programming is to first load two 24-bit instructions into the NVM write latches found in configuration memory space. Refer to Figure 3-3 through Figure 3-4 for write latch addresses. Then, the WR bit in the NVMCON register is set to initiate the write process. The processor stalls (waits) until the programming operation is finished. The WR bit is automatically cleared when the operation is finished.

Double instruction word writes are performed by manually loading both write latches, using TBLWTL and TBLWTH instructions, and then initiating the NVM write while the NVMOPx bits are set to '0x1'. The program space destination address is defined by the NVMADR/U registers.

EXAMPLE 3-1: FLASH WRITE/READ

```
////////Flash write ////////////////////////
//Sample code for writing 0x123456 to address locations  0x10000 / 10002
    NVMCON = 0x4001;
    TBLPAG = 0xFA;                  // write latch upper address
    NVMADR = 0x0000;                // set target write address of general segment
    NVMADRU = 0x0001;
    __builtin_tblwtl(0, 0x3456);    // load write latches
    __builtin_tblwth (0,0x12);

    __builtin_tblwtl(2, 0x3456);    // load write latches
    __builtin_tblwth (2,0x12);

    asm volatile ("disi #5");
    __builtin_write_NVM();
    while(_WR == 1 ) ;


////////////Flash Read///////////////
//Sample code to read the Flash content of address 0x10000
// readDataL/ readDataH variables need to defined
    TBLPAG = 0x0001;
    readDataL = __builtin_tblrdl(0x0000);
    readDataH = __builtin_tblrdh(0x0000);
```

3.5.3 INTERRUPT RESOURCES

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

3.5.3.1 Key Resources

- **"Interrupts"** (DS70000600) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

3.5.4 INTERRUPT CONTROL AND STATUS REGISTERS

The dsPIC33CH128MP508 family devices implement the following registers for the interrupt controller:

- INTCON1
- INTCON2
- INTCON3
- INTCON4
- INTTREG

3.5.4.1 INTCON1 through INTCON4

Global interrupt control functions are controlled from INTCON1, INTCON2, INTCON3 and INTCON4.

INTCON1 contains the Interrupt Nesting Disable bit (NSTDIS), as well as the control and status flags for the processor trap sources.

The INTCON2 register controls external interrupt request signal behavior, contains the Global Interrupt Enable bit (GIE) and the Alternate Interrupt Vector Table Enable bit (AIVTEN).

INTCON3 contains the status flags for the Auxiliary PLL and DO stack overflow status trap sources.

The INTCON4 register contains the Software Generated Hard Trap Status bit (SGHT).

3.5.4.2 IFSx

The IFSx registers maintain all of the interrupt request flags. Each source of interrupt has a status bit, which is set by the respective peripherals or external signal and is cleared via software.

3.5.4.3 IECx

The IECx registers maintain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals.

3.5.4.4 IPCx

The IPCx registers are used to set the Interrupt Priority Level (IPL) for each source of interrupt. Each user interrupt source can be assigned to one of seven priority levels.

3.5.4.5 INTTREG

The INTTREG register contains the associated interrupt vector number and the new CPU Interrupt Priority Level, which are latched into the Vector Number (VECNUM<7:0>) and Interrupt Level bits (ILR<3:0>) fields in the INTTREG register. The new Interrupt Priority Level is the priority of the pending interrupt.

The interrupt sources are assigned to the IFSx, IECx and IPCx registers in the same sequence as they are listed in Table 3-23. For example, INT0 (External Interrupt 0) is shown as having Vector Number 8 and a natural order priority of 0. Thus, the INT0IF bit is found in IFS0<0>, the INT0IE bit in IEC0<0> and the INT0IP<2:0> bits in the first position of IPC0 (IPC0<2:0>).

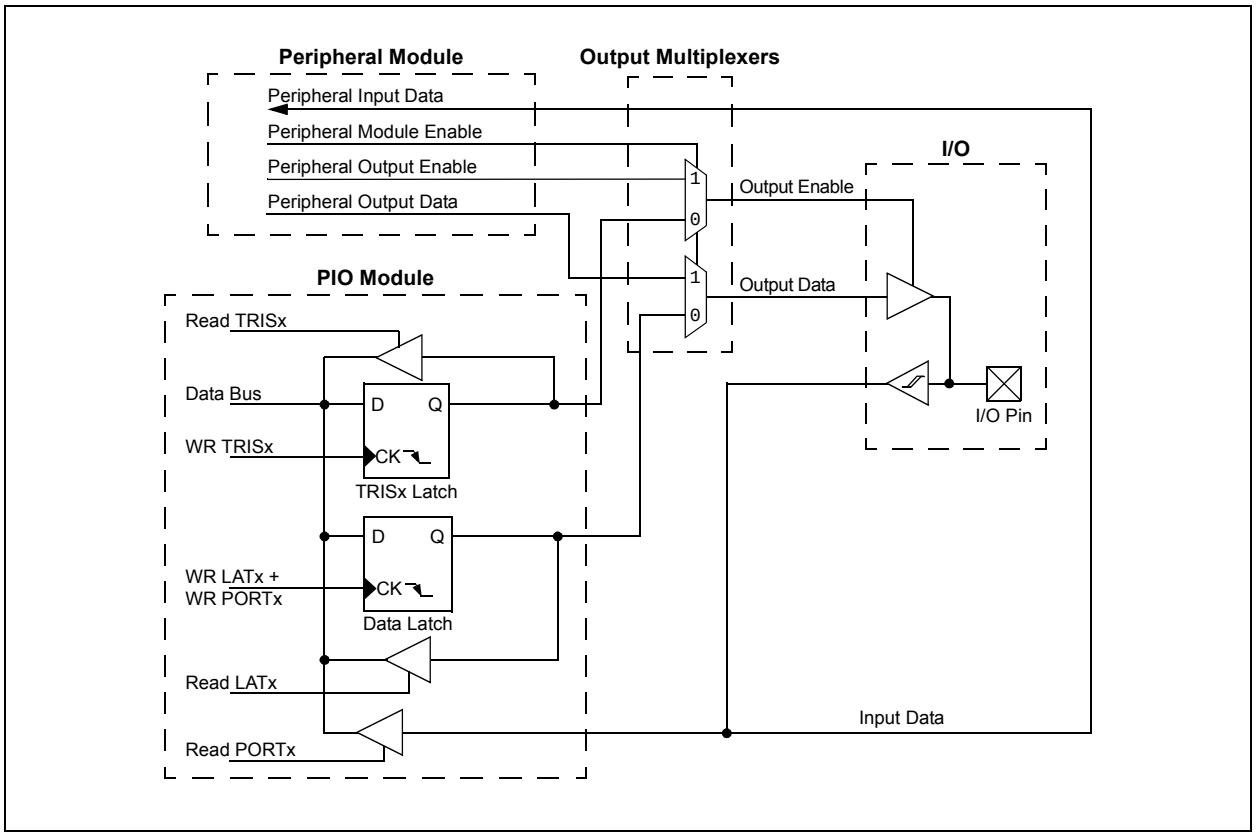
3.5.4.6 Status/Control Registers

Although these registers are not specifically part of the interrupt control hardware, two of the CPU Control registers contain bits that control interrupt functionality. For more information on these registers, refer to **"dsPIC33E Enhanced CPU"** (DS70005158) in the *"dsPIC33/PIC24 Family Reference Manual"*.

- The CPU STATUS Register, SR, contains the IPL<2:0> bits (SR<7:5>). These bits indicate the current CPU Interrupt Priority Level. The user software can change the current CPU Interrupt Priority Level by writing to the IPLx bits.
- The CORCON register contains the IPL3 bit, which together with IPL<2:0>, also indicates the current CPU priority level. IPL3 is a read-only bit so that trap events cannot be masked by the user software.

All Interrupt registers are described in Register 3-18 through Register 3-22 in the following pages.

FIGURE 3-19: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE



REGISTER 3-39: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ICM1R7	ICM1R6	ICM1R5	ICM1R4	ICM1R3	ICM1R2	ICM1R1	ICM1R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TCKI1R7	TCKI1R6	TCKI1R5	TCKI1R4	TCKI1R3	TCKI1R2	TCKI1R1	TCKI1R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **ICM1R<7:0>:** Assign SCCP Capture 1 (ICM1) Input to the Corresponding RPn Pin bits
See Table 3-30.

bit 7-0 **TCKI1<7:0>:** Assign SCCP Timer1 (TCKI1) Input to the Corresponding RPn Pin bits
See Table 3-30.

REGISTER 3-40: RPINR4: PERIPHERAL PIN SELECT INPUT REGISTER 4

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ICM2R7	ICM2R6	ICM2R5	ICM2R4	ICM2R3	ICM2R2	ICM2R1	ICM2R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TCKI2R7	TCKI2R6	TCKI2R5	TCKI2R4	TCKI2R3	TCKI2R2	TCKI2R1	TCKI2R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **ICM2R<7:0>:** Assign SCCP Capture 2 (ICM2) Input to the Corresponding RPn Pin bits
See Table 3-30.

bit 7-0 **TCKI2R<7:0>:** Assign SCCP Timer2 (TCKI2) Input to the Corresponding RPn Pin bits
See Table 3-30.

REGISTER 3-78: RPOR10: PERIPHERAL PIN SELECT OUTPUT REGISTER 10

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP53R5	RP53R4	RP53R3	RP53R2	RP53R1	RP53R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP52R5	RP52R4	RP52R3	RP52R2	RP52R1	RP52R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP53<5:0>:** Peripheral Output Function is Assigned to RP53 Output Pin bits (see Table 3-33 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP52R<5:0>:** Peripheral Output Function is Assigned to RP52 Output Pin bits (see Table 3-33 for peripheral function numbers)

REGISTER 3-79: RPOR11: PERIPHERAL PIN SELECT OUTPUT REGISTER 11

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP55R5	RP55R4	RP55R3	RP55R2	RP55R1	RP55R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP54R5	RP54R4	RP54R3	RP54R2	RP54R1	RP54R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP55R<5:0>:** Peripheral Output Function is Assigned to RP55 Output Pin bits (see Table 3-33 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP54R<5:0>:** Peripheral Output Function is Assigned to RP54 Output Pin bits (see Table 3-33 for peripheral function numbers)

REGISTER 3-97: DMTPSCNTL: DMT POST-CONFIGURE COUNT STATUS REGISTER LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSCNT<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSCNT<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PSCNT<15:0>:** Lower DMT Instruction Count Value Configuration Status bits
This is always the value of the FDMTCNTL Configuration register.

REGISTER 3-98: DMTPSCNTH: DMT POST-CONFIGURE COUNT STATUS REGISTER HIGH

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSCNT<31:24>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSCNT<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PSCNT<31:16>:** Higher DMT Instruction Count Value Configuration Status bits
This is always the value of the FDMTCNTH Configuration register.

REGISTER 3-126: C1TXREQH: CAN TRANSMIT REQUEST REGISTER HIGH

S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0
TXREQ<31:24>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	S/HC-0
TXREQ<23:16>							
bit 7							bit 0

Legend:	S = Settable bit	HC = Hardware Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **TXREQ<31:16>:** Unimplemented

REGISTER 3-127: C1TXREQL: CAN TRANSMIT REQUEST REGISTER LOW

S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0
TXREQ<15:8>							
bit 15							bit 8

S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0s
TXREQ<7:1>							TXREQ0
bit 7							bit 0

Legend:	S = Settable bit	HC = Hardware Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **TXREQ<15:8>:** Unimplemented

bit 7-1 **TXREQ<7:1>:** Message Send Request bits

TXEN = 1 (object configured as a transmit object):
Setting this bit to '1' requests sending a message. The bit will automatically clear when the message(s) queued in the object is (are) successfully sent. This bit can NOT be used for aborting a transmission.

TXEN = 0 (object configured as a receive object):
This bit has no effect.

bit 0 **TXREQ0:** Transmit Queue Message Send Request bit

Setting this bit to '1' requests sending a message. The bit will automatically clear when the message(s) queued in the object is (are) successfully sent. This bit can NOT be used for aborting a transmission.

REGISTER 3-139: C1FIFOUAHx: CAN FIFO USER ADDRESS REGISTER x (x = 1 TO 7) HIGH(1)

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
FIFOUA<31:24>							
bit 15							bit 8

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
FIFOUA<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **FIFOUA<31:16>:** FIFO User Address bits

TXEN = 1 (FIFO configured as a transmit buffer):
A read of this register will return the address where the next message is to be written (FIFO head).

TXEN = 0 (FIFO configured as a receive buffer):
A read of this register will return the address where the next message is to be read (FIFO tail).

Note 1: This register is not ensured to read correctly in Configuration mode and should only be accessed when the module is not in Configuration mode.

REGISTER 3-140: C1FIFOUALx: CAN FIFO USER ADDRESS REGISTER x (x = 1 TO 7) LOW(1)

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
FIFOUA<15:8>							
bit 15							bit 8

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
FIFOUA<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **FIFOUA<15:0>:** FIFO User Address bits

TXEN = 1 (FIFO configured as a transmit buffer):
A read of this register will return the address where the next message is to be written (FIFO head).

TXEN = 0 (FIFO configured as a receive buffer):
A read of this register will return the address where the next message is to be read (FIFO tail).

Note 1: This register is not ensured to read correctly in Configuration mode and should only be accessed when the module is not in Configuration mode.

REGISTER 3-173: ADMOD1L: ADC INPUT MODE CONTROL REGISTER 1 LOW

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	SIGN20
bit 15							bit 8

U-0	R/W-0	U-0	R/W-0	U-0	R/W-0	U-0	R/W-0
—	SIGN19	—	SIGN18	—	SIGN17	—	SIGN16
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-9 **Unimplemented:** Read as '0'

bit 8 **SIGN20:** Output Data Sign for Corresponding Analog Input bits
1 = Channel output data is signed
0 = Channel output data is unsigned

bit 7 **Unimplemented:** Read as '0'

bit 6 **SIGN19:** Output Data Sign for Corresponding Analog Input bits
1 = Channel output data is signed
0 = Channel output data is unsigned

bit 5 **Unimplemented:** Read as '0'

bit 4 **SIGN18:** Output Data Sign for Corresponding Analog Input bits
1 = Channel output data is signed
0 = Channel output data is unsigned

bit 3 **Unimplemented:** Read as '0'

bit 2 **SIGN17:** Output Data Sign for Corresponding Analog Input bits
1 = Channel output data is signed
0 = Channel output data is unsigned

bit 1 **Unimplemented:** Read as '0'

bit 0 **SIGN16:** Output Data Sign for Corresponding Analog Input bits
1 = Channel output data is signed
0 = Channel output data is unsigned

TABLE 3-46: PTG INPUT DESCRIPTIONS

PTG Input Number	PTG Input Description
PTG Trigger Input 0	Trigger Input from Master PWM Channel 1
PTG Trigger Input 1	Trigger Input from Master PWM Channel 2
PTG Trigger Input 2	Trigger Input from Master PWM Channel 3
PTG Trigger Input 3	Trigger Input from Master PWM Channel 4
PTG Trigger Input 4	Trigger Input from Slave PWM Channel 1
PTG Trigger Input 5	Trigger Input from Slave PWM Channel 2
PTG Trigger Input 6	Trigger Input from Slave PWM Channel 3
PTG Trigger Input 7	Trigger Input from Master SCCP4
PTG Trigger Input 8	Trigger Input from Slave SCCP4
PTG Trigger Input 9	Trigger Input from Master Comparator 1
PTG Trigger Input 10	Trigger Input from Slave Comparator 1
PTG Trigger Input 11	Trigger Input from Slave Comparator 2
PTG Trigger Input 12	Trigger Input from Slave Comparator 3
PTG Trigger Input 13	Trigger Input Master ADC Done Group Interrupt
PTG Trigger Input 14	Trigger Input Slave ADC Done Group Interrupt
PTG Trigger Input 15	Trigger Input from INT2 PPS

TABLE 3-47: PTG OUTPUT DESCRIPTIONS

PTG Output Number	PTG Output Description
PTGO0 to PTGO11	Reserved
PTGO12	Trigger for Master ADC TRGSRC<30>
PTGO13	Trigger for Slave ADC TRGSRC<30>
PTGO16 to PTGO23	Reserved
PTGO24	PPS Master Output RP46
PTGO25	PPS Master Output RP47
PTGO26	PPS Master Input RP6
PTGO27	PPS Master Input RP7
PTGO28	PPS Slave Output RP46
PTGO29	PPS Slave Output RP47
PTGO30	PPS Slave Input RP6
PTGO31	PPS Slave Input RP7

TABLE 4-11: SLAVE SFR BLOCK B00h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
ADC			ADCMP1LO	B44	0000000000000000	ADTRIG2L	B88	0000000000000000
ADCON1L	B00	000-00000---000	ADCMP1HI	B46	0000000000000000	ADTRIG2H	B8A	0000000000000000
ADCON1H	B02	--------011-----	ADCMP2ENL	B48	0000000000000000	ADTRIG3L	B8C	0000000000000000
ADCON2L	B04	00-0-00000000000	ADCMP2ENH	B4A	----------00000	ADTRIG3H	B8E	0000000000000000
ADCON2H	B06	00-0000000000000	ADCMP2LO	B4C	0000000000000000	ADTRIG4L	B90	0000000000000000
ADCON3L	B08	00000x0000000000	ADCMP2HI	B4E	0000000000000000	ADTRIG4H	B92	0000000000000000
ADCON3H	B0A	000000000------	ADCMP3ENL	B50	0000000000000000	ADTRIG5L	B94	000-----00000000
ADCON4L	B0C	0-----000-----xx	ADCMP3ENH	B52	----------00000	ADCMP0CON	BA0	0000000000000000
ADCON4H	B0E	00----------0000	ADCMP3LO	B54	0000000000000000	ADCMP1CON	BA4	0000000000000000
ADMOD0L	B10	-0-0-0-0-0-0-0-0	ADCMP3HI	B56	0000000000000000	ADCMP2CON	BA8	0000000000000000
ADIEL	B20	xxxxxxxxxxxxxxxx	ADFL0DAT	B68	0000000000000000	ADCMP3CON	BAC	0000000000000000
ADIEH	B22	----------xxxxx	ADFL0CON	B6A	0xx0000000000000	ADLVLTRGL	BD0	0000000000000000
ADCSS1L	B28	0000000000000000	ADFL1DAT	B6C	0000000000000000	ADLVLTRGH	BD2	----------xxxxx
ADCSS1H	B2A	------------000	ADFL1CON	B6E	0xx0000000000000	ADCORE0L	BD4	0000000000000000
ADSTATL	B30	0000000000000000	ADFL2DAT	B70	0000000000000000	ADCORE0H	BD6	0000001100000000
ADSTATH	B32	----------00000	ADFL2CON	B72	0xx0000000000000	ADCORE1L	BD8	0000000000000000
ADCMP0ENL	B38	0000000000000000	ADFL3DAT	B74	0000000000000000	ADCORE1H	BDA	0000001100000000
ADCMP0ENH	B3A	----------00000	ADFL3CON	B76	0xx0000000000000	ADEIEL	BF0	xxxxxxxxxxxxxxxx
ADCMP0LO	B3C	0000000000000000	ADTRIG0L	B80	0000000000000000	ADEIEH	BF2	----------xxxxx
ADCMP0HI	B3E	0000000000000000	ADTRIG0H	B82	0000000000000000	ADEISTATL	BF8	xxxxxxxxxxxxxxxx
ADCMP1ENL	B40	0000000000000000	ADTRIG1L	B84	0000000000000000	ADEISTATH	BFA	----------xxxxx
ADCMP1ENH	B42	----------00000	ADTRIG1H	B86	0000000000000000			

Legend: x = unknown or indeterminate value; "-" = unimplemented bits. Address and Reset values are in hexadecimal and binary, respectively.

TABLE 4-12: SLAVE SFR BLOCK C00h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
ADC (Continued)			ADCBUF12	C24	0000000000000000	SLP1CONL	C90	0000000000000000
ADCON5L	C00	0-------0-------	ADCBUF13	C26	0000000000000000	SLP1CONH	C92	0---000---------
ADCON5H	C02	0---xxxx0-------	ADCBUF14	C28	0000000000000000	SLP1DAT	C94	0000000000000000
ADCAL0L	C04	0000000000000000	ADCBUF15	C2A	0000000000000000	DAC2CONL	C98	000--000x0000000
ADCAL1H	C0A	00000-00-000----	ADCBUF16	C2C	0000000000000000	DAC2CONH	C9A	------0000000000
ADCBUF0	C0C	0000000000000000	ADCBUF17	C2E	0000000000000000	DAC2DATL	C9C	0000000000000000
ADCBUF1	C0E	0000000000000000	ADCBUF18	C30	0000000000000000	DAC2DATH	C9E	0000000000000000
ADCBUF2	C10	0000000000000000	ADCBUF19	C32	0000000000000000	SLP2CONL	CA0	0000000000000000
ADCBUF3	C12	0000000000000000	**DAC**			SLP2CONH	CA2	0---000---------
ADCBUF4	C14	0000000000000000	DACCTRL1L	C80	000-----0000-000	SLP2DAT	CA4	0000000000000000
ADCBUF5	C16	0000000000000000	DACCTRL2L	C84	------0001010101	DAC3CONL	CA8	000--000x0000000
ADCBUF6	C18	0000000000000000	DACCTRL2H	C86	------0010001010	DAC3CONH	CAA	------0000000000
ADCBUF7	C1A	0000000000000000	DAC1CONL	C88	000--000x0000000	DAC3DATL	CAC	0000000000000000
ADCBUF8	C1C	0000000000000000	ADCBUF12	C24	0000000000000000	DAC3DATH	CAE	0000000000000000
ADCBUF9	C1E	0000000000000000	DAC1CONH	C8A	------0000000000	SLP3CONL	CB0	0000000000000000
ADCBUF10	C20	0000000000000000	DAC1DATL	C8C	0000000000000000	SLP3CONH	CB2	0---000---------
ADCBUF11	C22	0000000000000000	DAC1DATH	C8E	0000000000000000	SLP3DAT	CB4	0000000000000000

Legend: x = unknown or indeterminate value; "-" = unimplemented bits. Address and Reset values are in hexadecimal and binary, respectively.

4.2.8.1 Data Access from Program Memory Using Table Instructions

The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the lower word of any address within the Program Space without going through Data Space. The TBLRDH and TBLWTH instructions are the only method to read or write the upper eight bits of a Program Space word as data.

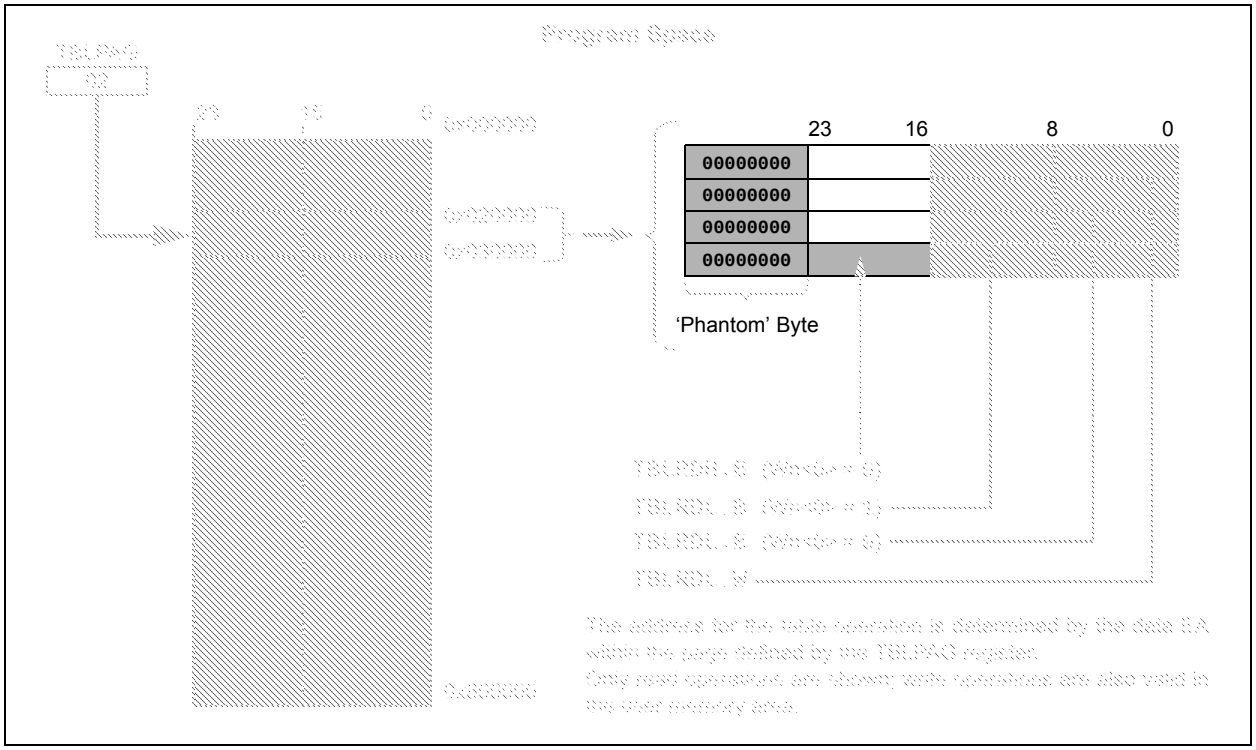
This allows program memory addresses to directly map to Data Space addresses. Program memory can thus be regarded as two 16-bit wide word address spaces, residing side by side, each with the same address range. TBLRDL and TBLWTL access the space that contains the least significant data word. TBLRDH and TBLWTH access the space that contains the upper data byte.

Two table instructions are provided to read byte or word-sized (16-bit) data from Program Space. Both function as either byte or word operations.

- TBLRDL (Table Read Low):
  - In Word mode, this instruction maps the lower word of the Program Space location (P<15:0>) to a data address (D<15:0>).
  - In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when Byte Select is '1'; the lower byte is selected when it is '0'.
- TBLRDH (Table Read High):
  - In Word mode, this instruction maps the entire upper word of a program address (P<23:16>) to a data address. The 'phantom' byte (D<15:8>) is always '0'.
  - In Byte mode, either the upper or lower byte of the upper program word is mapped to the lower byte of a data address. The upper byte is selected when Byte Select is '1'; the lower byte is selected when it is '0'. When the upper byte is selected, the 'phantom' byte is read as '0'.

In a similar fashion, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a Program Space address. For these writes, data is written to a set of NVM latches and subsequently copied to the Program Space address using an NVM write operation. The details of their operation are explained in **Section 4.3.2 "RTSP Operation"**.

FIGURE 4-12: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS



REGISTER 4-57: RPINR45: PERIPHERAL PIN SELECT INPUT REGISTER 45

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CLCINAR7	CLCINAR6	CLCINAR5	CLCINAR4	CLCINAR3	CLCINAR2	CLCINAR1	CLCINAR0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **CLCINAR<7:0>:** Assign CLC Input A (S1CLCINA) to the Corresponding S1RPn Pin bits
See Table 4-27.

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 4-58: RPINR46: PERIPHERAL PIN SELECT INPUT REGISTER 46

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CLCINCR7	CLCINCR6	CLCINCR5	CLCINCR4	CLCINCR3	CLCINCR2	CLCINCR1	CLCINCR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CLCINBR7	CLCINBR6	CLCINBR5	CLCINBR4	CLCINBR3	CLCINBR2	CLCINBR1	CLCINBR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **CLCINCR<7:0>:** Assign CLC Input C (S1CLCINC) to the Corresponding S1RPn Pin bits
See Table 4-27.

bit 7-0 **CLCINBR<7:0>:** Assign CLC Input B (S1CLCINB) to the Corresponding S1RPn Pin bits
See Table 4-27.

7.0 POWER-SAVING FEATURES (MASTER AND SLAVE)

Note 1: This data sheet summarizes the features of the dsPIC33CH128MP508 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Watchdog Timer and Power-Saving Modes"** (DS70615) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com). The power saving section is only relevant for this device. The WDT has its own family reference manual section.

2: This chapter is applicable to both the Master core and the Slave core. There are registers associated with PMD that are listed separately for Master and Slave at the end of this section. Other features related to power saving that are discussed are applicable to both the Master and Slave core.

3: All associated register names are the same on the Master core and the Slave core. The Slave code will be developed in a separate project in MPLAB® X IDE with the device selection, dsPIC33CH128MP508**S1**, where **S1** indicates the Slave device.

The dsPIC33CH128MP508 family devices provide the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of peripherals being clocked constitutes lower consumed power.

dsPIC33CH128MP508 family devices can manage power consumption in four ways:

- Clock Frequency
- Instruction-Based Sleep and Idle modes
- Software-Controlled Doze mode
- Selective Peripheral Control in Software

Combinations of these methods can be used to selectively tailor an application's power consumption while still maintaining critical application features, such as timing-sensitive communications.

7.1 Clock Frequency and Clock Switching

The dsPIC33CH128MP508 family devices allow a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSCx bits (OSCCON<10:8>). The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 6.0 "Oscillator with High-Frequency PLL"**.

7.2 Instruction-Based Power-Saving Modes

The dsPIC33CH128MP508 family devices have two special power-saving modes that are entered through the execution of a special PWRSAV instruction. Sleep mode stops clock operation and halts all code execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The assembler syntax of the PWRSAV instruction is shown in Example 7-1.

Note: SLEEP_MODE and IDLE_MODE are constants defined in the assembler include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to "wake-up".

EXAMPLE 7-1: PWRSAV INSTRUCTION SYNTAX

```
PWRSAV  #SLEEP_MODE    ; Put the device into Sleep mode
PWRSAV  #IDLE_MODE     ; Put the device into Idle mode
```

7.2.1 SLEEP MODE

The following occurs in Sleep mode:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption is reduced to a minimum, provided that no I/O pin is sourcing current.
- The Fail-Safe Clock Monitor does not operate, since the system clock source is disabled.
- The LPRC clock continues to run in Sleep mode if the WDT is enabled.
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode.
- Some device features or peripherals can continue to operate. This includes items such as the Input Change Notification on the I/O ports or peripherals that use an External Clock input.
- Any peripheral that requires the system clock source for its operation is disabled.

The device wakes up from Sleep mode on any of the these events:

- Any interrupt source that is individually enabled
- Any form of device Reset
- A WDT time-out

On wake-up from Sleep mode, the processor restarts with the same clock source that was active when Sleep mode was entered.

For optimal power savings, the internal regulator and the Flash regulator can be configured to go into stand-by when Sleep mode is entered by clearing the VREGS (RCON<8>) bit.

7.2.2 IDLE MODE

The following occurs in Idle mode:

- The CPU stops executing instructions.
- The WDT is automatically cleared.
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see **Section 7.4 “Peripheral Module Disable”**).
- If the WDT or FSCM is enabled, the LPRC also remains active.

The device wakes from Idle mode on any of these events:

- Any interrupt that is individually enabled
- Any device Reset
- A WDT time-out

On wake-up from Idle mode, the clock is reapplied to the CPU and instruction execution will begin (2-4 clock cycles later), starting with the instruction following the PWRSAV instruction or the first instruction in the ISR.

All peripherals also have the option to discontinue operation when Idle mode is entered to allow for increased power savings. This option is selectable in the control register of each peripheral; for example, the SIDL bit in the Timer1 Control register (T1CON<13>).

7.2.3 INTERRUPTS COINCIDENT WITH POWER SAVE INSTRUCTIONS

Any interrupt that coincides with the execution of a PWRSAV instruction is held off until entry into Sleep or Idle mode has completed. The device then wakes up from Sleep or Idle mode.

REGISTER 7-11: PMD2: SLAVE PERIPHERAL MODULE DISABLE 2 CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	CCP4MD	CCP3MD	CCP2MD	CCP1MD
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **CCP4MD:** SCCP4 Module Disable bit
1 = SCCP4 module is disabled
0 = SCCP4 module is enabled

bit 2 **CCP3MD:** SCCP3 Module Disable bit
1 = SCCP3 module is disabled
0 = SCCP3 module is enabled

bit 1 **CCP2MD:** SCCP2 Module Disable bit
1 = SCCP2 module is disabled
0 = SCCP2 module is enabled

bit 0 **CCP1MD:** SCCP1 Module Disable bit
1 = SCCP1 module is disabled
0 = SCCP1 module is enabled

12.1 QEI Control and Status Registers

REGISTER 12-1: QEIxCON: QEIx CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIEN	—	QEISIDL	PIMOD2	PIMOD1	PIMOD0	IMV1	IMV0
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	INTDIV2	INTDIV1	INTDIV0	CNTPOL	GATEN	CCM1	CCM0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **QEIEN:** Quadrature Encoder Interface Module Enable bit
1 = QEI module is enabled
0 = QEI module is disabled; however, SFRs can be read or written

bit 14 **Unimplemented:** Read as '0'

bit 13 **QEISIDL:** QEI Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-10 **PIMOD<2:0>:** Position Counter Initialization Mode Select bits
111 = Modulo Count mode for position counter and every Index event resets the position counter
110 = Modulo Count mode for position counter
101 = Resets the position counter when the position counter equals the QEIxGEC register
100 = Second Index event after Home event initializes the position counter with the contents of the QEIxIC register
011 = First Index event after Home event initializes the position counter with the contents of the QEIxIC register
010 = Next Index input event initializes the position counter with the contents of the QEIxIC register
001 = Every Index input event resets the position counter
000 = Index input event does not affect the position counter

bit 9-8 **IMV<1:0>:** Index Match Value bits
11 = Index match occurs when QEBx = 1 and QEAx = 1
10 = Index match occurs when QEBx = 1 and QEAx = 0
01 = Index match occurs when QEBx = 0 and QEAx = 1
00 = Index match occurs when QEBx = 0 and QEAx = 0

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **INTDIV<2:0>:** Timer Input Clock Prescale Select bits (interval timer, main timer (position counter), velocity counter and Index counter internal clock divider select)
111 = 1:128 prescale value
110 = 1:64 prescale value
101 = 1:32 prescale value
100 = 1:16 prescale value
011 = 1:8 prescale value
010 = 1:4 prescale value
001 = 1:2 prescale value
000 = 1:1 prescale value

bit 3 **CNTPOL:** Position, Velocity and Index Counter/Timer Direction Select bit
1 = Counter direction is negative unless modified by an external up/down signal
0 = Counter direction is positive unless modified by an external up/down signal

REGISTER 12-3: QEIxIOCH: QEIx I/O CONTROL HIGH REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	HCAPEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-1 **Unimplemented:** Read as ‘0’

bit 0 **HCAPEN:** Position Counter Input Capture by Home Event Enable bit
1 = HOMEx input event (positive edge) triggers a position capture event
0 = HOMEx input event (positive edge) does not trigger a position capture event