Microchip Technology - DSPIC33CH64MP202-I/2N Datasheet

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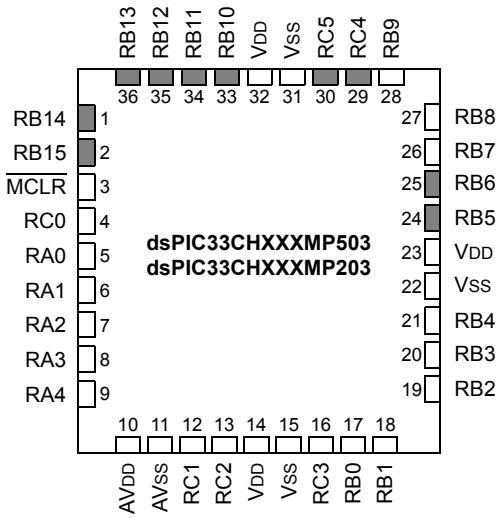
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit Dual-Core
Speed	180MHz, 200MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	21
Program Memory Size	88KB (88K x 8)
Program Memory Type	FLASH, PRAM
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 23x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UQFN Exposed Pad
Supplier Device Package	28-UQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ch64mp202-i-2n

Pin Diagrams (Continued)

36-Pin UQFN(1,2)



Note 1: **Shaded pins** are up to 5.5 VDC tolerant (refer to Table 3-28 and Table 4-25). For the list of analog ports, refer to Table 3-27 and Table 4-24.

2: The large center pad on the bottom of the package may be left floating or connected to VSS. The four-corner anchor pads are internally connected to the large bottom pad, and therefore, must be connected to the same net as the large center pad.

REGISTER 3-17: CORCON: CORE CONTROL REGISTER(1)

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0
VAR	—	US1	US0	EDT	DL2	DL1	DL0
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R-0	R/W-0	R/W-0
SATA	SATB	SATDW	ACCSAT	IPL3(2)	SFA	RND	IF
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1'= Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **VAR:** Variable Exception Processing Latency Control bit
1 = Variable exception processing is enabled
0 = Fixed exception processing is enabled

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3(2)
1 = CPU Interrupt Priority Level is greater than 7
0 = CPU Interrupt Priority Level is 7 or less

Note 1: For complete register details, see Register 3-2.
2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

3.7 Deadman Timer (DMT) (Master Only)

Note 1: This data sheet summarizes the features of the dsPIC33CH128MP508 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Deadman Timer (DMT)"** (DS70005155) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: The Slave core does not have any DMT module; only the Master has the DMT.

The primary function of the Deadman Timer (DMT) is to interrupt the processor in the event of a software malfunction. The DMT, which works on the system clock, is a free-running instruction fetch timer, which is clocked whenever an instruction fetch occurs, until a count match occurs. Instructions are not fetched when the processor is in Sleep mode.

DMT can be enabled in the Configuration fuse or by software in the DMTCON register by setting the ON bit. The DMT consists of a 32-bit counter with a time-out count match value, as specified by the two 16-bit Configuration Fuse registers: FDMTCNTL and FDMTCNTH.

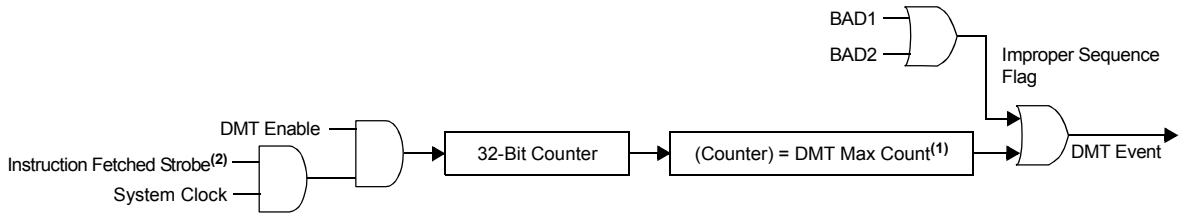
A DMT is typically used in mission-critical and safety-critical applications, where any single failure of the software functionality and sequencing must be detected. Table 3-41 shows an overview of the DMT module.

TABLE 3-41: DMT MODULE OVERVIEW

	No. of DMT Modules	Identical (Modules)
Master Core	1	No
Slave Core	None	NA

Figure 3-22 shows a block diagram of the Deadman Timer module.

FIGURE 3-22: DEADMAN TIMER BLOCK DIAGRAM



Note 1: DMT Max Count is controlled by the initial value of the FDMTCNTL and FDMTCNTH Configuration registers.

2: DMT window interval is controlled by the value of the FDMTIVTL and FDMTIVTH Configuration registers.

REGISTER 3-94: DMTSTAT: DEADMAN TIMER STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

HC/R-0	HC/R-0	HC/R-0	U-0	U-0	U-0	U-0	R-0
BAD1	BAD2	DMTEVENT	—	—	—	—	WINOPN
bit 7							bit 0

Legend:	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **BAD1:** Deadman Timer Bad STEP1<7:0> Value Detect bit
1 = Incorrect STEP1<7:0> value was detected
0 = Incorrect STEP1<7:0> value was not detected

bit 6 **BAD2:** Deadman Timer Bad STEP2<7:0> Value Detect bit
1 = Incorrect STEP2<7:0> value was detected
0 = Incorrect STEP2<7:0> value was not detected

bit 5 **DMTEVENT:** Deadman Timer Event bit
1 = Deadman Timer event was detected (counter expired, or bad STEP1<7:0> or STEP2<7:0> value was entered prior to counter increment)
0 = Deadman Timer event was not detected

bit 4-1 **Unimplemented:** Read as '0'

bit 0 **WINOPN:** Deadman Timer Clear Window bit
1 = Deadman Timer clear window is open
0 = Deadman Timer clear window is not open

REGISTER 3-153: C1FLTOBJxH: CAN FILTER OBJECT REGISTER x HIGH (x = 0 TO 15)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	EXIDE	SID11	EID17	EID16	EID15	EID14	EID13
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EID12	EID11	EID10	EID9	EID8	EID7	EID6	EID5
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **EXIDE:** Extended Identifier Enable bit

If MIDE = 1:

1 = Matches only messages with Extended Identifier addresses
0 = Matches only messages with Standard Identifier addresses

bit 13 **SID11:** Standard Identifier Filter bit

bit 12-0 **EID<17:5>:** Extended Identifier Filter bits

In DeviceNet™ mode, these are the filter bits for the first two data bytes.

REGISTER 3-154: C1FLTOBJxL: CAN FILTER OBJECT REGISTER x LOW (x = 0 TO 15)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EID4	EID3	EID2	EID1	EID0	SID10	SID9	SID8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 **EID<4:0>:** Extended Identifier Filter bits

In DeviceNet™ mode, these are the filter bits for the first two data bytes.

bit 10-0 **SID<10:0>:** Standard Identifier Filter bits

3.10.2 PTG CONTROL/STATUS REGISTERS

REGISTER 3-183: PTGCST: PTG CONTROL/STATUS LOW REGISTER

R/W-0	U-0	R/W-0	R/W-0	U-0	HC/R/W-0	R/W-0	R/W-0
PTGEN	—	PTGSIDL	PTGTOGL	—	PTGSWT(2)	PTGSSEN(3)	PTGIVIS
bit 15							bit 8

HC/R/W-0	HS/R/W-0	HS/HC/R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
PTGSTRT	PTGWDTO	PTGBUSY	—	—	—	PTGITM1(1)	PTGITM0(1)
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PTGEN:** PTG Enable bit
1 = PTG is enabled
0 = PTG is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **PTGSIDL:** PTG Freeze in Debug Mode bit
1 = Halts PTG operation when device is Idle
0 = PTG operation continues when device is Idle

bit 12 **PTGTOGL:** PTG Toggle Trigger Output bit
1 = Toggles state of TRIG output for each execution of PTGTRIG
0 = Generates a single TRIG pulse for each execution of PTGTRIG

bit 11 **Unimplemented:** Read as '0'

bit 10 **PTGSWT:** PTG Software Trigger bit(2)
1 = Toggles state of TRIG output for each execution of PTGTRIG
0 = Generates a single TRIG pulse for each execution of PTGTRIG

bit 9 **PTGSSEN:** PTG Single-Step Command bit(3)
1 = Enables single step when in Debug mode
0 = Disables single step

bit 8 **PTGIVIS:** PTG Counter/Timer Visibility bit
1 = Reading the PTGSDLIM, PTGCxLIM or PTGTxLIM registers returns the current values of their corresponding Counter/Timer registers (PTGSDLIM, PTGCxLIM and PTGTxLIM)
0 = Reading the PTGSDLIM, PTGCxLIM or PTGTxLIM registers returns the value of these Limit registers

bit 7 **PTGSTRT:** PTG Start Sequencer bit
1 = Starts to sequentially execute the commands (Continuous mode)
0 = Stops executing the commands

bit 6 **PTGWDTO:** PTG Watchdog Timer Time-out Status bit
1 = PTG Watchdog Timer has timed out
0 = PTG Watchdog Timer has not timed out

bit 5 **PTGBUSY:** PTG State Machine Busy bit
1 = PTG is running on the selected clock source; no SFR writes are allowed to PTGCLK<2:0> or PTGDIV<4:0>
0 = PTG state machine is not running

bit 4-2 **Unimplemented:** Read as '0'

Note 1: These bits apply to the PTGWHI and PTGWLO commands only.
2: This bit is only used with the PTGCTRL Step command software trigger option.
3: The PTGSSEN bit may only be written when in Debug mode.

4.1.5 PROGRAMMER'S MODEL

The programmer's model for the dsPIC33CH128MP508S1 family is shown in Figure 4-2. All registers in the programmer's model are memory-mapped and can be manipulated directly by instructions. Table 4-1 lists a description of each register.

In addition to the registers contained in the programmer's model, the dsPIC33CH128MP508S1 devices contain control registers for Modulo Addressing, Bit-Reversed Addressing and interrupts. These registers are described in subsequent sections of this document.

All registers associated with the programmer's model are memory-mapped, as shown in Figure 4-3.

TABLE 4-1: PROGRAMMER'S MODEL REGISTER DESCRIPTIONS

Register(s) Name	Description
W0 through W15(1)	Working Register Array
W0 through W14(1)	Alternate 1 Working Register Array
W0 through W14(1)	Alternate 2 Working Register Array
W0 through W14(1)	Alternate 3 Working Register Array
W0 through W14(1)	Alternate 4 Working Register Array
ACCA, ACCB	40-Bit DSP Accumulators (Additional 4 Alternate Accumulators)
PC	23-Bit Program Counter
SR	ALU and DSP Engine STATUS Register
SPLIM	Stack Pointer Limit Value Register
TBLPAG	Table Memory Page Address Register
DSRPAG	Extended Data Space (EDS) Read Page Register
RCOUNT	REPEAT Loop Counter Register
DCOUNT	DO Loop Counter Register
DOSTARTH(2), DOSTARTL(2)	DO Loop Start Address Register (High and Low)
DOENDH, DOENDL	DO Loop End Address Register (High and Low)
CORCON	Contains DSP Engine, DO Loop Control and Trap Status bits

Note 1: Memory-mapped W0 through W14 represent the value of the register in the currently active CPU context.

2: The DOSTARTH and DOSTARTL registers are read-only.

TABLE 4-23: SLAVE INTERRUPT PRIORITY REGISTERS (CONTINUED)

Register	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IPC36	—	—	—	—	—	—	—	—	—	MSTBRKIP2	MSTBRKIP1	MSTBRKIP0	—	—	—	—
IPC37	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
IPC38	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
IPC39	—	—	—	—	—	—	—	—	—	—	—	—	—	MCLKFIP2	MCLKFIP1	MCLKFIP0
IPC40	—	—	—	—	—	—	—	—	—	ADC1IP2	ADC1IP1	ADC1IP0	—	ADC0IP2	ADC0IP1	ADC0IP0
IPC41	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
IPC42	—	PEVTCIP2	PEVTCIP1	PEVTCIP0	—	PEVTBIP2	PEVTBIP1	PEVTBIP0	—	PEVTAIP2	PEVTAIP1	PEVTAIP0	—	ADFIFOIP2	ADFIFOIP1	ADFIFOIP0
IPC43	—	CLC3PIP2	CLC3PIP1	CLC3PIP0	—	PEVTFIP2	PEVTFIP1	PEVTFIP0	—	PEVTEIP2	PEVTEIP1	PEVTEIP0	—	PEVTDIP2	PEVTDIP1	PEVTDIP0
IPC44	—	CLC3NIP2	CLC3NIP1	CLC3NIP0	—	CLC2NIP2	CLC2NIP1	CLC2NIP0	—	CLC1NIP2	CLC1NIP1	CLC1NIP0	—	CLC4PIP2	CLC4PIP1	CLC4PIP0
IPC45	—	—	—	—	—	—	—	—	—	—	—	—	—	CLC4NIP2	CLC4NIP1	CLC4NIP0
IPC46	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
IPC47	—	—	—	—	—	—	—	—	—	U1EVTIP2	U1EVTIP1	U1EVTIP0	—	—	—	—

REGISTER 4-19: INTCON2: SLAVE INTERRUPT CONTROL REGISTER 2

R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
GIE	DISI	SWTRAP	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	INT3EP	INT2EP	INT1EP	INT0EP
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **GIE:** Global Interrupt Enable bit
1 = Interrupts and associated IE bits are enabled
0 = Interrupts are disabled, but traps are still enabled

bit 14 **DISI:** DISI Instruction Status bit
1 = DISI instruction is active
0 = DISI instruction is not active

bit 13 **SWTRAP:** Software Trap Status bit
1 = Software trap is enabled
0 = Software trap is disabled

bit 12-4 **Unimplemented:** Read as '0'

bit 3 **INT3EP:** External Interrupt 3 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 2 **INT2EP:** External Interrupt 2 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 1 **INT1EP:** External Interrupt 1 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 0 **INT0EP:** External Interrupt 0 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

REGISTER 4-82: RPOR22: PERIPHERAL PIN SELECT OUTPUT REGISTER 22

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP175R5(1)	RP175R4(1)	RP175R3(1)	RP175R2(1)	RP175R1(1)	RP175R0(1)
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP174R5(1)	RP174R4(1)	RP174R3(1)	RP174R2(1)	RP174R1(1)	RP174R0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP175R<5:0>:** Peripheral Output Function is Assigned to S1RP175 Output Pin bits(1)
(see Table 4-31 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP174R<5:0>:** Peripheral Output Function is Assigned to S1RP174 Output Pin bits(1)
(see Table 4-31 for peripheral function numbers)

Note 1: These are virtual output ports.

REGISTER 4-94: ADCOREXH: DEDICATED ADC CORE x CONTROL REGISTER HIGH (x = 0 TO 1)

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	EISEL2	EISEL1	EISEL0	RES1	RES2
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-10 **EISEL<2:0>:** ADC Core x Early Interrupt Time Selection bits
111 = Early interrupt is set and an interrupt is generated 8 TADCORE clocks prior to when the data is ready
110 = Early interrupt is set and an interrupt is generated 7 TADCORE clocks prior to when the data is ready
101 = Early interrupt is set and an interrupt is generated 6 TADCORE clocks prior to when the data is ready
100 = Early interrupt is set and an interrupt is generated 5 TADCORE clocks prior to when the data is ready
011 = Early interrupt is set and an interrupt is generated 4 TADCORE clocks prior to when the data is ready
010 = Early interrupt is set and an interrupt is generated 3 TADCORE clocks prior to when the data is ready
001 = Early interrupt is set and an interrupt is generated 2 TADCORE clocks prior to when the data is ready
000 = Early interrupt is set and an interrupt is generated 1 TADCORE clock prior to when the data is ready

bit 9-8 **RES<1:0>:** ADC Core x Resolution Selection bits
11 = 12-bit resolution
10 = 10-bit resolution
01 = 8-bit resolution(1)
00 = 6-bit resolution(1)

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **ADCS<6:0>:** ADC Core x Input Clock Divider bits
These bits determine the number of Source Clock Periods (TCORESRC) for one Core Clock Period (TADCORE).
1111111 = 254 Source Clock Periods
...
0000011 = 6 Source Clock Periods
0000010 = 4 Source Clock Periods
0000001 = 2 Source Clock Periods
0000000 = 2 Source Clock Periods

Note 1: For the 6-bit ADC core resolution (RES<1:0> = 00), the EISEL<2:0> bits settings, from '100' to '111', are not valid and should not be used. For the 8-bit ADC core resolution (RES<1:0> = 01), the EISEL<2:0> bits settings, '110' and '111', are not valid and should not be used.

REGISTER 4-99: ADEISTATL: ADC EARLY INTERRUPT STATUS REGISTER LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EISTAT<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EISTAT<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **EISTAT<15:0>:** Early Interrupt Status for Corresponding Analog Inputs bits
1 = Early interrupt was generated
0 = Early interrupt was not generated since the last ADCBUFx read

REGISTER 4-100: ADEISTATH: ADC EARLY INTERRUPT STATUS REGISTER HIGH

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	EISTAT<20:16>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as ‘0’

bit 4-0 **EISTAT<20:16>:** Early Interrupt Status for Corresponding Analog Inputs bits
1 = Early interrupt was generated
0 = Early interrupt was not generated since the last ADCBUFx read

REGISTER 4-106: ADTRIGnL/ADTRIGnH: ADC CHANNEL TRIGGER n(x) SELECTION REGISTERS LOW AND HIGH (x = 0 TO 19; n = 0 TO 4)

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	TRGSRC(x+1)4	TRGSRC(x+1)3	TRGSRC(x+1)2	TRGSRC(x+1)1	TRGSRC(x+1)0
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	TRGSRCx4	TRGSRCx3	TRGSRCx2	TRGSRCx1	TRGSRCx0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **TRGSRC(x+1)<4:0>:** Trigger Source Selection for Corresponding Analog Inputs bits (TRGSRC1 to TRGSRC19 – Odd)

11111 = ADTRG31 (PPS input)
11110 = Master PTG
11101 = Slave CLC1
11100 = Master CLC1
11011 = Reserved
11010 = Reserved
11001 = Master PWM3 Trigger 2
11000 = Master PWM1 Trigger 2
10111 = Slave SCCP4 PWM/IC interrupt
10110 = Slave SCCP3 PWM/IC interrupt
10101 = Slave SCCP2 PWM/IC interrupt
10100 = Slave SCCP1 PWM/IC interrupt
10011 = Reserved
10010 = Reserved
10001 = Reserved
10000 = Reserved
01111 = Slave PWM8 Trigger 1
01110 = Slave PWM7 Trigger 1
01101 = Slave PWM6 Trigger 1
01100 = Slave PWM5 Trigger 1
01011 = Slave PWM4 Trigger 2
01010 = Slave PWM4 Trigger 1
01001 = Slave PWM3 Trigger 2
01000 = Slave PWM3 Trigger 1
00111 = Slave PWM2 Trigger 2
00110 = Slave PWM2 Trigger 1
00101 = Slave PWM1 Trigger 2
00100 = Slave PWM1 Trigger 1
00011 = Reserved
00010 = Level software trigger
00001 = Common software trigger
00000 = No trigger is enabled

bit 7-5 **Unimplemented:** Read as '0'

REGISTER 9-9: LOGCONy: COMBINATORIAL PWM LOGIC CONTROL REGISTER y(2) (CONTINUED)

bit 6 **S2yPOL:** Combinatorial PWM Logic Source #2 Polarity bit
1 = Input is inverted
0 = Input is positive logic

bit 5-4 **PWMLFy<1:0>:** Combinatorial PWM Logic Function Selection bits
11 = Reserved
10 = PWMS1 ^ PWMS2 (XOR)
01 = PWMS1 & PWMS2 (AND)
00 = PWMS1 | PWMS2 (OR)

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **PWMLFyD<2:0>:** Combinatorial PWM Logic Destination Selection bits
111 = Logic function is assigned to the PWM8H or PWM8L pin
110 = Logic function is assigned to the PWM7H or PWM7L pin
101 = Logic function is assigned to the PWM6H or PWM6L pin
100 = Logic function is assigned to the PWM5H or PWM5Lpin
011 = Logic function is assigned to the PWM4H or PWM4Lpin
010 = Logic function is assigned to the PWM3H or PWM3Lpin
001 = Logic function is assigned to the PWM2H or PWM2Lpin
000 = No assignment, combinatorial PWM logic function is disabled

Note 1: Logic function input will be connected to '0' if the PWM channel is not present.
2: 'y' denotes a common instance (A-F).

REGISTER 9-13: PGxCONH: PWM GENERATOR x CONTROL REGISTER HIGH (CONTINUED)

bit 6 **TRGMOD:** PWM Generator Trigger Mode Selection bit
1 = PWM Generator operates in Retriggerable mode
0 = PWM Generator operates in Single Trigger mode

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **SOCS<3:0>:** Start-of-Cycle Selection bits(1,2,3)
1111 = TRIG bit or PCI Sync function only (no hardware trigger source is selected)
1110-0101 = Reserved
0100 = PWM4(8) PG1 or PG5 trigger output selected by PGTRGSEL<2:0> (PGxEVT<2:0>)
0011 = PWM3(7) PG1 or PG5 trigger output selected by PGTRGSEL<2:0> (PGxEVT<2:0>)
0010 = PWM2(6) PG1 or PG5 trigger output selected by PGTRGSEL<2:0> (PGxEVT<2:0>)
0001 = PWM1(5) PG1 or PG5 trigger output selected by PGTRGSEL<2:0> (PGxEVT<2:0>)
0000 = Local EOC – PWM Generator is self-triggered

Note 1: The PCI selected Sync signal is always available to be OR'd with the selected SOC signal per the SOCS<3:0> bits if the PCI Sync function is enabled.

2: The source selected by the SOCS<3:0> bits MUST operate from the same clock source as the local PWM Generator. If not, the source must be routed through the PCI Sync logic so the trigger signal may be synchronized to the PWM Generator clock domain.

3: PWM Generators are grouped into groups of four: PG1-PG4 and PG5-PG8, if available. Any generator within a group of four may be used to trigger another generator within the same group.

FIGURE 10-3: DUAL 16-BIT TIMER MODE

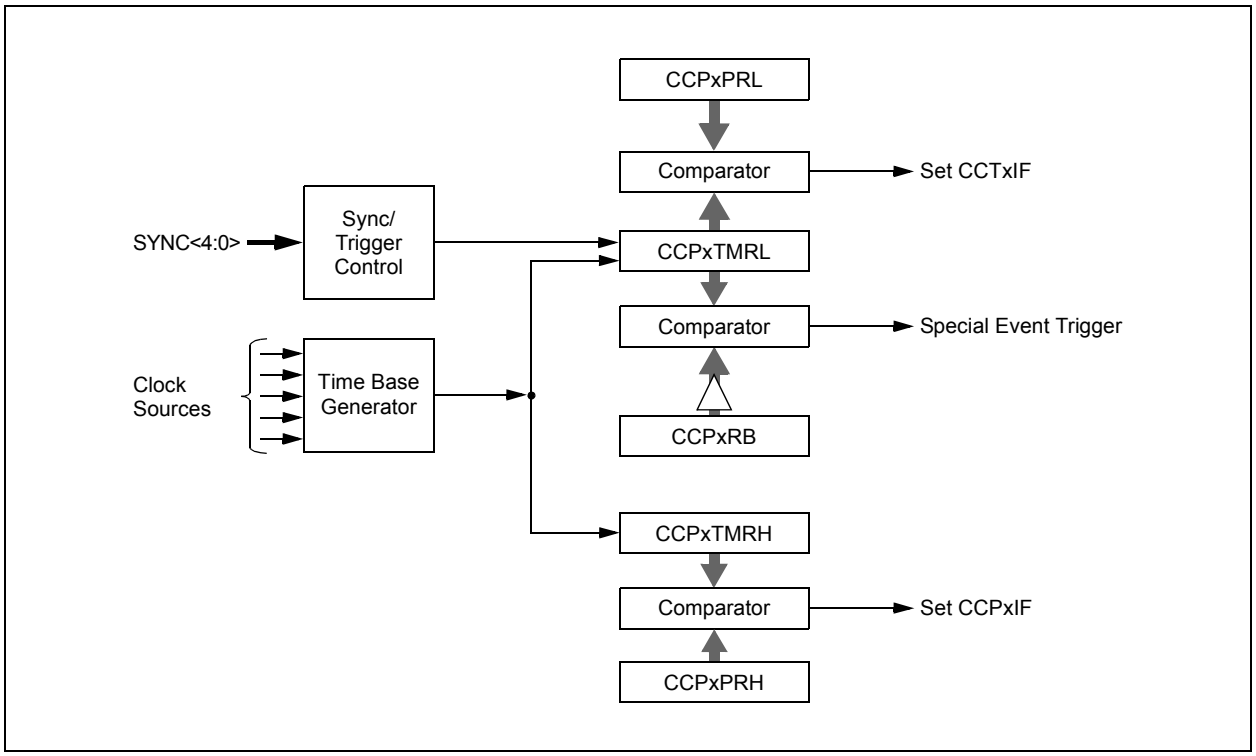
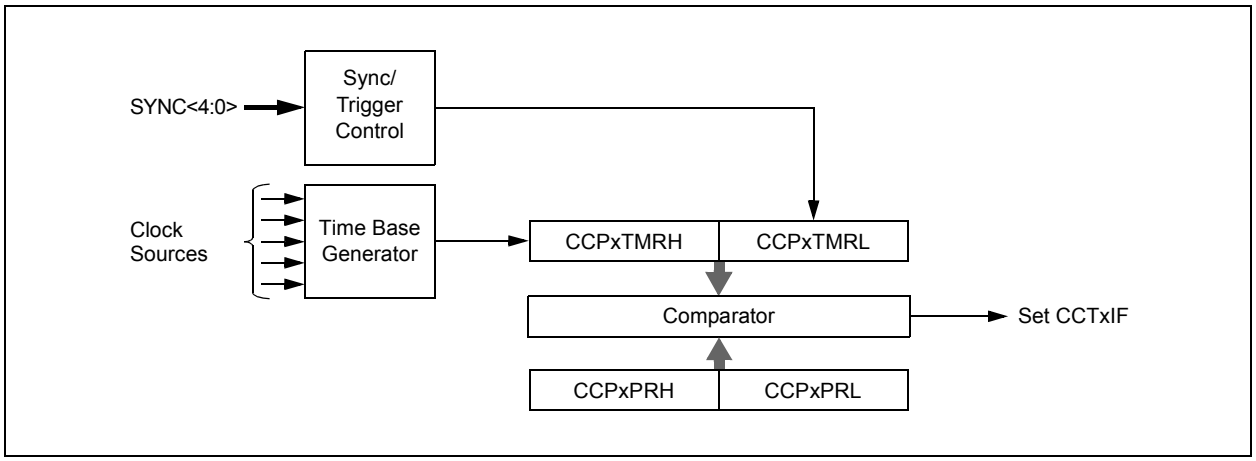


FIGURE 10-4: 32-BIT TIMER MODE



REGISTER 12-19: INDXxHLDL: INDEX x COUNTER HOLD REGISTER LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INDXHLD<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INDXHLD<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **INDXHLD<15:0>:** Hold for Reading/Writing Index x Counter Register (INDXCNT) bits

REGISTER 12-20: INDXxHLDH: INDEX x COUNTER HOLD REGISTER HIGH

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INDXHLD<31:24>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INDXHLD<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **INDXHLD<31:16>:** Hold for Reading/Writing Index x Counter Register (INDXCNT) bits

REGISTER 21-14: FDEVOPT CONFIGURATION REGISTER

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

U-1	U-1	R/PO-1	U-1	U-1	R/PO-1	r-1	r-1
—	—	SPI2PIN(1)	—	—	SMBEN	—	—
bit 15							bit 8

r-1	U-1	U-1	R/PO-1	R/PO-1	r-1	U-1	U-1
—	—	—	ALTI2C2	ALTI2C1	—	—	—
bit 7							bit 0

Legend:	PO = Program Once bit	r = Reserved bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 23-14 **Unimplemented:** Read as '1'

bit 13 **SPI2PIN:** Master SPI #2 Fast I/O Pad Disable bit(1)
1 = Master SPI2 uses PPS (I/O remap) to make connections with device pins
0 = Master SPI2 uses direct connections with specified device pins

bit 12-11 **Unimplemented:** Read as '1'

bit 10 **SMBEN:** Select Input Voltage Threshold for I^2C Pads to be SMBus 3.0 Compliant bit
1 = Enables SMBus 3.0 input threshold voltage
0 = I^2C pad input buffer operation

bit 9-7 **Reserved:** Maintain as '1'

bit 6-5 **Unimplemented:** Read as '1'

bit 4 **ALTI2C2:** Alternate I2C2 Pin Mapping bit
1 = Default location for SCL2/SDA2 pins
0 = Alternate location for SCL2/SDA2 pins (ASCL2/ASDA2)

bit 3 **ALTI2C1:** Alternate I2C1 Pin Mapping bit
1 = Default location for SCL1/SDA1 pins
0 = Alternate location for SCL1/SDA1 pins (ASCL1/ASDA1)

bit 2 **Reserved:** Maintain as '1'

bit 1-0 **Unimplemented:** Read as '1'

Note 1: Fixed pin option is only available for higher pin packages (48-pin, 64-pin and 80-pin).

REGISTER 21-21: FCFGPRB0: PORTB CONFIGURATION REGISTER

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
CPRB<15:8>							
bit 15							bit 8

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
CPRB<7:0>							
bit 7							bit 0

Legend:	PO = Program Once bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 23-16 **Unimplemented:** Read as '1'

bit 15-0 **CPRB<15:0>:** Configure PORTB Ownership bits
1 = Master core owns pin
0 = Slave core owns pin

REGISTER 21-22: FCFGPRC0: PORTC CONFIGURATION REGISTER

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
CPRC<15:8>							
bit 15							bit 8

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
CPRC<7:0>							
bit 7							bit 0

Legend:	PO = Program Once bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 23-16 **Unimplemented:** Read as '1'

bit 15-0 **CPRC<15:0>:** Configure PORTC Ownership bits
1 = Master core owns pin
0 = Slave core owns pin

21.7 Dual Watchdog Timer (WDT)

Note 1: This data sheet summarizes the features of the dsPIC33CH128MP508 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Dual Watchdog Timer",** (DS70005250) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: The WDT is identical for both Master core and Slave core. The x is common for both Master core and Slave core (where the x represents the number of the specific module being addressed). The number of WDT modules available on the Master and Slaves is different and they are located in different SFR locations.

3: All associated register names are the same on the Master core and the Slave core. The Slave code will be developed in a separate project in MPLAB® X IDE with the device selection, dsPIC33CH128MP508**S1**, where the **S1** indicates the Slave device.

Table 21-6 shows an overview of the WDT module.

TABLE 21-6: DUAL WDT MODULE OVERVIEW

	Number of WDT Modules	Identical (Modules)
Master Core	1	Yes
Slave Core	1	Yes

The dsPIC33 dual Watchdog Timer (WDT) is described in this section. Refer to Figure 21-2 for a block diagram of the WDT.

The WDT, when enabled, operates from the internal Low-Power RC (LPRC) Oscillator clock source or a selectable clock source in Run mode. The WDT can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. The WDT can be configured in Windowed mode or Non-Windowed mode. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode (Power Save mode). If the WDT expires and issues a device Reset, the WTDO bit of the RCON register (Register 21-37) will be set.

The following are some of the key features of the WDT modules:

- Configuration or Software Controlled
- Separate User-Configurable Time-out Periods for Run and Sleep/Idle
- Can Wake the Device from Sleep or Idle
- User-Selectable Clock Source in Run mode
- Operates from LPRC in Sleep/Idle mode

Note: While executing a clock switch, the WDT will not be reset. It is recommended to reset the WDT prior to executing a clock switch instruction.