



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit Dual-Core
Speed	180MHz, 200MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	21
Program Memory Size	88KB (88K x 8)
Program Memory Type	FLASH, PRAM
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 23x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ch64mp202-i-ss

dsPIC33CH128MP508 FAMILY

TABLE 3-10: MASTER SFR BLOCK 700h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
CAN FD (Continued)			C1FLTOBJ15L	6F8	0000000000000000	C1MASK15H	6FE	-0000000000000000
C1MASK14L	6F4	0000000000000000	C1FLTOBJ15H	6FA	-0000000000000000			
C1MASK14H	6F6	-0000000000000000	C1MASK15L	6FC	0000000000000000			

Legend: x = unknown or indeterminate value; "-" = unimplemented bits. Address and Reset values are in hexadecimal and binary, respectively.

TABLE 3-11: MASTER SFR BLOCK 800h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
Interrupts			IPC3	846	-100-100-100-100	IPC33	882	-100-100-100-100
IFS0	800	0000000000-00000	IPC4	848	-100-100-100-100	IPC34	884	-100-100-100-100
IFS1	802	0000000000000000	IPC5	84A	-100-100-100-100	IPC35	886	-----100-100
IFS2	804	00000-00-00000--	IPC6	84C	-100-100-100-100	IPC35	886	-----100-100
IFS3	806	000-----00000	IPC7	84E	-100-100-100-100	IPC36	888	-----100-----
IFS4	808	--000----0000-00	IPC8	850	-100-100-----	IPC37	88A	-----100-100----
IFS5	80A	0000000000000000-	IPC9	852	-----100-100-100	IPC38	88C	-----100-100
IFS6	80C	0000000000000000	IPC10	854	-100-----100-100	IPC39	88E	-----100----
IFS7	80E	000000000000000--	IPC11	856	-100-100-100-100	IPC42	894	-100-100-100-100
IFS8	810	--00000000000000-	IPC12	858	-100-100-100-100	IPC43	896	-100-100-100-100
IFS9	812	--0---00-00--0--	IPC13	85A	-----100	IPC44	898	-100-100-100-100
IFS10	814	00000000-----	IPC15	85E	-100-100-100----	IPC45	89A	-----100
IFS11	816	-00-----00000	IPC16	860	-100-----100-100	IPC47	89E	-----100-100----
IEC0	820	0000000000-00000	IPC17	862	-----100-100-100	INTCON1	8C0	000000000000000-
IEC1	822	0000000000000000	IPC18	864	-100-----	INTCON2	8C2	000---0---0000
IEC2	824	00000-00-00000--	IPC19	866	-----100-100	INTCON3	8C4	-----0---0---0
IEC3	826	000-----00000	IPC20	868	-100-100-100----	INTCON4	8C6	-----00
IEC4	828	--000----0000-00	IPC21	86A	-100-100-100-100	INTTREG	8C8	000-000000000000
IEC5	82A	000000000000000-	IPC22	86C	-100-100-100-100	Flash		
IEC6	82C	0000000000000000	IPC23	86E	-100-100-100-100	NVMCON	8D0	0000--00----0000
IEC7	82E	000000000000000--	IPC24	870	-100-100-100-100	NVMADR	8D2	0000000000000000
IEC8	830	--00000000000000-	IPC25	872	-100-100-100-100	NVMADRU	8D4	-----00000000
IEC8	830	--00000000000000-	IPC26	874	-100-100-100-100	NVMKEY	8D6	-----00000000
IEC9	832	--0---00-00--0--	IPC27	876	-100-100-100-100	NVMSRCADRL	8D8	0000000000000000
IEC10	834	00000000-----00	IPC28	878	-100-----	NVMSRCADRH	8DA	-----00000000
IEC11	836	-00-----00000	IPC29	87A	-100-100-100-100	CBG		
IPC0	840	-100-100-100-100	IPC30	87C	-100-100-100-100	BIASCON	8F0	-----0---0000
IPC1	842	-100-100-----100	IPC31	87E	-100-100-100-100	IBIASCONL	8F4	--000000--000000
IPC2	844	-100-100-100-100	IPC32	880	-100-100-100----	IBIASCONH	8F6	--000000--000000

Legend: x = unknown or indeterminate value; "-" = unimplemented bits. Address and Reset values are in hexadecimal and binary, respectively.

dsPIC33CH128MP508 FAMILY

3.4.2 RESET CONTROL REGISTER

REGISTER 3-15: RCON: RESET CONTROL REGISTER⁽¹⁾

R/W-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
TRAPR	IOPUWR	—	—	—	—	CM	VREGS
bit 15						bit 8	

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
EXTR	SWR	—	WDTO	SLEEP	IDLE	BOR	POR
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **TRAPR:** Trap Reset Flag bit

1 = A Trap Conflict Reset has occurred

0 = A Trap Conflict Reset has not occurred

bit 14 **IOPUWR:** Illegal Opcode or Uninitialized W Register Access Reset Flag bit

1 = An illegal opcode detection, an illegal address mode or Uninitialized W register used as an Address Pointer caused a Reset

0 = An illegal opcode or Uninitialized W Register Reset has not occurred

bit 13-10 **Unimplemented:** Read as '0'

bit 9 **CM:** Configuration Mismatch Flag bit

1 = A Configuration Mismatch Reset has occurred.

0 = A Configuration Mismatch Reset has not occurred

bit 8 **VREGS:** Voltage Regulator Standby During Sleep bit

1 = Voltage regulator is active during Sleep

0 = Voltage regulator goes into Standby mode during Sleep

bit 7 **EXTR:** External Reset ($\overline{\text{MCLR}}$) Pin bit

1 = A Master Clear (pin) Reset has occurred

0 = A Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software RESET (Instruction) Flag bit

1 = A RESET instruction has been executed

0 = A RESET instruction has not been executed

bit 5 **Unimplemented:** Read as '0'

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit

1 = WDT time-out has occurred

0 = WDT time-out has not occurred

bit 3 **SLEEP:** Wake-up from Sleep Flag bit

1 = Device has been in Sleep mode

0 = Device has not been in Sleep mode

bit 2 **IDLE:** Wake-up from Idle Flag bit

1 = Device has been in Idle mode

0 = Device has not been in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit

1 = A Brown-out Reset has occurred

0 = A Brown-out Reset has not occurred

Note 1: All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

dsPIC33CH128MP508 FAMILY

REGISTER 3-18: INTCON1: INTERRUPT CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **NSTDIS:** Interrupt Nesting Disable bit
1 = Interrupt nesting is disabled
0 = Interrupt nesting is enabled
- bit 14 **OVAERR:** Accumulator A Overflow Trap Flag bit
1 = Trap was caused by an overflow of Accumulator A
0 = Trap was not caused by an overflow of Accumulator A
- bit 13 **OVBERR:** Accumulator B Overflow Trap Flag bit
1 = Trap was caused by an overflow of Accumulator B
0 = Trap was not caused by an overflow of Accumulator B
- bit 12 **COVAERR:** Accumulator A Catastrophic Overflow Trap Flag bit
1 = Trap was caused by a catastrophic overflow of Accumulator A
0 = Trap was not caused by a catastrophic overflow of Accumulator A
- bit 11 **COVBERR:** Accumulator B Catastrophic Overflow Trap Flag bit
1 = Trap was caused by a catastrophic overflow of Accumulator B
0 = Trap was not caused by a catastrophic overflow of Accumulator B
- bit 10 **OVATE:** Accumulator A Overflow Trap Enable bit
1 = Trap overflow of Accumulator A
0 = Trap is disabled
- bit 9 **OVBTE:** Accumulator B Overflow Trap Enable bit
1 = Trap overflow of Accumulator B
0 = Trap is disabled
- bit 8 **COVTE:** Catastrophic Overflow Trap Enable bit
1 = Trap catastrophic overflow of Accumulator A or B is enabled
0 = Trap is disabled
- bit 7 **SFTACERR:** Shift Accumulator Error Status bit
1 = Math error trap was caused by an invalid accumulator shift
0 = Math error trap was not caused by an invalid accumulator shift

dsPIC33CH128MP508 FAMILY

REGISTER 3-30: CNCONx: CHANGE NOTIFICATION CONTROL FOR PORTx REGISTER

R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
ON	—	—	—	CNSTYLE	—	—	—
bit 15				bit 8			

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **ON:** Change Notification (CN) Control for PORTx On bit

1 = CN is enabled

0 = CN is disabled

bit 14-12 **Unimplemented:** Read as '0'

bit 11 **CNSTYLE:** Change Notification Style Selection bit

1 = Edge style (detects edge transitions, CNFx<15:0> bits are used for a Change Notification event)

0 = Mismatch style (detects change from last port read, CNSTATx<15:0> bits are used for a Change Notification event)

bit 10-0 **Unimplemented:** Read as '0'

REGISTER 3-31: CNEN0x: INTERRUPT CHANGE NOTIFICATION ENABLE FOR PORTx REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNEN0x<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNEN0x<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **CNEN0x<15:0>:** Interrupt Change Notification Enable for PORTx bits

1 = Interrupt-on-change (from the last read value) is enabled for PORTx[n]

0 = Interrupt-on-change is disabled for PORTx[n]

dsPIC33CH128MP508 FAMILY

TABLE 3-31: SELECTABLE INPUT SOURCES (MAPS INPUT TO FUNCTION)

Input Name ⁽¹⁾	Function Name	Register	Register Bits
External Interrupt 1	INT1	RPINR0	INT1R<7:0>
External Interrupt 2	INT2	RPINR1	INT2R<7:0>
External Interrupt 3	INT3	RPINR1	INT3R<7:0>
Timer1 External Clock	T1CK	RPINR2	T1CK<7:0>
SCCP Timer1	TCKI1	RPINR3	TCKI1R<7:0>
SCCP Capture 1	ICM1	RPINR3	ICM1R<7:0>
SCCP Timer2	TCKI2	RPINR4	TCKI2R<7:0>
SCCP Capture 2	ICM2	RPINR4	ICM2R<7:0>
SCCP Timer3	TCKI3	RPINR5	TCKI3R<7:0>
SCCP Capture 3	ICM3	RPINR5	ICM3R<7:0>
SCCP Timer4	TCKI4	RPINR6	TCKI4R<7:0>
SCCP Capture 4	ICM4	RPINR6	ICM4R<7:0>
SCCP Timer5	TCKI5	RPINR7	TCKI5R<7:0>
SCCP Capture 5	ICM5	RPINR7	ICM5R<7:0>
SCCP Timer6	TCKI6	RPINR8	TCKI6R<7:0>
SCCP Capture 6	ICM6	RPINR8	ICM6R<7:0>
SCCP Timer7	TCKI7	RPINR9	TCKI7R<7:0>
SCCP Capture 7	ICM7	RPINR9	ICM7R<7:0>
SCCP Timer8	TCKI8	RPINR10	TCKI8R<7:0>
SCCP Capture 8	ICM8	RPINR10	ICM8R<7:0>
SCCP Fault A	OCFA	RPINR11	OCFAR<7:0>
SCCP Fault B	OCFB	RPINR11	OCFBR<7:0>
PWM Input 8	PCI8	RPINR12	PCI8R<7:0>
PWM Input 9	PCI9	RPINR12	PCI9R<7:0>
PWM Input 10	PCI10	RPINR13	PCI10R<7:0>
PWM Input 11	PCI11	RPINR13	PCI11R<7:0>
QEI Input A	QEIA1	RPINR14	QEIA1R<7:0>
QEI Input B	QEIB1	RPINR14	QEIB1R<7:0>
QEI Index 1 Input	QEINDX1	RPINR15	QEINDX1R<7:0>
QEI Home 1 Input	QEIHOM1	RPINR15	QEIHOM1R<7:0>
UART1 Receive	U1RX	RPINR18	U1RXR<7:0>
UART1 Data-Set-Ready	$\overline{U1DSR}$	RPINR18	U1DSRR<7:0>
UART2 Receive	U2RX	RPINR19	U2RXR<7:0>
UART2 Data-Set-Ready	$\overline{U2DSR}$	RPINR19	U2DSRR<7:0>
SPI1 Data Input	SDI1	RPINR20	SDI1R<7:0>
SPI1 Clock Input	SCK1IN	RPINR20	SCK1R<7:0>
SPI1 Slave Select	$\overline{SS1}$	RPINR21	SS1R<7:0>
Reference Clock Input	REFOI	RPINR21	REFOIR<7:0>
SPI2 Data Input	SDI2	RPINR22	SDI2R<7:0>
SPI2 Clock Input	SCK2IN	RPINR22	SCK2R<7:0>
SPI2 Slave Select	$\overline{SS2}$	RPINR23	SS2R<7:0>
UART1 Clear-to-Send	$\overline{U1CTS}$	RPINR23	U1CTSR<7:0>

Note 1: Unless otherwise noted, all inputs use the Schmitt Trigger input buffers.

dsPIC33CH128MP508 FAMILY

REGISTER 3-82: RPOR14: PERIPHERAL PIN SELECT OUTPUT REGISTER 14

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP61R5	RP61R4	RP61R3	RP61R2	RP61R1	RP61R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP60R5	RP60R4	RP60R3	RP60R2	RP60R1	RP60R0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP61R<5:0>:** Peripheral Output Function is Assigned to RP61 Output Pin bits
(see Table 3-33 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP60R<5:0>:** Peripheral Output Function is Assigned to RP60 Output Pin bits
(see Table 3-33 for peripheral function numbers)

REGISTER 3-83: RPOR15: PERIPHERAL PIN SELECT OUTPUT REGISTER 15

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP63R5	RP63R4	RP63R3	RP63R2	RP63R1	RP63R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP62R5	RP62R4	RP62R3	RP62R2	RP62R1	RP62R0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP63R<5:0>:** Peripheral Output Function is Assigned to RP63 Output Pin bits
(see Table 3-33 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP62R<5:0>:** Peripheral Output Function is Assigned to RP62 Output Pin bits
(see Table 3-33 for peripheral function numbers)

dsPIC33CH128MP508 FAMILY

3.9.3 ADC CONTROL/STATUS REGISTERS

REGISTER 3-157: ADCON1L: ADC CONTROL REGISTER 1 LOW

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
ADON ⁽¹⁾	—	ADSIDL	—	—	—	—	—
bit 15				bit 8			

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **ADON:** ADC Enable bit⁽¹⁾

1 = ADC module is enabled

0 = ADC module is off

bit 14 **Unimplemented:** Read as '0'bit 13 **ADSIDL:** ADC Stop in Idle Mode bit

1 = Discontinues module operation when device enters Idle mode

0 = Continues module operation in Idle mode

bit 12-0 **Unimplemented:** Read as '0'

Note 1: Set the ADON bit only after the ADC module has been configured. Changing ADC Configuration bits when ADON = 1 will result in unpredictable behavior.

dsPIC33CH128MP508 FAMILY

REGISTER 4-57: RPINR45: PERIPHERAL PIN SELECT INPUT REGISTER 45

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CLCINAR7	CLCINAR6	CLCINAR5	CLCINAR4	CLCINAR3	CLCINAR2	CLCINAR1	CLCINAR0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **CLCINAR<7:0>**: Assign CLC Input A (S1CLCINA) to the Corresponding S1RPn Pin bits
See Table 4-27.

bit 7-0 **Unimplemented**: Read as '0'

REGISTER 4-58: RPINR46: PERIPHERAL PIN SELECT INPUT REGISTER 46

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CLCINCR7	CLCINCR6	CLCINCR5	CLCINCR4	CLCINCR3	CLCINCR2	CLCINCR1	CLCINCR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CLCINBR7	CLCINBR6	CLCINBR5	CLCINBR4	CLCINBR3	CLCINBR2	CLCINBR1	CLCINBR0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **CLCINCR<7:0>**: Assign CLC Input C (S1CLCINC) to the Corresponding S1RPn Pin bits
See Table 4-27.

bit 7-0 **CLCINBR<7:0>**: Assign CLC Input B (S1CLCINB) to the Corresponding S1RPn Pin bits
See Table 4-27.

dsPIC33CH128MP508 FAMILY

REGISTER 4-104: ADSTATL: ADC DATA READY STATUS REGISTER LOW

HSC/R-0	HSC/R-0	HSC/R-0	HSC/R-0	HSC/R-0	HSC/R-0	HSC/R-0	HSC/R-0
AN<15:8>RDY							
bit 15				bit 8			

HSC/R-0	HSC/R-0	HSC/R-0	HSC/R-0	HSC/R-0	HSC/R-0	HSC/R-0	HSC/R-0
AN<7:0>RDY							
bit 7				bit 0			

Legend: U = Unimplemented bit, read as '0'
R = Readable bit W = Writable bit HSC = Hardware Settable/Clearable bit
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **AN<15:0>RDY:** Common Interrupt Enable for Corresponding Analog Inputs bits
1 = Channel conversion result is ready in the corresponding ADCBUFx register
0 = Channel conversion result is not ready

REGISTER 4-105: ADSTATH: ADC DATA READY STATUS REGISTER HIGH

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15				bit 8			

U-0	U-0	U-0	HSC/R-0	HSC/R-0	HSC/R-0	HSC/R-0	HSC/R-0
—	—	—	AN<20:16>RDY				
bit 7				bit 0			

Legend: U = Unimplemented bit, read as '0'
R = Readable bit W = Writable bit HSC = Hardware Settable/Clearable bit
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'
bit 4-0 **AN<20:16>RDY:** Common Interrupt Enable for Corresponding Analog Inputs bits
1 = Channel conversion result is ready in the corresponding ADCBUFx register
0 = Channel conversion result is not ready

dsPIC33CH128MP508 FAMILY

REGISTER 7-15: PMD8: SLAVE PERIPHERAL MODULE DISABLE 8 CONTROL REGISTER

U-0	R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0
—	PGA3MD	—	—	—	PGA2MD	—	—
bit 15						bit 8	

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	CLC4MD	CLC3MD	CLC2MD	CLC1MD	—	—
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **Unimplemented:** Read as '0'
- bit 14 **PGA3MD:** PGA3 Module Disable bit
1 = PGA3 module is disabled
0 = PGA3 module is enabled
- bit 13-11 **Unimplemented:** Read as '0'
- bit 10 **PGA2MD:** PGA2 Module Disable bit
1 = PGA2 module is disabled
0 = PGA2 module is enabled
- bit 9-6 **Unimplemented:** Read as '0'
- bit 5 **CLC4MD:** CLC4 Module Disable bit
1 = CLC4 module is disabled
0 = CLC4 module is enabled
- bit 4 **CLC3MD:** CLC3 Module Disable bit
1 = CLC3 module is disabled
0 = CLC3 module is enabled
- bit 3 **CLC2MD:** CLC2 Module Disable bit
1 = CLC2 module is disabled
0 = CLC2 module is enabled
- bit 2 **CLC1MD:** CLC1 Module Disable bit
1 = CLC1 module is disabled
0 = CLC1 module is enabled
- bit 1-0 **Unimplemented:** Read as '0'

8.1.6 CHANNEL PRIORITY

Each DMA channel functions independently of the others, but also competes with the others for access to the data and DMA buses. When access collisions occur, the DMA Controller arbitrates between the channels using a user-selectable priority scheme. Two schemes are available:

- Round Robin: When two or more channels collide, the lower numbered channel receives priority on the first collision. On subsequent collisions, the higher numbered channels each receive priority based on their channel number.
- Fixed: When two or more channels collide, the lowest numbered channel always receives priority, regardless of past history; however, any channel being actively processed is not available for an immediate retrigger. If a higher priority channel is continually requesting service, it will be scheduled for service after the next lower priority channel with a pending request.

8.2 Typical Setup

To set up a DMA channel for a basic data transfer:

1. Enable the DMA Controller (DMAEN = 1) and select an appropriate channel priority scheme by setting or clearing PRSSEL.
2. Program DMAH and DMAL with appropriate upper and lower address boundaries for data RAM operations.
3. Select the DMA channel to be used and disable its operation (CHEN = 0).
4. Program the appropriate source and destination addresses for the transaction into the channel's DMASRCn and DMADSTn registers. For PIA mode addressing, use the base address value.
5. Program the DMACNTn register for the number of triggers per transfer (One-Shot or Continuous modes) or the number of words (bytes) to be transferred (Repeated modes).
6. Set or clear the SIZE bit to select the data size.
7. Program the TRMODE<1:0> bits to select the Data Transfer mode.
8. Program the SAMODE<1:0> and DAMODE<1:0> bits to select the addressing mode.
9. Enable the DMA channel by setting CHEN.
10. Enable the trigger source interrupt.

8.3 Peripheral Module Disable

The channels of the DMA Controller can be individually powered down using the Peripheral Module Disable (PMD) registers.

8.4 Registers

The DMA Controller uses a number of registers to control its operation. The number of registers depends on the number of channels implemented for a particular device.

There are always four module-level registers (one control and three buffer/address):

- DMACON: DMA Engine Control Register (Register 8-1)
- DMAH and DMAL: DMA High and Low Address Limit Registers
- DMABUF: DMA Transfer Data Buffer

Each of the DMA channels implements five registers (two control and three buffer/address):

- DMACHn: DMA Channel n Control Register (Register 8-2)
- DMAINTn: DMA Channel n Interrupt Register (Register 8-3)
- DMASRCn: DMA Data Source Address Pointer for Channel n Register
- DMADSTn: DMA Data Destination Source for Channel n Register
- DMACNTn: DMA Transaction Counter for Channel n Register

For dsPIC33CH128MP508 devices, there are a total of 34 registers.

dsPIC33CH128MP508 FAMILY

REGISTER 9-30: PGxDTL: PWM GENERATOR x DEAD-TIME REGISTER LOW

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DTL<13:8> ⁽¹⁾					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTL<7:0>							
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-0 **DTL<13:0>:** PWMxL Dead-Time Delay bits⁽¹⁾

Note 1: DTL<13:11> bits are not available when HREN (PGxCONL<7>) = 0.

REGISTER 9-31: PGxDTH: PWM GENERATOR x DEAD-TIME REGISTER HIGH

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DTH<13:8> ⁽¹⁾					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTH<7:0>							
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-0 **DTH<13:0>:** PWMxH Dead-Time Delay bits⁽¹⁾

Note 1: DTH<13:11> bits are not available when HREN (PGxCONL<7>) = 0.

dsPIC33CH128MP508 FAMILY

REGISTER 9-32: PGxCAP: PWM GENERATOR x CAPTURE REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
PGxCAP<15:8>							
bit 15				bit 8			

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
PGxCAP<7:0> ⁽¹⁾							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **PGxCAP<15:0>**: PGx Time Base Capture bits⁽¹⁾

Note 1: PGxCAP<1:0> will read as '0' in Standard Resolution mode. PGxCAP<4:0> will read as '0' in High-Resolution mode.

REGISTER 14-2: SPIxCON1H: SPIx CONTROL REGISTER 1 HIGH (CONTINUED)

- bit 6 **FRMSYNC**: Frame Sync Pulse Direction Control bit
1 = Frame Sync pulse input (Slave)
0 = Frame Sync pulse output (Master)
- bit 5 **FRMPOL**: Frame Sync/Slave Select Polarity bit
1 = Frame Sync pulse/Slave select is active-high
0 = Frame Sync pulse/Slave select is active-low
- bit 4 **MSEN**: Master Mode Slave Select Enable bit
1 = SPIx Slave select support is enabled with polarity determined by FRMPOL (\overline{SSx} pin is automatically driven during transmission in Master mode)
0 = Slave select SPIx support is disabled (\overline{SSx} pin will be controlled by port I/O)
- bit 3 **FRMSYPW**: Frame Sync Pulse-Width bit
1 = Frame Sync pulse is one serial word length wide (as defined by MODE<32,16>/WLENGTH<4:0>)
0 = Frame Sync pulse is one clock (SCKx) wide
- bit 2-0 **FRMCNT<2:0>**: Frame Sync Pulse Counter bits
Controls the number of serial words transmitted per Sync pulse.
111 = Reserved
110 = Reserved
101 = Generates a Frame Sync pulse on every 32 serial words
100 = Generates a Frame Sync pulse on every 16 serial words
011 = Generates a Frame Sync pulse on every 8 serial words
010 = Generates a Frame Sync pulse on every 4 serial words
001 = Generates a Frame Sync pulse on every 2 serial words (value used by audio protocols)
000 = Generates a Frame Sync pulse on each serial word

- Note 1:** AUDEN can only be written when the SPIEN bit = 0.
2: AUDMONO can only be written when the SPIEN bit = 0 and is only valid for AUDEN = 1.
3: URDTEN is only valid when IGNTUR = 1.
4: AUDMOD<1:0> can only be written when the SPIEN bit = 0 and is only valid when AUDEN = 1. When NOT in PCM/DSP mode, this module functions as if FRMSYPW = 1, regardless of its actual value.

dsPIC33CH128MP508 FAMILY

REGISTER 16-3: SENTxDATL: SENTx RECEIVE DATA REGISTER LOW⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATA4<3:0>				DATA5<3:0>			
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATA6<3:0>				CRC<3:0>			
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-12 **DATA4<3:0>**: Data Nibble 4 Data bits

bit 11-8 **DATA5<3:0>**: Data Nibble 5 Data bits

bit 7-4 **DATA6<3:0>**: Data Nibble 6 Data bits

bit 3-0 **CRC<3:0>**: CRC Nibble Data bits

Note 1: Register bits are read-only in Receive mode (RCVEN = 1). In Transmit mode, the CRC<3:0> bits are read-only when automatic CRC calculation is enabled (RCVEN = 0, CRCEN = 1).

REGISTER 16-4: SENTxDATH: SENTx RECEIVE DATA REGISTER HIGH⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STAT<3:0>				DATA1<3:0>			
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATA2<3:0>				DATA3<3:0>			
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-12 **STAT<3:0>**: Status Nibble Data bits

bit 11-8 **DATA1<3:0>**: Data Nibble 1 Data bits

bit 7-4 **DATA2<3:0>**: Data Nibble 2 Data bits

bit 3-0 **DATA3<3:0>**: Data Nibble 3 Data bits

Note 1: Register bits are read-only in Receive mode (RCVEN = 1). In Transmit mode, the CRC<3:0> bits are read-only when automatic CRC calculation is enabled (RCVEN = 0, CRCEN = 1).

dsPIC33CH128MP508 FAMILY

TABLE 22-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles ⁽¹⁾	Status Flags Affected
40	DIV2.U	DIV2.U Wm, Wn	Unsigned 16/16-bit Integer Divide (W1:W0 preserved)	1	6	N,Z,C,OV
		DIV2.UD Wm, Wn	Unsigned 32/16-bit Integer Divide (W1:W0 preserved)	1	6	N,Z,C,OV
41	DO	DO #lit15, Expr	Do Code to PC + Expr, lit15 + 1 Times	2	2	None
		DO Wn, Expr	Do code to PC + Expr, (Wn) + 1 Times	2	2	None
42	ED	ED Wm*Wm, Acc, Wx, Wy, Wxd	Euclidean Distance (no accumulate)	1	1	OA,OB,OAB,SA,SB,SAB
43	EDAC	EDAC Wm*Wm, Acc, Wx, Wy, Wxd	Euclidean Distance	1	1	OA,OB,OAB,SA,SB,SAB
44	EXCH	EXCH Wns, Wnd	Swap Wns with Wnd	1	1	None
46	FBCL	FBCL Ws, Wnd	Find Bit Change from Left (MSb) Side	1	1	C
47	FF1L	FF1L Ws, Wnd	Find First One from Left (MSb) Side	1	1	C
48	FF1R	FF1R Ws, Wnd	Find First One from Right (LSb) Side	1	1	C
49	FLIM	FLIM Wb, Ws	Force Data (Upper and Lower) Range Limit without Limit Excess Result	1	1	N,Z,OV
		FLIM.V Wb, Ws, Wd	Force Data (Upper and Lower) Range Limit with Limit Excess Result	1	1	N,Z,OV
50	GOTO	GOTO Expr	Go to Address	2	4/2 ⁽²⁾	None
		GOTO Wn	Go to Indirect	1	4/2 ⁽²⁾	None
		GOTO.L Wn	Go to Indirect (long address)	1	4/2 ⁽²⁾	None
51	INC	INC f	f = f + 1	1	1	C,DC,N,OV,Z
		INC f, WREG	WREG = f + 1	1	1	C,DC,N,OV,Z
		INC Ws, Wd	Wd = Ws + 1	1	1	C,DC,N,OV,Z
52	INC2	INC2 f	f = f + 2	1	1	C,DC,N,OV,Z
		INC2 f, WREG	WREG = f + 2	1	1	C,DC,N,OV,Z
		INC2 Ws, Wd	Wd = Ws + 2	1	1	C,DC,N,OV,Z
53	IOR	IOR f	f = f .IOR. WREG	1	1	N,Z
		IOR f, WREG	WREG = f .IOR. WREG	1	1	N,Z
		IOR #lit10, Wn	Wd = lit10 .IOR. Wd	1	1	N,Z
		IOR Wb, Ws, Wd	Wd = Wb .IOR. Ws	1	1	N,Z
		IOR Wb, #lit5, Wd	Wd = Wb .IOR. lit5	1	1	N,Z
54	LAC	LAC Wso, #Slit4, Acc	Load Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
		LAC.D Wso, #Slit4, Acc	Load Accumulator Double	1	2	OA,SA,OB,SB
55	LDSLV	LDSLV Wso, Wdo, lit2	Move a Single Instruction Word from Master to Slave PRAM	1	1	None
56	LNK	LNK #lit14	Link Frame Pointer	1	1	SFA
57	LSR	LSR f	f = Logical Right Shift f	1	1	C,N,OV,Z
		LSR f, WREG	WREG = Logical Right Shift f	1	1	C,N,OV,Z
		LSR Ws, Wd	Wd = Logical Right Shift Ws	1	1	C,N,OV,Z
		LSR Wb, Wns, Wnd	Wnd = Logical Right Shift Wb by Wns	1	1	N,Z
		LSR Wb, #lit5, Wnd	Wnd = Logical Right Shift Wb by lit5	1	1	N,Z
58	MAC	MAC Wm*Wn, Acc, Wx, Wxd, Wy, Wyd, AWB	Multiply and Accumulate	1	1	OA,OB,OAB,SA,SB,SAB
		MAC Wm*Wm, Acc, Wx, Wxd, Wy, Wyd	Square and Accumulate	1	1	OA,OB,OAB,SA,SB,SAB
59	MAX	MAX Acc	Force Data Maximum Range Limit	1	1	N,OV,Z
		MAX.V Acc, Wnd	Force Data Maximum Range Limit with Result	1	1	N,OV,Z

- Note**
- 1: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.
 - 2: Cycle times for Slave core are different for Master core, as shown in 2.
 - 3: For dsPIC33CH128MP508 devices, the divide instructions must be preceded with a "REPEAT #5" instruction, such that they are executed six consecutive times

dsPIC33CH128MP508 FAMILY

Capture/Compare/PWM/Timer		
Auto-Shutdown and Gating Sources (Master)	548	
Auto-Shutdown and Gating Sources (Slave)	548	
Auxiliary Output	541	
Control/Status Registers	542	
General Purpose Timer	537	
Input Capture Mode	540	
Output Compare Mode	539	
Overview	535	
Synchronization Sources (Master)	545	
Synchronization Sources (Slave)	546	
Time Base Generator	536	
Capture/Compare/PWM/Timer (SCCP)	535	
CLC		
Control Registers	650	
Overview	647	
Code Examples		
Configuring UART1 Input and Output Functions	125	
Flash Write/Read	79	
MSI Enable Operation	429	
MSI Enable Operation in C	429	
Port Write/Read	341	
PRAM Write/Read	299	
PWSAV Instruction Syntax	471	
Slave PRAM Load and Verify Routine	301	
Using Master or Slave Auxiliary PLL with		
Internal FRC	438	
Using Master PLL (50 MIPS) with POSC	467	
Using Master PLL with 8 MHz Internal FRC	469	
Using Master Primary PLL with 8 MHz		
Internal FRC	436	
Using Slave PLL (60 MIPS) with POSC	468	
Using Slave PLL with 8 MHz Internal FRC	470	
Using Slave Primary PLL with 8 MHz		
Internal FRC	436	
Code Protection	667	
Code Protection, CodeGuard Security (Master Flash)	711	
Code Protection, CodeGuard Security (Slave PRAM)	712	
CodeGuard Security	667	
Comparator/DAC		
Control Registers	555	
Features Overview	555	
Overview	553	
Configurable Logic Cell (CLC)	647	
Configurable Logic Cell. See CLC.		
Configuration Bits	667	
Bit Values for Master Clock Selection	440	
Bit Values for Slave Clock Selection	441	
Controller Area Network (CAN FD)	178	
Controller Area Network. See CAN.		
CRC		
Control Registers	660	
Overview	659	
Current Bias Generator		
Control Registers	664	
Current Bias Generator (CBG)	663	
Current Bias Generator. See CBG.		
Customer Change Notification Service	802	
Customer Notification Service	802	
Customer Support	802	
Cyclic Redundancy Check. See CRC.		
D		
Data Address Space	49	
Memory Map for dsPIC33CH128MP508 Devices	50	
Near Data Space	49	
Organization, Alignment	49	
SFR Space	49	
Width	49	
Data Address Space (Slave)	274	
Memory Map for Slave dsPIC33CH128MP508S1		
Devices	275	
Near Data Space	274	
Organization, Alignment	274	
Resources	276	
SFR Space	274	
Width	274	
Data Space		
Extended X	69	
Paged Data Memory Space (figure)	67	
Paged Memory Scheme	66	
Data Space (Slave)		
Extended X	289	
Paged Data Memory Space (figure)	287	
Paged Memory Scheme	286	
DC Characteristics		
ADC Delta Current	738	
APLL Delta Current	737	
Brown-out Reset (BOR)	741	
Comparator + DAC Delta Current	738	
Idle Current (IDLE) (Master Idle/Slave Sleep)	734	
Idle Current (IDLE) (Master Sleep/Slave Idle)	735	
Operating Current (IDD) (Master Run/Slave Run)	730	
Operating Current (IDD)		
(Master Run/Slave Sleep)	732	
Operating Current (IDD)		
(Master Sleep/Slave Run)	731	
Operating Current (IDLE) (Master Idle/Slave Idle)	733	
Operating MIPS vs. Voltage	728	
PGA Delta Current	738	
Power-Down Current (IPD)	736	
PWM Delta Current	737	
Watchdog Timer Delta Current (ΔI_{WDT})	736	
Deadman Timer (DMT)	170	
Control Registers	171	
Deadman Timer. See DMT.		
Demo/Development Boards, Evaluation and		
Starter Kits	726	
Development Support	723	
Device Calibration	697	
Addresses	697	
and Identification	697	
Device Overview	21	
Device Programmer		
MPLAB PM3	725	
Device Variants	699	
Direct Memory Access Controller. See DMA.		
DMA		
Channel Trigger Sources (Master)	499	
Channel Trigger Sources (Slave)	500	
Control Registers	496	
Overview	491	
Peripheral Module Disable (PMD)	495	
Summary of Operations	493	
Types of Data Transfers	494	
Typical Setup	495	

dsPIC33CH128MP508 FAMILY

ECCCONH (ECC Fault Injection Configuration High).....	86, 307	INTXxHLDL (Index x Counter Hold Low).....	578
ECCCONL (ECC Fault Injection Configuration Low).....	86, 307	LATx (Output Data for PORTx)	118, 336
ECCSTATH (ECC System Status Display High)	309	LFSR (Linear Feedback Shift)	513
ECCSTATL (ECC System Status Display Low).....	309	LOGCONy (Combinatorial PWM Logic Control y)....	509
FALTREG Configuration	681	MDC (Master Duty Cycle).....	505
FBSLIM Configuration.....	671	MPER (Master Period)	506
FCFGPRA0 (PORTA Configuration).....	686	MPHASE (Master Phase).....	505
FCFGPRB0 (PORTB Configuration).....	687	MRSWFDATA (Master Read (Slave Write) FIFO Data).....	423
FCFGPRC0 (PORTC Configuration)	687	MSI1CON (MSI1 Master Control).....	418
FCFGPRD0 (PORTD Configuration)	688	MSI1FIFOCS (MSI1 Master FIFO Control/Status).....	422
FCFGPRE0 (PORTE Configuration).....	688	MSI1KEY (MSI1 Master Interlock Key)	420
FDEVOPT Configuration.....	680	MSI1MBXnD (MSI1 Master Mailbox n Data)	421
FDMT Configuration.....	679	MSI1MBXS (MSI1 Master Mailbox Data Transfer Status).....	420
FDMTCNTH Configuration.....	678	MSI1STAT (MSI1 Master Status)	419
FDMTCNTL Configuration	678	MWSRFDATA (Master Write (Slave Read) FIFO Data).....	423
FDMTIVTH Configuration	677	NVMADR (Nonvolatile Memory Lower Address).....	84
FDMTIVTL Configuration	677	NVMADR (Slave Program Memory Lower Address).....	305
FICD Configuration	676	NVMADRU (Nonvolatile Memory Upper Address)	84
FMBXHS1 Configuration.....	684	NVMADRU (Slave Program Memory Upper Address)	305
FMBXHS2 Configuration.....	685	NVMCON (Nonvolatile Memory (NVM) Control)	82
FMBXHSEN Configuration.....	686	NVMCON (Program Memory Slave Control).....	303
FMBXM Configuration.....	682	NVMKEY (Nonvolatile Memory Key)	85
FOSC Configuration.....	673	NVMKEY (Slave Nonvolatile Memory Key)	306
FOSCSEL Configuration.....	672	NVMSRCADR (NVM Source Data Address).....	85
FPOR Configuration.....	675	NVMSRCADR (Slave NVM Source Data Address).....	306
FS1ALTREG Configuration (Slave)	695	ODCx (Open-Drain Enable for PORTx).....	118, 336
FS1DEVOPT Configuration (Slave).....	694	OSCCON (Master Oscillator Control)	442
FS1ICD Configuration (Slave)	693	OSCCON (Slave Oscillator Control).....	455
FS1OSC Configuration (Slave).....	690	OSCTUN (Master FRC Oscillator Tuning).....	447
FS1OSCSEL Configuration (Slave).....	689	PCLKCON (PWM Clock Control)	503
FS1POR Configuration (Slave).....	692	PGAxCAL (PGAx Calibration)	416
FS1WDT Configuration (Slave)	691	PGAxCON (PGAx Control).....	415
FSCL (Frequency Scale)	504	PGxCAP (PWM Generator x Capture)	534
FSEC Configuration	670	PGxCONH (PWM Generator x Control High)	515
FSIGN Configuration.....	671	PGxCONL (PWM Generator x Control Low)	514
FSMINPER (Frequency Scaling Minimum Period).....	504	PGxDC (PWM Generator x Duty Cycle).....	530
FWDT Configuration	674	PGxDCA (PWM Generator x Duty Cycle Adjustment).....	531
I2CxCONH (I2Cx Control High)	629	PGxDTH (PWM Generator x Dead-Time High)	533
I2CxCONL (I2Cx Control Low).....	627	PGxDTL (PWM Generator x Dead-Time Low)	533
I2CxMSK (I2Cx Slave Mode Address Mask)	631	PGxEVTH (PWM Generator x Event High)	527
I2CxSTAT (I2Cx Status)	630	PGxEVTL (PWM Generator x Event Low).....	526
IBIASCONH (Current Bias Generator Current Source Control High)	665	PGxIOCONH (PWM Generator x I/O Control High).....	520
IBIASCONL (Current Bias Generator Current Source Control Low)	666	PGxIOCONL (PWM Generator x I/O Control Low)	519
INDXxCNTH (Index x Counter High)	579	PGxLEBH (PWM Generator x Leading-Edge Blanking High)	529
INDXxCNTL (Index x Counter Low).....	579	PGxLEBL (PWM Generator x Leading-Edge Blanking Low).....	528
INDXxHLDH (Index x Counter Hold High)	580	PGxPER (PWM Generator x Period).....	531
INDXxHLDL (Index x Counter Hold Low).....	580	PGxPHASE (PWM Generator x Phase)	530
INTCON1 (Interrupt Control 1).....	106	PGxSTAT (PWM Generator x Status).....	517
INTCON1 (Slave Interrupt Control 1).....	325	PGxTRIGA (PWM Generator x Trigger A).....	532
INTCON2 (Interrupt Control 2).....	108	PGxTRIGB (PWM Generator x Trigger B).....	532
INTCON2 (Slave Interrupt Control 2).....	327	PGxTRIGC (PWM Generator x Trigger C)	532
INTCON3 (Interrupt Control 3).....	109	PGxyPCIH (PWM Generator xy PCI High).....	524
INTCON3 (Slave Interrupt Control 3).....	328	PGxyPCIL (PWM Generator xy PCI Low)	521
INTCON4 (Interrupt Control 4).....	110		
INTCON4 (Slave Interrupt Control 4).....	328		
INTTREG (Interrupt Control and Status).....	111		
INTTREG (Slave Interrupt Control and Status).....	329		
INTxTMRH (Interval x Timer High)	577		
INTxTMRL (Interval x Timer Low).....	577		
INTXxHLDH (Index x Counter Hold High).....	578		

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: <http://microchip.com/support>

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELoQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949 ==

Trademarks

The Microchip name and logo, the Microchip logo, AnyRate, AVR, AVR logo, AVR Freaks, BeaconThings, BitCloud, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPWR, Helder, JukeBlox, KEELoQ, KEELoQ logo, Klear, LANCheck, LINK MD, maxStylus, maxTouch, MediaLB, megaAVR, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, Prochip Designer, QTouch, RightTouch, SAM-BA, SpyNIC, SST, SST Logo, SuperFlash, tinyAVR, UNI/O, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ClockWorks, The Embedded Control Solutions Company, EtherSynch, Hyper Speed Control, HyperLight Load, IntelliMOS, mTouch, Precision Edge, and Quiet-Wire are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BodyCom, chipKIT, chipKIT logo, CodeGuard, CryptoAuthentication, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, Inter-Chip Connectivity, JitterBlocker, KlearNet, KlearNet logo, Mindi, MiWi, motorBench, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICKit, PICtail, PureSilicon, QMatrix, RightTouch logo, REAL ICE, Ripple Blocker, SAM-ICE, Serial Quad I/O, SMART-I.S., SQI, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2017-2018, Microchip Technology Incorporated, All Rights Reserved.

ISBN: 978-1-5224-3175-6