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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit Dual-Core
Speed	180MHz, 200MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	21
Program Memory Size	88KB (88K x 8)
Program Memory Type	FLASH, PRAM
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 23x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ch64mp202t-i-ss

Referenced Sources

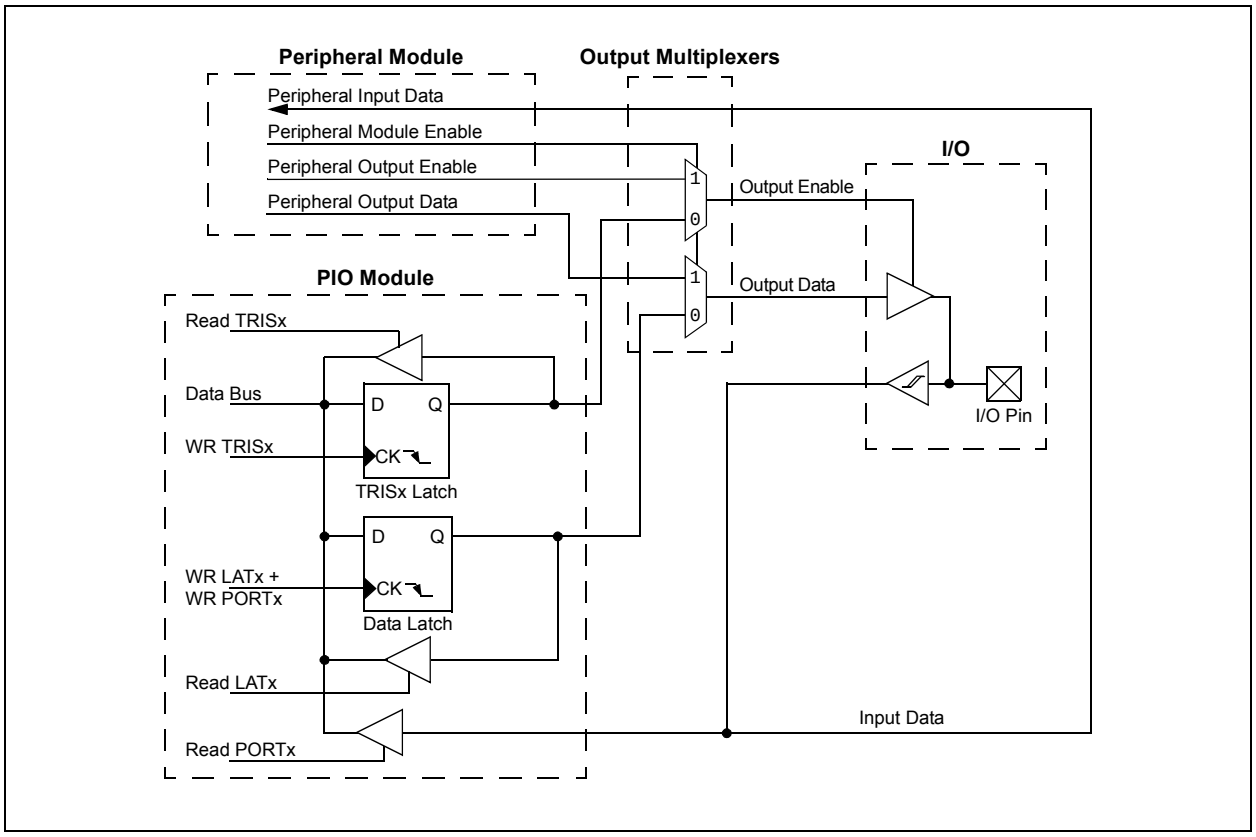
This device data sheet is based on the following individual chapters of the *"dsPIC33/PIC24 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note 1: To access the documents listed below, browse to the documentation section of the dsPIC33CH128MP508 product page of the Microchip web site (www.microchip.com) or select a family reference manual section from the following list.

In addition to parameters, features and other documentation, the resulting page provides links to the related family reference manual sections.

- **"Introduction"** (DS70573)
- **"dsPIC33E Enhanced CPU"** (DS70005158)
- **"dsPIC33E/PIC24E Program Memory"** (DS70000613)
- **"Data Memory"** (DS70595)
- **"Dual Partition Flash Program Memory"** (DS70005156)
- **"Flash Programming"** (DS70609)
- **"Reset"** (DS70602)
- **"Interrupts"** (DS70000600)
- **"I/O Ports with Edge Detect"** (DS70005322)
- **"Deadman Timer"** (DS70005155)
- **"CAN Flexible Data-Rate (FD) Protocol Module"** (DS70005340)
- **"12-Bit High-Speed, Multiple SARs A/D Converter (ADC)"** (DS70005213)
- **"Peripheral Trigger Generator (PTG)"** (DS70000669)
- **"Programmable Gain Amplifier (PGA)"** (DS70005146)
- **"Master Slave Interface (MSI) Module"** (DS70005278)
- **"Watchdog Timer and Power-Saving Modes"** (DS70615)
- **"Oscillator Module with High-Speed PLL"** (DS70005255)
- **"Timer1 Module"** (DS70005279)
- **"Direct Memory Access Controller (DMA)"** (DS39742)
- **"Capture/Compare/PWM/Timer (MCCP and SCCP)"** (DS33035)
- **"High-Resolution PWM with Fine Edge Placement"** (DS70005320)
- **"Serial Peripheral Interface (SPI) with Audio Codec Support"** (DS70005136)
- **"Inter-Integrated Circuit (I^2C)"** (DS70000195)
- **"Multiprotocol Universal Asynchronous Receiver Transmitter (UART) Module"** (DS70005288)
- **"Single-Edge Nibble Transmission (SENT) Module"** (DS70005145)
- **"32-Bit Programmable Cyclic Redundancy Check (CRC)"** (DS30009729)
- **"Configurable Logic Cell (CLC)"** (DS70005298)
- **"Quadrature Encoder Interface (QEI)"** (DS70000601)
- **"High-Speed Analog Comparator Module"** (DS70005280)
- **"Current Bias Generator (CBG)"** (DS70005253)
- **"Dual Watchdog Timer"** (DS70005250)
- **"Programming and Diagnostics"** (DS70608)
- **"CodeGuard™ Security"** (DS70634)

FIGURE 3-19: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE



REGISTER 3-78: RPOR10: PERIPHERAL PIN SELECT OUTPUT REGISTER 10

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP53R5	RP53R4	RP53R3	RP53R2	RP53R1	RP53R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP52R5	RP52R4	RP52R3	RP52R2	RP52R1	RP52R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP53<5:0>:** Peripheral Output Function is Assigned to RP53 Output Pin bits (see Table 3-33 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP52R<5:0>:** Peripheral Output Function is Assigned to RP52 Output Pin bits (see Table 3-33 for peripheral function numbers)

REGISTER 3-79: RPOR11: PERIPHERAL PIN SELECT OUTPUT REGISTER 11

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP55R5	RP55R4	RP55R3	RP55R2	RP55R1	RP55R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP54R5	RP54R4	RP54R3	RP54R2	RP54R1	RP54R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP55R<5:0>:** Peripheral Output Function is Assigned to RP55 Output Pin bits (see Table 3-33 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP54R<5:0>:** Peripheral Output Function is Assigned to RP54 Output Pin bits (see Table 3-33 for peripheral function numbers)

REGISTER 3-110: C1TBCH: CAN TIME BASE COUNTER REGISTER HIGH(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TBC<31:24>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TBC<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **TBC<31:16>** CAN Time Base Counter bits
This is a free-running timer that increments every TBCPREx clock when TBCEN is set.

Note 1: The Time Base Counter (TBC) will be stopped and reset when TBCEN = 0 to save power.
2: The TBC prescaler count will be reset on any write to C1TBCH/L (TBCPREx will be unaffected).

REGISTER 3-111: C1TBCL: CAN TIME BASE COUNTER REGISTER LOW(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TBC<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TBC<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **TBC<15:0>** CAN Time Base Counter bits
This is a free-running timer that increments every TBCPREx clock when TBCEN is set.

Note 1: The TBC will be stopped and reset when TBCEN = 0 to save power.
2: The TBC prescaler count will be reset on any write to C1TBCH/L (TBCPREx will be unaffected).

REGISTER 3-158: ADCON1H: ADC CONTROL REGISTER 1 HIGH

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-1	R/W-1	U-0	U-0	U-0	U-0	U-0
FORM	SHRRES1	SHRRES0	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **FORM:** Fractional Data Output Format bit
1 = Fractional
0 = Integer

bit 6-5 **SHRRES<1:0>:** Shared ADC Core Resolution Selection bits
11 = 12-bit resolution
10 = 10-bit resolution
01 = 8-bit resolution
00 = 6-bit resolution

bit 4-0 **Unimplemented:** Read as '0'

REGISTER 3-176: ADSTATL: ADC DATA READY STATUS REGISTER LOW

HSC/R-0	HSC/R-0	HSC/R-0	HSC/R-0	HSC/R-0	HSC/R-0	HSC/R-0	HSC/R-0
AN<15:8>RDY							
bit 15							bit 8

HSC/R-0	HSC/R-0	HSC/R-0	HSC/R-0	HSC/R-0	HSC/R-0	HSC/R-0	HSC/R-0
AN<7:0>RDY							
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **AN<15:0>RDY:** Common Interrupt Enable for Corresponding Analog Input bits
1 = Channel conversion result is ready in the corresponding ADCBUFx register
0 = Channel conversion result is not ready

REGISTER 3-177: ADSTATH: ADC DATA READY STATUS REGISTER HIGH

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	HSC/R-0	HSC/R-0	HSC/R-0	HSC/R-0	HSC/R-0
—	—	—	AN<20:16>RDY				
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4-0 **AN<20:16>RDY:** Common Interrupt Enable for Corresponding Analog Input bits
1 = Channel conversion result is ready in the corresponding ADCBUFx register
0 = Channel conversion result is not ready

TABLE 4-7: SLAVE SFR BLOCK 400h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
High-Speed PWM (Continued)			PG6CLPCIL	44A	0000000000000000	PG7DC	492	0000000000000000
PG5CONL	402	0-00000000000000	PG6CLPCIH	44C	0000-00000000000	PG7DCA	494	--------00000000
PG5CONH	404	000-000000--0000	PG6FFPCIL	44E	0000000000000000	PG7PER	496	0000000000000000
PG5STAT	406	0000000000000000	PG6FFPCIH	450	0000-00000000000	PG7TRIGA	498	0000000000000000
PG5IOCONL	408	0000000000000000	PG6SPCIL	452	0000000000000000	PG7TRIGB	49A	0000000000000000
PG5IOCONH	40A	-000---0--000000	PG6SPCIH	454	0000-00000000000	PG7TRIGC	49C	0000000000000000
PG5EVTL	40C	00000000---00000	PG6LEBL	456	0000000000000000	PG7DTL	49E	--00000000000000
PG5EVTH	40E	0000--0000000000	PG6LEBH	458	-----000----0000	PG7DTH	4A0	--00000000000000
PG5FPCIL	410	0000000000000000	PG6PHASE	45A	0000000000000000	PG7CAP	4A2	0000000000000000
PG5FPCIH	412	0000-00000000000	PG6DC	45C	0000000000000000	PG8CONL	4A4	0-00000000000000
PG5CLPCIL	414	0000000000000000	PG6DCA	45E	--------00000000	PG8CONH	4A6	000-000000--0000
PG5CLPCIH	416	0000-00000000000	PG6PER	460	0000000000000000	PG8STAT	4A8	0000000000000000
PG5FFPCIL	418	0000000000000000	PG6TRIGA	462	0000000000000000	PG8IOCONL	4AA	0000000000000000
PG5FFPCIH	41A	0000-00000000000	PG6TRIGB	464	0000000000000000	PG8IOCONH	4AC	-000---0--000000
PG5SPCIL	41C	0000000000000000	PG6TRIGC	466	0000000000000000	PG8EVTL	4AE	00000000---00000
PG5SPCIH	41E	0000-00000000000	PG6DTL	468	--00000000000000	PG8EVTH	4B0	0000--0000000000
PG5LEBL	420	0000000000000000	PG6DTH	46A	--00000000000000	PG8FPCIL	4B2	0000000000000000
PG5LEBH	422	-----000----0000	PG6CAP	46C	0000000000000000	PG8FPCIH	4B4	0000-00000000000
PG5PHASE	424	0000000000000000	PG7CONL	46E	0-00000000000000	PG8CLPCIL	4B6	0000000000000000
PG5DC	426	0000000000000000	PG7CONH	470	000-000000--0000	PG8CLPCIH	4B8	0000-00000000000
PG5DCA	428	--------00000000	PG7STAT	472	0000000000000000	PG8FFPCIL	4BA	0000000000000000
PG5PER	42A	0000000000000000	PG7IOCONL	474	0000000000000000	PG8FFPCIH	4BC	0000-00000000000
PG5TRIGA	42C	0000000000000000	PG7IOCONH	476	-000---0--000000	PG8SPCIL	4BE	0000000000000000
PG5TRIGB	42E	0000000000000000	PG7EVTL	478	00000000---00000	PG8SPCIH	4C0	0000-00000000000
PG5TRIGC	430	0000000000000000	PG7EVTH	47A	0000--0000000000	PG8LEBL	4C2	0000000000000000
PG5DTL	432	--00000000000000	PG7FPCIL	47C	0000000000000000	PG8LEBH	4C4	-----000----0000
PG5DTH	434	--00000000000000	PG7FPCIH	47E	0000-00000000000	PG8PHASE	4C6	0000000000000000
PG5CAP	436	0000000000000000	PG7CLPCIL	480	0000000000000000	PG8DC	4C8	0000000000000000
PG6CONL	438	0-00000000000000	PG7CLPCIH	482	0000-00000000000	PG8DCA	4CA	--------00000000
PG6CONH	43A	000-000000--0000	PG7FFPCIL	484	0000000000000000	PG8PER	4CC	0000000000000000
PG6STAT	43C	0000000000000000	PG7FFPCIH	486	0000-00000000000	PG8TRIGA	4CE	0000000000000000
PG6IOCONL	43E	0000000000000000	PG7SPCIL	488	0000000000000000	PG8TRIGB	4D0	0000000000000000
PG6IOCONH	440	-000---0--000000	PG7SPCIH	48A	0000-00000000000	PG8TRIGC	4D2	0000000000000000
PG6EVTL	442	00000000---00000	PG7LEBL	48C	0000000000000000	PG8DTL	4D4	--00000000000000
PG6EVTH	444	0000--0000000000	PG7LEBH	48E	-----000----0000	PG8DTH	4D6	--00000000000000
PG6FPCIL	446	0000000000000000	PG7PHASE	490	0000000000000000	PG8CAP	4D8	0000000000000000
PG6FPCIH	448	0000-00000000000						

Legend: x = unknown or indeterminate value; "-" = unimplemented bits. Address and Reset values are in hexadecimal and binary, respectively.

REGISTER 4-34: CNFx: INTERRUPT CHANGE NOTIFICATION FLAG FOR PORTx REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNFx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNFx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **CNFx<15:0>:** Interrupt Change Notification Flag for PORTx bits
When CNSTYLE (CNCONx<11>) = 1:
1 = An enabled edge event occurred on PORTx[n] pin
0 = An enabled edge event did not occur on PORTx[n] pin

REGISTER 4-76: RPOR16: PERIPHERAL PIN SELECT OUTPUT REGISTER 16

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP65R5	RP65R4	RP65R3	RP65R2	RP65R1	RP65R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP64R5	RP64R4	RP64R3	RP64R2	RP64R1	RP64R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP65R<5:0>:** Peripheral Output Function is Assigned to S1RP65 Output Pin bits (see Table 4-31 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP64R<5:0>:** Peripheral Output Function is Assigned to S1RP64 Output Pin bits (see Table 4-31 for peripheral function numbers)

REGISTER 4-77: RPOR17: PERIPHERAL PIN SELECT OUTPUT REGISTER 17

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP67R5	RP67R4	RP67R3	RP67R2	RP67R1	RP67R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP66R5	RP66R4	RP66R3	RP66R2	RP66R1	RP66R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP67R<5:0>:** Peripheral Output Function is Assigned to S1RP67 Output Pin bits (see Table 4-31 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP66R<5:0>:** Peripheral Output Function is Assigned to S1RP66 Output Pin bits (see Table 4-31 for peripheral function numbers)

REGISTER 6-2: CLKDIV: CLOCK DIVIDER REGISTER (MASTER) (CONTINUED)

bit 3-0 **PLLPRE<3:0>:** PLL Phase Detector Input Divider Select bits (also denoted as 'N1', PLL prescaler)(4)
11111 = Reserved
...
1001 = Reserved
1000 = Input divided by 8
0111 = Input divided by 7
0110 = Input divided by 6
0101 = Input divided by 5
0100 = Input divided by 4
0011 = Input divided by 3
0010 = Input divided by 2
0001 = Input divided by 1 (power-on default selection)
0000 = Reserved

Note 1: The DOZE<2:0> bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored.

2: This bit is cleared when the ROI bit is set and an interrupt occurs.

3: The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.

4: PLLPRE<3:0> may be updated while the PLL is operating, but the VCO may overshoot.

REGISTER 13-16: UxSCINT: UARTx SMART CARD INTERRUPT REGISTER

U-0	U-0	HS/R/W-0	HS/R/W-0	U-0	HS/R/W-0	HS/R/W-0	HS/R/W-0
—	—	RXRPTIF	TXRPTIF	—	BTCIF	WTCIF	GTCIF
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
—	—	RXRPTIE	TXRPTIE	—	BTCIE	WTCIE	GTCIE
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **RXRPTIF:** Receive Repeat Interrupt Flag bit
1 = Parity error has persisted after the same character has been received five times (four retransmits)
0 = Flag is cleared

bit 12 **TXRPTIF:** Transmit Repeat Interrupt Flag bit
1 = Line error has been detected after the last retransmit per TXRPT<1:0>
0 = Flag is cleared

bit 11 **Unimplemented:** Read as '0'

bit 10 **BTCIF:** Block Time Counter Interrupt Flag bit
1 = Block Time Counter has reached 0
0 = Block Time Counter has not reached 0

bit 9 **WTCIF:** Waiting Time Counter Interrupt Flag bit
1 = Waiting Time Counter has reached 0
0 = Waiting Time Counter has not reached 0

bit 8 **GTCIF:** Guard Time Counter Interrupt Flag bit
1 = Guard Time Counter has reached 0
0 = Guard Time Counter has not reached 0

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **RXRPTIE:** Receive Repeat Interrupt Enable bit
1 = An interrupt is invoked when a parity error has persisted after the same character has been received five times (four retransmits)
0 = Interrupt is disabled

bit 4 **TXRPTIE:** Transmit Repeat Interrupt Enable bit
1 = An interrupt is invoked when a line error is detected after the last retransmit per TXRPT<1:0> has been completed
0 = Interrupt is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2 **BTCIE:** Block Time Counter Interrupt Enable bit
1 = Block Time Counter interrupt is enabled
0 = Block Time Counter interrupt is disabled

bit 1 **WTCIE:** Waiting Time Counter Interrupt Enable bit
1 = Waiting Time Counter interrupt is enabled
0 = Waiting Time Counter Interrupt is disabled

bit 0 **GTCIE:** Guard Time Counter interrupt enable bit
1 = Guard Time Counter interrupt is enabled
0 = Guard Time Counter interrupt is disabled

To set up the SPIx module for Audio mode:

1. Clear the SPIxBUFL and SPIxBUFH registers.
2. If using interrupts:
   a) Clear the interrupt flag bits in the respective IFSx register.
   b) Set the interrupt enable bits in the respective IECx register.
   a) Write the SPIxIP bits in the respective IPCx register to set the interrupt priority.
3. Write the desired settings to the SPIxCON1L, SPIxCON1H and SPIxCON2L registers with AUDEN (SPIxCON1H<15>) = 1.
4. Clear the SPIROV bit (SPIxSTATL<6>).
5. Enable SPIx operation by setting the SPIEN bit (SPIxCON1L<15>).
6. Write the data to be transmitted to the SPIxBUFL and SPIxBUFH registers. Transmission (and reception) will start as soon as data is written to the SPIxBUFL and SPIxBUFH registers.

TABLE 15-2: I2Cx RESERVED ADDRESSES(1)

Slave Address	R/$\overline{W}$ Bit	Description
0000 000	0	General Call Address(2)
0000 000	1	Start Byte
0000 001	x	Cbus Address
0000 01x	x	Reserved
0000 1xx	x	HS Mode Master Code
1111 0xx	x	10-Bit Slave Upper Byte(3)
1111 1xx	x	Reserved

Note 1: The address bits listed here will never cause an address match independent of address mask settings.

2: This address will be Acknowledged only if GCEN = 1.

3: A match on this address can only occur on the upper byte in 10-Bit Addressing mode.

20.1 Current Bias Generator Control Registers

REGISTER 20-1: BIASCON: CURRENT BIAS GENERATOR CONTROL REGISTER

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
ON	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	I10EN3	I10EN2	I10EN1	I10EN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ON:** Current Bias Module Enable bit
1 = Module is enabled
0 = Module is disabled

bit 14-4 **Unimplemented:** Read as '0'

bit 3 **I10EN3:** 10 µA Enable for Output 3 bit
1 = 10 µA output is enabled
0 = 10 µA output is disabled

bit 2 **I10EN2:** 10 µA Enable for Output 2 bit
1 = 10 µA output is enabled
0 = 10 µA output is disabled

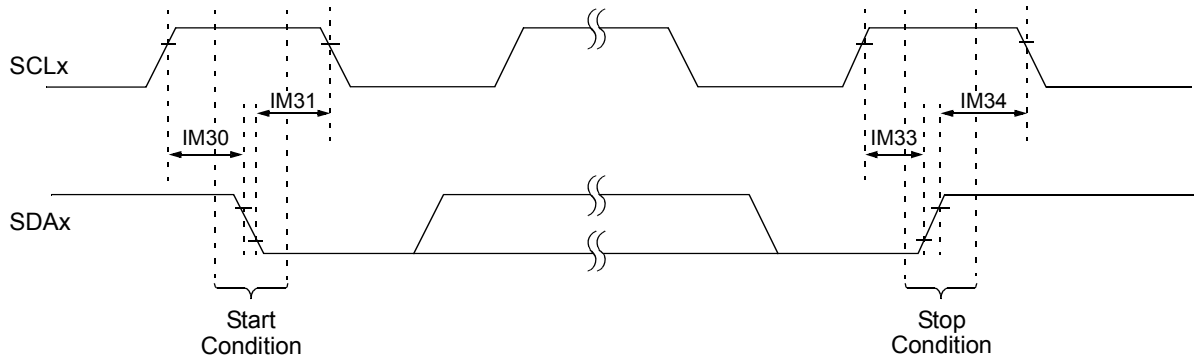
bit 1 **I10EN1:** 10 µA Enable for Output 1 bit
1 = 10 µA output is enabled
0 = 10 µA output is disabled

bit 0 **I10EN0:** 10 µA Enable for Output 0 bit
1 = 10 µA output is enabled
0 = 10 µA output is disabled

REGISTER 21-31: FS1ALTREG CONFIGURATION REGISTER (SLAVE) (CONTINUED)

bit 2-0 **S1CTXT1<2:0>:** Alternate Working Register Set #1 Interrupt Priority Level Selection bits
111 = Not assigned
110 = Alternate Register Set #1 is assigned to IPL Level 7
101 = Alternate Register Set #1 is assigned to IPL Level 6
100 = Alternate Register Set #1 is assigned to IPL Level 5
011 = Alternate Register Set #1 is assigned to IPL Level 4
010 = Alternate Register Set #1 is assigned to IPL Level 3
001 = Alternate Register Set #1 is assigned to IPL Level 2
000 = Alternate Register Set #1 is assigned to IPL Level 1

FIGURE 24-13: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)



Note: Refer to Figure 24-1 for load conditions.

FIGURE 24-14: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)

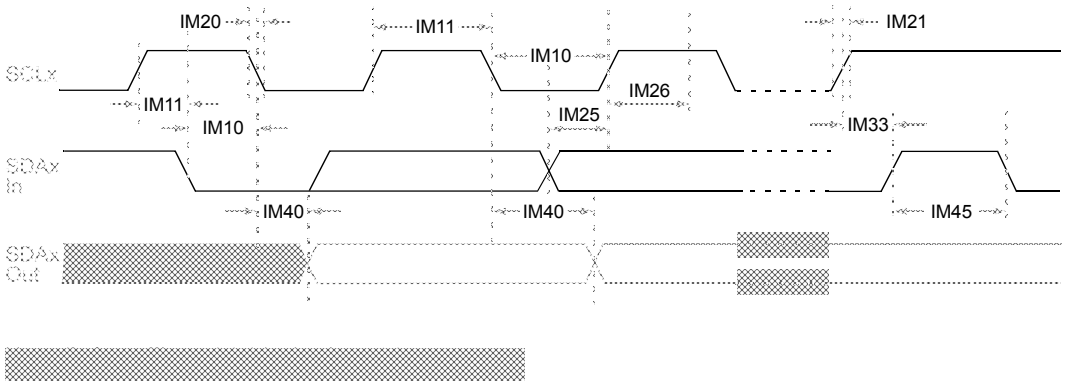


TABLE 24-40: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param No.	**Symbol**	**Characteristic(4)**		**Min.(1)**	**Max.**	**Units**	**Conditions**
IM10	TLO:SCL	Clock Low Time	100 kHz mode	TCY (BRG + 1)	—	µs	
			400 kHz mode	TCY (BRG + 1)	—	µs	
			1 MHz mode(2)	TCY (BRG + 1)	—	µs	
IM11	THI:SCL	Clock High Time	100 kHz mode	TCY (BRG + 1)	—	µs	
			400 kHz mode	TCY (BRG + 1)	—	µs	
			1 MHz mode(2)	TCY (BRG + 1)	—	µs	
IM20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 x (VDD/5.5V)	300	ns	
			1 MHz mode(2)	—	120	ns	
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(2)	—	120	ns	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode(2)	50	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	µs	
			400 kHz mode	0	0.9	µs	
			1 MHz mode(2)	0	0.3	µs	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	TCY (BRG + 1)	—	µs	Only relevant for Repeated Start condition
			400 kHz mode	TCY (BRG + 1)	—	µs	
			1 MHz mode(2)	TCY (BRG + 1)	—	µs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	TCY (BRG + 1)	—	µs	After this period, the first clock pulse is generated
			400 kHz mode	TCY (BRG + 1)	—	µs	
			1 MHz mode(2)	TCY (BRG + 1)	—	µs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	TCY (BRG + 1)	—	µs	
			400 kHz mode	TCY (BRG + 1)	—	µs	
			1 MHz mode(2)	TCY (BRG + 1)	—	µs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	TCY (BRG + 1)	—	µs	
			400 kHz mode	TCY (BRG + 1)	—	µs	
			1 MHz mode(2)	TCY (BRG + 1)	—	µs	
IM40	TAA:SCL	Output Valid from Clock	100 kHz mode	—	3450	ns	
			400 kHz mode	—	900	ns	
			1 MHz mode(2)	—	450	ns	
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode(2)	0.5	—	µs	
IM50	CB	Bus Capacitive Loading		—	400	pF	
IM51	TPGD	Pulse Gobbler Delay		65	390	ns	**(Note 3)**

Note 1: BRG is the value of the I^2C Baud Rate Generator.

2: Maximum Pin Capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: Typical value for this parameter is 130 ns.

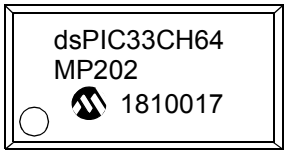
4: These parameters are characterized but not tested in manufacturing.

25.0 PACKAGING INFORMATION

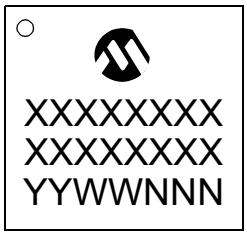
25.1 Package Marking Information

28-Lead SSOP (5.30 mm)

Example

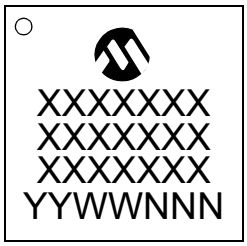


28-Lead UQFN (6x6 mm)



Example

36-Lead UQFN (5x5 mm)



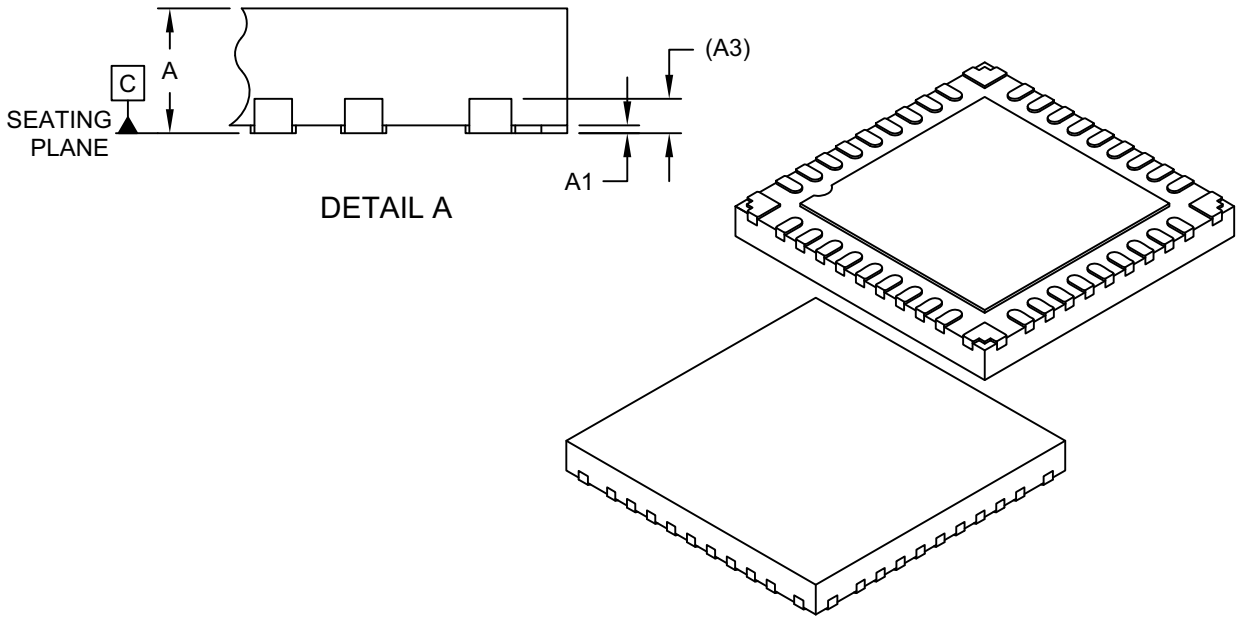
Example

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

36-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M5) - 5x5 mm Body [UQFN] With Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		36	
Pitch	e		0.40 BSC	
Overall Height	A	0.50	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.152 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.60	3.70	3.80
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.60	3.70	3.80
Terminal Width	b	0.15	0.20	0.25
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K		0.25 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

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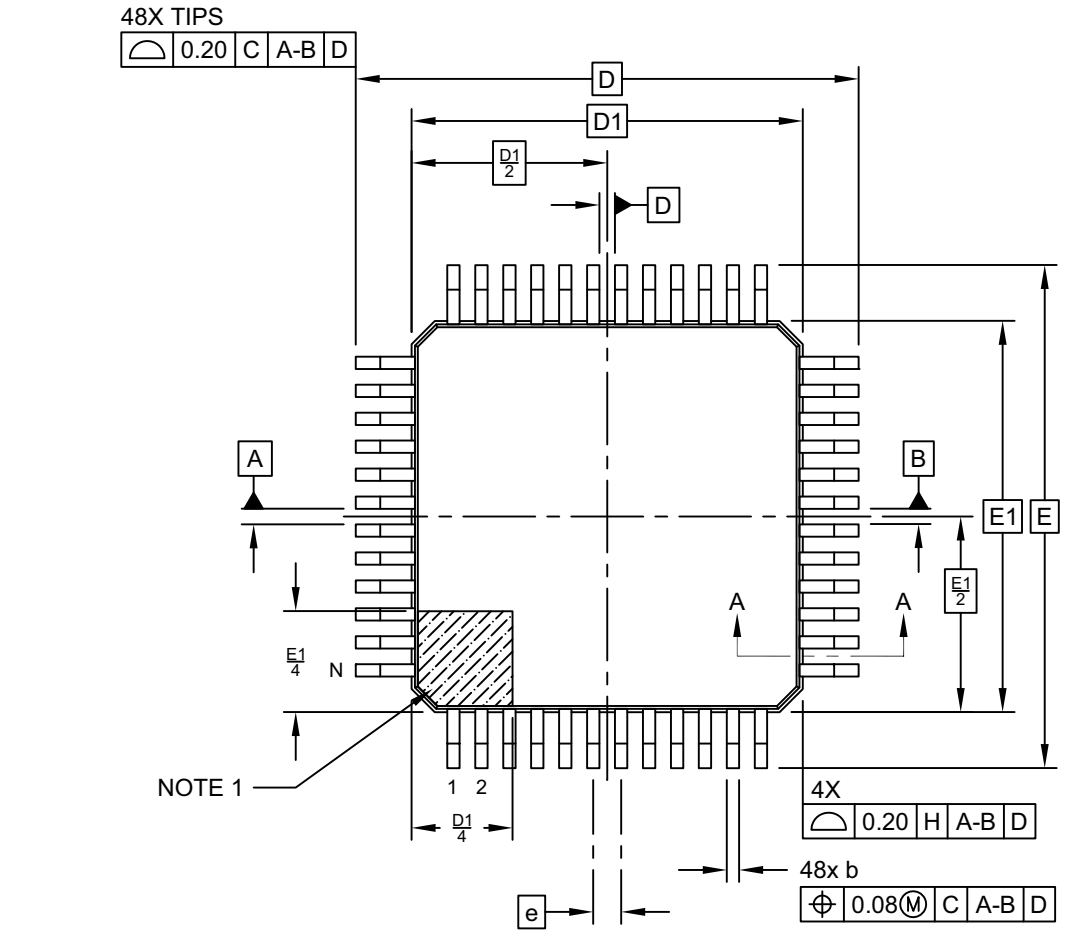
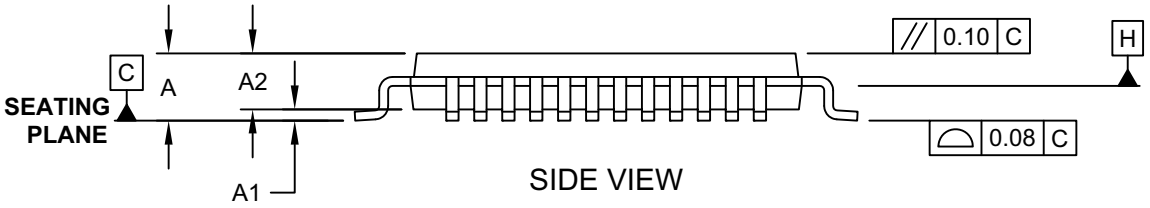
48-Lead Thin Quad Flatpack (PT) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

Microchip Technology Drawing C04-300-PT Rev A Sheet 1 of 2