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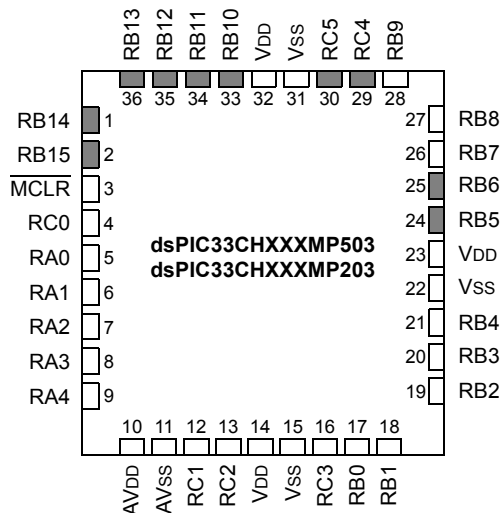
Applications of "[Embedded - Microcontrollers](#)"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit Dual-Core
Speed	180MHz, 200MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	27
Program Memory Size	88KB (88K x 8)
Program Memory Type	FLASH, PRAM
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-UQFN Exposed Pad
Supplier Device Package	36-UQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ch64mp203-i-m5

dsPIC33CH128MP508 FAMILY

Pin Diagrams (Continued)

36-Pin UQFN^(1,2)



- Note 1:** Shaded pins are up to 5.5 VDC tolerant (refer to Table 3-28 and Table 4-25). For the list of analog ports, refer to Table 3-27 and Table 4-24.
- Note 2:** The large center pad on the bottom of the package may be left floating or connected to VSS. The four-corner anchor pads are internally connected to the large bottom pad, and therefore, must be connected to the same net as the large center pad.

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TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name ⁽¹⁾	Pin Type	Buffer Type	PPS	Description
MCLR/S1MCLR1/S1MCLR2/S1MCLR3	I/P	ST	No	Master Clear (Reset) input. This pin is an active-low Reset to the device. S1MCLR _x is valid only for slave debug in Dual Debug mode.
AVDD	P	P	No	Positive supply for analog modules. This pin must be connected at all times.
AVSS	P	P	No	Ground reference for analog modules. This pin must be connected at all times.
VDD	P	—	No	Positive supply for peripheral logic and I/O pins
VSS	P	—	No	Ground reference for logic and I/O pins

Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power
 ST = Schmitt Trigger input with CMOS levels O = Output I = Input
 PPS = Peripheral Pin Select TTL = TTL input buffer

- Note 1:** Not all pins are available in all package variants. See the “**Pin Diagrams**” section for pin availability.
- 2:** These pins are remappable as well as dedicated. Some of the pins are associated with the Slave function and have S1 attached to the beginning of the name. For example, AN0 for the Slave is S1AN0.
- 3:** S1 attached to the beginning of the name indicates the Slave feature for that function. For example, AN0 for the Slave is S1AN0.

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REGISTER 3-28: CNPUx: CHANGE NOTIFICATION PULL-UP ENABLE FOR PORTx REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNPUx<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNPUx<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **CNPUx<15:0>**: Change Notification Pull-up Enable for PORTx bits
 1 = The pull-up for PORTx[n] is enabled – takes precedence over the pull-down selection
 0 = The pull-up for PORTx[n] is disabled

REGISTER 3-29: CNPDx: CHANGE NOTIFICATION PULL-DOWN ENABLE FOR PORTx REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNPDx<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNPDx<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **CNPDx<15:0>**: Change Notification Pull-Down Enable for PORTx bits
 1 = The pull-down for PORTx[n] is enabled (if the pull-up for PORTx[n] is not enabled)
 0 = The pull-down for PORTx[n] is disabled

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REGISTER 3-30: CNCONx: CHANGE NOTIFICATION CONTROL FOR PORTx REGISTER

R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
ON	—	—	—	CNSTYLE	—	—	—
bit 15				bit 8			

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **ON:** Change Notification (CN) Control for PORTx On bit
 1 = CN is enabled
 0 = CN is disabled
- bit 14-12 **Unimplemented:** Read as '0'
- bit 11 **CNSTYLE:** Change Notification Style Selection bit
 1 = Edge style (detects edge transitions, CNFx<15:0> bits are used for a Change Notification event)
 0 = Mismatch style (detects change from last port read, CNSTATx<15:0> bits are used for a Change Notification event)
- bit 10-0 **Unimplemented:** Read as '0'

REGISTER 3-31: CNEN0x: INTERRUPT CHANGE NOTIFICATION ENABLE FOR PORTx REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNEN0x<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNEN0x<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-0 **CNEN0x<15:0>:** Interrupt Change Notification Enable for PORTx bits
 1 = Interrupt-on-change (from the last read value) is enabled for PORTx[n]
 0 = Interrupt-on-change is disabled for PORTx[n]

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REGISTER 3-53: RPINR19: PERIPHERAL PIN SELECT INPUT REGISTER 19

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
U2DSRR7	U2DSRR6	U2DSRR5	U2DSRR4	U2DSRR3	U2DSRR2	U2DSRR1	U2DSRR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
U2RXR7	U2RXR6	U2RXR5	U2RXR4	U2RXR3	U2RXR2	U2RXR1	U2RXR0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **U2DSRR<7:0>**: Assign UART2 Data-Set-Ready ($\overline{U2DSR}$) to the Corresponding RPn Pin bits
 See Table 3-30.

bit 7-0 **U2RXR<7:0>**: Assign UART2 Receive (U2RX) to the Corresponding RPn Pin bits
 See Table 3-30.

REGISTER 3-54: RPINR20: PERIPHERAL PIN SELECT INPUT REGISTER 20

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SCK1R7	SCK1R6	SCK1R5	SCK1R4	SCK1R3	SCK1R2	SCK1R1	SCK1R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SDI1R7	SDI1R6	SDI1R5	SDI1R4	SDI1R3	SDI1R2	SDI1R1	SDI1R0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **SCK1R<7:0>**: Assign SPI1 Clock Input (SCK1IN) to the Corresponding RPn Pin bits
 See Table 3-30.

bit 7-0 **SDI1R<7:0>**: Assign SPI1 Data Input (SDI1) to the Corresponding RPn Pin bits
 See Table 3-30.

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REGISTER 3-55: RPINR21: PERIPHERAL PIN SELECT INPUT REGISTER 21

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
REFOIR7	REFOIR6	REFOIR5	REFOIR4	REFOIR3	REFOIR2	REFOIR1	REFOIR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SS1R7	SS1R6	SS1R5	SS1R4	SS1R3	SS1R2	SS1R1	SS1R0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **REFOIR<7:0>**: Assign Reference Clock Input (REFOI) to the Corresponding RPn Pin bits
 See Table 3-30.

bit 7-0 **SS1R<7:0>**: Assign SPI1 Slave Select ($\overline{SS1}$) to the Corresponding RPn Pin bits
 See Table 3-30.

REGISTER 3-56: RPINR22: PERIPHERAL PIN SELECT INPUT REGISTER 22

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SCK2R7	SCK2R6	SCK2R5	SCK2R4	SCK2R3	SCK2R2	SCK2R1	SCK2R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SDI2R7	SDI2R6	SDI2R5	SDI2R4	SDI2R3	SDI2R2	SDI2R1	SDI2R0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **SCK2R<7:0>**: Assign SPI2 Clock Input (SCK2IN) to the Corresponding RPn Pin bits
 See Table 3-30.

bit 7-0 **SDI2R<7:0>**: Assign SPI2 Data Input (SDI2) to the Corresponding RPn Pin bits
 See Table 3-30.

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REGISTER 3-93: DMTCLR: DEADMAN TIMER CLEAR REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STEP2<7:0>							
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **STEP2<7:0>:** DMT Clear Timer bits

00001000 = Clears STEP1<7:0>, STEP2<7:0> and the Deadman Timer if preceded by the correct loading of the STEP1<7:0> bits in the correct sequence. The write to these bits may be verified by reading the DMTCNTL/H register and observing the counter being reset.

All Other

Write Patterns = Sets the BAD2 bit; the value of STEP1<7:0> will remain unchanged and the new value being written to STEP2<7:0> will be captured. These bits are cleared when a DMT Reset event occurs.

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REGISTER 3-94: DMTSTAT: DEADMAN TIMER STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

HC/R-0	HC/R-0	HC/R-0	U-0	U-0	U-0	U-0	R-0
BAD1	BAD2	DMTEVENT	—	—	—	—	WINOPN
bit 7							bit 0

Legend:	HC = Hardware Clearable bit
R = Readable bit	W = Writable bit
-n = Value at POR	'1' = Bit is set
	U = Unimplemented bit, read as '0'
	'0' = Bit is cleared
	x = Bit is unknown

- bit 15-8 **Unimplemented:** Read as '0'
- bit 7 **BAD1:** Deadman Timer Bad STEP1<7:0> Value Detect bit
 1 = Incorrect STEP1<7:0> value was detected
 0 = Incorrect STEP1<7:0> value was not detected
- bit 6 **BAD2:** Deadman Timer Bad STEP2<7:0> Value Detect bit
 1 = Incorrect STEP2<7:0> value was detected
 0 = Incorrect STEP2<7:0> value was not detected
- bit 5 **DMTEVENT:** Deadman Timer Event bit
 1 = Deadman Timer event was detected (counter expired, or bad STEP1<7:0> or STEP2<7:0> value
 was entered prior to counter increment)
 0 = Deadman Timer event was not detected
- bit 4-1 **Unimplemented:** Read as '0'
- bit 0 **WINOPN:** Deadman Timer Clear Window bit
 1 = Deadman Timer clear window is open
 0 = Deadman Timer clear window is not open

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REGISTER 3-108: C1TDCH: CAN TRANSMITTER DELAY COMPENSATION REGISTER HIGH⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	EDGFLTEN	SID11EN
bit 15						bit 8	

U-0	U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0
—	—	—	—	—	—	TDCMOD1	TDCMOD0
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-10 **Unimplemented:** Read as '0'

bit 9 **EDGFLTEN:** Enable Edge Filtering During Bus Integration State bit

1 = Edge filtering is enabled according to ISO11898-1:2015

0 = Edge filtering is disabled

bit 8 **SID11EN:** Enable 12-Bit SID in CAN FD Base Format Messages bit

1 = RRS is used as SID11 in CAN FD base format messages: SID<11:0> = {SID<10:0>, SID11}

0 = Does not use RRS; SID<10:0>

bit 7-2 **Unimplemented:** Read as '0'

bit 1-0 **TDCMOD<1:0>:** Transmitter Delay Compensation Mode bits (Secondary Sample Point (SSP))

10-11 = Auto: Measures delay and adds TSEG1<4:0> (C1DBTCFGH<4:0>), adds TDCO<6:0>

01 = Manual: Does not measure, uses TDCV<5:0> + TDCO<6:0> from register

00 = Disable

Note 1: This register can only be modified in Configuration mode (OPMOD<2:0> = 100).

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REGISTER 3-131: C1TXQCONL: CAN TRANSMIT QUEUE CONTROL REGISTER LOW

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	FRESET	TXREQ	UINC
bit 15							bit 8

R-0	U-0	U-0	HS/C-0	U-0	R/W-0	U-0	R/W-0
TXEN	—	—	TXATIE	—	TXQEIE	—	TXQNIE
bit 7							bit 0

Legend:	HS = Hardware Settable bit	C = Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

- bit 15-11 **Unimplemented:** Read as '0'
- bit 10 **FRESET:** FIFO Reset bit
 1 = FIFO will be reset when bit is set, cleared by hardware when FIFO is reset; user should poll whether this bit is clear before taking any action
 0 = No effect
- bit 9 **TXREQ:** Message Send Request bit
 1 = Requests sending a message; the bit will automatically clear when all the messages queued in the TXQ are successfully sent
 0 = Clearing the bit to '0' while set ('1') will request a message abort
- bit 8 **UINC:** Increment Head/Tail bit
 When this bit is set, the FIFO head will increment by a single message.
- bit 7 **TXEN:** TX Enable bit
- bit 6-5 **Unimplemented:** Read as '0'
- bit 4 **TXATIE:** Transmit Attempts Exhausted Interrupt Enable bit
 1 = Enables interrupt
 0 = Disables interrupt
- bit 3 **Unimplemented:** Read as '0'
- bit 2 **TXQEIE:** Transmit Queue Empty Interrupt Enable bit
 1 = Interrupt is enabled for TXQ empty
 0 = Interrupt is disabled for TXQ empty
- bit 1 **Unimplemented:** Read as '0'
- bit 0 **TXQNIE:** Transmit Queue Not Full Interrupt Enable bit
 1 = Interrupt is enabled for TXQ not full
 0 = Interrupt is disabled for TXQ not full

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REGISTER 4-17: CORCON: SLAVE CORE CONTROL REGISTER⁽¹⁾

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0
VAR	—	US1	US0	EDT	DL2	DL1	DL0
bit 15						bit 8	

R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R-0	R/W-0	R/W-0
SATA	SATB	SATDW	ACCSAT	IPL3 ⁽²⁾	SFA	RND	IF
bit 7						bit 0	

Legend:	C = Clearable bit
R = Readable bit	W = Writable bit
-n = Value at POR	'1' = Bit is set
	U = Unimplemented bit, read as '0'
	'0' = Bit is cleared
	x = Bit is unknown

bit 15 **VAR:** Variable Exception Processing Latency Control bit
 1 = Variable exception processing is enabled
 0 = Fixed exception processing is enabled

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3⁽²⁾
 1 = CPU Interrupt Priority Level is greater than 7
 0 = CPU Interrupt Priority Level is 7 or less

- Note 1:** For complete register details, see Register 4-2.
Note 2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

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REGISTER 4-66: RPOR6: PERIPHERAL PIN SELECT OUTPUT REGISTER 6

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP45R5	RP45R4	RP45R3	RP45R2	RP45R1	RP45R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP44R5	RP44R4	RP44R3	RP44R2	RP44R1	RP44R0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13-8 **RP45R<5:0>:** Peripheral Output Function is Assigned to S1RP45 Output Pin bits
 (see Table 4-31 for peripheral function numbers)
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-0 **RP44R<5:0>:** Peripheral Output Function is Assigned to S1RP44 Output Pin bits
 (see Table 4-31 for peripheral function numbers)

REGISTER 4-67: RPOR7: PERIPHERAL PIN SELECT OUTPUT REGISTER 7

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP47R5	RP47R4	RP47R3	RP47R2	RP47R1	RP47R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP46R5	RP46R4	RP46R3	RP46R2	RP46R1	RP46R0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13-8 **RP47R<5:0>:** Peripheral Output Function is Assigned to S1RP47 Output Pin bits
 (see Table 4-31 for peripheral function numbers)
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-0 **RP46R<5:0>:** Peripheral Output Function is Assigned to S1RP46 Output Pin bits
 (see Table 4-31 for peripheral function numbers)

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REGISTER 4-99: ADEISTATL: ADC EARLY INTERRUPT STATUS REGISTER LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EISTAT<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EISTAT<7:0>							
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **EISTAT<15:0>**: Early Interrupt Status for Corresponding Analog Inputs bits
 1 = Early interrupt was generated
 0 = Early interrupt was not generated since the last ADCBUFx read

REGISTER 4-100: ADEISTATH: ADC EARLY INTERRUPT STATUS REGISTER HIGH

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	EISTAT<20:16>				
bit 7							bit 0

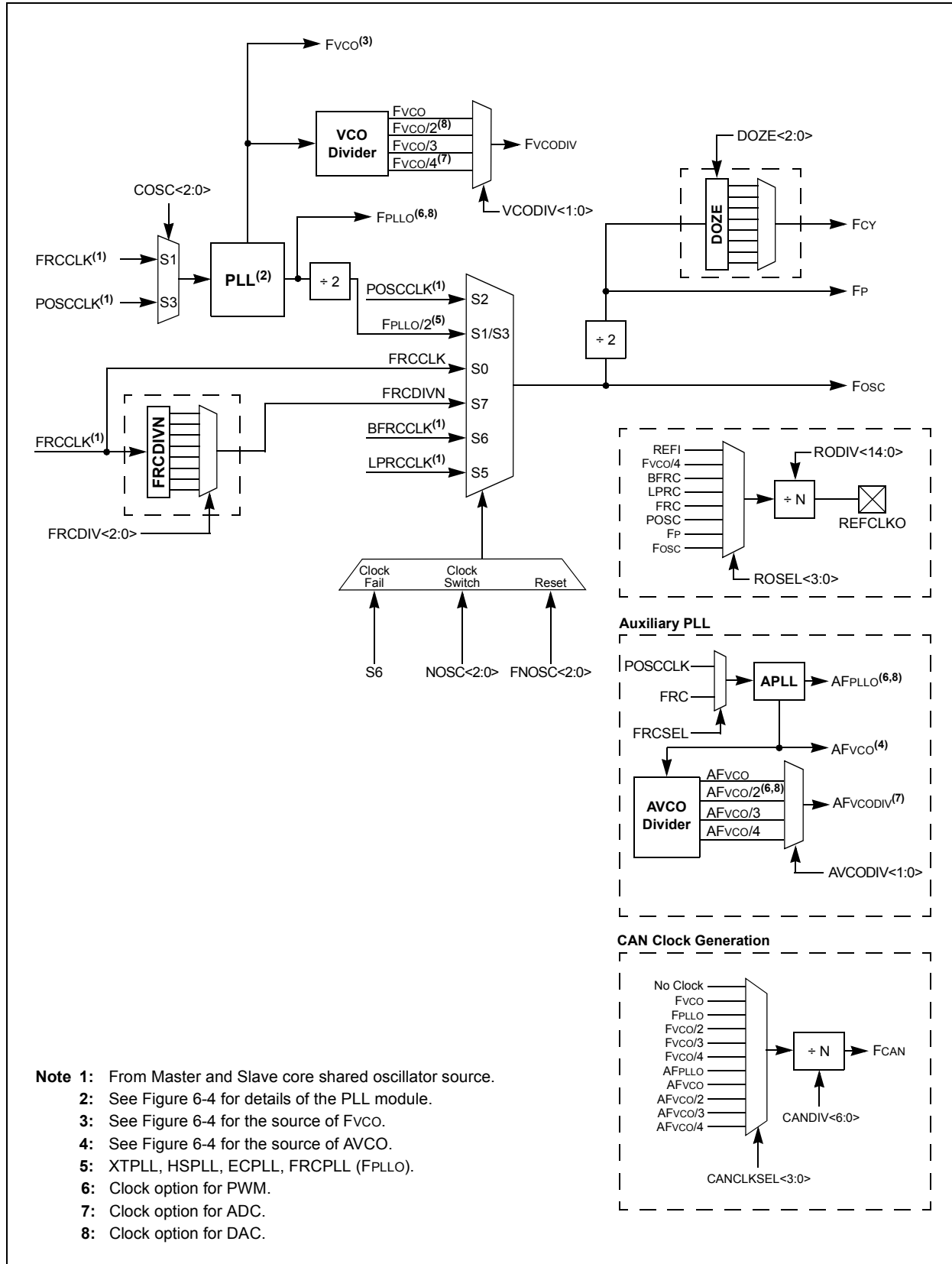
Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'
 bit 4-0 **EISTAT<20:16>**: Early Interrupt Status for Corresponding Analog Inputs bits
 1 = Early interrupt was generated
 0 = Early interrupt was not generated since the last ADCBUFx read

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FIGURE 6-2: MASTER CORE OSCILLATOR SUBSYSTEM



- Note 1:** From Master and Slave core shared oscillator source.
Note 2: See Figure 6-4 for details of the PLL module.
Note 3: See Figure 6-4 for the source of $Fvco$.
Note 4: See Figure 6-4 for the source of AVCO.
Note 5: XTPLL, HSPLL, ECPLL, FRCPLL ($FPLLO$).
Note 6: Clock option for PWM.
Note 7: Clock option for ADC.
Note 8: Clock option for DAC.

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REGISTER 11-8: SLPxCONH: DACx SLOPE CONTROL HIGH REGISTER

R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0
SLOPEN	—	—	—	HME ⁽¹⁾	TWME ⁽²⁾	PSE	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

- bit 15 **SLOPEN:** Slope Function Enable/On bit
 1 = Enables slope function
 0 = Disables slope function; slope accumulator is disabled to reduce power consumption
- bit 14-12 **Unimplemented:** Read as '0'
- bit 11 **HME:** Hysteretic Mode Enable bit⁽¹⁾
 1 = Enables Hysteretic mode for DACx
 0 = Disables Hysteretic mode for DACx
- bit 10 **TWME:** Triangle Wave Mode Enable bit⁽²⁾
 1 = Enables Triangle Wave mode for DACx
 0 = Disables Triangle Wave mode for DACx
- bit 9 **PSE:** Positive Slope Mode Enable bit
 1 = Slope mode is positive (increasing)
 0 = Slope mode is negative (decreasing)
- bit 8-0 **Unimplemented:** Read as '0'

Note 1: HME mode requires the user to disable the slope function (SLOPEN = 0).

2: TWME mode requires the user to enable the slope function (SLOPEN = 1).

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REGISTER 13-3: UxSTA: UARTx STATUS REGISTER (CONTINUED)

- bit 5 **ABDOVF**: Auto-Baud Rate Acquisition Interrupt Flag bit (must be cleared by software)
 1 = BRG rolled over during the auto-baud rate acquisition sequence (must be cleared in software)
 0 = BRG has not rolled over during the auto-baud rate acquisition sequence
- bit 4 **CERIF**: Checksum Error Interrupt Flag bit (must be cleared by software)
 1 = Checksum error
 0 = No checksum error
- bit 3 **FERR**: Framing Error Interrupt Flag bit
 1 = Framing Error: Inverted level of the Stop bit corresponding to the topmost character in the buffer;
 propagates through the buffer with the received character
 0 = No framing error
- bit 2 **RXBKIF**: Receive Break Interrupt Flag bit (must be cleared by software)
 1 = A Break was received
 0 = No Break was detected
- bit 1 **OERR**: Receive Buffer Overflow Interrupt Flag bit (must be cleared by software)
 1 = Receive buffer has overflowed
 0 = Receive buffer has not overflowed
- bit 0 **TXCIF**: Transmit Collision Interrupt Flag bit (must be cleared by software)
 1 = Transmitted word is not equal to the received word
 0 = Transmitted word is equal to the received word

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REGISTER 13-4: UxSTAH: UARTx STATUS REGISTER HIGH

U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
—	UTXISEL2	UTXISEL1	UTXISEL0	—	URXISEL2 ⁽¹⁾	URXISEL1 ⁽¹⁾	URXISEL0 ⁽¹⁾
bit 15				bit 8			

HS/R/W-0	R/W-0	R/S-1	R-0	R-1	R-1	R/S-1	R-0
TXWRE	STPMD	UTXBE	UTXBF	RIDLE	XON	URXBE	URXBF
bit 7							bit 0

Legend:	HS = Hardware Settable bit	S = Settable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

- bit 15 **Unimplemented:** Read as '0'
- bit 14-12 **UTXISEL<2:0>:** UART Transmit Interrupt Select bits
 111 = Sets transmit interrupt when there is one empty slot left in the buffer
 ...
 010 = Sets transmit interrupt when there are six empty slots or more in the buffer
 001 = Sets transmit interrupt when there are seven empty slots or more in the buffer
 000 = Sets transmit interrupt when there are eight empty slots in the buffer; TX buffer is empty
- bit 11 **Unimplemented:** Read as '0'
- bit 10-8 **URXISEL<2:0>:** UART Receive Interrupt Select bits⁽¹⁾
 111 = Triggers receive interrupt when there are eight words in the buffer; RX buffer is full
 ...
 001 = Triggers receive interrupt when there are two words or more in the buffer
 000 = Triggers receive interrupt when there is one word or more in the buffer
- bit 7 **TXWRE:** TX Write Transmit Error Status bit
LIN and Parity Modes:
 1 = A new byte was written when the buffer was full or when P2<8:0> = 0 (must be cleared by software)
 0 = No error
Address Detect Mode:
 1 = A new byte was written when the buffer was full or to P1<8:0> when P1x was full (must be cleared by software)
 0 = No error
Other Modes:
 1 = A new byte was written when the buffer was full (must be cleared by software)
 0 = No error
- bit 6 **STPMD:** Stop Bit Detection Mode bit
 1 = Triggers RXIF at the end of the last Stop bit
 0 = Triggers RXIF in the middle of the first (or second, depending on the STSEL<1:0> setting) Stop bit
- bit 5 **UTXBE:** UART TX Buffer Empty Status bit
 1 = Transmit buffer is empty; writing '1' when UTXEN = 0 will reset the TX FIFO Pointers and counters
 0 = Transmit buffer is not empty
- bit 4 **UTXBF:** UART TX Buffer Full Status bit
 1 = Transmit buffer is full
 0 = Transmit buffer is not full
- bit 3 **RIDLE:** Receive Idle bit
 1 = UART RX line is in the Idle state
 0 = UART RX line is receiving something

Note 1: The receive watermark interrupt is not set if PERIF or FERIF is set and the corresponding IE bit is set.

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REGISTER 21-26: FS1OSC CONFIGURATION REGISTER (SLAVE)

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23						bit 16	

U-1	U-1	U-1	U-1	U-1	U-1	U-1	r-1
—	—	—	—	—	—	—	—
bit 15						bit 8	

R/PO-1	R/PO-1	U-1	U-1	U-1	R/PO-1	U-1	U-1
S1FCKSM1	S1FCKSM0	—	—	—	S1OSCIOFNC ⁽¹⁾	—	—
bit 7						bit 0	

Legend:	PO = Program Once bit	r = Reserved bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

- bit 23-9 **Unimplemented:** Read as '1'
- bit 8 **Reserved:** Maintain as '1'
- bit 7-6 **S1FCKSM<1:0>:** Clock Switching and Monitor Selection Configuration bits
 - 1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled
 - 01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled
 - 00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
- bit 5-3 **Unimplemented:** Read as '1'
- bit 2 **S1OSCIOFNC:** OSCO Pin Function bit (except in XT and HS modes)⁽¹⁾
 - 1 = OSCO is the clock output
 - 0 = OSCO is the general purpose digital I/O pin
- bit 1-0 **Unimplemented:** Read as '1'

Note 1: The OSCO pin function is determined by the S1OSCIOFNC Configuration bit. If both the Master core OSCIOFNC and Slave core S1OSCIOFNC bits are set, the Master core OSCIOFNC bit has priority.

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21.9 JTAG Interface

The dsPIC33CH128MP508 family devices implement a JTAG interface, which supports boundary scan device testing. Detailed information on this interface will be provided in future revisions of this document.

Note: Refer to “**Programming and Diagnostics**” (DS70608) in the “*dsPIC33/PIC24 Family Reference Manual*” for further information on usage, configuration and operation of the JTAG interface.

21.10 In-Circuit Serial Programming™ (ICSP™)

The dsPIC33CH128MP508 family devices can be serially programmed while in the end application circuit. This is done with two lines for clock and data, and three other lines for power, ground and the programming sequence. Serial programming allows customers to manufacture boards with unprogrammed devices and then program the device just before shipping the product. Serial programming also allows the most recent firmware or a custom firmware to be programmed. Refer to the “*dsPIC33CH128MP508 Family Flash Programming Specification*” (DS70005285) for details about In-Circuit Serial Programming (ICSP).

Any of the three pairs of programming clock/data pins can be used:

- PGC1 and PGD1
- PGC2 and PGD2
- PGC3 and PGD3

Note: Both Master core and Slave core can be used with MPLAB® ICD to debug at the same time. There are PGCx and PGDx pins dedicated for the Master core and Slave core (S1PGCx and S1PGDx) to make this possible. MCLR is the same for programming the Master core and the Slave core. S1MCLR_x is used only when the Master and Slave are debugged simultaneously.

21.11 In-Circuit Debugger

When MPLAB® ICD 3 or the REAL ICE™ emulator is selected as a debugger, the in-circuit debugging functionality is enabled. This function allows simple debugging functions when used with MPLAB IDE. Debugging functionality is controlled through the PGCx (Emulation/Debug Clock) and PGDx (Emulation/Debug Data) pin functions.

Any of the three pairs of debugging clock/data pins can be used:

- PGC1 and PGD1 Master Debug or Slave Debug
- PGC2 and PGD2 Master Debug or Slave Debug
- PGC3 and PGD3 Master Debug or Slave Debug for debugging Master and Slave simultaneously, two MPLAB ICD debuggers or the REAL ICE™ emulator are required. This mode of debugging, where the Master and Slave are simultaneously debugged, is called the Dual Debug mode. S1MCLR_x and S1PGCx/S1PGD_x are used only in Dual Debug mode.

The Dual Debug mode of operation needs the following PGCx/PGDx pins:

- MCLR, PGC1 and PGD1 for Master Debug, and S1MCLR1, S1PGC1 and S1PGD1 for Slave Debug
- MCLR, PGC2 and PGD2 for Master Debug, and S1MCLR2, S1PGC2 and S1PGD2 for Slave Debug
- MCLR, PGC3 and PGD3 for Master Debug, and S1MCLR3, S1PGC3 and S1PGD3 for Slave Debug

To use the in-circuit debugger function of the device, the design must implement ICSP connections to MCLR, VDD, Vss and the PGCx/PGDx pin pair. In addition, when the feature is enabled, some of the resources are not available for general use. These resources include the first 80 bytes of data RAM and two or five (in Dual Debug) I/O pins (PGCx and PGDx).

There are three modes of debugging the dual core family of dsPIC33CH128MP508:

1. Master Only Debug
2. Slave Only Debug
3. Dual Debug

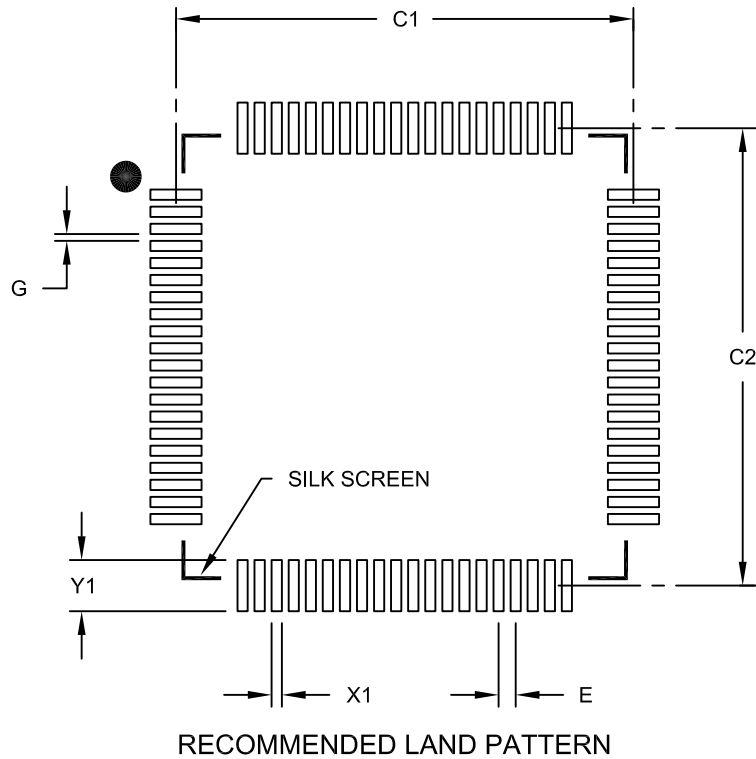
21.11.1 MASTER ONLY DEBUG

In Master Only Debug, only the Master project will be debugged. There is no project for Slave or no Slave code. The main project will be for dsPIC33CHXXXMP50X/20X and the user has to use MCLR and PGCx/PGDx for debugging. This is similar to debugging any single core existing device.

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80-Lead Plastic Thin Quad Flatpack (PT)-12x12x1mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0,50 BSC		
Contact Pad Spacing	C1		13,40	
Contact Pad Spacing	C2		13,40	
Contact Pad Width (X80)	X1			0,30
Contact Pad Length (X80)	Y1			1,50
Distance Between Pads	G	0,20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2092B