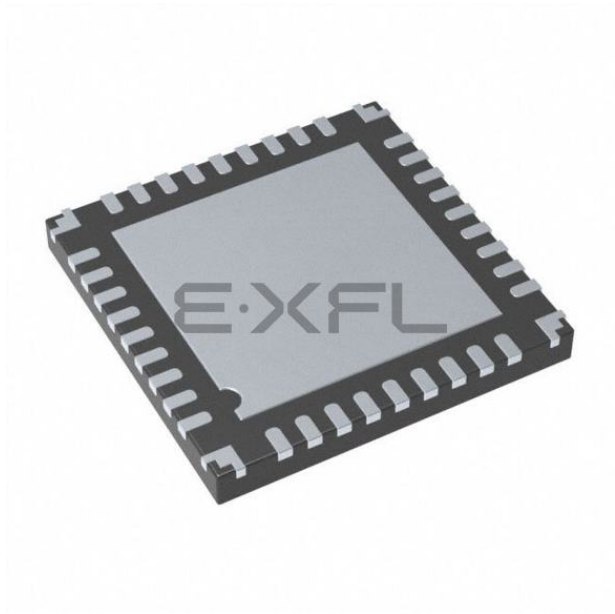
Microchip Technology - DSPIC33CH64MP203T-I/M5 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit Dual-Core
Speed	180MHz, 200MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	27
Program Memory Size	88KB (88K x 8)
Program Memory Type	FLASH, PRAM
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-UFQFN Exposed Pad
Supplier Device Package	36-UQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ch64mp203t-i-m5

TABLE 1: MASTER AND SLAVE CORE FEATURES

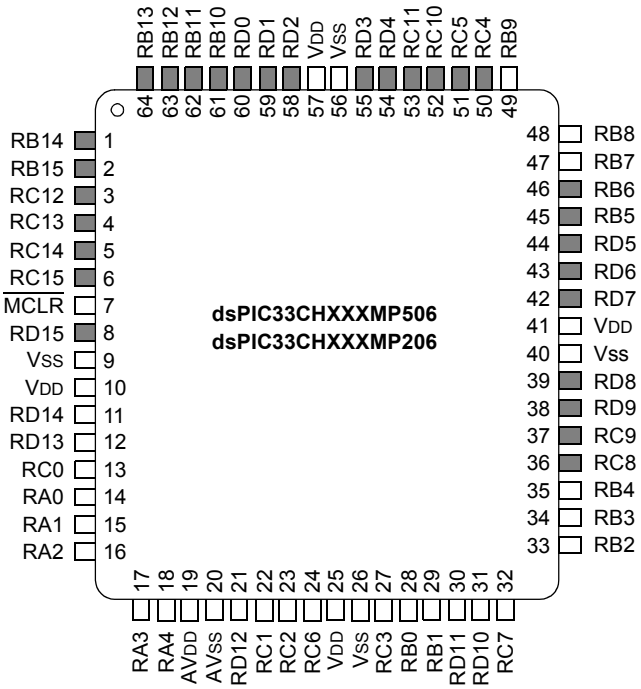
Feature	Master Core	Slave Core	Shared
Core Frequency	90 MIPS @ 180 MHz	100 MIPS @ 200 MHz	—
Program Memory	64K-128 Kbytes	24 Kbytes (PRAM)(2)	—
Internal Data RAM	16 Kbytes	4 Kbytes	—
16-Bit Timer	1	1	—
DMA	6	2	—
SCCP (Capture/Compare/Timer)	8	4	—
UART	2	1	—
SPI/I²S	2	1	—
I²C	2	1	—
CAN FD	1	—	—
SENT	2	—	—
CRC	1	—	—
QEI	1	1	—
PTG	1	—	—
CLC	4	4	—
16-Bit High-Speed PWM	4	8	—
ADC 12-Bit	1	3	—
Digital Comparator	4	4	—
12-Bit DAC/Analog CMP Module	1	3	—
Watchdog Timer	1	1	—
Deadman Timer	1	—	—
Input/Output	69	69	69
Simple Breakpoints	5	2	—
PGAs(1)	—	3	3
DAC Output Buffer	—	—	1
Oscillator	1	1	1

Note 1: Slave owns the peripheral/feature, but it is shared with the Master.

2: Dual Partition feature is available on Slave PRAM.

Pin Diagrams (Continued)

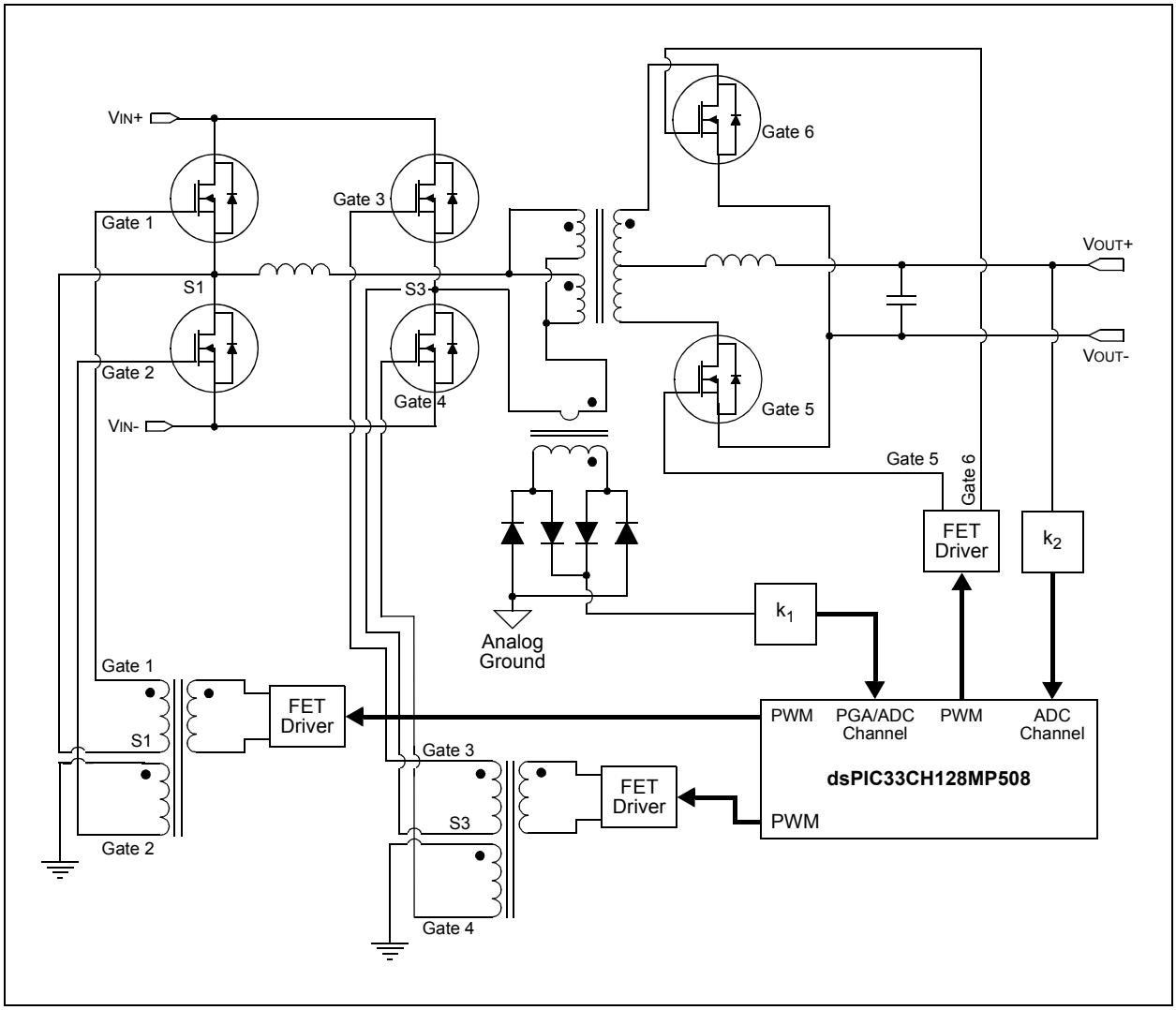
64-Pin TQFP/QFN(1,2)



Note 1: **Shaded pins** are up to 5.5 VDC tolerant (refer to Table 3-28 and Table 4-25). For the list of analog ports, refer to Table 3-27 and Table 4-24.

2: The large center pad on the bottom of the package may be left floating or connected to VSS. The four-corner anchor pads are internally connected to the large bottom pad, and therefore, must be connected to the same net as the large center pad.

FIGURE 2-5: PHASE-SHIFTED FULL-BRIDGE CONVERTER



3.2 Master Memory Organization

Note:	This data sheet summarizes the features of the dsPIC33CH128MP508 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"dsPIC33E/PIC24E Program Memory"** (DS70000613) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

The dsPIC33CH128MP508 family architecture features separate program and data memory spaces, and buses. This architecture also allows the direct access of program memory from the Data Space (DS) during code execution.

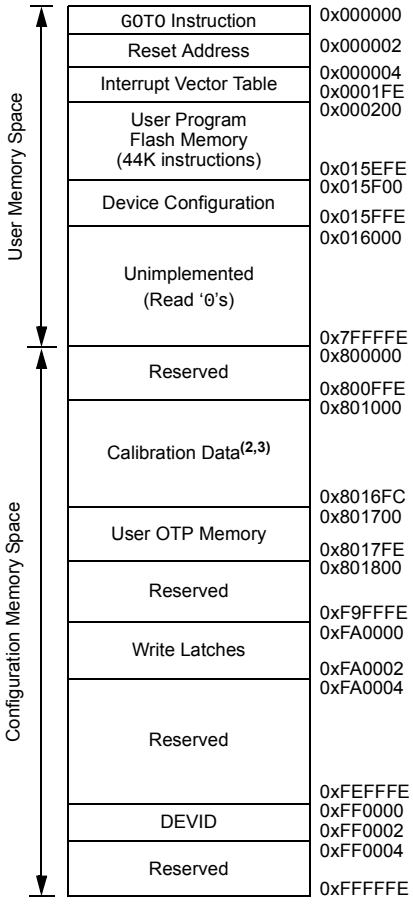
3.2.1 PROGRAM ADDRESS SPACE

The program address memory space of the dsPIC33CH128MP508 family devices is 4M instructions. The space is addressable by a 24-bit value derived either from the 23-bit PC during program execution, or from table operation or Data Space remapping, as described in **Section 3.2.9 "Interfacing Program and Data Memory Spaces"**.

User application access to the program memory space is restricted to the lower half of the address range (0x000000 to 0x7FFFFF). The exception is the use of TBLRD operations, which use TBLPAG<7> to permit access to calibration data and Device ID sections of the configuration memory space.

The program memory maps for the Master dsPIC33CHXXXMPX08 device are shown in Figure 3-3 and Figure 3-4.

FIGURE 3-3: PROGRAM MEMORY MAP FOR MASTER dsPIC33CH128MPXXX DEVICES(1)



Note 1: Memory areas are not shown to scale.
2: Calibration data area must be maintained during programming.
3: Calibration data area includes UDID locations.

REGISTER 3-5: NVMADR: NONVOLATILE MEMORY LOWER ADDRESS REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
NVMADR<15:8>							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
NVMADR<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **NVMADR<15:0>:** Nonvolatile Memory Lower Write Address bits
Selects the lower 16 bits of the location to program or erase in Program Flash Memory. This register may be read or written to by the user application.

REGISTER 3-6: NVMADRU: NONVOLATILE MEMORY UPPER ADDRESS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
NVMADRU<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **NVMADRU<23:16>:** Nonvolatile Memory Upper Write Address bits
Selects the upper 8 bits of the location to program or erase in Program Flash Memory. This register may be read or written to by the user application.

TABLE 3-23: MASTER INTERRUPT VECTOR DETAILS (CONTINUED)

Interrupt Source	Vector #	IRQ #	IVT Address	Interrupt Bit Location		
				Flag	Enable	Priority
QEI1 – QEI Position Counter Compare	56	48	0x000074	IFS3<0>	IEC3<0>	IPC12<2:0>
U1E – UART1 Error	57	49	0x000076	IFS3<1>	IEC3<1>	IPC12<6:4>
U2E – UART2 Error	58	50	0x000078	IFS3<2>	IEC3<2>	IPC12<10:8>
CRC – CRC Generator	59	51	0x00007A	IFS3<3>	IEC3<3>	IPC12<14:12>
C1TX – CAN1 TX Data Request	60	52	0x00007C	IFS3<4>	IEC3<4>	IPC13<2:0>
Reserved	61-68	53-68	0x00007E-0x00008C	—	—	—
ICD – In-Circuit Debugger	69	61	0x00008E	IFS3<13>	IEC3<13>	IPC15<6:4>
JTAG – JTAG Programming	70	62	0x000090	IFS3<14>	IEC3<14>	IPC15<10:8>
PTGSTEP – PTG Step	71	63	0x000092	IFS3<15>	IEC3<15>	IPC15<14:12>
I2C1BC – I2C1 Bus Collision	72	64	0x000094	IFS4<0>	IEC4<0>	IPC16<2:0>
I2C2BC – I2C2 Bus Collision	73	65	0x000096	IFS4<1>	IEC4<1>	IPC16<6:4>
Reserved	74	66	0x000098	—	—	—
PWM1 – PWM Generator 1	75	67	0x00009A	IFS4<3>	IEC4<3>	IPC16<14:12>
PWM2 – PWM Generator 2	76	68	0x00009C	IFS4<4>	IEC4<4>	IPC17<2:0>
PWM3 – PWM Generator 3	77	69	0x00009E	IFS4<5>	IEC4<5>	IPC17<6:4>
PWM4 – PWM Generator 4	78	70	0x0000A0	IFS4<6>	IEC4<6>	IPC17<10:8>
Reserved	79-82	71-74	0x0000A2	—	—	—
CND – Change Notice D	83	75	0x0000AA	IFS4<11>	IEC4<11>	IPC18<14:12>
CNE – Change Notice E	84	76	0x0000AC	IFS4<12>	IEC4<12>	IPC19<2:0>
CMP1 – Comparator 1	85	77	0x0000AE	IFS4<13>	IEC4<13>	IPC19<6:4>
Reserved	86-88	78-80	0x0000B0-0x0000B4	—	—	—
PTGWDT – PTG Watchdog Timer Time-out	89	81	0x0000B6	IFS5<1>	IEC5<1>	IPC20<6:4>
PTG0 – PTG Trigger 0	90	82	0x0000B8	IFS5<2>	IEC5<2>	IPC20<10:8>
PTG1 – PTG Trigger 1	91	83	0x0000BA	IFS5<3>	IEC5<3>	IPC20<14:12>
PTG2 – PTG Trigger 2	92	84	0x0000BC	IFS5<4>	IEC5<4>	IPC21<2:0>
PTG3 – PTG Trigger 3	93	85	0x0000BE	IFS5<5>	IEC5<6>	IPC21<6:4>
SENT1 – SENT1 TX/RX	94	86	0x0000C0	IFS5<6>	IEC5<6>	IPC21<10:8>
SENT1E – SENT1 Error	95	87	0x0000C2	IFS5<7>	IEC5<7>	IPC21<14:12>
SENT2 – SENT2 TX/RX	96	88	0x0000C4	IFS5<8>	IEC5<8>	IPC22<2:0>
SENT2E – SENT2 Error	97	89	0x0000C6	IFS5<9>	IEC5<9>	IPC22<6:4>
ADC – ADC Global Interrupt	98	90	0x0000C8	IFS5<10>	IEC5<10>	IPC22<10:8>
ADCAN0 – ADC AN0 Interrupt	99	91	0x0000CA	IFS5<11>	IEC5<11>	IPC22<14:12>
ADCAN1 – ADC AN1 Interrupt	100	92	0x0000CC	IFS5<12>	IEC5<12>	IPC23<2:0>
ADCAN2 – ADC AN2 Interrupt	101	93	0x0000CE	IFS5<13>	IEC5<13>	IPC23<6:4>
ADCAN3 – ADC AN3 Interrupt	102	94	0x0000D0	IFS5<14>	IEC5<14>	IPC23<10:8>
ADCAN4 – ADC AN4 Interrupt	103	95	0x0000D2	IFS5<15>	IEC5<15>	IPC23<14:12>
ADCAN5 – ADC AN5 Interrupt	104	96	0x0000D4	IFS6<0>	IEC6<0>	IPC24<2:0>
ADCAN6 – ADC AN6 Interrupt	105	97	0x0000D6	IFS6<1>	IEC6<1>	IPC24<6:4>
ADCAN7 – ADC AN7 Interrupt	106	98	0x0000D8	IFS6<2>	IEC6<2>	IPC24<10:8>
ADCAN8 – ADC AN8 Interrupt	107	99	0x0000DA	IFS6<3>	IEC6<3>	IPC24<14:12>
ADCAN9 – ADC AN9 Interrupt	108	100	0x0000DC	IFS6<4>	IEC6<4>	IPC25<2:0>
ADCAN10 – ADC AN10 Interrupt	109	101	0x0000DE	IFS6<5>	IEC6<5>	IPC25<6:4>
ADCAN11 – ADC AN11 Interrupt	110	102	0x0000E0	IFS6<6>	IEC6<6>	IPC25<10:8>
ADCAN12 – ADC AN12 Interrupt	111	103	0x0000E2	IFS6<7>	IEC6<7>	IPC25<14:12>
ADCAN13 – ADC AN13 Interrupt	112	104	0x0000E4	IFS6<8>	IEC6<8>	IPC26<2:0>
ADCAN14 – ADC AN14 Interrupt	113	105	0x0000E6	IFS6<9>	IEC6<9>	IPC26<6:4>
ADCAN15 – ADC AN15 Interrupt	114	106	0x0000E8	IFS6<10>	IEC6<10>	IPC26<10:8>

3.7.1 DEADMAN TIMER CONTROL REGISTERS

REGISTER 3-91: DMTCON: DEADMAN TIMER CONTROL REGISTER

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
ON(1)	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ON:** DMT Module Enable bit(1)
1 = Deadman Timer module is enabled
0 = Deadman Timer module is not enabled

bit 14-0 **Unimplemented:** Read as '0'

Note 1: This bit has control only when DMTDIS = 0 in the FDMT register.

REGISTER 3-92: DMTPRECLR: DEADMAN TIMER PRECLEAR REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STEP1<7:0>							
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **STEP1<7:0>:** DMT Preclear Enable bits
01000000 = Enables the Deadman Timer preclear (Step 1)
All Other Write Patterns = Sets the BAD1 flag; these bits are cleared when a DMT Reset event occurs. STEP1<7:0> bits are also cleared if the STEP2<7:0> bits are loaded with the correct value in the correct sequence.

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 3-110: C1TBCH: CAN TIME BASE COUNTER REGISTER HIGH(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TBC<31:24>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TBC<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **TBC<31:16>** CAN Time Base Counter bits
This is a free-running timer that increments every TBCPREx clock when TBCEN is set.

Note 1: The Time Base Counter (TBC) will be stopped and reset when TBCEN = 0 to save power.
2: The TBC prescaler count will be reset on any write to C1TBCH/L (TBCPREx will be unaffected).

REGISTER 3-111: C1TBCL: CAN TIME BASE COUNTER REGISTER LOW(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TBC<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TBC<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **TBC<15:0>** CAN Time Base Counter bits
This is a free-running timer that increments every TBCPREx clock when TBCEN is set.

Note 1: The TBC will be stopped and reset when TBCEN = 0 to save power.
2: The TBC prescaler count will be reset on any write to C1TBCH/L (TBCPREx will be unaffected).

REGISTER 3-162: ADCON3H: ADC CONTROL REGISTER 3 HIGH

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CLKSEL1	CLKSEL0	CLKDIV5	CLKDIV4	CLKDIV3	CLKDIV2	CLKDIV1	CLKDIV0
bit 15							bit 8

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
SHREN	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **CLKSEL<1:0>:** ADC Module Clock Source Selection bits
11 = FVCO/4
10 = AFVCODIV
01 = FOSC
00 = FP (FOSC/2)

bit 13-8 **CLKDIV<5:0>:** ADC Module Clock Source Divider bits
The divider forms a TCORESRC clock used by all ADC cores (shared and dedicated), from the TSRC ADC module clock source, selected by the CLKSEL<1:0> bits. Then, each ADC core individually divides the TCORESRC clock to get a core-specific TADCORE clock using the ADCS<6:0> bits in the ADCOREXH register or the SHRADCS<6:0> bits in the ADCON2L register.
111111 = 64 Source Clock Periods
...
000011 = 4 Source Clock Periods
000010 = 3 Source Clock Periods
000001 = 2 Source Clock Periods
000000 = 1 Source Clock Period

bit 7 **SHREN:** Shared ADC Core Enable bit
1 = Shared ADC core is enabled
0 = Shared ADC core is disabled

bit 6-0 **Unimplemented:** Read as '0'

FIGURE 4-10: BIT-REVERSED ADDRESSING EXAMPLE

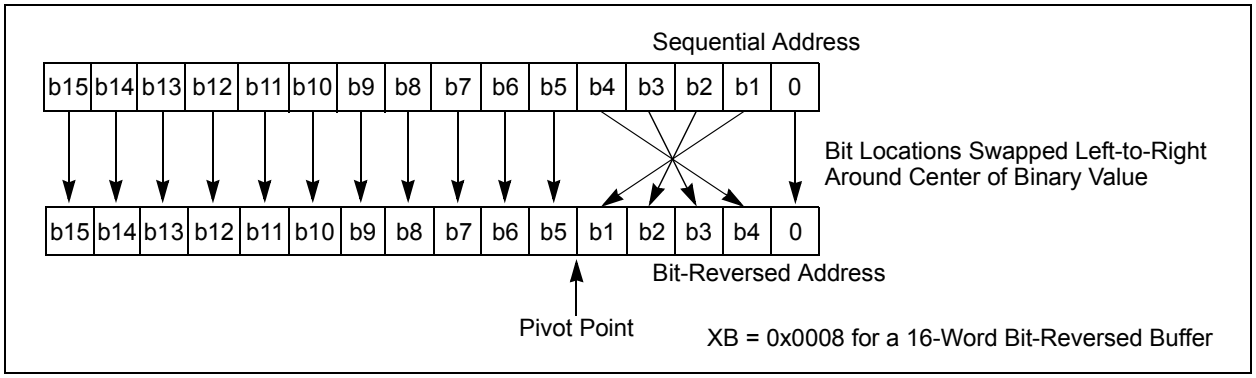


TABLE 4-18: BIT-REVERSED ADDRESSING SEQUENCE (16-ENTRY)

Normal Address					Bit-Reversed Address				
A3	**A2**	**A1**	**A0**	**Decimal**	**A3**	**A2**	**A1**	**A0**	**Decimal**
0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	0	0	0	8
0	0	1	0	2	0	1	0	0	4
0	0	1	1	3	1	1	0	0	12
0	1	0	0	4	0	0	1	0	2
0	1	0	1	5	1	0	1	0	10
0	1	1	0	6	0	1	1	0	6
0	1	1	1	7	1	1	1	0	14
1	0	0	0	8	0	0	0	1	1
1	0	0	1	9	1	0	0	1	9
1	0	1	0	10	0	1	0	1	5
1	0	1	1	11	1	1	0	1	13
1	1	0	0	12	0	0	1	1	3
1	1	0	1	13	1	0	1	1	11
1	1	1	0	14	0	1	1	1	7
1	1	1	1	15	1	1	1	1	15

TABLE 4-20: SLAVE INTERRUPT VECTOR DETAILS (CONTINUED)

Interrupt Source	Vector #	IRQ #	IVT Address	Interrupt Bit Location		
				Flag	Enable	Priority
SPI1 – SPI1 Error	134	126	0x000110	IFS7<14>	IEC7<14>	IPC31<10:8>
Reserved	135-136	127-128	0x000112-0x000114	—	—	—
MSIM – MSI Master Initiated Interrupt	137	129	0x000116	IFS8<1>	IEC8<1>	IPC32<6:4>
MSIA – MSI Protocol A	138	130	0x000118	IFS8<2>	IEC8<2>	IPC32<10:8>
MSIB – MSI Protocol B	139	131	0x00011A	IFS8<3>	IEC8<3>	IPC32<14:12>
MSIC – MSI Protocol C	140	132	0x00011C	IFS8<4>	IEC8<4>	IPC33<2:0>
MSID – MSI Protocol D	141	133	0x00011E	IFS8<5>	IEC8<5>	IPC33<6:4>
MSIE – MSI Protocol E	142	134	0x000120	IFS8<6>	IEC8<6>	IPC33<10:8>
MSIF – MSI Protocol F	143	135	0x000122	IFS8<7>	IEC8<7>	IPC33<14:12>
MSIG – MSI Protocol G	144	136	0x000124	IFS8<8>	IEC8<8>	IPC34<2:0>
MSIH – MSI Protocol H	145	137	0x000126	IFS8<9>	IEC8<9>	IPC34<6:4>
MSIDT – MSI Slave Read FIFO Data Ready	146	138	0x000128	IFS8<10>	IEC8<10>	IPC34<10:8>
MSIWFE – MSI Slave Write FIFO Empty	147	139	0x00012A	IFS8<11>	IEC8<11>	IPC34<14:12>
MSIFLT – Read or Write FIFO Fault (Over/Underflow)	148	140	0x00012C	IFS8<12>	IEC8<12>	IPC35<2:0>
MSIMRST– MSI Master Reset	149	141	0x00012E-0x000134	IFS8<13>	IEC8<13>	IPC35<6:4>
Reserved	150-152	142-144	0x000130	—	—	—
MSTBRK – Master Break	153	145	0x000136	IFS9<1>	IEC9<1>	IPC36<6:4>
Reserved	154-163	146-163	0x000138-0x00014A	—	—	—
MCLKF – Master Clock Fail	164	156	0x00014C	IFS9<12>	IEC9<12>	IPC39<2:0>
Reserved	165-175	157-167	0x00014E-0x000162	—	—	—
ADFIFO – ADC FIFO Ready	176	168	0x000164	IFS10<8>	IEC10<8>	IPC42<2:0>
PEVTA – PWM Event A	177	169	0x000166	IFS10<9>	IEC10<9>	IPC42<6:4>
PEVTB – PWM Event B	178	170	0x000168	IFS10<10>	IEC10<10>	IPC42<10:8>
PEVTC – PWM Event C	179	171	0x00016A	IFS10<11>	IEC10<11>	IPC42<14:12>
PEVTD – PWM Event D	180	172	0x00016C	IFS10<12>	IEC10<12>	IPC43<2:0>
PEVTE – PWM Event E	181	173	0x00016E	IFS10<13>	IEC10<13>	IPC43<6:4>
PEVTF – PWM Event F	182	174	0x000170	IFS10<14>	IEC10<14>	IPC43<10:8>
CLC3P – CLC3 Positive Edge	183	175	0x000172	IFS10<15>	IEC10<15>	IPC43<14:12>
CLC4P – CLC4 Positive Edge	184	176	0x000174	IFS11<0>	IEC11<0>	IPC44<2:0>
CLC1N – CLC1 Negative Edge	185	177	0x000176	IFS11<1>	IEC11<1>	IPC44<6:4>
CLC2N – CLC2 Negative Edge	186	178	0x000178	IFS11<2>	IEC11<2>	IPC44<10:8>
CLC3N – CLC3 Negative Edge	187	179	0x00017A	IFS11<3>	IEC11<3>	IPC44<14:>
CLC4N – CLC4 Negative Edge	188	180	0x00017C	IFS11<4>	IEC11<4>	IPC45<2:0>
Reserved	189-196	181-188	0x0017E- 0x0018C	—	—	—
U1EVT – UART1 Event	197	189	0x00018E	IFS11<13>	IF2C11<13>	IPC47<6:4>

REGISTER 6-10: REFOCONL: REFERENCE CLOCK CONTROL LOW REGISTER (MASTER)

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	HC/R/W-0	HSC/R-0
ROEN	—	ROSIDL	ROOUT	ROSLP	—	ROSWEN	ROACTIV
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	ROSEL3	ROSEL2	ROSEL1	ROSEL0
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ROEN:** Reference Clock Enable bit
1 = Reference Oscillator is enabled on the REFCLKO pin
0 = Reference Oscillator is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **ROSIDL:** Reference Clock Stop in Idle bit
1 = Reference Oscillator continues to run in Idle mode
0 = Reference Oscillator is disabled in Idle mode

bit 12 **ROOUT:** Reference Clock Output Enable bit
1 = Reference clock external output is enabled and available on the REFCLKO pin
0 = Reference clock external output is disabled

bit 11 **ROSLP:** Reference Clock Stop in Sleep bit
1 = Reference Oscillator continues to run in Sleep modes
0 = Reference Oscillator is disabled in Sleep modes

bit 10 **Unimplemented:** Read as '0'

bit 9 **ROSWEN:** Reference Clock Output Enable bit
1 = Clock divider change (requested by changes to RODIVx) is requested or is in progress (set in software, cleared by hardware upon completion)
0 = Clock divider change has completed or is not pending

bit 8 **ROACTIV:** Reference Clock Status bit
1 = Reference clock is active; do not change clock source
0 = Reference clock is stopped; clock source and configuration may be safely changed

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **ROSEL<3:0>:** Reference Clock Source Select bits
1111 = Reserved
... = Reserved
1000 = Reserved
0111 = REFI pin
0110 = FVCO/4
0101 = BFRC
0100 = LPRC
0011 = FRC
0010 = Primary Oscillator
0001 = Peripheral clock (FP)
0000 = System clock (FOSC)

Table 12-2 shows the truth table that describes how the Quadrature signals are decoded.

TABLE 12-2: TRUTH TABLE FOR QUADRATURE ENCODER

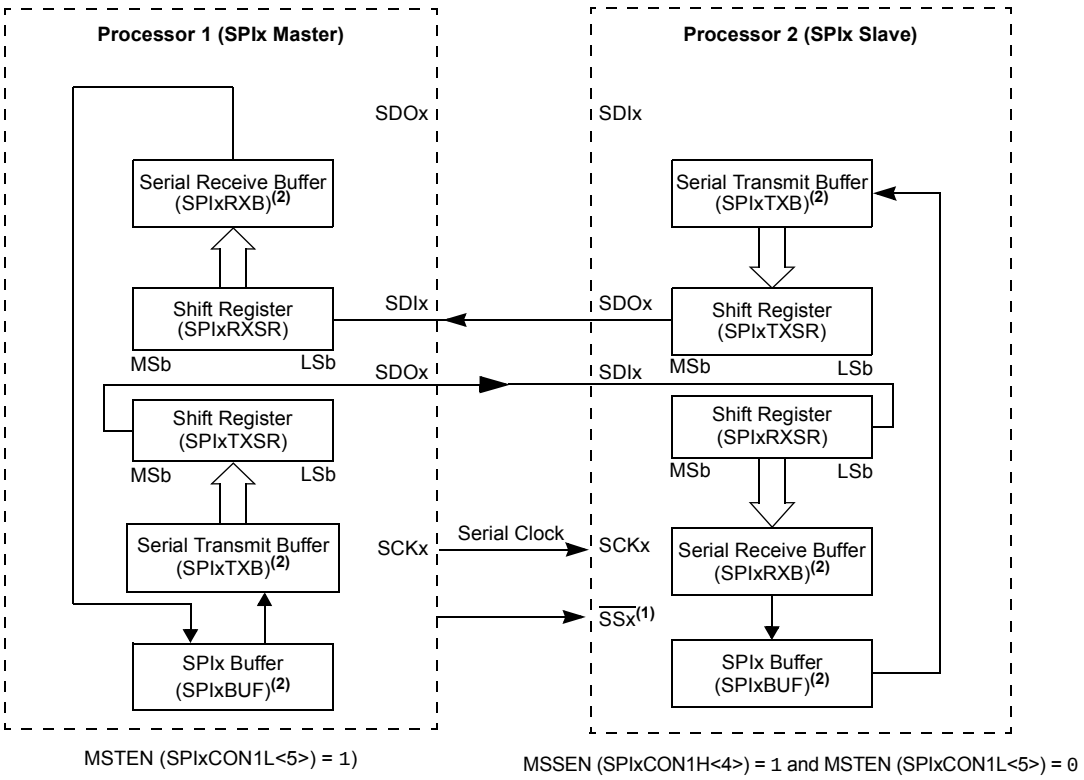
Current Quadrature State		Previous Quadrature State		Action
QA	QB	QA	QB	
1	1	1	1	No count or direction change
1	1	1	0	Count up
1	1	0	1	Count down
1	1	0	0	Invalid state change; ignore
1	0	1	1	Count down
1	0	1	0	No count or direction change
1	0	0	1	Invalid state change; ignore
1	0	0	0	Count up
0	1	1	1	Count up
0	1	1	0	Invalid state change; ignore
0	1	0	1	No count or direction change
0	1	0	0	Count down
0	0	1	1	Invalid state change; ignore
0	0	1	0	Count down
0	0	0	1	Count up
0	0	0	0	No count or direction change

Figure 12-2 illustrates the simplified block diagram of the QEI module. The QEI module consists of decoder logic to interpret the Phase A (QEAx) and Phase B (QEBx) signals, and an up/down counter to accumulate the count. The counter pulses are generated when the Quadrature state changes. The count direction information must be maintained in a register until a direction change is detected. The module also includes digital noise filters, which condition the input signal.

The QEI module consists of the following major features:

- Four Input Pins: Two Phase Signals, an Index Pulse and a Home Pulse
- Programmable Digital Noise Filters on Inputs
- Quadrature Decoder providing Counter Pulses and Count Direction
- Count Direction Status
- 4x Count Resolution
- Index (INDXx) Pulse to Reset the Position Counter
- General Purpose 32-Bit Timer/Counter mode
- Interrupts generated by QEI or Counter Events
- 32-Bit Velocity Counter
- 32-Bit Position Counter
- 32-Bit Index Pulse Counter
- 32-Bit Interval Timer
- 32-Bit Position Initialization/Capture Register
- 32-Bit Compare Less Than and Greater Than Registers
- External Up/Down Count mode
- External Gated Count mode
- External Gated Timer mode
- Interval Timer mode

FIGURE 14-3: SPIx MASTER/SLAVE CONNECTION (STANDARD MODE)



Note 1: Using the $\overline{SSx}$ pin in Slave mode of operation is optional.

2: User must write transmit data to read the received data from SPIxBUF. The SPIxTXB and SPIxRXB registers are memory-mapped to SPIxBUF.

REGISTER 21-18: FMBXHS2 CONFIGURATION REGISTER

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
MBXHSH3	MBXHSH2	MBXHSH1	MBXHSH0	MBXHSG3	MBXHSG2	MBXHSG1	MBXHSG0
bit 15							bit 8

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
MBXHSF3	MBXHSF2	MBXHSF1	MBXHSF0	MBXHSE3	MBXHSE2	MBXHSE1	MBXHSE0
bit 7							bit 0

Legend:	PO = Program Once bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-16 **Unimplemented:** Read as ‘1’

bit 15-12 **MBXHSH<3:0>:** Mailbox Handshake Protocol Block H Register Assignment bits
1111 = MSIxMBXD15 is assigned to Mailbox Handshake Protocol Block H
...
0001 = MSIxMBXD1 is assigned to Mailbox Handshake Protocol Block H
0000 = MSIxMBXD0 is assigned to Mailbox Handshake Protocol Block H

bit 11-8 **MBXHSG<3:0>:** Mailbox Handshake Protocol Block G Register Assignment bits
1111 = MSIxMBXD15 is assigned to Mailbox Handshake Protocol Block G
...
0001 = MSIxMBXD1 is assigned to Mailbox Handshake Protocol Block G
0000 = MSIxMBXD0 is assigned to Mailbox Handshake Protocol Block G

bit 7-4 **MBXHSF<3:0>:** Mailbox Handshake Protocol Block F Register Assignment bits
1111 = MSIxMBXD15 is assigned to Mailbox Handshake Protocol Block F
...
0001 = MSIxMBXD1 is assigned to Mailbox Handshake Protocol Block F
0000 = MSIxMBXD0 is assigned to Mailbox Handshake Protocol Block F

bit 3-0 **MBXHSE<3:0>:** Mailbox Handshake Protocol Block E Register Assignment bits
1111 = MSIxMBXD15 is assigned to Mailbox Handshake Protocol Block E
...
0001 = MSIxMBXD1 is assigned to Mailbox Handshake Protocol Block E
0000 = MSIxMBXD0 is assigned to Mailbox Handshake Protocol Block E

TABLE 24-13: DC CHARACTERISTICS: PWM DELTA CURRENT(1,2,3)

DC CHARACTERISTICS	Master and Slave		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended		
Parameter No.	**Typ.**	**Max.**	**Units**	**Conditions**	
DC100	6	8	mA	-40°C, 3.3V	PWM Output 500 MHz, PWM Input (AFPLLO = 500 MHz), AVCO = 1000 MHz, PLLFBD = 125, APLLDIV = 2
	6	6.7	mA	+25°C, 3.3V	
	6.3	8	mA	+125°C, 3.3V	
DC101	4.9	6	mA	-40°C, 3.3V	PWM Output 500 MHz, PWM Input (AFPLLO = 400 MHz), AVCO = 400 MHz, PLLFBD = 50, APLLDIV = 1
	4.9	5.5	mA	+25°C, 3.3V	
	4.9	5.6	mA	+125°C, 3.3V	
DC102	2.6	3.4	mA	-40°C, 3.3V	PWM Output 500 MHz, PWM Input (AFPLLO = 200 MHz), AVCO = 400 MHz, PLLFBD = 50, APLLDIV = 2
	2.7	3	mA	+25°C, 3.3V	
	2.7	3.2	mA	+125°C, 3.3V	
DC103	1.5	2.9	mA	-40°C, 3.3V	PWM Output 500 MHz, PWM Input (AFPLLO = 100 MHz), AVCO = 400 MHz, PLLFBD = 50, APLLDIV = 4
	1.5	2.1	mA	+25°C, 3.3V	
	1.5	2.2	mA	+125°C, 3.3V	

Note 1: The APLL current is not included. The APLL current will be the same if more than one PWM or all eight PWMs are running.

2: Delta current is for the one instance of PWM running.

3: PWM configured for Low-Resolution mode. All parameters are characterized but not tested during manufacturing.

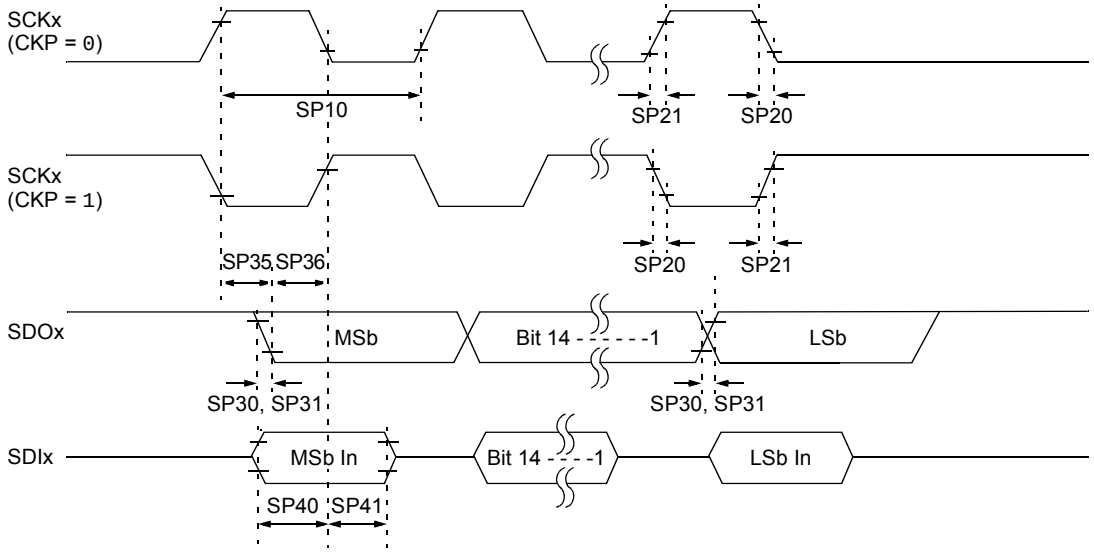
TABLE 24-14: DC CHARACTERISTICS: APLL DELTA CURRENT

DC CHARACTERISTICS	Master or Slave(2)		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended		
Parameter No.	**Typ.**	**Max.**	**Units**	**Conditions(1)**	
DC110	—	9.4	mA	-40°C.,3.3V	AFPLLO @ 500 MHz, AVCO = 1000 MHz, PLLFBD = 125, APLLDIV = 2
	7.2	9.4	mA	+25°C,3.3V	
	—	18	mA	+125°C,3.3V	
DC111	—	5.7	mA	-40°C.,3.3V	AFPLLO @ 400 MHz, AVCO = 400 MHz, PLLFBD = 50, APLLDIV = 1
	5	5.8	mA	+25°C,3.3V	
	—	14	mA	+125°C,3.3V	
DC112	—	4.7	mA	-40°C.,3.3V	AFPLLO @ 200 MHz, AVCO = 400 MHz, PLLFBD = 50, APLLDIV = 2
	2.9	4.7	mA	+25°C,3.3V	
	—	14	mA	+125°C,3.3V	
DC113	—	4	mA	-40°C.,3.3V	AFPLLO @ 100 MHz, AVCO = 400 MHz, PLLFBD = 50, APLLDIV = 4
	2.3	4	mA	+25°C,3.3V	
	—	12	mA	+125°C,3.3V	

Note 1: The APLL current will be the same if more than one PWM or DAC is run to the APLL clock. All parameters are characterized but not tested during manufacturing.

2: Current is for the APLL for the Master or Slave, not the combined current.

FIGURE 24-10: SPIx MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 24-1 for load conditions.

TABLE 24-37: SPIx MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP10	FscP	Maximum SCKx Frequency	—	—	15	MHz	Using PPS pins
			—	—	40	MHz	SPI2 dedicated pins
SP20	TscF	SCKx Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 3)**
SP21	TscR	SCKx Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 3)**
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 3)**
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 3)**
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid After SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	Using PPS pins
			20	—	—	ns	SPI2 dedicated pins
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	Using PPS pins
			10	—	—	ns	SPI2 dedicated pins
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	Using PPS pins
			15	—	—	ns	SPI2 dedicated pins

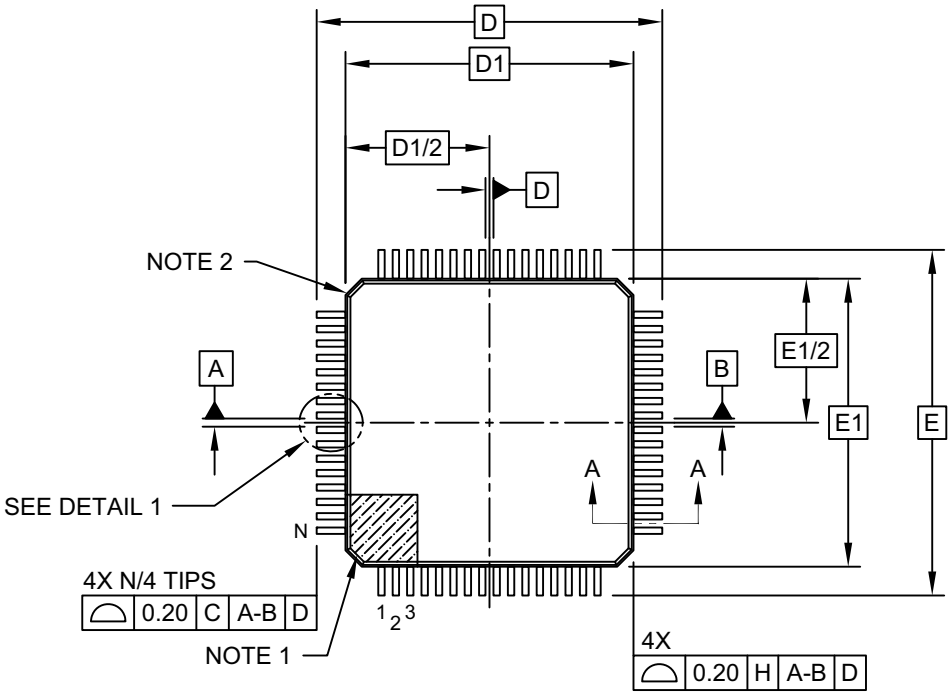
Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column is at 3.3V, +25°C unless otherwise stated.

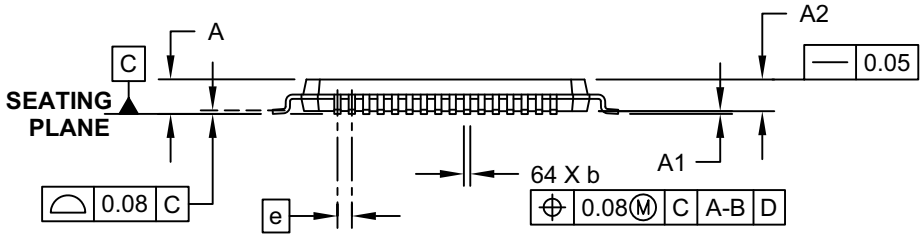
3: Assumes 50 pF load on all SPIx pins.

64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW

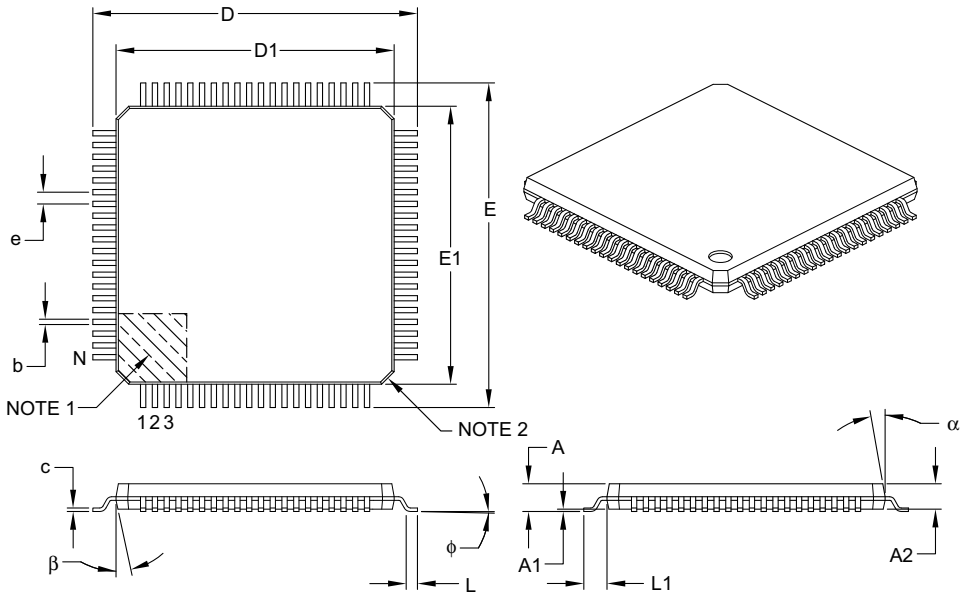


SIDE VIEW

Microchip Technology Drawing C04-085C Sheet 1 of 2

80-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		80	
Lead Pitch	e		0.50 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		14.00 BSC	
Overall Length	D		14.00 BSC	
Molded Package Width	E1		12.00 BSC	
Molded Package Length	D1		12.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-092B

NOTES: