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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit Dual-Core
Speed	180MHz, 200MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	39
Program Memory Size	88KB (88K x 8)
Program Memory Type	FLASH, PRAM
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 31x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ch64mp205-i-pt

3.2.6 INSTRUCTION ADDRESSING MODES

The addressing modes shown in Table 3-20 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the `MAC` class of instructions differ from those in the other instruction types.

3.2.6.1 File Register Instructions

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a Working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the `MUL` instruction), which writes the result to a register or register pair. The `MOV` instruction allows additional flexibility and can access the entire Data Space.

3.2.6.2 MCU Instructions

The three-operand MCU instructions are of the form:

`Operand 3 = Operand 1 <function> Operand 2`

where `Operand 1` is always a Working register (that is, the addressing mode can only be Register Direct), which is referred to as Wb. `Operand 2` can be a W register fetched from data memory or a 5-bit literal. The result location can either be a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-Bit or 10-Bit Literal

> **Note:** Not all instructions support all the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

TABLE 3-20: FUNDAMENTAL ADDRESSING MODES SUPPORTED

Addressing Mode	Description
File Register Direct	The address of the file register is specified explicitly.
Register Direct	The contents of a register are accessed directly.
Register Indirect	The contents of Wn form the Effective Address (EA).
Register Indirect Post-Modified	The contents of Wn form the EA. Wn is post-modified (incremented or decremented) by a constant value.
Register Indirect Pre-Modified	Wn is pre-modified (incremented or decremented) by a signed constant value to form the EA.
Register Indirect with Register Offset (Register Indexed)	The sum of Wn and Wb forms the EA.
Register Indirect with Literal Offset	The sum of Wn and a literal forms the EA.

REGISTER 3-4: NVMCON: NONVOLATILE MEMORY (NVM) CONTROL REGISTER (CONTINUED)

bit 3-0	**NVMOP<3:0>:** NVM Operation Select bits(1,3,4) `1111` = Reserved `1110` = User memory bulk erase operation `1101` = Reserved `1100` = Reserved `1011` = Reserved `1010` = Reserved `1001` = Reserved `1000` = Reserved `0111` = Reserved `0101` = Reserved `0100` = Reserved `0011` = Memory page erase operation `0010` = Memory row program operation `0001` = Memory double-word operation(5) `0000` = Reserved

Note 1: These bits can only be reset on a POR.

2: If this bit is set, there will be minimal power savings (IIDLE), and upon exiting Idle mode, there is a delay (TVREG) before Flash memory becomes operational.

3: All other combinations of NVMOP<3:0> are unimplemented.

4: Execution of the PWRSAV instruction is ignored while any of the NVM operations are in progress.

5: Two adjacent words on a 4-word boundary are programmed during execution of this operation.

REGISTER 3-133: C1FIFOCONHx: CAN FIFO CONTROL REGISTER x (x = 1 TO 7) HIGH

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PLSIZE2(1)	PLSIZE1(1)	PLSIZE0(1)	FSIZE4(1)	FSIZE3(1)	FSIZE2(1)	FSIZE1(1)	FSIZE0(1)
bit 15							bit 8

U-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TXAT1	TXAT0	TXPRI4	TXPRI3	TXPRI2	TXPRI1	TXPRI0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-13 **PLSIZE<2:0>:** Payload Size bits(1)
111 = 64 data bytes
110 = 48 data bytes
101 = 32 data bytes
100 = 24 data bytes
011 = 20 data bytes
010 = 16 data bytes
001 = 12 data bytes
000 = 8 data bytes

bit 12-8 **FSIZE<4:0>:** FIFO Size bits(1)
11111 = FIFO is 32 messages deep
...
00010 = FIFO is 3 messages deep
00001 = FIFO is 2 messages deep
00000 = FIFO is 1 message deep

bit 7 **Unimplemented:** Read as ‘0’

bit 6-5 **TXAT<1:0>:** Retransmission Attempts bits
This feature is enabled when RTXAT (C1CONH<0>) is set.
11 = Unlimited number of retransmission attempts
10 = Unlimited number of retransmission attempts
01 = Three retransmission attempts
00 = Disables retransmission attempts

bit 4-0 **TXPRI<4:0>:** Message Transmit Priority bits
11111 = Highest message priority
...
00000 = Lowest message priority

Note 1: These bits can only be modified in Configuration mode (OPMOD<2:0> = 100).

REGISTER 3-136: C1TEFCONH: CAN TRANSMIT EVENT FIFO CONTROL REGISTER HIGH

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	FSIZE<4:0>[1]				
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12-8 **FSIZE<4:0>:** FIFO Size bits[1]
`11111` = FIFO is 32 messages deep
`...`
`00010` = FIFO is 3 messages deep
`00001` = FIFO is 2 messages deep
`00000` = FIFO is 1 message deep

bit 7-0 **Unimplemented:** Read as ‘0’

Note 1: These bits can only be modified in Configuration mode (OPMOD<2:0> = `100`).

REGISTER 3-147: C1BDIAG0H: CAN BUS DIAGNOSTICS REGISTER 0 HIGH

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTERRCNT<7:0>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DRERRCNT<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **DTERRCNT<7:0>:** Data Bit Rate Transmit Error Counter bits

bit 7-0 **DRERRCNT<7:0>:** Data Bit Rate Receive Error Counter bits

REGISTER 3-148: C1BDIAG0L: CAN BUS DIAGNOSTICS REGISTER 0 LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NTERRCNT<7:0>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NRERRCNT<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **NTERRCNT<7:0>:** Nominal Bit Rate Transmit Error Counter bits

bit 7-0 **NRERRCNT<7:0>:** Nominal Bit Rate Receive Error Counter bits

3.9 High-Speed, 12-Bit Analog-to-Digital Converter (Master ADC)

Note 1: This data sheet summarizes the features of the dsPIC33CH128MP508 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"12-Bit High-Speed, Multiple SARs A/D Converter (ADC)"** (DS70005213) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: This section describes the Master ADC module, which implements one shared core, and no dedicated cores.

dsPIC33CH128MP508 devices have a high-speed, 12-bit Analog-to-Digital Converter (ADC) that features a low conversion latency, high resolution and over-sampling capabilities to improve performance in AC/DC and DC/DC power converters. The Master implements one SAR core ADC.

3.9.1 MASTER ADC FEATURES OVERVIEW

The high-speed, 12-bit multiple SARs Analog-to-Digital Converter (ADC) includes the following features:

- One Shared (common) Core
- User-Configurable Resolution of up to 12 Bits
- Up to 3.5 Msps Conversion Rate per Channel at 12-Bit Resolution
- Low Latency Conversion
- Up to 20 Analog Input Channels, with a Separate 16-Bit Conversion Result Register for each Input Channel
- Conversion Result can be Formatted as Unsigned or Signed Data, on a per Channel Basis, for All Channels
- Channel Scan Capability
- Multiple Conversion Trigger Options, including:
  - PWM triggers from Master and Slave CPU cores
  - SCCP modules triggers
  - CLC modules triggers
  - External pin trigger event (ADTRG31)
  - Software trigger
- Four Integrated Digital Comparators with Dedicated Interrupts:
  - Multiple comparison options
  - Assignable to specific analog inputs
- Four Oversampling Filters with Dedicated Interrupts:
  - Provide increased resolution
  - Assignable to a specific analog input

Simplified block diagrams of the 12-bit ADC are shown in Figure 3-24 and Figure 3-25.

The analog inputs (channels) are connected through multiplexers and switches to the Sample-and-Hold (S&H) circuit of the ADC core. The core uses the channel information (the output format, the Measurement mode and the input number) to process the analog sample. When conversion is complete, the result is stored in the result buffer for the specific analog input, and passed to the digital filter and digital comparator if they were configured to use data from this particular channel.

The ADC provides each analog input the ability to specify its own trigger source. This capability allows the ADC to sample and convert analog inputs that are associated with PWM generators operating on independent time bases.

FIGURE 4-10: BIT-REVERSED ADDRESSING EXAMPLE

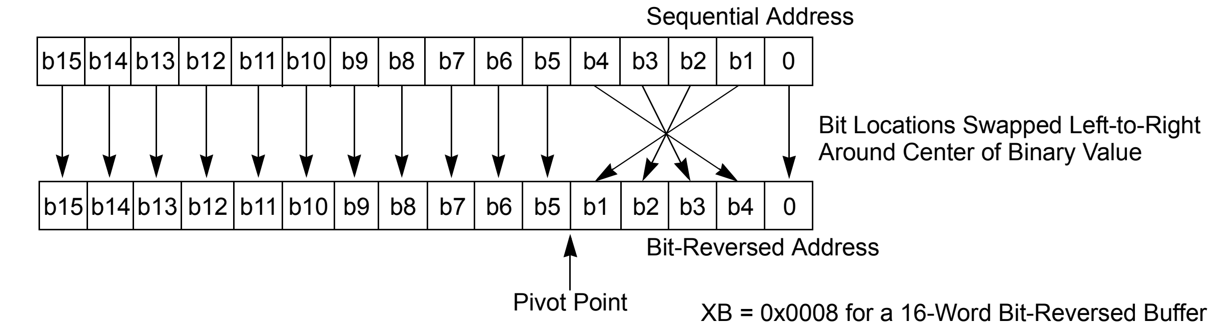


TABLE 4-18: BIT-REVERSED ADDRESSING SEQUENCE (16-ENTRY)

Normal Address					Bit-Reversed Address				
A3	A2	A1	A0	Decimal	A3	A2	A1	A0	Decimal
0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	0	0	0	8
0	0	1	0	2	0	1	0	0	4
0	0	1	1	3	1	1	0	0	12
0	1	0	0	4	0	0	1	0	2
0	1	0	1	5	1	0	1	0	10
0	1	1	0	6	0	1	1	0	6
0	1	1	1	7	1	1	1	0	14
1	0	0	0	8	0	0	0	1	1
1	0	0	1	9	1	0	0	1	9
1	0	1	0	10	0	1	0	1	5
1	0	1	1	11	1	1	0	1	13
1	1	0	0	12	0	0	1	1	3
1	1	0	1	13	1	0	1	1	11
1	1	1	0	14	0	1	1	1	7
1	1	1	1	15	1	1	1	1	15

TABLE 4-23: SLAVE INTERRUPT PRIORITY REGISTERS

Register	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IPC0	—	CNBIP2	CNBIP1	CNBIP0	—	CNAIP2	CNAIP1	CNAIP0	—	T1IP2	T1IP1	T1IP0	—	INT0IP2	INT0IP1	INT0IP0
IPC1	—	CCT1IP2	CCT1IP1	CCT1IP0	—	CCP1IP2	CCP1IP1	CCP1IP0	—	—	—	—	—	DMA0IP2	DMA0IP1	DMA0IP0
IPC2	—	U1RXIP2	U1RXIP1	U1RXIP0	—	SPI1TXIP2	SPI1TXIP1	SPI1TXIP0	—	SPI1RXIP2	SPI1RXIP1	SPI1RXIP0	—	DMA1IP2	DMA1IP1	DMA1IP0
IPC3	—	INT1IP2	INT1IP1	INT1IP0	—	NVMIP2	NVMIP1	NVMIP0	—	ECCSBEIP2	ECCSBEIP1	ECCSBEIP0	—	U1TXIP2	U1TXIP1	U1TXIP0
IPC4	—	CNCIP2	CNCIP1	CNCIP0	—	—	—	—	—	MI2C1IP2	MI2C1IP1	MI2C1IP0	—	SI2C1IP2	SI2C1IP1	SI2C1IP0
IPC5	—	CCP2IP2	CCP2IP1	CCP2IP0	—	—	—	—	—	—	—	—	—	INT2IP2	INT2IP1	INT2IP0
IPC6	—	—	—	—	—	INT3IP2	INT3IP1	INT3IP0	—	—	—	—	—	CCT2IP2	CCT2IP1	CCT2IP0
IPC7	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
IPC8	—	CCP3IP2	CCP3IP1	CCP3IP0	—	—	—	—	—	—	—	—	—	—	—	—
IPC9	—	—	—	—	—	—	—	—	—	—	—	—	—	CCT3IP2	CCT3IP1	CCT3IP0
IPC10	—	—	—	—	—	—	—	—	—	CCT4IP2	CCT4IP1	CCT4IP0	—	CCP4IP2	CCP4IP1	CCP4IP0
IPC11	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
IPC12	—	—	—	—	—	—	—	—	—	U1EIP2	U1EIP1	U1EIP0	—	QEI1IP2	QEI1IP1	QEI1IP0
IPC13	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
IPC14	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
IPC15	—	—	—	—	—	JTAGIP2	JTAGIP1	JTAGIP0	—	ICDIP2	ICDIP1	ICDIP0	—	—	—	—
IPC16	—	PWM1IP2	PWM1IP1	PWM1IP0	—	—	—	—	—	—	—	—	—	I2C1BCIP2	I2C1BCIP1	I2C1BCIP0
IPC17	—	PWM5IP2	PWM5IP1	PWM5IP0	—	PWM4IP2	PWM4IP1	PWM4IP0	—	PWM3IP2	PWM3IP1	PWM3IP0	—	PWM2IP2	PWM2IP1	PWM2IP0
IPC18	—	CNDIP2	CNDIP1	CNDIP0	—	PWM8IP2	PWM8IP1	PWM8IP0	—	PWM7IP2	PWM7IP1	PWM7IP0	—	PWM6IP2	PWM6IP1	PWM6IP0
IPC19	—	CMP2IP2	CMP2IP1	CMP2IP0	—	CMP1IP2	CMP1IP1	CMP1IP0	—	—	—	—	—	CNEIP2	CNEIP1	CNEIP0
IPC20	—	PTG1IP2	PTG1IP1	PTG1IP0	—	PTG0IP2	PTG0IP1	PTG0IP0	—	—	—	—	—	CMP3IP2	CMP3IP1	CMP3IP0
IPC21	—	—	—	—	—	—	—	—	—	PTG3IP2	PTG3IP1	PTG3IP0	—	PTG12P2	PTG12P1	PTG12P0
IPC22	—	ADCAN0IP2	ADCAN0IP1	ADCAN0IP0	—	ADCIP2	ADCIP1	ADCIP	—	—	—	—	—	—	—	—
IPC23	—	ADCAN4IP2	ADCAN4IP1	ADCAN4IP0	—	ADCAN3IP2	ADCAN3IP1	ADCAN3IP0	—	ADCAN2IP2	ADCAN2IP1	ADCAN2IP0	—	ADCAN1IP2	ADCAN1IP1	ADCAN1IP0
IPC24	—	ADCAN8IP2	ADCAN8IP1	ADCAN8IP0	—	ADCAN7IP2	ADCAN7IP1	ADCAN7IP0	—	ADCAN6IP2	ADCAN6IP1	ADCAN6IP0	—	ADCAN5IP2	ADCAN5IP1	ADCAN5IP0
IPC25	—	ADCAN12IP2	ADCAN12IP1	ADCAN12IP0	—	ADCAN11IP2	ADCAN11IP1	ADCAN11IP0	—	ADCAN10IP2	ADCAN10IP1	ADCAN10IP0	—	ADCAN9IP2	ADCAN9IP1	ADCAN9IP0
IPC26	—	ADCAN16IP2	ADCAN16IP1	ADCAN16IP0	—	ADCAN15IP2	ADCAN15IP1	ADCAN15IP0	—	ADCAN14IP2	ADCAN14IP1	ADCAN14IP0	—	ADCAN13IP2	ADCAN13IP1	ADCAN13IP0
IPC27	—	ADCAN20IP2	ADCAN20IP1	ADCAN20IP0	—	ADCAN19IP2	ADCAN19IP1	ADCAN19IP0	—	ADCAN18IP2	ADCAN18IP1	ADCAN18IP0	—	ADCAN17IP2	ADCAN17IP1	ADCAN17IP0
IPC28	—	ADFLTIP2	ADFLTIP1	ADFLTIP0	—	—	—	—	—	—	—	—	—	ADCAN21IP2	ADCAN21IP1	ADCAN21IP0
IPC29	—	ADCMP3IP2	ADCMP3IP1	ADCMP3IP0	—	ADCMP2IP2	ADCMP2IP1	ADCMP2IP0	—	ADCMP1IP2	ADCMP1IP1	ADCMP1IP0	—	ADCMP0IP2	ADCMP0IP1	ADCMP0IP0
IPC30	—	ADFLTR3IP2	ADFLTR3IP1	ADFLTR3IP0	—	ADFLTR2IP2	ADFLTR2IP1	ADFLTR2IP0	—	ADFLTR1IP2	ADFLTR1IP1	ADFLTR1IP0	—	ADFLTR0IP2	ADFLTR0IP1	ADFLTR0IP0
IPC31	—	—	—	—	—	SPI1IP2	SPI1IP1	SPI1IP0	—	CLC2PEIP2	CLC2PEIP1	CLC2PEIP0	—	CLC1PEIP2	CLC1PEIP1	CLC1PEIP0
IPC32	—	MSIBIP2	MSIBIP1	MSIBIP0	—	MSIAIP2	MSIAIP1	MSIAIP0	—	MSMIP2	MSMIP1	MSMIP0	—	—	—	—
IPC33	—	MSIFIP2	MSIFIP1	MSIFIP0	—	MSIEIP2	MSIEIP1	MSIEIP0	—	MSIDIP2	MSIDIP1	MSIDIP0	—	MSICIP2	MSICIP1	MSICIP0
IPC34	—	MSIWFEIP2	MSIWFEIP1	MSIWFEIP0	—	MSIDTIP2	MSIDTIP1	MSIDTIP0	—	MSIHIP2	MSIHIP1	MSIHIP0	—	MSIGIP2	MSIGIP1	MSIGIP0
IPC35	—	—	—	—	—	—	—	—	—	MSIMRSTIP2	MSIMRSTIP1	MSIMRSTIP0	—	MSIFLTIP2	MSIFLTIP1	MSIFLTIP0

REGISTER 4-39: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ICM1R7	ICM1R6	ICM1R5	ICM1R4	ICM1R3	ICM1R2	ICM1R1	ICM1R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TCKI1R7	TCKI1R6	TCKI1R5	TCKI1R4	TCKI1R3	TCKI1R2	TCKI1R1	TCKI1R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **ICM1R<7:0>:** Assign SCCP Capture 1 (S1ICM1) to the Corresponding S1RPn Pin bits
See Table 4-27.

bit 7-0 **TCKI1R<7:0>:** Assign SCCP Timer1 (S1TCKI1) to the Corresponding S1RPn Pin bits
See Table 4-27.

REGISTER 4-40: RPINR4: PERIPHERAL PIN SELECT INPUT REGISTER 4

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ICM2R7	ICM2R6	ICM2R5	ICM2R4	ICM2R3	ICM2R2	ICM2R1	ICM2R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TCKI2R7	TCKI2R6	TCKI2R5	TCKI2R4	TCKI2R3	TCKI2R2	TCKI2R1	TCKI2R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **ICM2R<7:0>:** Assign SCCP Capture 2 (S1ICM2) to the Corresponding S1RPn Pin bits
See Table 4-27.

bit 7-0 **TCKI2R<7:0>:** Assign SCCP Timer2 (S1TCKI2) to the Corresponding S1RPn Pin bits
See Table 4-27.

REGISTER 4-106: ADTRIGnL/ADTRIGnH: ADC CHANNEL TRIGGER n(x) SELECTION REGISTERS LOW AND HIGH (x = 0 TO 19; n = 0 TO 4) (CONTINUED)

bit 4-0 **TRGSRCx<4:0>:** Common Interrupt Enable for Corresponding Analog Inputs bits (TRGSRC0 to TRGSRC20 – Even)

`11111` = ADTRG31 (PPS input)
`11110` = Master PTG
`11101` = Slave CLC1
`11100` = Master CLC1
`11011` = Reserved
`11010` = Reserved
`11001` = Master PWM3 Trigger 2
`11000` = Master PWM1 Trigger 2
`10111` = Slave SCCP4 PWM/IC interrupt
`10110` = Slave SCCP3 PWM/IC interrupt
`10101` = Slave SCCP2 PWM/IC interrupt
`10100` = Slave SCCP1 PWM/IC interrupt
`10011` = Reserved
`10010` = Reserved
`10001` = Reserved
`10000` = Reserved
`01111` = Slave PWM8 Trigger 1
`01110` = Slave PWM7 Trigger 1
`01101` = Slave PWM6 Trigger 1
`01100` = Slave PWM5 Trigger 1
`01011` = Slave PWM4 Trigger 2
`01010` = Slave PWM4 Trigger 1
`01001` = Slave PWM3 Trigger 2
`01000` = Slave PWM3 Trigger 1
`00111` = Slave PWM2 Trigger 2
`00110` = Slave PWM2 Trigger 1
`00101` = Slave PWM1 Trigger 2
`00100` = Slave PWM1 Trigger 1
`00011` = Reserved
`00010` = Level software trigger
`00001` = Common software trigger
`00000` = No trigger is enabled

REGISTER 6-13: CLKDIV: CLOCK DIVIDER REGISTER (SLAVE) (CONTINUED)

bit 3-0 **PLLPRE<3:0>:** PLL Phase Detector Input Divider Select bits (also denoted as ‘N1’, PLL prescaler)[(4)]

11111 = Reserved
...
1001 = Reserved
1000 = Input divided by 8
0111 = Input divided by 7
0110 = Input divided by 6
0101 = Input divided by 5
0100 = Input divided by 4
0011 = Input divided by 3
0010 = Input divided by 2
0001 = Input divided by 1 (power-on default selection)
0000 = Reserved

Note 1: The DOZE<2:0> bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored.

2: This bit is cleared when the ROI bit is set and an interrupt occurs.

3: The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.

4: PLLPRE<3:0> may be updated while the PLL is operating, but the VCO may overshoot.

REGISTER 7-5: PMD4: MASTER PERIPHERAL MODULE DISABLE 4 CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
—	—	—	—	REFOMD	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as ‘0’

bit 3 **REFOMD:** Reference Clock Module Disable bit
1 = Reference clock module is disabled
0 = Reference clock module is enabled

bit 2-0 **Unimplemented:** Read as ‘0’

REGISTER 7-6: PMD6: MASTER PERIPHERAL MODULE DISABLE 6 CONTROL REGISTER HIGH

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DMA5MD	DMA4MD	DMA3MD	DMA2MD	DMA1MD	DMA0MD
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13 **DMA5MD:** DMA5 Module Disable bit
1 = DMA5 module is disabled
0 = DMA5 module is enabled

bit 12 **DMA4MD:** DMA4 Module Disable bit
1 = DMA4 module is disabled
0 = DMA4 module is enabled

bit 11 **DMA3MD:** DMA3 Module Disable bit
1 = DMA3 module is disabled
0 = DMA3 module is enabled

bit 10 **DMA2MD:** DMA2 Module Disable bit
1 = DMA2 module is disabled
0 = DMA2 module is enabled

bit 9 **DMA1MD:** DMA1 Module Disable bit
1 = DMA1 module is disabled
0 = DMA1 module is enabled

bit 8 **DMA0MD:** DMA0 Module Disable bit
1 = DMA0 module is disabled
0 = DMA0 module is enabled

bit 7-0 **Unimplemented:** Read as ‘0’

REGISTER 9-4: MPHASE: MASTER PHASE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MPHASE<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MPHASE<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **MPHASE<15:0>:** Master Phase Register bits

REGISTER 9-5: MDC: MASTER DUTY CYCLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MDC<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MDC<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **MDC<15:0>:** Master Duty Cycle Register bits

REGISTER 9-20: PGxEVTH: PWM GENERATOR x EVENT REGISTER HIGH

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
FLTIEN(1)	CLIEN(2)	FFIEN(3)	SIEN(4)	—	—	IEVTSEL1	IEVTSEL0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADTR2EN3	ADTR2EN2	ADTR2EN1	ADTR1OFS4	ADTR1OFS3	ADTR1OFS2	ADTR1OFS1	ADTR1OFS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **FLTIEN:** PCI Fault Interrupt Enable bit(1)
1 = Fault interrupt is enabled
0 = Fault interrupt is disabled

bit 14 **CLIEN:** PCI Current-Limit Interrupt Enable bit(2)
1 = Current-limit interrupt is enabled
0 = Current-limit interrupt is disabled

bit 13 **FFIEN:** PCI Feed-Forward Interrupt Enable bit(3)
1 = Feed-forward interrupt is enabled
0 = Feed-forward interrupt is disabled

bit 12 **SIEN:** PCI Sync Interrupt Enable bit(4)
1 = Sync interrupt is enabled
0 = Sync interrupt is disabled

bit 11-10 **Unimplemented:** Read as ‘0’

bit 9-8 **IEVTSEL<1:0>:** Interrupt Event Selection bits
11 = Time base interrupts are disabled (Sync, Fault, current-limit and feed-forward events can be independently enabled)
10 = Interrupts CPU at ADC Trigger 1 event
01 = Interrupts CPU at TRIGA compare event
00 = Interrupts CPU at EOC

bit 7 **ADTR2EN3:** ADC Trigger 2 Source is PGxTRIGC Compare Event Enable bit
1 = PGxTRIGC register compare event is enabled as trigger source for ADC Trigger 2
0 = PGxTRIGC register compare event is disabled as trigger source for ADC Trigger 2

bit 6 **ADTR2EN2:** ADC Trigger 2 Source is PGxTRIGB Compare Event Enable bit
1 = PGxTRIGB register compare event is enabled as trigger source for ADC Trigger 2
0 = PGxTRIGB register compare event is disabled as trigger source for ADC Trigger 2

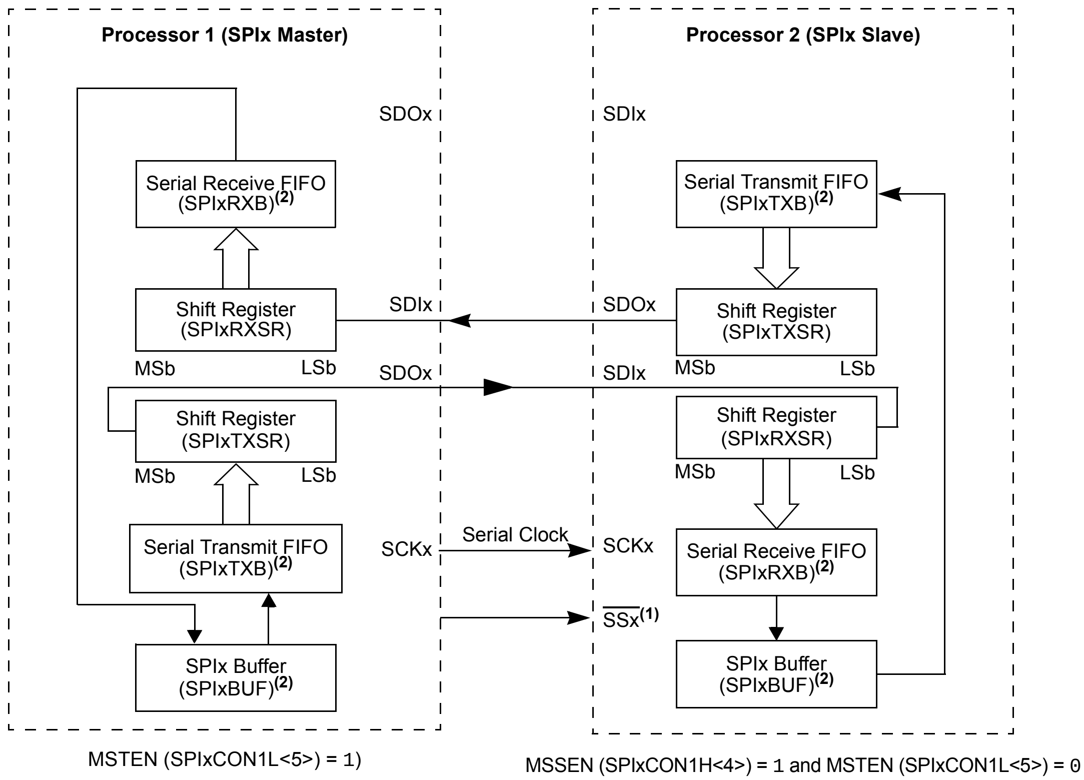
bit 5 **ADTR2EN1:** ADC Trigger 2 Source is PGxTRIGA Compare Event Enable bit
1 = PGxTRIGA register compare event is enabled as trigger source for ADC Trigger 2
0 = PGxTRIGA register compare event is disabled as trigger source for ADC Trigger 2

Note 1: An interrupt is only generated on the rising edge of the PCI Fault active signal.
2: An interrupt is only generated on the rising edge of the PCI current-limit active signal.
3: An interrupt is only generated on the rising edge of the PCI feed-forward active signal.
4: An interrupt is only generated on the rising edge of the PCI Sync active signal.

TABLE 10-6: SYNCHRONIZATION SOURCES (MASTER)

SYNC<4:0>	Synchronization Source
00000	None; Timer with Rollover on CCPxPR Match or FFFFh
00001	Module's Own Timer Sync Out
00010	Sync Output SCCP1
00011	Sync Output SCCP2
00100	Sync Output SCCP3
00101	Sync Output SCCP4
00110	Sync Output SCCP5
00111	Sync Output SCCP6
01000	Sync Output SCCP7
01001	INT0
01010	INT1
01011	INT2
01100-01111	Reserved
10000	Master CLC1 Output
10001	Master CLC2 Output
10010	Slave CLC1 Output
10011	Slave CLC2 Output
10100-10110	Reserved
10111	Comparator 1 Output
11000	Slave Comparator 1 Output
11001	Slave Comparator 2 Output
11010	Slave Comparator 3 Output
11011-11110	Reserved
11111	None; Timer with Auto-Rollover (FFFFh → 0000h)

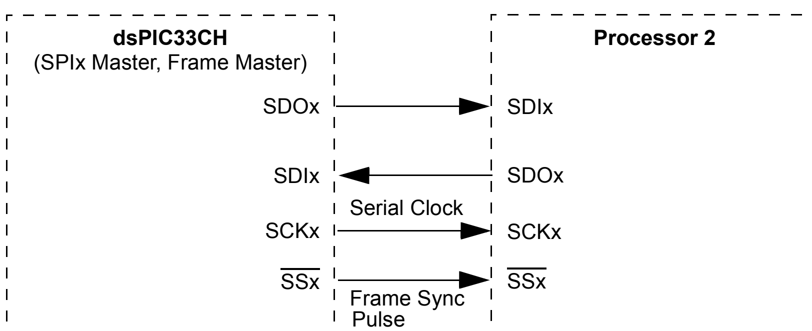
FIGURE 14-4: SPIx MASTER/SLAVE CONNECTION (ENHANCED BUFFER MODES)



Note 1: Using the $\overline{\text{SSx}}$ pin in Slave mode of operation is optional.

2: User must write transmit data to read the received data from SPIxBUF. The SPIxTXB and SPIxRXB registers are memory-mapped to SPIxBUF.

FIGURE 14-5: SPIx MASTER, FRAME MASTER CONNECTION DIAGRAM



REGISTER 21-8: FICD CONFIGURATION REGISTER

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 15							bit 8

r-1	U-1	R/PO-1	U-1	U-1	U-1	R/PO-1	R/PO-1
—	—	JTAGEN	—	—	—	ICS1	ICS0
bit 7							bit 0

Legend:	PO = Program Once bit	r = Reserved bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-8 **Unimplemented:** Read as ‘1’

bit 7 **Reserved:** Maintain as ‘1’

bit 6 **Unimplemented:** Read as ‘1’

bit 5 **JTAGEN:** JTAG Enable bit
1 = JTAG port is enabled
0 = JTAG port is disabled

bit 4-2 **Unimplemented:** Read as ‘1’

bit 1-0 **ICS<1:0>:** ICD Communication Channel Select bits
11 = Master communicates on PGC1 and PGD1
10 = Master communicates on PGC2 and PGD2
01 = Master communicates on PGC3 and PGD3
00 = Reserved, do not use

TABLE 24-5: DC CHARACTERISTICS: OPERATING CURRENT (I_{DD}) (MASTER RUN/SLAVE RUN)

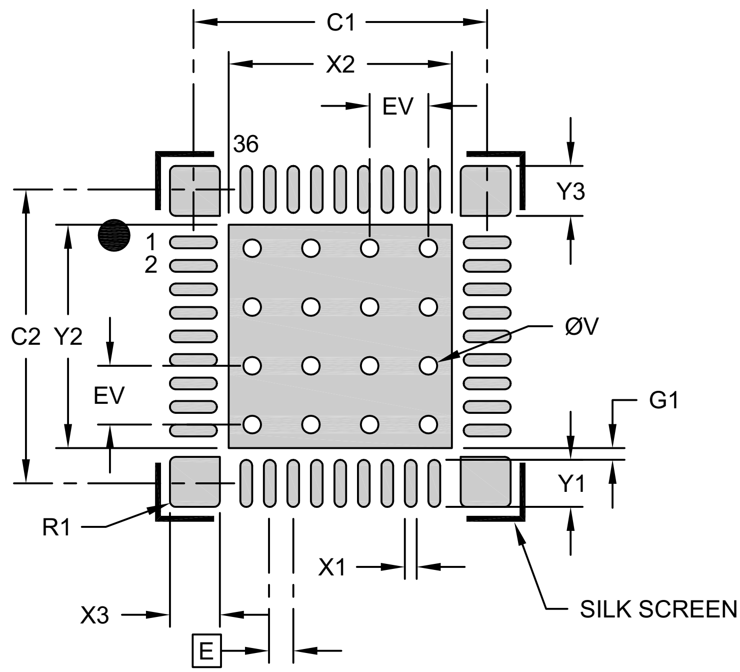
DC CHARACTERISTICS	Master (Run) + Slave (Run)		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended			
Parameter No.	**Typ.**	**Max.**	**Units**	**Conditions**		
Operating Current (I_{DD})(1)						
DC20	11.6	13.7	mA	-40°C	3.3V	10 MIPS (N = 1, N2 = 5, N3 = 2, M = 50, F_{VCO} = 400 MHz, F_{PLLO} = 40 MHz)
	11.7	17.5	mA	+25°C		
	11.9	23.5	mA	+85°C		
	15.8	30.0	mA	+125°C		
DC21	15.9	18.3	mA	-40°C	3.3V	20 MIPS (N = 1, N2 = 5, N3 = 1, M = 60, F_{VCO} = 480 MHz, F_{PLLO} = 280 MHz)
	16.0	22.2	mA	+25°C		
	16.1	28.0	mA	+85°C		
	20.0	34.3	mA	+125°C		
DC22	23.7	26.9	mA	-40°C	3.3V	40 MIPS (N = 1, N2 = 3, N3 = 1, M = 60, F_{VCO} = 480 MHz, F_{PLLO} = 160 MHz)
	23.9	30.9	mA	+25°C		
	25.9	36.6	mA	+85°C		
	27.8	42.1	mA	+125°C		
DC23	37.3	42.0	mA	-40°C	3.3V	70 MIPS (N = 1, N2 = 2, N3 = 1, M = 70, F_{VCO} = 560 MHz, F_{PLLO} = 280 MHz)
	37.5	46.1	mA	+25°C		
	37.2	51.1	mA	+85°C		
	41.1	55.7	mA	+125°C		
DC24	45.0	50.4	mA	-40°C	3.3V	90 MIPS (N = 1, N2 = 2, N3 = 1, M = 90, F_{VCO} = 720 MHz, F_{PLLO} = 360 MHz)
	45.2	54.8	mA	+25°C		
	44.8	59.1	mA	+85°C		
	48.3	63.1	mA	+125°C		
DC25	45.5	51.0	mA	-40°C	3.3V	100 MIPS (N = 1, N2 = 1, N3 = 1, M = 50, F_{VCO} = 400 MHz, F_{PLLO} = 400 MHz); Slave runs at 100 MIPS but Master is still at 90 MIPS
	45.7	55.3	mA	+25°C		
	45.3	59.6	mA	+85°C		
	48.9	63.6	mA	+125°C		

Note 1: I_{DD} is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all I_{DD} measurements are as follows:

- F_{IN} = 8 MHz, F_{PFD} = 8 MHz
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as output low
- $\overline{MCLR}$ = V_{DD}, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating or being clocked (all defined PMDx bits are set)
- CPU is executing `while(1)` statement
- JTAG is disabled

36-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M5) - 5x5 mm Body [UQFN] With Corner Anchors

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	X2			3.80
Optional Center Pad Length	Y2			3.80
Contact Pad Spacing	C1		5.00	
Contact Pad Spacing	C2		5.00	
Contact Pad Width (X36)	X1			0.20
Contact Pad Length (X36)	Y1			0.80
Corner Pad Width (X4)	X3			0.20
Corner Pad Length (X36)	Y3			0.85
Corner Pad Radius	R1		0.10	
Contact Pad to Center Pad (X36)	G1	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2436A–M5