Microchip Technology - DSPIC33CH64MP205T-I/PT Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit Dual-Core
Speed	180MHz, 200MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	39
Program Memory Size	88KB (88K x 8)
Program Memory Type	FLASH, PRAM
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 31x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ch64mp205t-i-pt

TABLE 3-23: MASTER INTERRUPT VECTOR DETAILS (CONTINUED)

Interrupt Source	Vector #	IRQ #	IVT Address	Interrupt Bit Location		
				Flag	Enable	Priority
ADCAN16 – ADC AN16 Interrupt	115	107	0x0000EA	IFS6<11>	IEC6<11>	IPC26<14:12>
ADCAN17 – ADC AN17 Interrupt	116	108	0x0000EC	IFS6<12>	IEC6<12>	IPC27<2:0>
ADCAN18 – ADC AN18 Interrupt	117	109	0x0000EE	IFS6<13>	IEC6<13>	IPC27<6:4>
ADCAN19 – ADC AN19 Interrupt	118	110	0x0000F0	IFS6<14>	IEC6<14>	IPC27<10:8>
ADCAN20 – ADC AN20 Interrupt	119	111	0x0000F2	IFS6<15>	IEC6<15>	IPC27<14:12>
Reserved	120-122	112-114	0x0000F4-0x0000F8	—	—	—
ADFLT – ADC Fault	123	115	0x0000FA	IFS7<3>	IEC7<3>	IPC28<14:12>
ADCMP0 – ADC Digital Comparator 0	124	116	0x0000FC	IFS7<4>	IEC7<4>	IPC29<2:0>
ADCMP1 – ADC Digital Comparator 1	125	117	0x0000FE	IFS7<5>	IEC7<5>	IPC29<6:4>
ADCMP2 – ADC Digital Comparator 2	126	118	0x000100	IFS7<6>	IEC7<6>	IPC29<10:8>
ADCMP3 – ADC Digital Comparator 3	127	119	0x000102	IFS7<7>	IEC7<7>	IPC29<14:12>
ADFLTR0 – ADC Oversample Filter 0	128	120	0x000104	IFS7<8>	IEC7<8>	IPC30<2:0>
ADFLTR1 – ADC Oversample Filter 1	129	121	0x000106	IFS7<9>	IEC7<9>	IPC30<6:4>
ADFLTR2 – ADC Oversample Filter 2	130	122	0x000108	IFS7<10>	IEC7<10>	IPC30<10:8>
ADFLTR3 – ADC Oversample Filter 3	131	123	0x00010A	IFS7<11>	IEC7<11>	IPC30<14:12>
CLC1P – CLC1 Positive Edge	132	124	0x00010C	IFS7<12>	IEC7<12>	IPC31<2:0>
CLC2P – CLC2 Positive Edge	133	125	0x00010E	IFS7<13>	IEC7<13>	IPC31<6:4>
SPI1G – SPI1 Error	134	126	0x000110	IFS7<14>	IEC7<14>	IPC31<10:8>
SPI2G – SPI2 Error	135	127	0x000112	IFS7<15>	IEC7<15>	IPC31<14:12>
Reserved	136	128	0x000114	—	—	—
MSIS1 – MSI Slave Initiated Interrupt	137	129	0x000116	IFS8<1>	IEC8<1>	IPC32<6:4>
MSIA – MSI Protocol A	138	130	0x000118	IFS8<2>	IEC8<2>	IPC32<10:8>
MSIB – MSI Protocol B	139	131	0x00011A	IFS8<3>	IEC8<3>	IPC32<14:12>
MSIC – MSI Protocol C	140	132	0x00011C	IFS8<4>	IEC8<4>	IPC33<2:0>
MSID – MSI Protocol D	141	133	0x00011E	IFS8<5>	IEC8<5>	IPC33<6:4>
MSIE – MSI Protocol E	142	134	0x000120	IFS8<6>	IEC8<6>	IPC33<10:8>
MSIF – MSI Protocol F	143	135	0x000122	IFS8<7>	IEC8<7>	IPC33<14:12>
MSIG – MSI Protocol G	144	136	0x000124	IFS8<8>	IEC8<8>	IPC34<2:0>
MSIH – MSI Protocol H	145	137	0x000126	IFS8<9>	IEC8<9>	IPC34<6:4>
MSIDT – Master Read FIFO Data Ready	146	138	0x000128	IFS8<10>	IEC8<10>	IPC34<10:8>
MSIWFE – Master Write FIFO Empty	147	139	0x00012A	IFS8<11>	IEC8<11>	IPC34<14:12>
MSIFLT – Read or Write FIFO Fault (Over/Underflow)	148	140	0x00012C	IFS8<12>	IEC8<12>	IPC35<2:0>
S1SRST – MSI Slave Reset	149	141	0x00012E	IFS8<13>	IEC8<13>	IPC35<6:4>
Reserved	150-153	142-145	0x000130-0x000136	—	—	—
S1BRK – Slave Break	154	146	0x000138	IFS9<2>	IEC9<2>	IPC36<10:8>
Reserved	155-156	147-148	0x00013A-0x00013C	—	—	—
CCP7 – Input Capture/Output Compare 7	157	149	0x00013E	IFS9<5>	IEC9<5>	IPC37<6:4>
CCT7 – CCP7 Timer	158	150	0x000140	IFS9<6>	IEC9<6>	IPC37<10:8>
Reserved	159	151	0x000142	—	—	—
CCP8 – Input Capture/Output Compare 8	160	152	0x000144	IFS9<8>	IEC9<8>	IPC38<2:0>
CCT8 – CCP8 Timer	161	153	0x000146	IFS9<9>	IEC9<9>	IPC38<6:4>
Reserved	162-164	154-156	0x000148-0x00014C	—	—	—
S1CLKF – Slave Clock Fail	165	157	0x00014E	IFS9<13>	IEC9<13>	IPC39<6:4>
Reserved	166-175	158-167	0x000150-0x000162	—	—	—
ADFIFO – ADC FIFO Ready	176	168	0x000164	IFS10<8>	IEC10<8>	IPC42<2:0>

TABLE 3-23: MASTER INTERRUPT VECTOR DETAILS (CONTINUED)

Interrupt Source	Vector #	IRQ #	IVT Address	Interrupt Bit Location		
				Flag	Enable	Priority
PEVTA – PWM Event A	177	169	0x000166	IFS10<9>	IEC10<9>	IPC42<6:4>
PEVTB – PWM Event B	178	170	0x000168	IFS10<10>	IEC10<10>	IPC42<10:8>
PEVTC – PWM Event C	179	171	0x00016A	IFS10<11>	IEC10<11>	IPC42<14:12>
PEVTD – PWM Event D	180	172	0x00016C	IFS10<12>	IEC10<12>	IPC43<2:0>
PEVTE – PWM Event E	181	173	0x00016E	IFS10<13>	IEC10<13>	IPC43<6:4>
PEVTF – PWM Event F	182	174	0x000170	IFS10<14>	IEC10<14>	IPC43<10:8>
CLC3P – CLC3 Positive Edge	183	175	0x000172	IFS10<15>	IEC10<15>	IPC43<14:12>
CLC4P – CLC4 Positive Edge	184	176	0x000174	IFS11<0>	IEC11<0	IPC44<2:0>
CLC1N – CLC1 Negative Edge	185	177	0x000176	IFS11<1>	IEC11<1	IPC44<6:4>
CLC2N – CLC2 Negative Edge	186	178	0x000178	IFS11<2>	IEC11<2	IPC44<10:8>
CLC3N – CLC3 Negative Edge	187	179	0x00017A	IFS11<3>	IEC11<3	IPC44<14:>12>
CLC4N – CLC4 Negative Edge	188	180	0x00017C	IFS11<4>	IEC11<4	IPC45<2:0>
Reserved	189-196	181-188	0x0017E-0x0018C	—	—	—
U1EVT – UART1 Event	197	189	0x00018E	IFS11<13>	IF2C11<13>	IPC47<6:4>
U2EVT – UART2 Event	198	190	0x000190	IFS11<14>	IF2C11<14>	IPC47<12:8>

3.5.3 INTERRUPT RESOURCES

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

3.5.3.1 Key Resources

- **"Interrupts"** (DS70000600) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

3.5.4 INTERRUPT CONTROL AND STATUS REGISTERS

The dsPIC33CH128MP508 family devices implement the following registers for the interrupt controller:

- INTCON1
- INTCON2
- INTCON3
- INTCON4
- INTTREG

3.5.4.1 INTCON1 through INTCON4

Global interrupt control functions are controlled from INTCON1, INTCON2, INTCON3 and INTCON4.

INTCON1 contains the Interrupt Nesting Disable bit (NSTDIS), as well as the control and status flags for the processor trap sources.

The INTCON2 register controls external interrupt request signal behavior, contains the Global Interrupt Enable bit (GIE) and the Alternate Interrupt Vector Table Enable bit (AIVTEN).

INTCON3 contains the status flags for the Auxiliary PLL and DO stack overflow status trap sources.

The INTCON4 register contains the Software Generated Hard Trap Status bit (SGHT).

3.5.4.2 IFSx

The IFSx registers maintain all of the interrupt request flags. Each source of interrupt has a status bit, which is set by the respective peripherals or external signal and is cleared via software.

3.5.4.3 IECx

The IECx registers maintain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals.

3.5.4.4 IPCx

The IPCx registers are used to set the Interrupt Priority Level (IPL) for each source of interrupt. Each user interrupt source can be assigned to one of seven priority levels.

3.5.4.5 INTTREG

The INTTREG register contains the associated interrupt vector number and the new CPU Interrupt Priority Level, which are latched into the Vector Number (VECNUM<7:0>) and Interrupt Level bits (ILR<3:0>) fields in the INTTREG register. The new Interrupt Priority Level is the priority of the pending interrupt.

The interrupt sources are assigned to the IFSx, IECx and IPCx registers in the same sequence as they are listed in Table 3-23. For example, INT0 (External Interrupt 0) is shown as having Vector Number 8 and a natural order priority of 0. Thus, the INT0IF bit is found in IFS0<0>, the INT0IE bit in IEC0<0> and the INT0IP<2:0> bits in the first position of IPC0 (IPC0<2:0>).

3.5.4.6 Status/Control Registers

Although these registers are not specifically part of the interrupt control hardware, two of the CPU Control registers contain bits that control interrupt functionality. For more information on these registers, refer to **"dsPIC33E Enhanced CPU"** (DS70005158) in the *"dsPIC33/PIC24 Family Reference Manual"*.

- The CPU STATUS Register, SR, contains the IPL<2:0> bits (SR<7:5>). These bits indicate the current CPU Interrupt Priority Level. The user software can change the current CPU Interrupt Priority Level by writing to the IPLx bits.
- The CORCON register contains the IPL3 bit, which together with IPL<2:0>, also indicates the current CPU priority level. IPL3 is a read-only bit so that trap events cannot be masked by the user software.

All Interrupt registers are described in Register 3-18 through Register 3-22 in the following pages.

TABLE 3-34: PORTA REGISTER SUMMARY

ANSELA	—	—	—	—	—	—	—	—	—	—	—	ANSELA<4:0>					
TRISA	—	—	—	—	—	—	—	—	—	—	—	TRISA<4:0>					
PORTA	—	—	—	—	—	—	—	—	—	—	—	RA<4:0>					
LATA	—	—	—	—	—	—	—	—	—	—	—	LATA<4:0>					
ODCA	—	—	—	—	—	—	—	—	—	—	—	ODCA<4:0>					
CNPUA	—	—	—	—	—	—	—	—	—	—	—	CNPUA<4:0>					
CNPDA	—	—	—	—	—	—	—	—	—	—	—	CNPDA<4:0>					
CNCONA	ON	—	—	—	CNSTYLE	—	—	—	—	—	—	—	—	—	—	—	
CNEN0A	—	—	—	—	—	—	—	—	—	—	—	CNEN0A<4:0>					
CNSTATA	—	—	—	—	—	—	—	—	—	—	—	CNSTATA<4:0>					
CNEN1A	—	—	—	—	—	—	—	—	—	—	—	CNEN1A<4:0>					
CNFA	—	—	—	—	—	—	—	—	—	—	—	CNFA<4:0>					

TABLE 3-35: PORTB REGISTER SUMMARY

ANSELB	—	—	—	—	—	—	ANSELB<9:7>			—	—	—	ANSELB<3:0>				
TRISB	TRISB<15:0>																
PORTB	RB<15:0>																
LATB	LATB<15:0>																
ODCB	ODCB<15:0>																
CNPUB	CNPUB<15:0>																
CNPDB	CNPDB<15:0>																
CNCONB	ON	—	—	—	CNSTYLE	—	—	—	—	—	—	—	—	—	—	—	
CNEN0B	CNEN0<15:0>																
CNSTATB	CNSTATB<15:0>																
CNEN1B	CNEN1B<15:0>																
CNFB	CNFB<15:0>																

FIGURE 4-7: PAGED DATA MEMORY SPACE

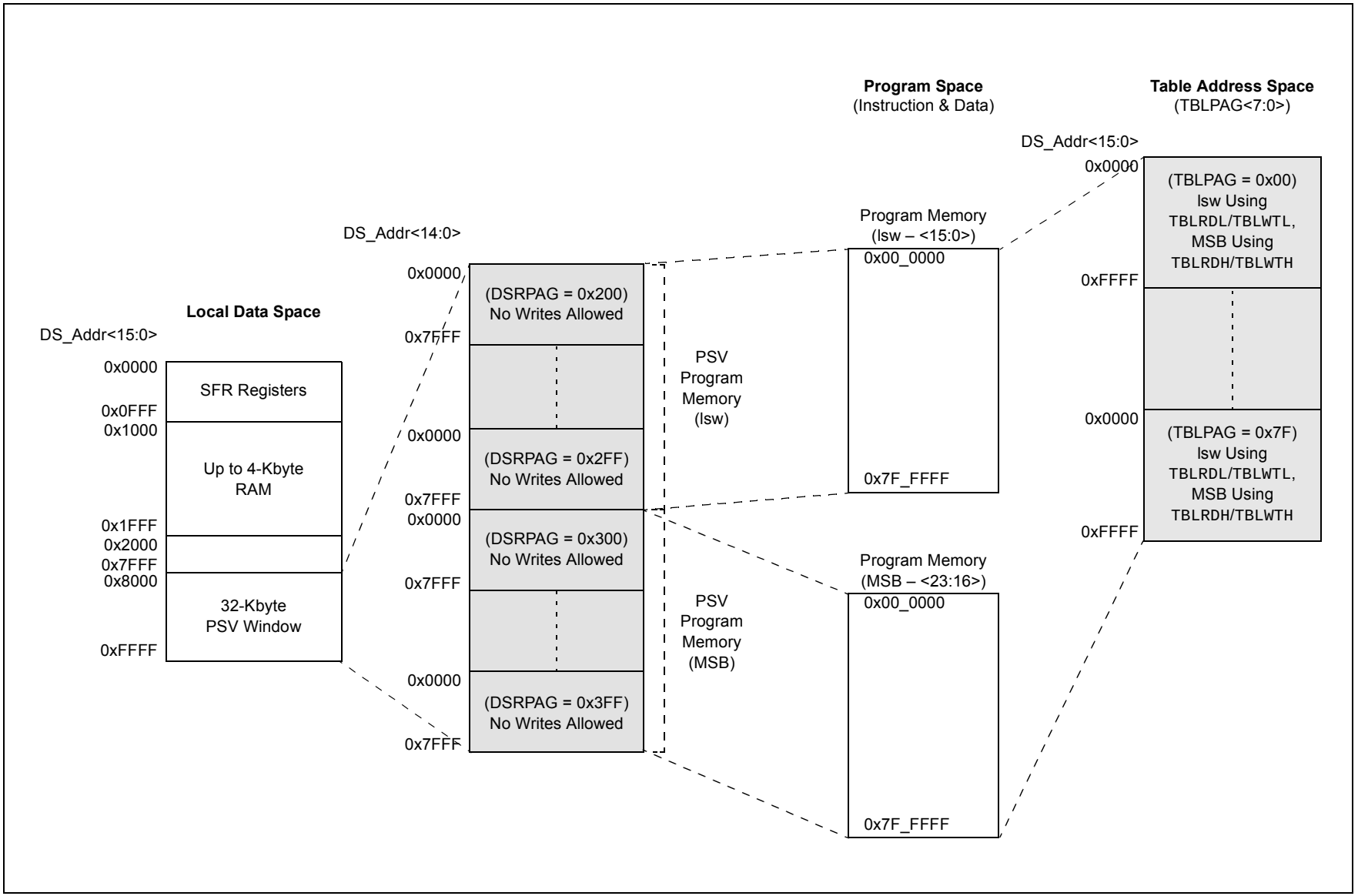


TABLE 4-24: PIN AND ANSELx AVAILABILITY

Device	Rx15	Rx14	Rx13	Rx12	Rx11	Rx10	Rx9	Rx8	Rx7	Rx6	Rx5	Rx4	Rx3	Rx2	Rx1	Rx0
PORTA																
dsPIC33XXXMP508/208	—	—	—	—	—	—	—	—	—	—	—	X	X	X	X	X
dsPIC33XXXMP506/206	—	—	—	—	—	—	—	—	—	—	—	X	X	X	X	X
dsPIC33XXXMP505/205	—	—	—	—	—	—	—	—	—	—	—	X	X	X	X	X
dsPIC33XXXMP503/203	—	—	—	—	—	—	—	—	—	—	—	X	X	X	X	X
dsPIC33XXXMP502/202	—	—	—	—	—	—	—	—	—	—	—	X	X	X	X	X
ANSELA	—	—	—	—	—	—	—	—	—	—	—	X	X	X	X	—
PORTB																
dsPIC33XXXMP508/208	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
dsPIC33XXXMP506/206	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
dsPIC33XXXMP505/205	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
dsPIC33XXXMP503/203	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
dsPIC33XXXMP502/202	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
ANSELB	—	—	—	—	—	—	—	X	X	—	—	X	X	X	X	X
PORTC																
dsPIC33XXXMP508/208	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
dsPIC33XXXMP506/206	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
dsPIC33XXXMP505/205	—	—	X	X	X	X	X	X	X	X	X	X	X	X	X	X
dsPIC33XXXMP503/203	—	—	—	—	—	—	—	—	—	—	X	X	X	X	X	X
dsPIC33XXXMP502/202	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
ANSELC	—	—	—	—	—	—	—	—	X	X	—	—	X	X	X	X
PORTD																
dsPIC33XXXMP508/208	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
dsPIC33XXXMP506/206	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
dsPIC33XXXMP505/205	—	—	X	—	—	X	—	X	—	—	—	—	—	—	X	—
dsPIC33XXXMP503/203	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
dsPIC33XXXMP502/202	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
ANSELD	—	X	X	X	X	X	—	—	—	—	—	—	—	—	—	—
PORTE																
dsPIC33XXXMP508/208	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
dsPIC33XXXMP506/206	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
dsPIC33XXXMP505/205	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
dsPIC33XXXMP503/203	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
dsPIC33XXXMP502/202	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
ANSELE	—	—	—	—	—	—	—	—	—	X	—	—	—	—	—	—

TABLE 4-25: 5V INPUT TOLERANT PORTS

PORTA	—	—	—	—	—	—	—	—	—	—	—	RA4	RA3	RA2	RA1	RA0
PORTB	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
PORTC	RC15	RC14	RC13	RC12	RC11	RC10	RC9	RC8	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
PORTD	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
PORTE	RE15	RE14	RE13	RE12	RE11	RE10	RE9	RE8	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0

Legend: **Shaded pins** are up to 5.5 VDC input tolerant.

REGISTER 4-51: RPINR23: PERIPHERAL PIN SELECT INPUT REGISTER 23

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
U1CTSR7	U1CTSR6	U1CTSR5	U1CTSR4	U1CTSR3	U1CTSR2	U1CTSR1	U1CTSR0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **U1CTSR<7:0>:** Assign UART1 Clear-to-Send ($\overline{\text{S1U1CTS}}$) to the Corresponding S1RPn Pin bits
See Table 4-27.

bit 7-0 **Unimplemented:** Read as ‘0’

REGISTER 4-52: RPINR37: PERIPHERAL PIN SELECT INPUT REGISTER 37

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PCI17R7	PCI17R6	PCI17R5	PCI17R4	PCI17R3	PCI17R2	PCI17R1	PCI17R0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **PCI17R<7:0>:** Assign PWM Input 17 (S1PCI17) to the Corresponding S1RPn Pin bits
See Table 4-27.

bit 7-0 **Unimplemented:** Read as ‘0’

REGISTER 6-13: CLKDIV: CLOCK DIVIDER REGISTER (SLAVE) (CONTINUED)

bit 3-0 **PLLPRE<3:0>:** PLL Phase Detector Input Divider Select bits (also denoted as 'N1', PLL prescaler)(4)

11111 = Reserved
...
1001 = Reserved
1000 = Input divided by 8
0111 = Input divided by 7
0110 = Input divided by 6
0101 = Input divided by 5
0100 = Input divided by 4
0011 = Input divided by 3
0010 = Input divided by 2
0001 = Input divided by 1 (power-on default selection)
0000 = Reserved

Note 1: The DOZE<2:0> bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored.

2: This bit is cleared when the ROI bit is set and an interrupt occurs.

3: The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.

4: PLLPRE<3:0> may be updated while the PLL is operating, but the VCO may overshoot.

7.2.1 SLEEP MODE

The following occurs in Sleep mode:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption is reduced to a minimum, provided that no I/O pin is sourcing current.
- The Fail-Safe Clock Monitor does not operate, since the system clock source is disabled.
- The LPRC clock continues to run in Sleep mode if the WDT is enabled.
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode.
- Some device features or peripherals can continue to operate. This includes items such as the Input Change Notification on the I/O ports or peripherals that use an External Clock input.
- Any peripheral that requires the system clock source for its operation is disabled.

The device wakes up from Sleep mode on any of the these events:

- Any interrupt source that is individually enabled
- Any form of device Reset
- A WDT time-out

On wake-up from Sleep mode, the processor restarts with the same clock source that was active when Sleep mode was entered.

For optimal power savings, the internal regulator and the Flash regulator can be configured to go into stand-by when Sleep mode is entered by clearing the VREGS (RCON<8>) bit.

7.2.2 IDLE MODE

The following occurs in Idle mode:

- The CPU stops executing instructions.
- The WDT is automatically cleared.
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see **Section 7.4 “Peripheral Module Disable”**).
- If the WDT or FSCM is enabled, the LPRC also remains active.

The device wakes from Idle mode on any of these events:

- Any interrupt that is individually enabled
- Any device Reset
- A WDT time-out

On wake-up from Idle mode, the clock is reapplied to the CPU and instruction execution will begin (2-4 clock cycles later), starting with the instruction following the PWRSAV instruction or the first instruction in the ISR.

All peripherals also have the option to discontinue operation when Idle mode is entered to allow for increased power savings. This option is selectable in the control register of each peripheral; for example, the SIDL bit in the Timer1 Control register (T1CON<13>).

7.2.3 INTERRUPTS COINCIDENT WITH POWER SAVE INSTRUCTIONS

Any interrupt that coincides with the execution of a PWRSAV instruction is held off until entry into Sleep or Idle mode has completed. The device then wakes up from Sleep or Idle mode.

REGISTER 7-13: PMD6: SLAVE PERIPHERAL MODULE DISABLE 6 CONTROL REGISTER HIGH

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	DMA1MD	DMA0MD
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10 **Unimplemented:** Read as '0'

bit 9 **DMA1MD:** DMA1 Module Disable bit
1 = DMA1 module is disabled
0 = DMA1 module is enabled

bit 8 **DMA0MD:** DMA0 Module Disable bit
1 = DMA0 module is disabled
0 = DMA0 module is enabled

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 11-4: DACxCONH: DACx CONTROL HIGH REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	TMCB<9:8>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TMCB<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **TMCB<9:0>:** DACx Leading-Edge Blanking bits

These register bits specify the blanking period for the comparator, following changes to the DAC output during Change-of-State (COS), for the input signal selected by the HCFSEL<3:0> bits in Register 11-9.

REGISTER 11-5: DACxCONL: DACx CONTROL LOW REGISTER

R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
DACEN	IRQM1(1,2)	IRQM0(1,2)	—	—	CBE	DACOEN	FLTREN
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMPSTAT	CMPPOL	INSEL2	INSEL1	INSEL0	HYSPOL	HYSSEL1	HYSSEL0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 15 **DACEN:** Individual DACx Module Enable bit

1 = Enables DACx module
0 = Disables DACx module to reduce power consumption; any pending Slope mode and/or underflow conditions are cleared

bit 14-13 **IRQM<1:0>:** Interrupt Mode select bits(1,2)

11 = Generates an interrupt on either a rising or falling edge detect
10 = Generates an interrupt on a falling edge detect
01 = Generates an interrupt on a rising edge detect
00 = Interrupts are disabled

bit 12-11 **Unimplemented:** Read as '0'

Note 1: Changing these bits during operation may generate a spurious interrupt.
2: The edge selection is a post-polarity selection via the CMPPOL bit.

REGISTER 12-4: QEIxSTAT: QEIx STATUS REGISTER

U-0	U-0	HS/R/C-0	R/W-0	HS/R/C-0	R/W-0	HS/R/C-0	R/W-0
—	—	PCHEQIRQ	PCHEQIEN	PCLEQIRQ	PCLEQIEN	POSOVIRQ	POSOVIEN
bit 15							bit 8

HS/R/C-0	R/W-0	HS/R/C-0	R/W-0	HS/R/C-0	R/W-0	HS/R/C-0	R/W-0
PCIIRQ(1)	PCIIEN	VELOVIRQ	VELOVIEN	HOMIRQ	HOMIEN	IDXIRQ	IDXIEN
bit 7							bit 0

Legend:	C = Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **PCHEQIRQ:** Position Counter Greater Than Compare Status bit
1 = POSxCNT ≥ QEIxGEC
0 = POSxCNT < QEIxGEC

bit 12 **PCHEQIEN:** Position Counter Greater Than Compare Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 11 **PCLEQIRQ:** Position Counter Less Than Compare Status bit
1 = POSxCNT ≤ QEIxLEC
0 = POSxCNT > QEIxLEC

bit 10 **PCLEQIEN:** Position Counter Less Than Compare Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 9 **POSOVIRQ:** Position Counter Overflow Status bit
1 = Overflow has occurred
0 = No overflow has occurred

bit 8 **POSOVIEN:** Position Counter Overflow Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 7 **PCIIRQ:** Position Counter (Homing) Initialization Process Complete Status bit(1)
1 = POSxCNT was reinitialized
0 = POSxCNT was not reinitialized

bit 6 **PCIIEN:** Position Counter (Homing) Initialization Process Complete Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 5 **VELOVIRQ:** Velocity Counter Overflow Status bit
1 = Overflow has occurred
0 = No overflow has occurred

bit 4 **VELOVIEN:** Velocity Counter Overflow Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 3 **HOMIRQ:** Status Flag for Home Event Status bit
1 = Home event has occurred
0 = No Home event has occurred

Note 1: This status bit is only applicable to PIMOD<2:0> modes, '011' and '100'.

REGISTER 12-15: INTXxHLDL: INDEX x COUNTER HOLD REGISTER LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTHLD<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTHLD<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **INTXHLD<15:0>:** Hold for Reading/Writing Interval Timer Value Register (INDXCNT) bits

REGISTER 12-16: INTXxHLDH: INDEX x COUNTER HOLD REGISTER HIGH

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTHLD<31:24>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTHLD<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **INTHLD<31:16>:** Hold for Reading/Writing Interval Timer Value Register (INDXCNT) bits

REGISTER 13-2: UxMODEH: UARTx CONFIGURATION REGISTER HIGH

R/W-0	R-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
SLPEN	ACTIVE	—	—	BCLKMOD	BCLKSEL1	BCLKSEL0	HALFDPLX
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RUNOVF	URXINV	STSEL1	STSEL0	C0EN	UTXINV	FLO1	FLO0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **SLPEN:** Run During Sleep Enable bit
1 = UART BRG clock runs during Sleep
0 = UART BRG clock is turned off during Sleep

bit 14 **ACTIVE:** UART Running Status bit
1 = UART clock request is active (user can not update the UxMODE/UxMODEH registers)
0 = UART clock request is not active (user can update the UxMODE/UxMODEH registers)

bit 13-12 **Unimplemented:** Read as '0'

bit 11 **BCLKMOD:** Baud Clock Generation Mode Select bit
1 = Uses fractional Baud Rate Generation
0 = Uses legacy divide-by-x counter for baud clock generation (x = 4 or 16 depending on the BRGH bit)

bit 10-9 **BCLKSEL<1:0>:** Baud Clock Source Selection bits
11 = Reserved
10 = FOSC
01 = Reserved
00 = FOSC/2 (FP)

bit 8 **HALFDPLX:** UART Half-Duplex Selection Mode bit
1 = Half-Duplex mode: UxTX is driven as an output when transmitting and tri-stated when TX is Idle
0 = Full-Duplex mode: UxTX is driven as an output at all times when both UARTEN and UTXEN are set

bit 7 **RUNOVF:** Run During Overflow Condition Mode bit
1 = When an Overflow Error (OERR) condition is detected, the RX shifter continues to run so as to remain synchronized with incoming RX data; data is not transferred to UxRXREG when it is full (i.e., no UxRXREG data is overwritten)
0 = When an Overflow Error (OERR) condition is detected, the RX shifter stops accepting new data (Legacy mode)

bit 6 **URXINV:** UART Receive Polarity bit
1 = Inverts RX polarity; Idle state is low
0 = Input is not inverted; Idle state is high

bit 5-4 **STSEL<1:0>:** Number of Stop Bits Selection bits
11 = 2 Stop bits sent, 1 checked at receive
10 = 2 Stop bits sent, 2 checked at receive
01 = 1.5 Stop bits sent, 1.5 checked at receive
00 = 1 Stop bit sent, 1 checked at receive

bit 3 **C0EN:** Enable Legacy Checksum (C0) Transmit and Receive bit
1 = Checksum Mode 1 (enhanced LIN checksum in LIN mode; add all TX/RX words in all other modes)
0 = Checksum Mode 0 (legacy LIN checksum in LIN mode; not used in all other modes)

15.0 INTER-INTEGRATED CIRCUIT (I^2C)

Note 1: This data sheet summarizes the features of the dsPIC33CH128MP508 family of devices. It is not intended to be a comprehensive reference source. For more information, refer to **"Inter-Integrated Circuit (I^2C)"** (DS70000195) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: The I^2C is identical for both Master core and Slave core. The x is common for both Master and Slave (where the x represents the number of the specific module being addressed). The number of I^2C modules available on the Master and Slave is different and they are located in different SFR locations.

3: All associated register names are the same on the Master core and the Slave core. The Slave code will be developed in a separate project in MPLAB® X IDE with the device selection, dsPIC33CH128MP508**S1**, where the **S1** indicates the Slave device. The Master I^2C is I2C1 and I2C2, and the Slave is I2C1.

The Inter-Integrated Circuit (I^2C) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, display drivers, A/D Converters, etc.

The I^2C module supports these features:

- Independent Master and Slave Logic
- 7-Bit and 10-Bit Device Addresses
- General Call Address as Defined in the I^2C Protocol
- Clock Stretching to Provide Delays for the Processor to Respond to a Slave Data Request
- Both 100 kHz and 400 kHz Bus Specifications
- Configurable Address Masking
- Multi-Master modes to Prevent Loss of Messages in Arbitration
- Bus Repeater mode, Allowing the Acceptance of All Messages as a Slave, regardless of the Address
- Automatic SCL

A block diagram of the module is shown in Figure 15-1.

15.1 Communicating as a Master in a Single Master Environment

The details of sending a message in Master mode depends on the communication protocol for the device being communicated with. Typically, the sequence of events is as follows:

1. Assert a Start condition on SDAx and SCLx.
2. Send the I^2C device address byte to the Slave with a write indication.
3. Wait for and verify an Acknowledge from the Slave.
4. Send the first data byte (sometimes known as the command) to the Slave.
5. Wait for and verify an Acknowledge from the Slave.
6. Send the serial memory address low byte to the Slave.
7. Repeat Steps 4 and 5 until all data bytes are sent.
8. Assert a Repeated Start condition on SDAx and SCLx.
9. Send the device address byte to the Slave with a read indication.
10. Wait for and verify an Acknowledge from the Slave.
11. Enable Master reception to receive serial memory data.
12. Generate an ACK or NACK condition at the end of a received byte of data.
13. Generate a Stop condition on SDAx and SCLx.

17.1 Timer1 Control Register

REGISTER 17-1: T1CON: TIMER1 CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0
TON(1)	—	SIDL	TMWDIS	TMWIP	PRWIP	TECS1	TECS0
bit 15							bit 8

R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
TGATE	—	TCKPS1	TCKPS0	—	TSYNC(1)	TCS(1)	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TON:** Timer1 On bit(1)
1 = Starts 16-bit Timer1
0 = Stops 16-bit Timer1

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Timer1 Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **TMWDIS:** Asynchronous Timer1 Write Disable bit
1 = Timer writes are ignored while a posted write to TMR1 or PR1 is synchronized to the asynchronous clock domain
0 = Back-to-back writes are enabled in Asynchronous mode

bit 11 **TMWIP:** Asynchronous Timer1 Write in Progress bit
1 = Write to the timer in Asynchronous mode is pending
0 = Write to the timer in Asynchronous mode is complete

bit 10 **PRWIP:** Asynchronous Period Write in Progress bit
1 = Write to the Period register in Asynchronous mode is pending
0 = Write to the Period register in Asynchronous mode is complete

bit 9-8 **TECS<1:0>:** Timer1 Extended Clock Select bits
11 = FRC clock
10 = 2 TCY
01 = TCY
00 = External Clock comes from the T1CK pin

bit 7 **TGATE:** Timer1 Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 6 **Unimplemented:** Read as '0'

Note 1: When Timer1 is enabled in External Synchronous Counter mode (TCS = 1, TSYNC = 1, TON = 1), any attempts by user software to write to the TMR1 register are ignored.

REGISTER 21-29: FS1ICD CONFIGURATION REGISTER (SLAVE)

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

RP/O-1	U-1	R/PO-1	U-1	U-1	U-1	U-1	U-1
S1NOBTSWP	—	S1ISOLAT	—	—	—	—	—
bit 15							bit 8

r-1	U-1	U-1	U-1	U-1	U-1	R/PO-1	R/PO-1
—	—	—	—	—	—	S1ICS1	S1ICS0
bit 7							bit 0

Legend:	PO = Program Once bit	r = Reserved bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 23-16 **Unimplemented:** Read as '1'

bit 15 **S1NOBTSWP:** BOOTSWP Instruction Disable bit
1 = BOOTSWP instruction is disabled
0 = BOOTSWP instruction is enabled

bit 14 **Unimplemented:** Read as '1'

bit 13 **S1ISOLAT:** Slave Core Isolation bit
1 = The Slave can operate (in Debug mode), even if the SLVEN bit in the MSI is zero
0 = The Slave can only operate if the SLVEN bit in the MSI is set

bit 12-8 **Unimplemented:** Read as '1'

bit 7 **Reserved:** Maintain as '1'

bit 6-2 **Unimplemented:** Read as '1'

bit 1-0 **S1ICS<1:0>:** ICD Pin Placement Select bits
11 = Slave ICD pins are S1PGC1/S1PGD1/$\overline{\text{S1MCLR1}}$
10 = Slave ICD pins are S1PGC2/S1PGD2/$\overline{\text{S1MCLR2}}$
01 = Slave ICD pins are S1PGC3/S1PGD3/$\overline{\text{S1MCLR3}}$
00 = None ($\overline{\text{S1MCLR1}}$ pin is released and can be used as a regular I/O)

REGISTER 21-31: FS1ALTREG CONFIGURATION REGISTER (SLAVE)

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

U-1	R/PO-1	R/PO-1	R/PO-1	U-1	R/PO-1	R/PO-1	R/PO-1
—	S1CTXT4<2:0>			—	S1CTXT3<2:0>		
bit 15							bit 8

U-1	R/PO-1	R/PO-1	R/PO-1	U-1	R/PO-1	R/PO-1	R/PO-1
—	S1CTXT2<2:0>			—	S1CTXT1<2:0>		
bit 7							bit 0

Legend:	PO = Program Once bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-15 **Unimplemented:** Read as ‘1’

bit 14-12 **S1CTXT4<2:0>:** Alternate Working Register Set #4 Interrupt Priority Level Selection bits
111 = Not assigned
110 = Alternate Register Set #4 is assigned to IPL Level 7
101 = Alternate Register Set #4 is assigned to IPL Level 6
100 = Alternate Register Set #4 is assigned to IPL Level 5
011 = Alternate Register Set #4 is assigned to IPL Level 4
010 = Alternate Register Set #4 is assigned to IPL Level 3
001 = Alternate Register Set #4 is assigned to IPL Level 2
000 = Alternate Register Set #4 is assigned to IPL Level 1

bit 11 **Unimplemented:** Read as ‘1’

bit 10-8 **S1CTXT3<2:0>:** Alternate Working Register Set #3 Interrupt Priority Level Selection bits
111 = Not assigned
110 = Alternate Register Set #3 is assigned to IPL Level 7
101 = Alternate Register Set #3 is assigned to IPL Level 6
100 = Alternate Register Set #3 is assigned to IPL Level 5
011 = Alternate Register Set #3 is assigned to IPL Level 4
010 = Alternate Register Set #3 is assigned to IPL Level 3
001 = Alternate Register Set #3 is assigned to IPL Level 2
000 = Alternate Register Set #3 is assigned to IPL Level 1

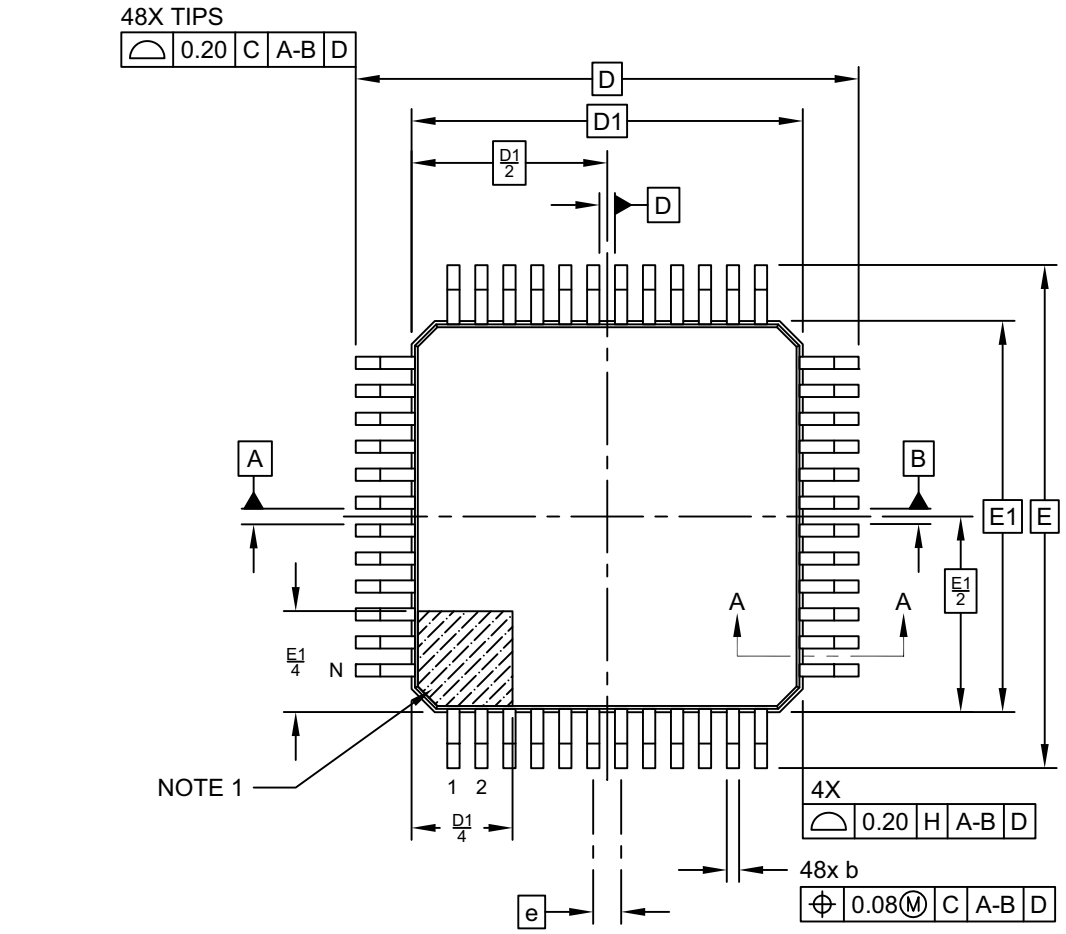
bit 7 **Unimplemented:** Read as ‘1’

bit 6-4 **S1CTXT2<2:0>:** Alternate Working Register Set #2 Interrupt Priority Level Selection bits
111 = Not assigned
110 = Alternate Register Set #2 is assigned to IPL Level 7
101 = Alternate Register Set #2 is assigned to IPL Level 6
100 = Alternate Register Set #2 is assigned to IPL Level 5
011 = Alternate Register Set #2 is assigned to IPL Level 4
010 = Alternate Register Set #2 is assigned to IPL Level 3
001 = Alternate Register Set #2 is assigned to IPL Level 2
000 = Alternate Register Set #2 is assigned to IPL Level 1

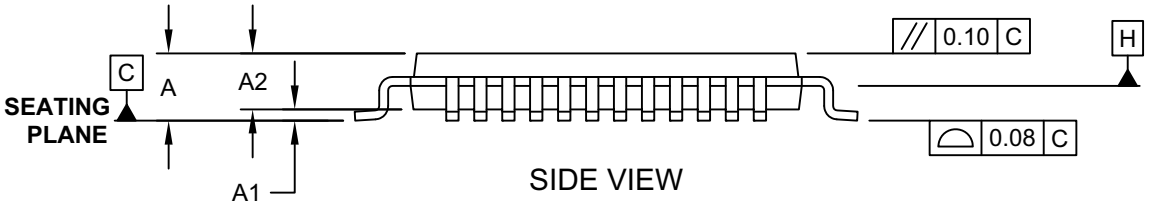
bit 3 **Unimplemented:** Read as ‘1’

48-Lead Thin Quad Flatpack (PT) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

Microchip Technology Drawing C04-300-PT Rev A Sheet 1 of 2

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