Microchip Technology - DSPIC33CH64MP208-I/PT Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit Dual-Core
Speed	180MHz, 200MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	69
Program Memory Size	88KB (88K x 8)
Program Memory Type	FLASH, PRAM
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 34x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ch64mp208-i-pt

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TABLE 3-18: MASTER SFR BLOCK F00h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
Reset			PMD1	FA4	----000-00000-00	PCTRAPH	FC2	--------00000000
RCON	F80	00--x-0000000011	PMD2	FA6	--------00000000	FEXL	FC4	xxxxxxxxxxxxxxxx
Oscillator			PMD3	FA8	--------0-----0-	FEXH	FC6	--------xxxxxxxx
OSCCON	F84	-000-yyy0-0-0--0	PMD4	FAA	------------0---	DPCL	FCE	xxxxxxxxxxxxxxxx
CLKDIV	F86	00110000--000001	PMD6	FAE	--000000--------	DPCH	FD0	--------xxxxxxxx
PLLFBD	F88	----000010010110	PMD7	FB0	-------x----0---	APPO	FD2	xxxxxxxxxxxxxxxx
PLLDIV	F8A	------00-011-001	PMD8	FB2	---00--0--xx000-	APPI	FD4	xxxxxxxxxxxxxxxx
OSCTUN	F8C	----------000000	**WDT**			APPS	FD6	----------xxxxx
ACLKCON1	F8E	00-----0--000001	WDTCONL	FB4	0--0000000000000	STROUTL	FD8	xxxxxxxxxxxxxxxx
APLLFBD1	F90	----000010010110	WDTCONH	FB6	0000000000000000	STROUTH	FDA	xxxxxxxxxxxxxxxx
APLLDIV1	F92	------00-011-001	REFOCONL	FB8	0-000-00----0000	STROVCNT	FDC	xxxxxxxxxxxxxxxx
CANCLKCON	F9A	----xxxx-xxxxxxx	REFOCONH	FBA	-000000000000000	JDATAH	FFA	xxxxxxxxxxxxxxxx
PMD			REFOTRIML	FBC	0000000000000000	JDATAL	FFC	xxxxxxxxxxxxxxxx
PMDCON	FA0	----0----------	PCTRAPL	FC0	0000000000000000			

Legend: x = unknown or indeterminate value; "-" =unimplemented bits; y = value set by Configuration bits. Address and Reset values are in hexadecimal and binary, respectively.

When a PSV page overflow or underflow occurs, EA<15> is cleared as a result of the register indirect EA calculation. An overflow or underflow of the EA in the PSV pages can occur at the page boundaries when:

- The initial address, prior to modification, addresses the PSV page
- The EA calculation uses Pre- or Post-Modified Register Indirect Addressing; however, this does not include Register Offset Addressing

In general, when an overflow is detected, the DSRPAG register is incremented and the EA<15> bit is set to keep the base address within the PSV window. When an underflow is detected, the DSRPAG register is decremented and the EA<15> bit is set to keep the base address within the PSV window. This creates a linear PSV address space, but only when using Register Indirect Addressing modes.

Exceptions to the operation described above arise when entering and exiting the boundaries of Page 0 and PSV spaces. Table 3-19 lists the effects of overflow and underflow scenarios at different boundaries.

In the following cases, when overflow or underflow occurs, the EA<15> bit is set and the DSRPAG is not modified; therefore, the EA will wrap to the beginning of the current page:

- Register Indirect with Register Offset Addressing
- Modulo Addressing
- Bit-Reversed Addressing

TABLE 3-19: OVERFLOW AND UNDERFLOW SCENARIOS AT PAGE 0 AND PSV SPACE BOUNDARIES(2,3,4)

O/U, R/W	Operation	Before			After		
		DSRPAG	DS EA<15>	Page Description	DSRPAG	DS EA<15>	Page Description
O, Read	[++Wn] or [Wn++]	DSRPAG = 0x2FF	1	PSV: Last lsw page	DSRPAG = 0x300	1	PSV: First MSB page
O, Read		DSRPAG = 0x3FF	1	PSV: Last MSB page	DSRPAG = 0x3FF	0	See **Note 1**
U, Read	[--Wn] or [Wn--]	DSRPAG = 0x001	1	PSV page	DSRPAG = 0x001	0	See **Note 1**
U, Read		DSRPAG = 0x200	1	PSV: First lsw page	DSRPAG = 0x200	0	See **Note 1**
U, Read		DSRPAG = 0x300	1	PSV: First MSB page	DSRPAG = 0x2FF	1	PSV: Last lsw page

Legend: O = Overflow, U = Underflow, R = Read, W = Write

Note 1: The Register Indirect Addressing now addresses a location in the base Data Space (0x0000-0x8000).

2: An EDS access, with DSRPAG = 0x000, will generate an address error trap.

3: Only reads from PS are supported using DSRPAG.

4: Pseudolinear Addressing is not supported for large offsets.

3.3.2 RTSP OPERATION

RTSP allows the user application to program one double instruction word or one row at a time.The double instruction word write blocks and single row write blocks are edge-aligned, from the beginning of program memory, on boundaries of one double instruction word and 64 double instruction words, respectively.

The basic sequence for RTSP programming is to first load two 24-bit instructions into the NVM write latches found in configuration memory space. Refer to Figure 3-3 through Figure 3-4 for write latch addresses. Then, the WR bit in the NVMCON register is set to initiate the write process. The processor stalls (waits) until the programming operation is finished. The WR bit is automatically cleared when the operation is finished.

Double instruction word writes are performed by manually loading both write latches, using TBLWTL and TBLWTH instructions, and then initiating the NVM write while the NVMOPx bits are set to '0x1'. The program space destination address is defined by the NVMADR/U registers.

EXAMPLE 3-1: FLASH WRITE/READ

```
////////Flash write ////////////////////////
//Sample code for writing 0x123456 to address locations  0x10000 / 10002
    NVMCON = 0x4001;
    TBLPAG = 0xFA;                  // write latch upper address
    NVMADR = 0x0000;                // set target write address of general segment
    NVMADRU = 0x0001;
    __builtin_tblwtl(0, 0x3456);    // load write latches
    __builtin_tblwth (0,0x12);

    __builtin_tblwtl(2, 0x3456);    // load write latches
    __builtin_tblwth (2,0x12);

    asm volatile ("disi #5");
    __builtin_write_NVM();
    while(_WR == 1 ) ;


////////////Flash Read///////////////
//Sample code to read the Flash content of address 0x10000
// readDataL/ readDataH variables need to defined
    TBLPAG = 0x0001;
    readDataL = __builtin_tblrdl(0x0000);
    readDataH = __builtin_tblrdh(0x0000);
```

REGISTER 3-104: C1NBTCFGH: CAN NOMINAL BIT TIME CONFIGURATION REGISTER HIGH(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BRP<7:0>							
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
TSEG1<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **BRP<7:0>:** Baud Rate Prescaler bits
1111 1111 = TQ = 256/FSYS
...
0000 0000 = TQ = 1/FSYS

bit 7-0 **TSEG1<7:0>:** Time Segment 1 bits (Propagation Segment + Phase Segment 1)
1111 1111 = Length is 256 x TQ
...
0000 0000 = Length is 1 x TQ

Note 1: These bits can only be modified in Configuration mode (OPMOD<2:0> = 100).

REGISTER 3-105: C1NBTCFGL: CAN NOMINAL BIT TIME CONFIGURATION REGISTER LOW(1)

U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1
—	TSEG2<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1
—	SJW<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **TSEG2<6:0>:** Time Segment 2 bits (Phase Segment 2)
111 1111 = Length is 128 x TQ
...
000 0000 = Length is 1 x TQ

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **SJW<6:0>:** Synchronization Jump Width bits
111 1111 = Length is 128 x TQ
...
000 0000 = Length is 1 x TQ

Note 1: These bits can only be modified in Configuration mode (OPMOD<2:0> = 100).

REGISTER 3-122: C1TXIFH: CAN TRANSMIT INTERRUPT STATUS REGISTER HIGH(1)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TFIF<31:24>							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TFIF<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **TFIF<31:16>:** Unimplemented

Note 1: C1TXIFH: FIFO: TFIFx = 'or' of the enabled TX FIFO flags (flags need to be cleared in the FIFO register).

REGISTER 3-123: C1TXIFL: CAN TRANSMIT INTERRUPT STATUS REGISTER LOW(1)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TFIF<15:8>							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TFIF<7:0>(2)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **TFIF<15:8>:** Unimplemented

bit 7-0 **TFIF<7:0>:** Transmit FIFO/TXQ Interrupt Pending bits(2)

1 = One or more enabled transmit FIFO/TXQ interrupts are pending

0 = No enabled transmit FIFO/TXQ interrupts are pending

Note 1: C1TXIFL: FIFO: TFIFx = 'or' of the enabled TX FIFO flags (flags need to be cleared in the FIFO register).

2: TFIF0 is for the transmit queue.

REGISTER 3-138: C1TEFSTA: CAN TRANSMIT EVENT FIFO STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	S/HC-0	R-0	R-0	R-0
—	—	—	—	TEFOVIF	TEFFIF(1)	TEFHIF(1)	TEFNEIF(1)
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	S = Settable by ‘1’ bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as ‘0’

bit 3 **TEFOVIF:** Transmit Event FIFO Overflow Interrupt Flag bit
1 = Overflow event has occurred
0 = No overflow event has occurred

bit 2 **TEFFIF:** Transmit Event FIFO Full Interrupt Flag bit(1)
1 = FIFO is full
0 = FIFO is not full

bit 1 **TEFHIF:** Transmit Event FIFO Half Full Interrupt Flag bit(1)
1 = FIFO is ≥ half full
0 = FIFO is < half full

bit 0 **TEFNEIF:** Transmit Event FIFO Not Empty Interrupt Flag bit(1)
1 = FIFO is not empty
0 = FIFO is empty

Note 1: These bits are read-only and reflect the status of the FIFO.

REGISTER 3-189: PTGT1LIM: PTG TIMER1 LIMIT REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT1LIM<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT1LIM<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTGT1LIM<15:0>:** PTG Timer1 Limit Register bits
General Purpose Timer1 Limit register.

Note 1: These bits are read-only when the module is executing Step commands.

REGISTER 3-190: PTGSDLIM: PTG STEP DELAY LIMIT REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGSDLIM<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGSDLIM<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTGSDLIM<15:0>:** PTG Step Delay Limit Register bits
This register holds a PTG Step delay value representing the number of additional PTG clocks between the start of a Step command and the completion of a Step command.

Note 1: These bits are read-only when the module is executing Step commands.

REGISTER 4-17: CORCON: SLAVE CORE CONTROL REGISTER(1)

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0
VAR	—	US1	US0	EDT	DL2	DL1	DL0
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R-0	R/W-0	R/W-0
SATA	SATB	SATDW	ACCSAT	IPL3(2)	SFA	RND	IF
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1'= Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **VAR:** Variable Exception Processing Latency Control bit
1 = Variable exception processing is enabled
0 = Fixed exception processing is enabled

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3(2)
1 = CPU Interrupt Priority Level is greater than 7
0 = CPU Interrupt Priority Level is 7 or less

Note 1: For complete register details, see Register 4-2.
2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

REGISTER 4-45: RPINR13: PERIPHERAL PIN SELECT INPUT REGISTER 13

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PCI11R7	PCI11R6	PCI11R5	PCI11R4	PCI11R3	PCI11R2	PCI11R1	PCI11R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PCI10R7	PCI10R6	PCI10R5	PCI10R4	PCI10R3	PCI10R2	PCI10R1	PCI10R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **PCI11R<7:0>:** Assign PWM Input 11 (S1PCI11) to the Corresponding S1RPn Pin bits
See Table 4-27.

bit 7-0 **PCI10R<7:0>:** Assign PWM Input 10 (S1PCI10) to the Corresponding S1RPn Pin bits
See Table 4-27.

REGISTER 4-46: RPINR14: PERIPHERAL PIN SELECT INPUT REGISTER 14

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIB1R7	QEIB1R6	QEIB1R5	QEIB1R4	QEIB1R3	QEIB1R2	QEIB1R1	QEIB1R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIA1R7	QEIA1R6	QEIA1R5	QEIA1R4	QEIA1R3	QEIA1R2	QEIA1R1	QEIA1R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **QEIB1R<7:0>:** Assign QEI Input B (S1QEIB1) to the Corresponding S1RPn Pin bits
See Table 4-27.

bit 7-0 **QEIA1R<7:0>:** Assign QEI Input A (S1QEIA1) to the Corresponding S1RPn Pin bits
See Table 4-27.

REGISTER 4-86: ADCON2H: ADC CONTROL REGISTER 2 HIGH

HSC/R-0	HSC/R-0	U-0	r-0	r-0	r-0	R/W-0	R/W-0
REFRDY	REFERR	—	r	r	r	SHRSAMC9	SHRSAMC8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SHRSAMC7	SHRSAMC6	SHRSAMC5	SHRSAMC4	SHRSAMC3	SHRSAMC2	SHRSAMC1	SHRSAMC0
bit 7							bit 0

Legend:	r = Reserved bit	U = Unimplemented bit, read as ‘0’	
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **REFRDY:** Band Gap and Reference Voltage Ready Flag bit
1 = Band gap is ready
0 = Band gap is not ready

bit 14 **REFERR:** Band Gap or Reference Voltage Error Flag bit
1 = Band gap was removed after the ADC module was enabled (ADON = 1)
0 = No band gap error was detected

bit 13 **Unimplemented:** Read as ‘0’

bit 12-10 **Reserved:** Maintain as ‘0’

bit 9-0 **SHRSAMC<9:0>:** Shared ADC Core Sample Time Selection bits
These bits specify the number of shared ADC Core Clock Periods (TADCORE) for the shared ADC core sample time.
1111111111 = 1025 TADCORE
...
0000000001 = 3 TADCORE
0000000000 = 2 TADCORE

Example 6-7 illustrates code for using the Slave PLL with an 8 MHz internal FRC.

EXAMPLE 6-7: CODE EXAMPLE FOR USING SLAVE PLL WITH 8 MHz INTERNAL FRC

```
//code example for 60 MIPS system clock using 8MHz FRC

// Select FRC on POR
#pragma config S1FNOSC = FRC             // Oscillator Source Selection (Internal Fast RC (FRC))
#pragma config S1IESO = OFF              // Two-speed Oscillator Start-up Enable bit (Start up
                                            with user-selected oscillator source)
// Enable Clock Switching
#pragma config S1FCKSM = CSECMD

int     main()
{
        // Configure PLL prescaler, both PLL postscalers, and PLL feedback divider
        CLKDIVbits.PLLPRE = 1;           // N1=1
        PLLFBDbits.PLLFBDIV = 150;       // M = 150
        PLLDIVbits.POST1DIV = 5;         // N2=5
        PLLDIVbits.POST2DIV = 1;         // N3=1

        // Initiate Clock Switch to FRC with PLL (NOSC=0b001)
        __builtin_write_OSCCONH(0x01);
        __builtin_write_OSCCONL(OSCCON | 0x01);

        // Wait for Clock switch to occur
        while (OSCCONbits.OSWEN!= 0);
        // Wait for PLL to lock
        while (OSCCONbits.LOCK!= 1);
}
```

Note: *FPLLO = FPLLI * M/(N1 * N2 * N3); FPLLI = 8; M = 150; N1 = 1; N2 = 5; N3 = 1;* so *FPLLO = 10 * 100/(1 * 5 * 1) = 240 MHz* or *60 MIPS.*

11.2 Features Overview

- Four Rail-to-Rail Analog Comparators
- Up to Five Selectable Input Sources per Comparator:
  - Three external inputs
  - Two internal inputs from PGA module
- Programmable Comparator Hysteresis
- Programmable Output Polarity
- Interrupt Generation Capability
- Dedicated Pulse Density Modulation DAC for each Analog Comparator:
  - PDM unit followed by a digitally controlled multimode multipole RC filter
- Multimode Multipole RC Output Filter:
  - Transition mode: Provides the fastest response
  - Fast mode: For tracking DAC slopes
  - Steady-State mode: Provides 12-bit resolution
- Slope Compensation along with each DAC:
  - Slope Generation mode
  - Hysteretic Control mode
  - Triangle Wave mode
- Functional Support for the High-Speed PWM module which Includes:
  - PWM duty cycle control
  - PWM period control
  - PWM Fault detect

11.3 DAC Control Registers

The DACCTRL1L and DACCTRL2H/L registers are common configuration registers for Master and Slave DAC modules. The Master and Slave DAC modules are controlled by separate sets of DACCTRL1/2 registers. The DACxCON, DACxDAT, SLPxCON and SLPxDAT registers specify the operation of individual modules. Note that x = 1 for the Master module and x = 1-3 for the Slave modules.

REGISTER 11-6: DACxDATH: DACx DATA HIGH REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DACDAT<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DACDAT<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared

bit 15-0 **DACDAT<15:0>:** DACx Data bits
This register specifies the high DACx data value.

REGISTER 11-7: DACxDATL: DACx DATA LOW REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DACLOW<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DACLOW<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared

bit 15-0 **DACLOW<15:0>:** DACx Low Data bits
In Hysteretic mode, Slope Generator mode and Triangle mode, this register specifies the low data value and/or limit for the DACx module.

REGISTER 12-2: QEIxIOCL: QEIx I/O CONTROL LOW REGISTER (CONTINUED)

bit 6 **IDXPOL:** INDXx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

bit 5 **QEBPOL:** QEBx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

bit 4 **QEAPOL:** QEAx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

bit 3 **HOME:** Status of HOMEx Input Pin after Polarity Control bit (read-only)
1 = Pin is at logic '1' if the HOMPOL bit is set to '0'; pin is at logic '0' if the HOMPOL bit is set to '1'
0 = Pin is at logic '0' if the HOMPOL bit is set to '0'; pin is at logic '1' if the HOMPOL bit is set to '1'

bit 2 **INDEX:** Status of INDXx Input Pin After Polarity Control bit (read-only)
1 = Pin is at logic '1' if the IDXPOL bit is set to '0'; pin is at logic '0' if the IDXPOL bit is set to '1'
0 = Pin is at logic '0' if the IDXPOL bit is set to '0'; pin is at logic '1' if the IDXPOL bit is set to '1'

bit 1 **QEB:** Status of QEBx Input Pin After Polarity Control and SWPAB Pin Swapping bit (read-only)
1 = Physical pin, QEBx, is at logic '1' if the QEBPOL bit is set to '0' and the SWPAB bit is set to '0';
physical pin, QEBx, is at logic '0' if the QEBPOL bit is set to '1' and the SWPAB bit is set to '0';
physical pin, QEAx, is at logic '1' if the QEBPOL bit is set to '0' and the SWPAB bit is set to '1';
physical pin, QEAx, is at logic '0' if the QEBPOL bit is set to '1' and the SWPAB bit is set to '1'
0 = Physical pin, QEBx, is at logic '0' if the QEBPOL bit is set to '0' and the SWPAB bit is set to '0';
physical pin, QEBx, is at logic '1' if the QEBPOL bit is set to '1' and the SWPAB bit is set to '0';
physical pin, QEAx, is at logic '0' if the QEBPOL bit is set to '0' and the SWPAB bit is set to '1';
physical pin, QEAx, is at logic '1' if the QEBPOL bit is set to '1' and the SWPAB bit is set to '1'

bit 0 **QEA:** Status of QEAx Input Pin After Polarity Control and SWPAB Pin Swapping bit (read-only)
1 = Physical pin, QEAx, is at logic '1' if the QEAPOL bit is set to '0' and the SWPAB bit is set to '0';
physical pin, QEAx, is at logic '0' if the QEAPOL bit is set to '1' and the SWPAB bit is set to '0';
physical pin, QEBx, is at logic '1' if the QEAPOL bit is set to '0' and the SWPAB bit is set to '1';
physical pin, QEBx, is at logic '0' if the QEAPOL bit is set to '1' and the SWPAB bit is set to '1'
0 = Physical pin, QEAx, is at logic '0' if the QEAPOL bit is set to '0' and the SWPAB bit is set to '0';
physical pin, QEAx, is at logic '1' if the QEAPOL bit is set to '1' and the SWPAB bit is set to '0';
physical pin, QEBx, is at logic '0' if the QEAPOL bit is set to '0' and the SWPAB bit is set to '1'

REGISTER 15-2: I2CxCONH: I2Cx CONTROL REGISTER HIGH

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6 **PCIE:** Stop Condition Interrupt Enable bit (I^2C Slave mode only).
1 = Enables interrupt on detection of Stop condition
0 = Stop detection interrupts are disabled

bit 5 **SCIE:** Start Condition Interrupt Enable bit (I^2C Slave mode only)
1 = Enables interrupt on detection of Start or Restart conditions
0 = Start detection interrupts are disabled

bit 4 **BOEN:** Buffer Overwrite Enable bit (I^2C Slave mode only)
1 = I2CxRCV is updated and an ACK is generated for a received address/data byte, ignoring the state of the I2COV bit only if RBF bit = 0
0 = I2CxRCV is only updated when I2COV is clear

bit 3 **SDAHT:** SDAx Hold Time Selection bit
1 = Minimum of 300 ns hold time on SDAx after the falling edge of SCLx
0 = Minimum of 100 ns hold time on SDAx after the falling edge of SCLx

bit 2 **SBCDE:** Slave Mode Bus Collision Detect Enable bit (I^2C Slave mode only)
If, on the rising edge of SCLx, SDAx is sampled low when the module is outputting a high state, the BCL bit is set and the bus goes Idle. This Detection mode is only valid during data and ACK transmit sequences.
1 = Enables Slave bus collision interrupts
0 = Slave bus collision interrupts are disabled

bit 1 **AHEN:** Address Hold Enable bit (I^2C Slave mode only)
1 = Following the 8th falling edge of SCLx for a matching received address byte; SCLREL bit (I2CxCONL<12>) will be cleared and the SCLx will be held low
0 = Address holding is disabled

bit 0 **DHEN:** Data Hold Enable bit (I^2C Slave mode only)
1 = Following the 8th falling edge of SCLx for a received data byte; Slave hardware clears the SCLREL bit (I2CxCONL<12>) and SCLx is held low
0 = Data holding is disabled

16.0 SINGLE-EDGE NIBBLE TRANSMISSION (SENT)

Note 1: This data sheet summarizes the features of this group of dsPIC33CH128MP508 family devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Single-Edge Nibble Transmission (SENT) Module"** (DS70005145) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 3.2 "Master Memory Organization"** in this data sheet for device-specific register and bit information.

3: This SENT module is available only on the Master.

Table 16-1 shows an overview of the SENT module.

TABLE 16-1: SENT MODULE OVERVIEW

	Number of SENT Modules	Identical (Modules)
Master Core	2	Yes
Slave Core	None	NA

16.1 Module Introduction

The Single-Edge Nibble Transmission (SENT) module is based on the SAE J2716, *"SENT – Single-Edge Nibble Transmission for Automotive Applications"*. The SENT protocol is a one-way, single wire time modulated serial communication, based on successive falling edges. It is intended for use in applications where high-resolution sensor data needs to be communicated from a sensor to an Engine Control Unit (ECU).

The SENTx module has the following major features:

- Selectable Transmit or Receive mode
- Synchronous or Asynchronous Transmit modes
- Automatic Data Rate Synchronization
- Optional Automatic Detection of CRC Errors in Receive mode
- Optional Hardware Calculation of CRC in Transmit mode
- Support for Optional Pause Pulse Period
- Data Buffering for One Message Frame
- Selectable Data Length for Transmit/Receive from Three to Six Nibbles
- Automatic Detection of Framing Errors

SENT protocol timing is based on a predetermined time unit, TTICK. Both the transmitter and receiver must be preconfigured for TTICK, which can vary from 3 to 90 µs. A SENT message frame starts with a Sync pulse. The purpose of the Sync pulse is to allow the receiver to calculate the data rate of the message encoded by the transmitter. The SENT specification allows messages to be validated with up to a 20% variation in TTICK. This allows for the transmitter and receiver to run from different clocks that may be inaccurate, and drift with time and temperature. The data nibbles are four bits in length and are encoded as the data value + 12 ticks. This yields a 0 value of 12 ticks and the maximum value, 0xF, of 27 ticks.

A SENT message consists of the following:

- A synchronization/calibration period of 56 tick times
- A status nibble of 12-27 tick times
- Up to six data nibbles of 12-27 tick times
- A CRC nibble of 12-27 tick times
- An optional pause pulse period of 12-768 tick times

Figure 16-1 shows a block diagram of the SENTx module.

Figure 16-2 shows the construction of a typical 6-nibble data frame, with the numbers representing the minimum or maximum number of tick times for each section.

REGISTER 20-2: IBIASCONH: CURRENT BIAS GENERATOR 50 µA CURRENT SOURCE CONTROL HIGH REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	SHRSRCEN3	SHRSNKEN3	GENSRCEN3	GENSNKEN3	SRCEN3	SNKEN3
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	SHRSRCEN2	SHRSNKEN2	GENSRCEN2	GENSNKEN2	SRCEN2	SNKEN2
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **SHRSRCEN3:** Share Source Enable for Output #3 bit
1 = Sourcing Current Mirror mode is enabled (uses reference from another source)
0 = Sourcing Current Mirror mode is disabled

bit 12 **SHRSNKEN3:** Share Sink Enable for Output #3 bit
1 = Sinking Current Mirror mode is enabled (uses reference from another source)
0 = Sinking Current Mirror mode is disabled

bit 11 **GENSRCEN3:** Generated Source Enable for Output #3 bit
1 = Source generates the current source mirror reference
0 = Source does not generate the current source mirror reference

bit 10 **GENSNKEN3:** Generated Sink Enable for Output #3 bit
1 = Source generates the current source mirror reference
0 = Source does not generate the current source mirror reference

bit 9 **SRCEN3:** Source Enable for Output #3 bit
1 = Current source is enabled
0 = Current source is disabled

bit 8 **SNKEN3:** Sink Enable for Output #3 bit
1 = Current sink is enabled
0 = Current sink is disabled

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **SHRSRCEN2:** Share Source Enable for Output #2 bit
1 = Sourcing Current Mirror mode is enabled (uses reference from another source)
0 = Sourcing Current Mirror mode is disabled

bit 4 **SHRSNKEN2:** Share Sink Enable for Output #2 bit
1 = Sinking Current Mirror mode is enabled (uses reference from another source)
0 = Sinking Current Mirror mode is disabled

bit 3 **GENSRCEN2:** Generated Source Enable for Output #2 bit
1 = Source generates the current source mirror reference
0 = Source does not generate the current source mirror reference

bit 2 **GENSNKEN2:** Generated Sink Enable for Output #2 bit
1 = Source generates the current source mirror reference
0 = Source does not generate the current source mirror reference

bit 1 **SRCEN2:** Source Enable for Output #2 bit
1 = Current source is enabled
0 = Current source is disabled

bit 0 **SNKEN2:** Sink Enable for Output #2 bit
1 = Current sink is enabled
0 = Current sink is disabled

FIGURE 24-17: UARTx MODULE I/O TIMING CHARACTERISTICS

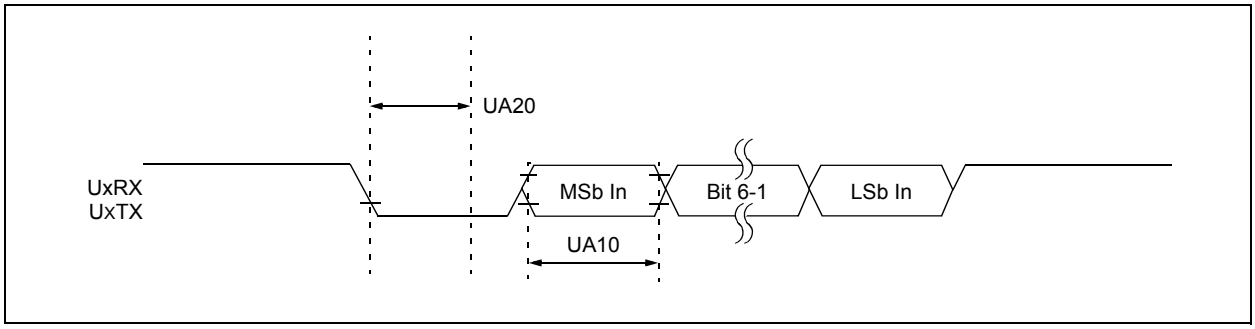


TABLE 24-42: UARTx MODULE I/O TIMING REQUIREMENTS

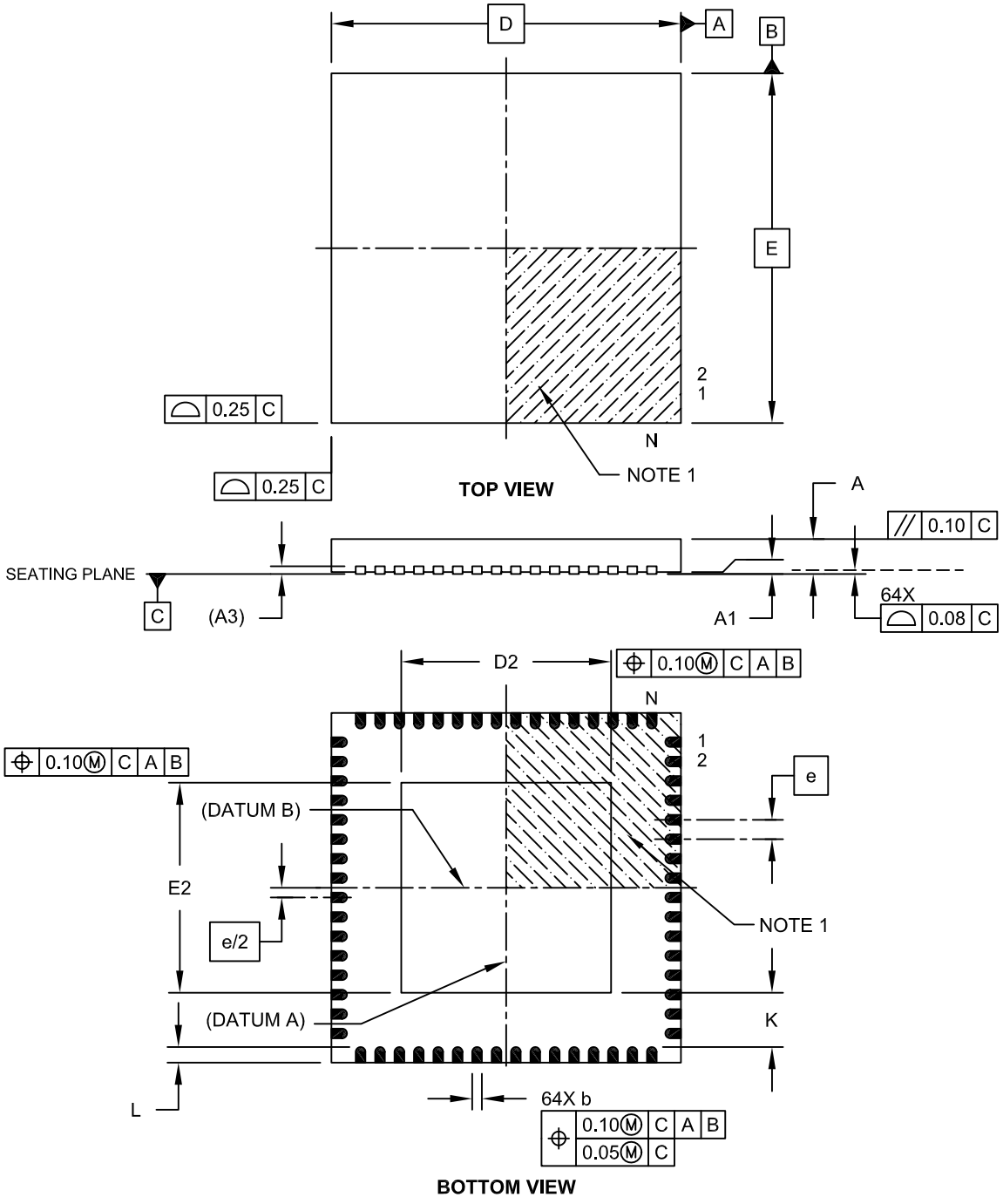
AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
UA10	TUABAUD	UARTx Baud Time	66.67	—	—	ns	
UA11	FBAUD	UARTx Baud Frequency	—	—	15	Mbps	
UA20	TCWF	Start Bit Pulse Width to Trigger UARTx Wake-up	500	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in “Typ.” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-154A Sheet 1 of 2