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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit Dual-Core
Speed	180MHz, 200MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	21
Program Memory Size	88KB (88K x 8)
Program Memory Type	FLASH, PRAM
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 23x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ch64mp502t-i-ss

3.0 MASTER MODULES

3.1 Master CPU

Note 1: This data sheet summarizes the features of the dsPIC33CH128MP508 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"dsPIC33E Enhanced CPU"** (DS70005158) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

There are two independent CPU cores in the dsPIC33CH128MP508 family. The Master and Slave cores are similar, except for the fact that the Slave core can run at a higher speed than the Master core.

The Slave core fetches instructions from the PRAM and the Master core fetches the code from the Flash. The Master and Slave cores can run independently asynchronously, at the same speed or at a different speed. This section discusses the Master core.

Note: All of the associated register names are the same on the Master, as well as on the Slave. The Slave code will be developed in a separate project in MPLAB® X IDE with the device selection, dsPIC33CH128MP508**S1**, where the **S1** indicates the Slave device.

The dsPIC33CH128MP508 family CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for Digital Signal Processing (DSP). The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space.

An instruction prefetch mechanism helps maintain throughput and provides predictable execution. Most instructions execute in a single-cycle effective execution rate, with the exception of instructions that change the program flow, the double-word move (`MOV.D`) instruction, PSV accesses and the table instructions. Overhead-free program loop constructs are supported using the `DO` and `REPEAT` instructions, both of which are interruptible at any point.

3.1.1 REGISTERS

The dsPIC33CH128MP508 devices have sixteen, 16-bit Working registers in the programmer's model. Each of the Working registers can act as a Data, Address or Address Offset register. The 16th Working register (W15) operates as a Software Stack Pointer for interrupts and calls.

In addition, the dsPIC33CH128MP508 devices include four Alternate Working register sets, which consist of W0 through W14. The Alternate Working registers can be made persistent to help reduce the saving and restoring of register content during Interrupt Service Routines (ISRs). The Alternate Working registers can be assigned to a specific Interrupt Priority Level (IPL1 through IPL7) by configuring the CTXTx<2:0> bits in the FALTREG Configuration register. The Alternate Working registers can also be accessed manually by using the `CTXTSWP` instruction. The CCTXI<2:0> and MCTXI<2:0> bits in the CTXTSTAT register can be used to identify the current, and most recent, manually selected Working register sets.

3.1.2 INSTRUCTION SET

The instruction set for dsPIC33CH128MP508 devices has two classes of instructions: the MCU class of instructions and the DSP class of instructions. These two instruction classes are seamlessly integrated into the architecture and execute from a single execution unit. The instruction set includes many addressing modes and was designed for optimum C compiler efficiency.

TABLE 3-5: MASTER SFR BLOCK 100h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
Timers			INT1TMRH	15E	0000000000000000	MSI1MBX3D	1E0	0000000000000000
T1CON	100	0-0000000-00-00-	INT1HLDL	160	0000000000000000	MSI1MBX4D	1E2	0000000000000000
TMR1	104	0000000000000000	INT1HLDH	162	0000000000000000	MSI1MBX5D	1E4	0000000000000000
PR1	108	0000000000000000	INDX1CNTL	164	0000000000000000	MSI1MBX6D	1E6	0000000000000000
QEI			INDX1CNTH	166	0000000000000000	MSI1MBX7D	1E8	0000000000000000
QEI1CON	140	0000000000000000	INDX1HLDL	168	0000000000000000	MSI1MBX8D	1EA	0000000000000000
QEI1IOCL	144	0000000000000xxxx	INDX1HLDH	16A	0000000000000000	MSI1MBX9D	1EC	0000000000000000
QEI1IOCH	146	---------------0	QEI1GECL	16C	0000000000000000	MSI1MBX10D	1EE	0000000000000000
QEI1STAT	148	--00000000000000	QEI1GECH	16E	0000000000000000	MSI1MBX11D	1F0	0000000000000000
POS1CNTL	14C	0000000000000000	QEI1LECL	170	0000000000000000	MSI1MBX12D	1F2	0000000000000000
POS1CNTH	14E	0000000000000000	QEI1LECH	172	0000000000000000	MSI1MBX13D	1F4	0000000000000000
POS1HLDL	150	0000000000000000	MSI1CON	1D2	0---xx0000000000	MSI1MBX14D	1F6	0000000000000000
POS1HLDH	152	0000000000000000	MSI1STAT	1D4	0000000000000000	MSI1MBX15D	1F8	0000000000000000
VEL1CNTL	154	0000000000000000	MSI1KEY	1D6	--------00000000	MSI1FIFOCS	1FA	0---00000---0000
VEL1CNTH	156	0000000000000000	MSI1MBXS	1D8	--------00000000	MRSWFDATA	1FC	0000000000000000
VEL1HLDL	158	0000000000000000	MSI1MBX0D	1DA	0000000000000000	MWSRFDATA	1FE	0000000000000000
VEL1HLDH	15A	0000000000000000	MSI1MBX1D	1DC	0000000000000000			
INT1TMRL	15C	0000000000000000	MSI1MBX2D	1DE	0000000000000000			

Legend: x = unknown or indeterminate value; "-" = unimplemented bits. Address and Reset values are in hexadecimal and binary, respectively.

REGISTER 3-17: CORCON: CORE CONTROL REGISTER(1)

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0
VAR	—	US1	US0	EDT	DL2	DL1	DL0
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R-0	R/W-0	R/W-0
SATA	SATB	SATDW	ACCSAT	IPL3(2)	SFA	RND	IF
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1'= Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **VAR:** Variable Exception Processing Latency Control bit
1 = Variable exception processing is enabled
0 = Fixed exception processing is enabled

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3(2)
1 = CPU Interrupt Priority Level is greater than 7
0 = CPU Interrupt Priority Level is 7 or less

Note 1: For complete register details, see Register 3-2.
2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

REGISTER 3-30: CNCONx: CHANGE NOTIFICATION CONTROL FOR PORTx REGISTER

R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
ON	—	—	—	CNSTYLE	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ON:** Change Notification (CN) Control for PORTx On bit
1 = CN is enabled
0 = CN is disabled

bit 14-12 **Unimplemented:** Read as '0'

bit 11 **CNSTYLE:** Change Notification Style Selection bit
1 = Edge style (detects edge transitions, CNFx<15:0> bits are used for a Change Notification event)
0 = Mismatch style (detects change from last port read, CNSTATx<15:0> bits are used for a Change Notification event)

bit 10-0 **Unimplemented:** Read as '0'

REGISTER 3-31: CNEN0x: INTERRUPT CHANGE NOTIFICATION ENABLE FOR PORTx REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNEN0x<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNEN0x<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **CNEN0x<15:0>:** Interrupt Change Notification Enable for PORTx bits
1 = Interrupt-on-change (from the last read value) is enabled for PORTx[n]
0 = Interrupt-on-change is disabled for PORTx[n]

REGISTER 3-67: RPINR47: PERIPHERAL PIN SELECT INPUT REGISTER 47

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCTRGR7	ADCTRGR6	ADCTRGR5	ADCTRGR4	ADCTRGR3	ADCTRGR2	ADCTRGR1	ADCTRGR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CLCINDR7	CLCINDR6	CLCINDR5	CLCINDR4	CLCINDR3	CLCINDR2	CLCINDR1	CLCINDR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **ADCTRGR<7:0>:** Assign ADC Trigger Input (ADCTRG) to the Corresponding RPn Pin bits
See Table 3-30.

bit 7-0 **CLCINDR<7:0>:** Assign CLC Input D (CLCIND) to the Corresponding RPn Pin bits
See Table 3-30.

REGISTER 3-110: C1TBCH: CAN TIME BASE COUNTER REGISTER HIGH(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TBC<31:24>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TBC<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **TBC<31:16>** CAN Time Base Counter bits
This is a free-running timer that increments every TBCPREx clock when TBCEN is set.

Note 1: The Time Base Counter (TBC) will be stopped and reset when TBCEN = 0 to save power.
2: The TBC prescaler count will be reset on any write to C1TBCH/L (TBCPREx will be unaffected).

REGISTER 3-111: C1TBCL: CAN TIME BASE COUNTER REGISTER LOW(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TBC<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TBC<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **TBC<15:0>** CAN Time Base Counter bits
This is a free-running timer that increments every TBCPREx clock when TBCEN is set.

Note 1: The TBC will be stopped and reset when TBCEN = 0 to save power.
2: The TBC prescaler count will be reset on any write to C1TBCH/L (TBCPREx will be unaffected).

FIGURE 4-1: dsPIC33CH128MP508S1 FAMILY (SLAVE) CPU BLOCK DIAGRAM

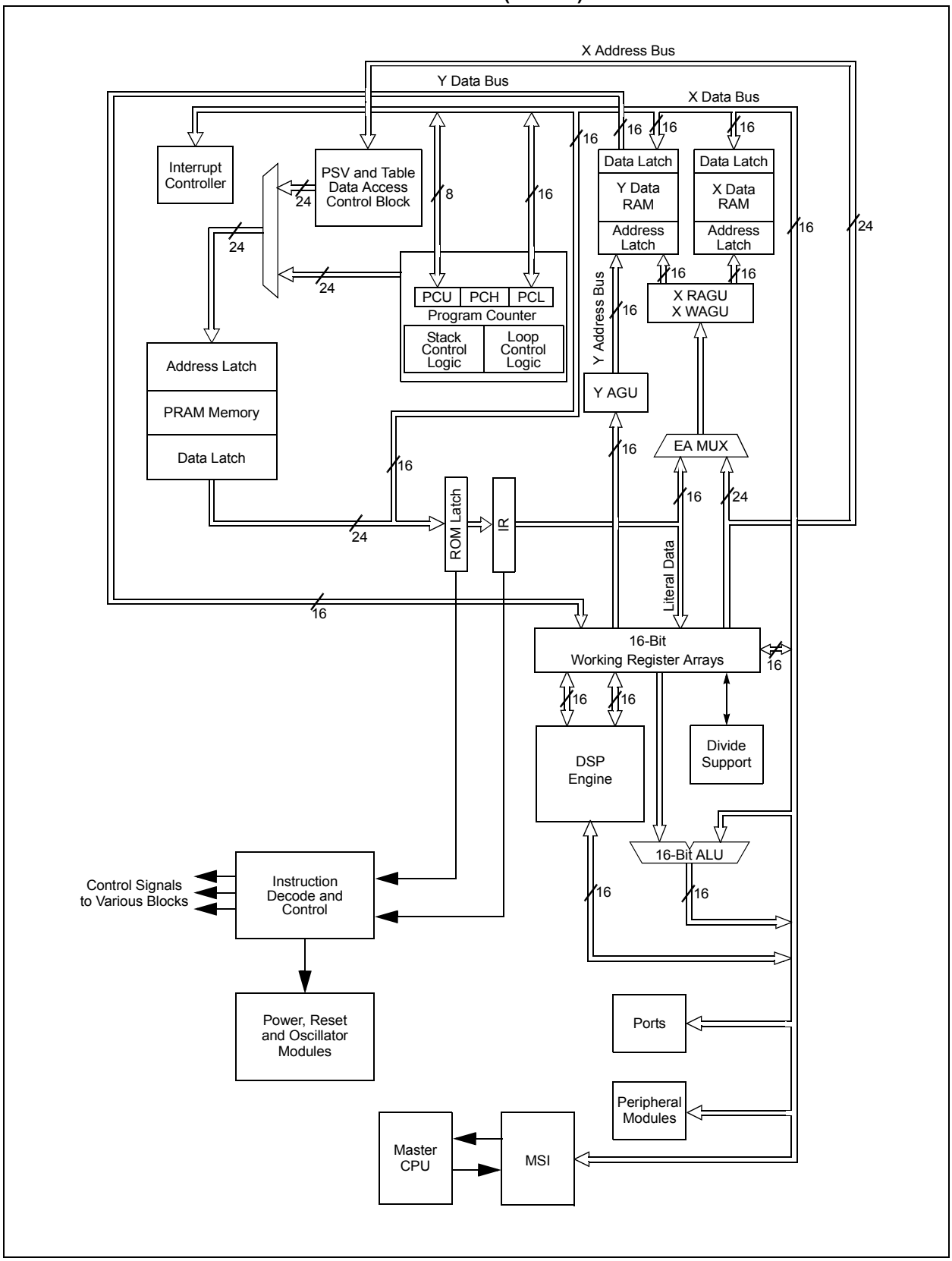


TABLE 4-14: SLAVE SFR BLOCK E00h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
I/O Ports (Continued)			CNEN0B	E2C	0000000000000000	CNPUD	E5E	0000000000000000
ANSELA	E00	----------1111-	CNSTATB	E2E	0000000000000000	CNPDD	E60	0000000000000000
TRISA	E02	----------11111	CNEN1B	E30	0000000000000000	CNCOND	E62	0---0----------
PORTA	E04	----------xxxxx	CNFB	E32	0000000000000000	CNEN0D	E64	0000000000000000
LATA	E06	----------xxxxx	ANSELC	E38	--------11--1111	CNSTATD	E66	0000000000000000
ODCA	E08	----------00000	TRISC	E3A	1111111111111111	CNEN1D	E68	0000000000000000
CNPUA	E0A	----------00000	PORTC	E3C	xxxxxxxxxxxxxxxx	CNFD	E6A	0000000000000000
CNPDA	E0C	----------00000	LATC	E3E	xxxxxxxxxxxxxxxx	ANSELE	E70	---------1------
CNEN0A	E10	----------00000	ODCC	E40	0000000000000000	TRISE	E72	1111111111111111
CNSTATA	E12	----------00000	CNPUC	E42	0000000000000000	PORTE	E74	xxxxxxxxxxxxxxxx
CNEN1A	E14	----------00000	CNPDC	E44	0000000000000000	LATE	E76	xxxxxxxxxxxxxxxx
CNFA	E16	----------00000	CNCONC	E46	0---0----------	ODCE	E78	0000000000000000
ANSELB	E1C	-------11--11111	CNEN0C	E48	0000000000000000	CNPUE	E7A	0000000000000000
TRISB	E1E	1111111111111111	CNSTATC	E4A	0000000000000000	CNPDE	E7C	0000000000000000
PORTB	E20	xxxxxxxxxxxxxxxx	CNEN1C	E4C	0000000000000000	CNCONE	E7E	0---0----------
LATB	E22	xxxxxxxxxxxxxxxx	CNFC	E4E	0000000000000000	CNEN0E	E80	0000000000000000
ODCB	E24	0000000000000000	ANSELD	E54	-11111----------	CNSTATE	E82	0000000000000000
CNPUB	E26	0000000000000000	TRISD	E56	1111111111111111	CNEN1E	E84	0000000000000000
CNPDB	E28	0000000000000000	PORTD	E58	xxxxxxxxxxxxxxxx	CNFE	E86	0000000000000000
CNEN0A	E10	----------00000	LATD	E5A	xxxxxxxxxxxxxxxx			
CNCONB	E2A	0---0----------	ODCD	E5C	0000000000000000			

Legend: x = unknown or indeterminate value; "-" = unimplemented bits. Address and Reset values are in hexadecimal and binary, respectively.

TABLE 4-15: SLAVE SFR BLOCK F00h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
Reset			PMD1	FA4	----000-00000-00	REFOTRIML	FBC	0000000000000000
RCON	F80	00--x-0000000011	PMD2	FA6	--------00000000	REFOTRIMH	FBE	----------------
Oscillator			PMD4	FAA	------------0---	PCTRAPL	FBF	0000000000000000
OSCCON	F84	-000-xxx0-0-0--0	PMD6	FAE	--000000--------	PCTRAPL	FC0	0000000000000000
CLKDIV	F86	00110000--000001	PMD7	FB0	-------x----0---	PCTRAPH	FC2	--------00000000
PLLFBD	F88	----000010010110	PMD8	FB2	---00--0--xx000-			
PLLDIV	F8A	------00-011-001	**WDT**					
APLLFBD1	F90	----000010010110	WDTCONL	FB4	0--0000000000000			
APLLDIV1	F92	------00-011-001	WDTCONH	FB6	0000000000000000			
PMD			REFOCONL	FB8	0-000-00----0000			
PMDCON	FA0	----0----------	REFOCONH	FBA	-000000000000000			

Legend: x = unknown or indeterminate value; "-" = unimplemented bits. Reset and address values are in hexadecimal.

REGISTER 7-2: PMD1: MASTER PERIPHERAL MODULE DISABLE 1 CONTROL REGISTER LOW

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0
—	—	—	—	T1MD	QEIMD	PWMMD	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	C1MD	ADC1MD
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11 **T1MD:** Timer1 Module Disable bit
1 = Timer1 module is disabled
0 = Timer1 module is enabled

bit 10 **QEIMD:** QEI Module Disable bit
1 = QEI module is disabled
0 = QEI module is enabled

bit 9 **PWMMD:** PWM Module Disable bit
1 = PWM module is disabled
0 = PWM module is enabled

bit 8 **Unimplemented:** Read as '0'

bit 7 **I2C1MD:** I2C1 Module Disable bit
1 = I2C1 module is disabled
0 = I2C1 module is enabled

bit 6 **U2MD:** UART2 Module Disable bit
1 = UART2 module is disabled
0 = UART2 module is enabled

bit 5 **U1MD:** UART1 Module Disable bit
1 = UART1 module is disabled
0 = UART1 module is enabled

bit 4 **SPI2MD:** SPI2 Module Disable bit
1 = SPI2 module is disabled
0 = SPI2 module is enabled

bit 3 **SPI1MD:** SPI1 Module Disable bit
1 = SPI1 module is disabled
0 = SPI1 module is enabled

bit 2 **Unimplemented:** Read as '0'

bit 1 **C1MD:** CAN1 Module Disable bit
1 = CAN1 module is disabled
0 = CAN1 module is enabled

bit 0 **ADC1MD:** ADC Module Disable bit
1 = ADC module is disabled
0 = ADC module is enabled

8.0 DIRECT MEMORY ACCESS (DMA) CONTROLLER

Note 1: This data sheet summarizes the features of this group of dsPIC33 devices. It is not intended to be a comprehensive reference source. For more information, refer to **"Direct Memory Access Controller (DMA)"** (DS39742) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: The DMA is identical for both Master core and Slave core. The x is common for both Master and Slave (where the x represents the number of the specific module being addressed).

3: All associated register names are the same on the Master core and the Slave core. The Slave code will be developed in a separate project in MPLAB® X IDE with the device selection, dsPIC33CH128MP508**S1**, where **S1** indicates the Slave device.

Table 8-1 shows an overview of the DMA module.

TABLE 8-1: DMA MODULE OVERVIEW

	Number of DMA Modules	Identical (Modules)
Master Core	6	Yes
Slave Core	2	Yes

The Direct Memory Access (DMA) Controller is designed to service high data throughput peripherals operating on the SFR bus, allowing them to access data memory directly and alleviating the need for CPU-intensive management. By allowing these data-intensive peripherals to share their own data path, the main data bus is also deloaded, resulting in additional power savings.

The DMA Controller functions both as a peripheral and a direct extension of the CPU. It is located on the microcontroller data bus, between the CPU and DMA-enabled peripherals, with direct access to SRAM. This partitions the SFR bus into two buses, allowing the DMA Controller access to the DMA-capable peripherals located on the new DMA SFR bus. The controller serves as a Master device on the DMA SFR bus, controlling data flow from DMA-capable peripherals.

The controller also monitors CPU instruction processing directly, allowing it to be aware of when the CPU requires access to peripherals on the DMA bus and automatically relinquishing control to the CPU as needed. This increases the effective bandwidth for handling data without DMA operations, causing a processor Stall. This makes the controller essentially transparent to the user.

The DMA Controller has these features:

- A Total of Eight (Six Master, Two Slave), Independently Programmable Channels
- Concurrent Operation with the CPU (no DMA caused Wait states)
- DMA Bus Arbitration
- Five Programmable Address modes
- Four Programmable Transfer modes
- Four Flexible Internal Data Transfer modes
- Byte or Word Support for Data Transfer
- 16-Bit Source and Destination Address Register for each Channel, Dynamically Updated and Reloadable
- 16-Bit Transaction Count Register, Dynamically Updated and Reloadable
- Upper and Lower Address Limit Registers
- Counter Half-Full Level Interrupt
- Software Triggered Transfer
- Null Write mode for Symmetric Buffer Operations

A simplified block diagram of the DMA Controller is shown if Figure 8-1.

REGISTER 8-2: DMACHn: DMA CHANNEL n CONTROL REGISTER

U-0	U-0	U-0	r-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	NULLW	RELOAD(1)	CHREQ(3)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SAMODE1	SAMODE0	DAMODE1	DAMODE0	TRMODE1	TRMODE0	SIZE	CHEN
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **Reserved:** Maintain as '0'

bit 11 **Unimplemented:** Read as '0'

bit 10 **NULLW:** Null Write Mode bit
1 = A dummy write is initiated to DMASRCn for every write to DMADSTn
0 = No dummy write is initiated

bit 9 **RELOAD:** Address and Count Reload bit(1)
1 = DMASRCn, DMADSTn and DMACNTn registers are reloaded to their previous values upon the start of the next operation
0 = DMASRCn, DMADSTn and DMACNTn are not reloaded on the start of the next operation(2)

bit 8 **CHREQ:** DMA Channel Software Request bit(3)
1 = A DMA request is initiated by software; automatically cleared upon completion of a DMA transfer
0 = No DMA request is pending

bit 7-6 **SAMODE<1:0>:** Source Address Mode Selection bits
11 = DMASRCn is used in Peripheral Indirect Addressing and remains unchanged
10 = DMASRCn is decremented based on the SIZE bit after a transfer completion
01 = DMASRCn is incremented based on the SIZE bit after a transfer completion
00 = DMASRCn remains unchanged after a transfer completion

bit 5-4 **DAMODE<1:0>:** Destination Address Mode Selection bits
11 = DMADSTn is used in Peripheral Indirect Addressing and remains unchanged
10 = DMADSTn is decremented based on the SIZE bit after a transfer completion
01 = DMADSTn is incremented based on the SIZE bit after a transfer completion
00 = DMADSTn remains unchanged after a transfer completion

bit 3-2 **TRMODE<1:0>:** Transfer Mode Selection bits
11 = Repeated Continuous
10 = Continuous
01 = Repeated One-Shot
00 = One-Shot

bit 1 **SIZE:** Data Size Selection bit
1 = Byte (8-bit)
0 = Word (16-bit)

bit 0 **CHEN:** DMA Channel Enable bit
1 = The corresponding channel is enabled
0 = The corresponding channel is disabled

Note 1: Only the original DMACNTn is required to be stored to recover the original DMASRCn and DMADSTn values.
2: DMACNTn will always be reloaded in Repeated mode transfers, regardless of the state of the RELOAD bit.
3: The number of transfers executed while CHREQ is set depends on the configuration of TRMODE<1:0>.

REGISTER 16-3: SENTxDATL: SENTx RECEIVE DATA REGISTER LOW(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATA4<3:0>				DATA5<3:0>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATA6<3:0>				CRC<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **DATA4<3:0>:** Data Nibble 4 Data bits

bit 11-8 **DATA5<3:0>:** Data Nibble 5 Data bits

bit 7-4 **DATA6<3:0>:** Data Nibble 6 Data bits

bit 3-0 **CRC<3:0>:** CRC Nibble Data bits

Note 1: Register bits are read-only in Receive mode (RCVEN = 1). In Transmit mode, the CRC<3:0> bits are read-only when automatic CRC calculation is enabled (RCVEN = 0, CRCEN = 1).

REGISTER 16-4: SENTxDATH: SENTx RECEIVE DATA REGISTER HIGH(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STAT<3:0>				DATA1<3:0>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATA2<3:0>				DATA3<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **STAT<3:0>:** Status Nibble Data bits

bit 11-8 **DATA1<3:0>:** Data Nibble 1 Data bits

bit 7-4 **DATA2<3:0>:** Data Nibble 2 Data bits

bit 3-0 **DATA3<3:0>:** Data Nibble 3 Data bits

Note 1: Register bits are read-only in Receive mode (RCVEN = 1). In Transmit mode, the CRC<3:0> bits are read-only when automatic CRC calculation is enabled (RCVEN = 0, CRCEN = 1).

REGISTER 21-2: FBSLIM CONFIGURATION REGISTER

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

U-1	U-1	U-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
—	—	—	BSLIM<12:8>				
bit 15							bit 8

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
BSLIM<7:0>							
bit 7							bit 0

Legend:	PO = Program Once bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-13 **Unimplemented:** Read as ‘1’

bit 12-0 **BSLIM<12:0>:** Boot Segment Code Flash Page Address Limit bits

Contains the page address of the first active General Segment page. The value to be programmed is the inverted page address, such that programming additional ‘0’s can only increase the Boot Segment size.

REGISTER 21-3: FSIGN CONFIGURATION REGISTER

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

r-0	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 15							bit 8

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:	r = Reserved bit	PO = Program Once bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-16 **Unimplemented:** Read as ‘1’

bit 15 **Reserved:** Maintain as ‘0’

bit 14-0 **Unimplemented:** Read as ‘1’

24.1 DC Characteristics

TABLE 24-1: OPERATING MIPS vs. VOLTAGE

Characteristic	VDD Range (in Volts)	Temperature Range (in °C)	Maximum MIPS dsPIC33CH128MP508 Family	
			Master	Slave
—	3.0V to 3.6V	-40°C to +85°C	90	100
	3.0V to 3.6V	-40°C to +125°C	90	100

TABLE 24-2: THERMAL OPERATING CONDITIONS

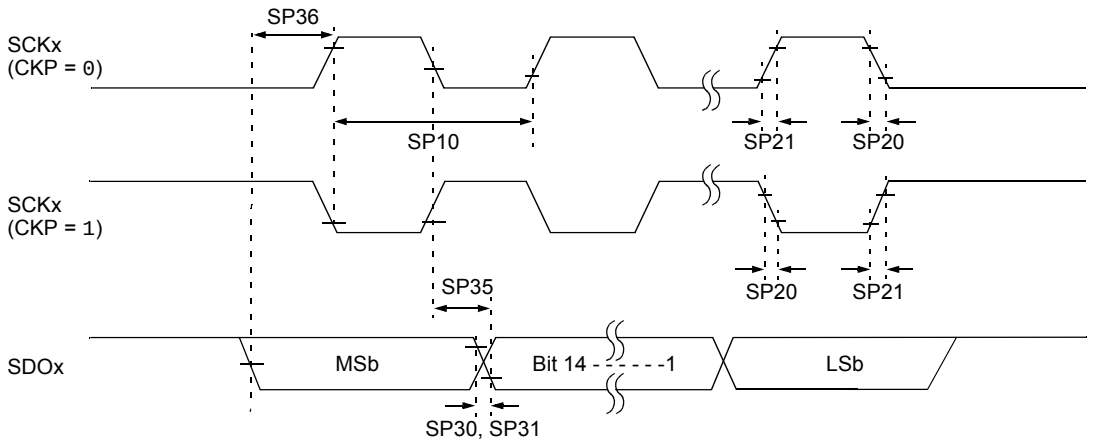
Rating	Symbol	Min.	Typ.	Max.	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+125	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
Extended Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+140	°C
Operating Ambient Temperature Range	TA	-40	—	+125	°C
Power Dissipation: Internal Chip Power Dissipation: PINT = VDD x (IDD – Σ IOH) I/O Pin Power Dissipation: I/O = Σ ({VDD – VOH} x IOH) + Σ (VOL x IOL)	PD	PINT + PI/O			W
Maximum Allowed Power Dissipation	PDMAX	(TJ – TA)/θJA			W

TABLE 24-3: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Typ.	Max.	Unit	Notes
Package Thermal Resistance, 80-Pin TQFP 12x12x1 mm	θJA	50.67	—	°C/W	**1**
Package Thermal Resistance, 64-Pin TQFP 10x10x1 mm	θJA	45.7	—	°C/W	**1**
Package Thermal Resistance, 64-Pin QFN 9x9 mm	θJA	18.7	—	°C/W	**1**
Package Thermal Resistance, 48-Pin TQFP 7x7 mm	θJA	62.76	—	°C/W	**1**
Package Thermal Resistance, 48-Pin UQFN 6x6 mm	θJA	27.6	—	°C/W	**1**
Package Thermal Resistance, 36-Pin UQFN 5x5 mm	θJA	29.2	—	°C/W	**1**
Package Thermal Resistance, 28-Pin UQFN 6x6 mm	θJA	22.41	—	°C/W	**1**
Package Thermal Resistance, 28-Pin SSOP 5.30 mm	θJA	52.84	—	°C/W	**1**

Note 1: Junction to ambient thermal resistance, Theta-JA (θJA) numbers are achieved by package simulations.

FIGURE 24-8: SPIx MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 24-1 for load conditions.

TABLE 24-35: SPIx MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP10	FscP	Maximum SCKx Frequency	—	—	15	MHz	Using PPS pins
			—	—	40	MHz	SPI2 dedicated pins
SP20	TscF	SCKx Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 3)**
SP21	TscR	SCKx Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 3)**
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 3)**
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 3)**
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid After SCKx Edge	—	6	20	ns	
SP36	TdiV2scH, TdiV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	Using PPS pins
			3	—	—	ns	SPI2 dedicated pins

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column is at 3.3V, +25°C unless otherwise stated.

3: Assumes 50 pF load on all SPIx pins.

TABLE 24-43: ADC MODULE SPECIFICATIONS

Operating Conditions: 3.0V to 3.6V (unless otherwise stated)[4] Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended							
Param No.	**Symbol**	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
Analog Input							
AD12	VINH-VINL	Full-Scale Input Span	AVSS	—	AVDD	V	
AD14	VIN	Absolute Input Voltage	AVSS – 0.3	—	AVDD + 0.3	V	
AD17	RIN	Recommended Impedance of Analog Voltage Source	—	100	—	Ω	For minimum sampling time **(Note 1)**
AD66	VBG	Internal Voltage Reference Source	—	1.2	—	V	
ADC Accuracy							
AD20c	Nr	Resolution	12 data bits			bits	
AD21c	INL	Integral Nonlinearity	> -11.3	—	< 11.3	LSb	AVSS = 0V, AVDD = 3.3V
AD22c	DNL	Differential Nonlinearity	> -1.5	—	< 11.5	LSb	AVSS = 0V, AVDD = 3.3V
AD23c	GERR	Gain Error	> -12	—	< 12	LSb	AVSS = 0V, AVDD = 3.3V
AD24c	EOFF	Offset Error	> 7.5	—	< 7.5	LSb	AVSS = 0V, AVDD = 3.3V
Dynamic Performance							
AD31b	SINAD	Signal-to-Noise and Distortion	56	—	70	dB	**(Notes 2, 3)**
AD34b	ENOB	Effective Number of Bits	9	—	11.4	bits	**(Notes 2, 3)**

Note 1: These parameters are not characterized or tested in manufacturing.

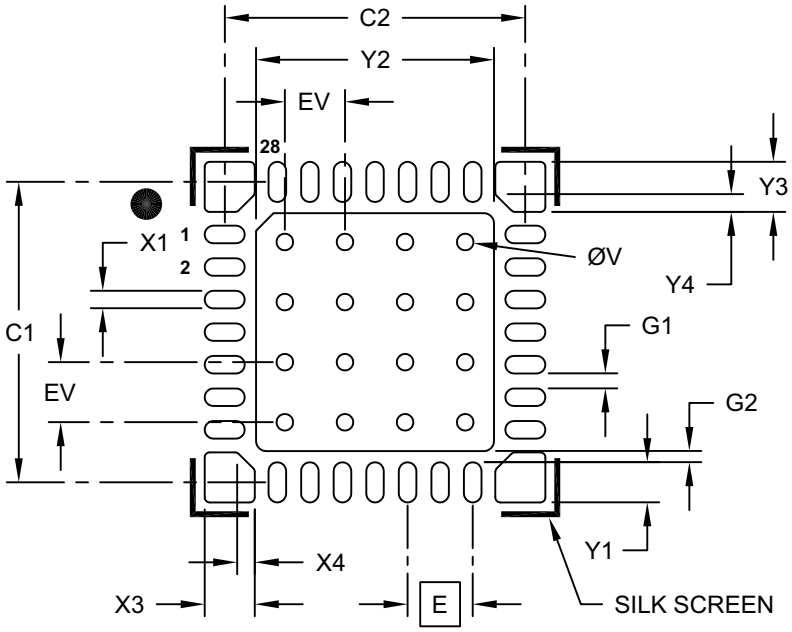
2: These parameters are characterized but not tested in manufacturing.

3: Characterized with a 1 kHz sine wave.

4: The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is ensured, but not characterized.

28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (2N) - 6x6x0.55 mm Body [UQFN] With 4.65x4.65 mm Exposed Pad and Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	X2			4.75
Optional Center Pad Length	Y2			4.75
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.35
Contact Pad Length (X28)	Y1			0.80
Corner Anchor (X4)	X3			1.00
Corner Anchor (X4)	Y3			1.00
Corner Anchor Chamfer (X4)	X4			0.35
Corner Anchor Chamfer (X4)	Y4			0.35
Contact Pad to Pad (X28)	G1	0.20		
Contact Pad to Center Pad (X28)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

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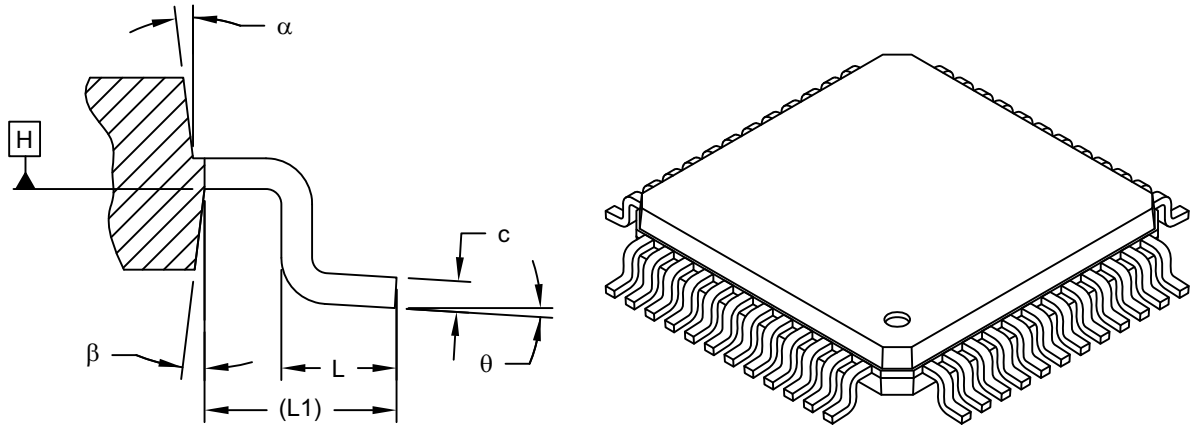
48-Lead Thin Quad Flatpack (PT) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A-A

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		48	
Lead Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.05	-	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		9.00 BSC	
Overall Length	D		9.00 BSC	
Molded Package Width	E1		7.00 BSC	
Molded Package Length	D1		7.00 BSC	
Lead Thickness	c	0.09	-	0.16
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A-B and D to be determined at center line between leads where leads exit plastic body at datum plane H

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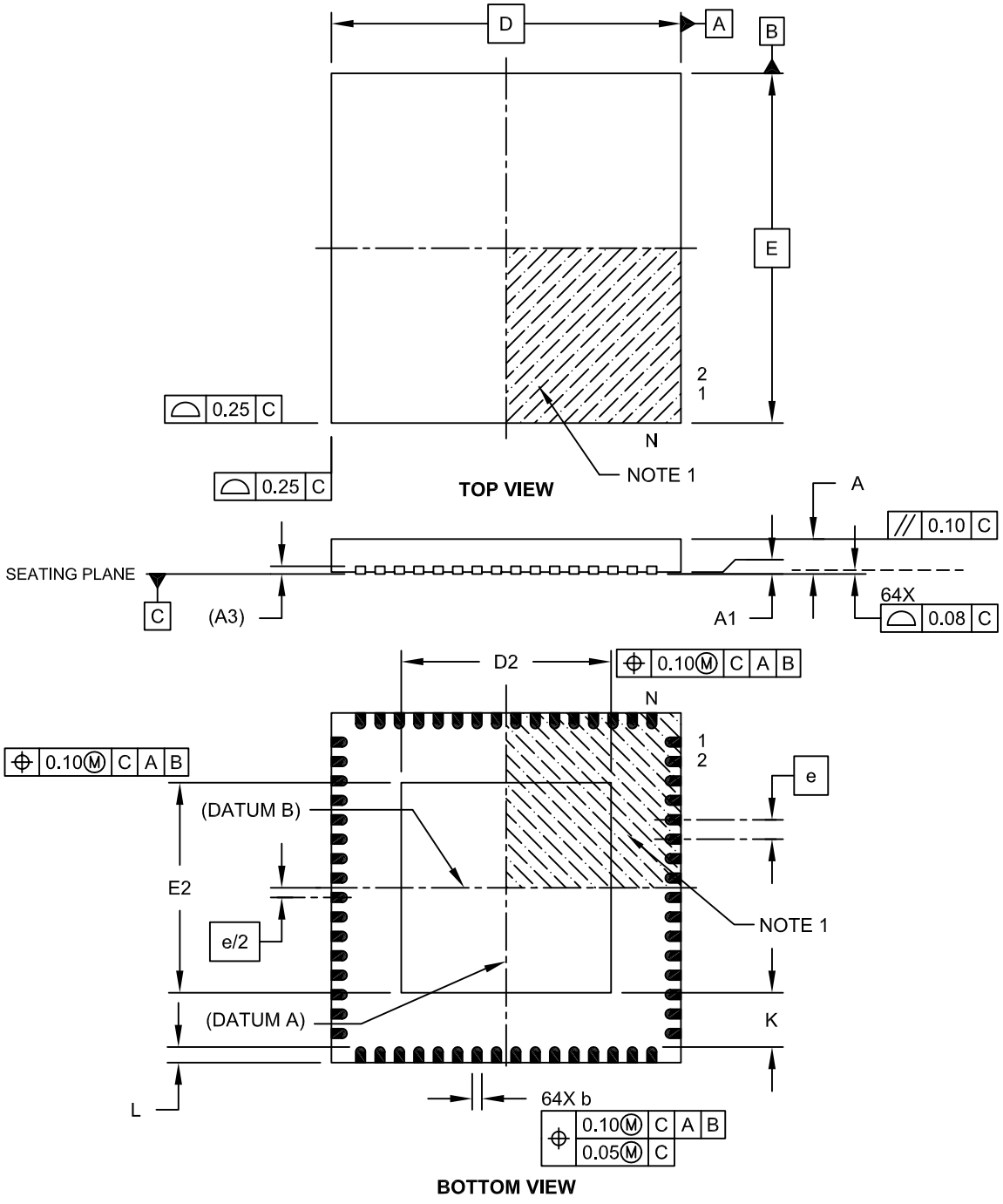
64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-154A Sheet 1 of 2

APPENDIX A: REVISION HISTORY

Revision A (August 2017)

This is the initial version of the document.

Revision B (June 2018)

This revision incorporates the following updates:

- Registers:
  - Updates Register 3-10, Register 3-13, Register 3-14, Register 3-15, Register 3-102, Register 3-103, Register 3-116, Register 3-117, Register 3-126, Register 3-127, Register 3-129, Register 3-132, Register 3-134, Register 3-135, Register 3-137, Register 3-138, Register 3-162, Register 3-196, Register 4-10, Register 4-11, Register 4-12, Register 4-13, Register 4-14, Register 4-15, Register 4-83 Register 4-86, Register 4-88, Register 10-1, Register 10-5, Register 11-1, Register 11-5, Register 15-3, Register 12-4, Register 12-15, Register 12-16, Register 12-23, Register 12-24, Register 18-3, Register 21-5, Register 21-14, Register 21-26, Register 21-33, Register 21-34, Register 21-35 and Register 21-37.
  - Deletes ADCSSL: ADC CVD Scan Select Register Low, FOSCSEL: Oscillator Source Selection Register, FOSC: Oscillator Configuration Register, FS1OSCSEL: Slave Oscillator Source Selection Register and FS1OSC: Slave Oscillator Configuration Register.
- Tables:
  - Updates Table 2, Table 3, Table 4, Table 5, Table 6, Table 7, Table 8, Table 9, Table 1-1, Table 3-4-Table 3-18 (adds additional information to the legend), Table 3-27, Table 3-35, Table 3-36, Table 3-37, Table 3-45, Table 4-3-Table 4-15 (adds additional information to the legend), Table 4-24, Table 4-33 through Table 4-37, Table 15-1, Table 21-2, Table 21-5, Table 22-2, Table 24-3, Table 24-5, Table 24-6, Table 24-7, Table 24-8, Table 24-9, Table 24-10, Table 24-11, Table 24-12, Table 24-13, Table 24-15, Table 24-16 Table 24-14, Table 24-17, Table 24-22, Table 24-29, Table 24-34-Table 24-40, Table 24-41, Table 24-44, Table 24-45 and Table 24-48.
  - Adds Table 24-13 through Table 24-17.
- Figures:
  - Updates Figure 3-24, Figure 3-26, Figure 4-7, Figure 4-20, Figure 14-5, Figure 14-6, Figure 14-7, Figure 14-8, Figure 20-1, Figure 21-2 and Figure .
- Sections:
  - Adds **"Referenced Sources"** section to front matter.
- Miscellaneous:
  - Adds headings to all SFR and Register tables.
  - Adds Error Correcting Code (ECC) information.
  - Adds the 48-Lead UQFN package to the document.
  - Removes External Count with External Gate information.