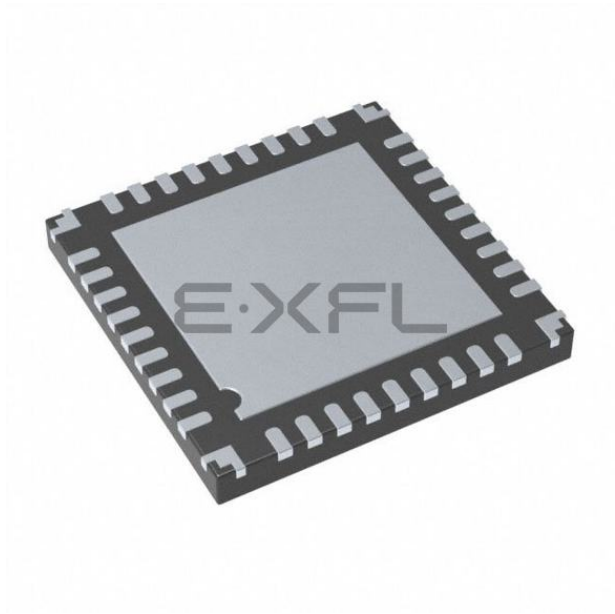
Microchip Technology - DSPIC33CH64MP503T-I/M5 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit Dual-Core
Speed	180MHz, 200MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	27
Program Memory Size	88KB (88K x 8)
Program Memory Type	FLASH, PRAM
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-UFQFN Exposed Pad
Supplier Device Package	36-UQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ch64mp503t-i-m5

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TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name(1)	Pin Type	Buffer Type	PPS	Description
U1CTS/S1U1CTS(3)	I	ST	Yes	UART1 Clear-to-Send
U1RTS/S1U1RTS(3)	O	—	Yes	UART1 Request-to-Send
U1RX/S1U1RX(3)	I	ST	Yes	UART1 receive
U1TX/S1U1TX(3)	O	—	Yes	UART1 transmit
U1DSR/S1U1DSR	I	ST	Yes	UART1 Data-Set-Ready
U1DTR/S1U1DTR	O	—	Yes	UART1 Data-Terminal-Ready
U2CTS	I	ST	Yes	UART2 Clear-to-Send
U2RTS	O	—	Yes	UART2 Request-to-Send
U2RX	I	ST	Yes	UART2 receive
U2TX	O	—	Yes	UART2 transmit
U2DSR	I	ST	Yes	UART2 Data-Set-Ready
U2DTR	O	—	Yes	UART2 Data-Terminal-Ready
SENT1	I	ST	Yes	SENT1 input
SENT2	I	ST	Yes	SENT2 input
SENT1OUT	O	—	Yes	SENT1 output
SENT2OUT	O	—	Yes	SENT2 output
PTGTRG24	O	—	Yes	PTG Trigger Output 24
PTGTRG25	O	—	Yes	PTG Trigger Output 25
TCKI1-TCKI8/ S1TCKI1-S1TCKI4(3)	I	ST	Yes	SCCP Timer Inputs 1 through 8/1 through 4
ICM1-ICM8/ S1ICM1-S1ICM4(3)	I	ST	Yes	SCCP Capture Inputs 1 through 8/1 through 4
OCFA-OCFB/ S1OCFA-S1OCFB(3)	I	ST	Yes	SCCP Fault Inputs A through B
OCM1-OCM8/ S1OCM1-S1OCM4(3)	O	—	Yes	SCCP Compare Outputs 1 through 8/1 through 4
SCK1/S1SCK1(3)	I/O	ST	Yes	Synchronous serial clock input/output for SPI1
SDI1/S1SDI1(3)	I	ST	Yes	SPI1 data in
SDO1/S1SDO1(3)	O	—	Yes	SPI1 data out
SS1/S1SS1(3)	I/O	ST	Yes	SPI1 Slave synchronization or frame pulse I/O
SCK2	I/O	ST	Yes	Synchronous serial clock input/output for SPI2
SDI2	I	ST	Yes	SPI2 data in
SDO2	O	—	Yes	SPI2 data out
SS2	I/O	ST	Yes	SPI2 Slave synchronization or frame pulse I/O
SCL1/S1SCL1(3)	I/O	ST	No	Synchronous serial clock input/output for I2C1
SDA1/S1SDA1(3)	I/O	ST	No	Synchronous serial data input/output for I2C1
ASCL1	I/O	ST	No	Alternate synchronous serial clock input/output for I2C1
ASDA1	I/O	ST	No	Alternate synchronous serial data input/output for I2C1
SCL2	I/O	ST	No	Synchronous serial clock input/output for I2C2
SDA2	I/O	ST	No	Synchronous serial data input/output for I2C2
ASCL2	I/O	ST	No	Alternate synchronous serial clock input/output for I2C2
ASDA2	I/O	ST	No	Alternate synchronous serial data input/output for I2C2

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

Note 1: Not all pins are available in all package variants. See the **"Pin Diagrams"** section for pin availability.

2: These pins are remappable as well as dedicated. Some of the pins are associated with the Slave function and have S1 attached to the beginning of the name. For example, AN0 for the Slave is S1AN0.

3: S1 attached to the beginning of the name indicates the Slave feature for that function. For example, AN0 for the Slave is S1AN0.

3.0 MASTER MODULES

3.1 Master CPU

Note 1: This data sheet summarizes the features of the dsPIC33CH128MP508 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"dsPIC33E Enhanced CPU"** (DS70005158) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

There are two independent CPU cores in the dsPIC33CH128MP508 family. The Master and Slave cores are similar, except for the fact that the Slave core can run at a higher speed than the Master core.

The Slave core fetches instructions from the PRAM and the Master core fetches the code from the Flash. The Master and Slave cores can run independently asynchronously, at the same speed or at a different speed. This section discusses the Master core.

Note: All of the associated register names are the same on the Master, as well as on the Slave. The Slave code will be developed in a separate project in MPLAB® X IDE with the device selection, dsPIC33CH128MP508**S1**, where the **S1** indicates the Slave device.

The dsPIC33CH128MP508 family CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for Digital Signal Processing (DSP). The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space.

An instruction prefetch mechanism helps maintain throughput and provides predictable execution. Most instructions execute in a single-cycle effective execution rate, with the exception of instructions that change the program flow, the double-word move (`MOV.D`) instruction, PSV accesses and the table instructions. Overhead-free program loop constructs are supported using the `DO` and `REPEAT` instructions, both of which are interruptible at any point.

3.1.1 REGISTERS

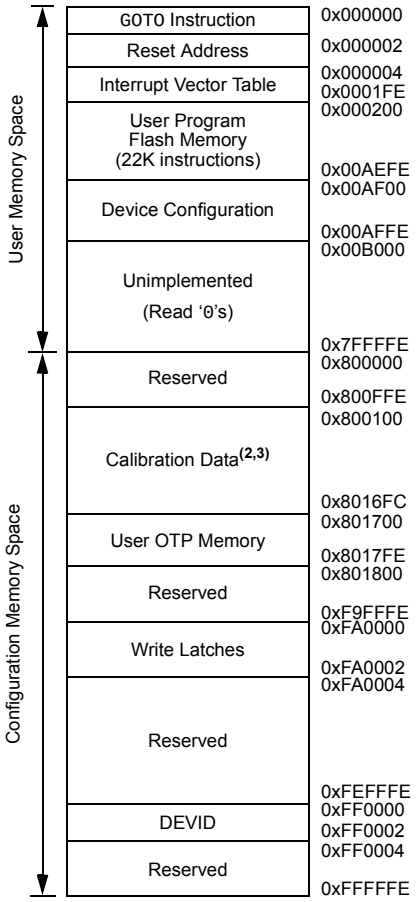
The dsPIC33CH128MP508 devices have sixteen, 16-bit Working registers in the programmer's model. Each of the Working registers can act as a Data, Address or Address Offset register. The 16th Working register (W15) operates as a Software Stack Pointer for interrupts and calls.

In addition, the dsPIC33CH128MP508 devices include four Alternate Working register sets, which consist of W0 through W14. The Alternate Working registers can be made persistent to help reduce the saving and restoring of register content during Interrupt Service Routines (ISRs). The Alternate Working registers can be assigned to a specific Interrupt Priority Level (IPL1 through IPL7) by configuring the CTXTx<2:0> bits in the FALTREG Configuration register. The Alternate Working registers can also be accessed manually by using the `CTXTSWP` instruction. The CCTXI<2:0> and MCTXI<2:0> bits in the CTXTSTAT register can be used to identify the current, and most recent, manually selected Working register sets.

3.1.2 INSTRUCTION SET

The instruction set for dsPIC33CH128MP508 devices has two classes of instructions: the MCU class of instructions and the DSP class of instructions. These two instruction classes are seamlessly integrated into the architecture and execute from a single execution unit. The instruction set includes many addressing modes and was designed for optimum C compiler efficiency.

FIGURE 3-4: PROGRAM MEMORY MAP FOR MASTER dsPIC33CH64MPXXX DEVICES(1)



Note 1: Memory areas are not shown to scale.

2: Calibration data area must be maintained during programming.

3: Calibration data area includes UDID locations.

TABLE 3-10: MASTER SFR BLOCK 700h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
CAN FD (Continued)			C1FLTOBJ15L	6F8	0000000000000000	C1MASK15H	6FE	-000000000000000
C1MASK14L	6F4	0000000000000000	C1FLTOBJ15H	6FA	-000000000000000			
C1MASK14H	6F6	-000000000000000	C1MASK15L	6FC	0000000000000000			

Legend: x = unknown or indeterminate value; "-" = unimplemented bits. Address and Reset values are in hexadecimal and binary, respectively.

TABLE 3-11: MASTER SFR BLOCK 800h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
Interrupts			IPC3	846	-100-100-100-100	IPC33	882	-100-100-100-100
IFS0	800	0000000000-00000	IPC4	848	-100-100-100-100	IPC34	884	-100-100-100-100
IFS1	802	0000000000000000	IPC5	84A	-100-100-100-100	IPC35	886	---------100-100
IFS2	804	00000-00-00000--	IPC6	84C	-100-100-100-100	IPC35	886	---------100-100
IFS3	806	000--------00000	IPC7	84E	-100-100-100-100	IPC36	888	-----100--------
IFS4	808	--000----0000-00	IPC8	850	-100-100--------	IPC37	88A	-----100-100----
IFS5	80A	000000000000000-	IPC9	852	-----100-100-100	IPC38	88C	---------100-100
IFS6	80C	0000000000000000	IPC10	854	-100-----100-100	IPC39	88E	---------100----
IFS7	80E	0000000000000---	IPC11	856	-100-100-100-100	IPC42	894	-100-100-100-100
IFS8	810	--0000000000000-	IPC12	858	-100-100-100-100	IPC43	896	-100-100-100-100
IFS9	812	--0---00-00--0--	IPC13	85A	------------100	IPC44	898	-100-100-100-100
IFS10	814	00000000--------	IPC15	85E	-100-100-100----	IPC45	89A	------------100
IFS11	816	-00--------00000	IPC16	860	-100-----100-100	IPC47	89E	-----100-100----
IEC0	820	0000000000-00000	IPC17	862	-----100-100-100	INTCON1	8C0	000000000000000-
IEC1	822	0000000000000000	IPC18	864	-100----------	INTCON2	8C2	000----0----0000
IEC2	824	00000-00-00000--	IPC19	866	---------100-100	INTCON3	8C4	-------0---0---0
IEC3	826	000--------00000	IPC20	868	-100-100-100----	INTCON4	8C6	--------------00
IEC4	828	--000----0000-00	IPC21	86A	-100-100-100-100	INTTREG	8C8	000-000000000000
IEC5	82A	000000000000000-	IPC22	86C	-100-100-100-100	**Flash**		
IEC6	82C	0000000000000000	IPC23	86E	-100-100-100-100	NVMCON	8D0	0000--00----0000
IEC7	82E	0000000000000---	IPC24	870	-100-100-100-100	NVMADR	8D2	0000000000000000
IEC8	830	--0000000000000-	IPC25	872	-100-100-100-100	NVMADRU	8D4	--------00000000
IEC8	830	--0000000000000-	IPC26	874	-100-100-100-100	NVMKEY	8D6	--------00000000
IEC9	832	--0---00-00--0--	IPC27	876	-100-100-100-100	NVMSRCADRL	8D8	0000000000000000
IEC10	834	00000000------00	IPC28	878	-100----------	NVMSRCADRH	8DA	--------00000000
IEC11	836	-00--------00000	IPC29	87A	-100-100-100-100	**CBG**		
IPC0	840	-100-100-100-100	IPC30	87C	-100-100-100-100	BIASCON	8F0	--------0---0000
IPC1	842	-100-100-----100	IPC31	87E	-100-100-100-100	IBIASCONL	8F4	--000000--000000
IPC2	844	-100-100-100-100	IPC32	880	-100-100-100----	IBIASCONH	8F6	--000000--000000

Legend: x = unknown or indeterminate value; "-" = unimplemented bits. Address and Reset values are in hexadecimal and binary, respectively.

TABLE 3-23: MASTER INTERRUPT VECTOR DETAILS (CONTINUED)

Interrupt Source	Vector #	IRQ #	IVT Address	Interrupt Bit Location		
				Flag	Enable	Priority
ADCAN16 – ADC AN16 Interrupt	115	107	0x0000EA	IFS6<11>	IEC6<11>	IPC26<14:12>
ADCAN17 – ADC AN17 Interrupt	116	108	0x0000EC	IFS6<12>	IEC6<12>	IPC27<2:0>
ADCAN18 – ADC AN18 Interrupt	117	109	0x0000EE	IFS6<13>	IEC6<13>	IPC27<6:4>
ADCAN19 – ADC AN19 Interrupt	118	110	0x0000F0	IFS6<14>	IEC6<14>	IPC27<10:8>
ADCAN20 – ADC AN20 Interrupt	119	111	0x0000F2	IFS6<15>	IEC6<15>	IPC27<14:12>
Reserved	120-122	112-114	0x0000F4-0x0000F8	—	—	—
ADFLT – ADC Fault	123	115	0x0000FA	IFS7<3>	IEC7<3>	IPC28<14:12>
ADCMP0 – ADC Digital Comparator 0	124	116	0x0000FC	IFS7<4>	IEC7<4>	IPC29<2:0>
ADCMP1 – ADC Digital Comparator 1	125	117	0x0000FE	IFS7<5>	IEC7<5>	IPC29<6:4>
ADCMP2 – ADC Digital Comparator 2	126	118	0x000100	IFS7<6>	IEC7<6>	IPC29<10:8>
ADCMP3 – ADC Digital Comparator 3	127	119	0x000102	IFS7<7>	IEC7<7>	IPC29<14:12>
ADFLTR0 – ADC Oversample Filter 0	128	120	0x000104	IFS7<8>	IEC7<8>	IPC30<2:0>
ADFLTR1 – ADC Oversample Filter 1	129	121	0x000106	IFS7<9>	IEC7<9>	IPC30<6:4>
ADFLTR2 – ADC Oversample Filter 2	130	122	0x000108	IFS7<10>	IEC7<10>	IPC30<10:8>
ADFLTR3 – ADC Oversample Filter 3	131	123	0x00010A	IFS7<11>	IEC7<11>	IPC30<14:12>
CLC1P – CLC1 Positive Edge	132	124	0x00010C	IFS7<12>	IEC7<12>	IPC31<2:0>
CLC2P – CLC2 Positive Edge	133	125	0x00010E	IFS7<13>	IEC7<13>	IPC31<6:4>
SPI1G – SPI1 Error	134	126	0x000110	IFS7<14>	IEC7<14>	IPC31<10:8>
SPI2G – SPI2 Error	135	127	0x000112	IFS7<15>	IEC7<15>	IPC31<14:12>
Reserved	136	128	0x000114	—	—	—
MSIS1 – MSI Slave Initiated Interrupt	137	129	0x000116	IFS8<1>	IEC8<1>	IPC32<6:4>
MSIA – MSI Protocol A	138	130	0x000118	IFS8<2>	IEC8<2>	IPC32<10:8>
MSIB – MSI Protocol B	139	131	0x00011A	IFS8<3>	IEC8<3>	IPC32<14:12>
MSIC – MSI Protocol C	140	132	0x00011C	IFS8<4>	IEC8<4>	IPC33<2:0>
MSID – MSI Protocol D	141	133	0x00011E	IFS8<5>	IEC8<5>	IPC33<6:4>
MSIE – MSI Protocol E	142	134	0x000120	IFS8<6>	IEC8<6>	IPC33<10:8>
MSIF – MSI Protocol F	143	135	0x000122	IFS8<7>	IEC8<7>	IPC33<14:12>
MSIG – MSI Protocol G	144	136	0x000124	IFS8<8>	IEC8<8>	IPC34<2:0>
MSIH – MSI Protocol H	145	137	0x000126	IFS8<9>	IEC8<9>	IPC34<6:4>
MSIDT – Master Read FIFO Data Ready	146	138	0x000128	IFS8<10>	IEC8<10>	IPC34<10:8>
MSIWFE – Master Write FIFO Empty	147	139	0x00012A	IFS8<11>	IEC8<11>	IPC34<14:12>
MSIFLT – Read or Write FIFO Fault (Over/Underflow)	148	140	0x00012C	IFS8<12>	IEC8<12>	IPC35<2:0>
S1SRST – MSI Slave Reset	149	141	0x00012E	IFS8<13>	IEC8<13>	IPC35<6:4>
Reserved	150-153	142-145	0x000130-0x000136	—	—	—
S1BRK – Slave Break	154	146	0x000138	IFS9<2>	IEC9<2>	IPC36<10:8>
Reserved	155-156	147-148	0x00013A-0x00013C	—	—	—
CCP7 – Input Capture/Output Compare 7	157	149	0x00013E	IFS9<5>	IEC9<5>	IPC37<6:4>
CCT7 – CCP7 Timer	158	150	0x000140	IFS9<6>	IEC9<6>	IPC37<10:8>
Reserved	159	151	0x000142	—	—	—
CCP8 – Input Capture/Output Compare 8	160	152	0x000144	IFS9<8>	IEC9<8>	IPC38<2:0>
CCT8 – CCP8 Timer	161	153	0x000146	IFS9<9>	IEC9<9>	IPC38<6:4>
Reserved	162-164	154-156	0x000148-0x00014C	—	—	—
S1CLKF – Slave Clock Fail	165	157	0x00014E	IFS9<13>	IEC9<13>	IPC39<6:4>
Reserved	166-175	158-167	0x000150-0x000162	—	—	—
ADFIFO – ADC FIFO Ready	176	168	0x000164	IFS10<8>	IEC10<8>	IPC42<2:0>

REGISTER 3-39: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ICM1R7	ICM1R6	ICM1R5	ICM1R4	ICM1R3	ICM1R2	ICM1R1	ICM1R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TCKI1R7	TCKI1R6	TCKI1R5	TCKI1R4	TCKI1R3	TCKI1R2	TCKI1R1	TCKI1R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **ICM1R<7:0>:** Assign SCCP Capture 1 (ICM1) Input to the Corresponding RPn Pin bits
See Table 3-30.

bit 7-0 **TCKI1<7:0>:** Assign SCCP Timer1 (TCKI1) Input to the Corresponding RPn Pin bits
See Table 3-30.

REGISTER 3-40: RPINR4: PERIPHERAL PIN SELECT INPUT REGISTER 4

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ICM2R7	ICM2R6	ICM2R5	ICM2R4	ICM2R3	ICM2R2	ICM2R1	ICM2R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TCKI2R7	TCKI2R6	TCKI2R5	TCKI2R4	TCKI2R3	TCKI2R2	TCKI2R1	TCKI2R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **ICM2R<7:0>:** Assign SCCP Capture 2 (ICM2) Input to the Corresponding RPn Pin bits
See Table 3-30.

bit 7-0 **TCKI2R<7:0>:** Assign SCCP Timer2 (TCKI2) Input to the Corresponding RPn Pin bits
See Table 3-30.

REGISTER 3-51: RPINR15: PERIPHERAL PIN SELECT INPUT REGISTER 15

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIHOM1R7	QEIHOM1R6	QEIHOM1R5	QEIHOM1R4	QEIHOM1R3	QEIHOM1R2	QEIHOM1R1	QEIHOM1R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEINDX1R7	QEINDX1R6	QEINDX1R5	QEINDX1R4	QEINDX1R3	QEINDX1R2	QEINDX1R1	QEINDX1R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **QEIHOM1R<7:0>:** Assign QEI Home 1 Input (QEIHOM1) to the Corresponding RPn Pin bits
See Table 3-30.

bit 7-0 **QEINDX1R<7:0>:** Assign QEI Index 1 Input (QEINDX1) to the Corresponding RPn Pin bits
See Table 3-30.

REGISTER 3-52: RPINR18: PERIPHERAL PIN SELECT INPUT REGISTER 18

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
U1DSRR7	U1DSRR6	U1DSRR5	U1DSRR4	U1DSRR3	U1DSRR2	U1DSRR1	U1DSRR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
U1RXR7	U1RXR6	U1RXR5	U1RXR4	U1RXR3	U1RXR2	U1RXR1	U1RXR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **U1DSRR<7:0>:** Assign UART1 Data-Set-Ready ($\overline{\text{U1DSR}}$) to the Corresponding RPn Pin bits
See Table 3-30.

bit 7-0 **U1RXR<7:0>:** Assign UART1 Receive (U1RX) to the Corresponding RPn Pin bits
See Table 3-30.

REGISTER 3-102: C1CONH: CAN CONTROL REGISTER HIGH (CONTINUED)

bit 4 **TXQEN:** Enable Transmit Queue bit(1)
1 = Enables Transmit Message Queue (TXQ) and reserves space in RAM
0 = Does not reserve space in RAM for TXQ

bit 3 **STEF:** Store in Transmit Event FIFO bit(1)
1 = Saves transmitted messages in TEF
0 = Does not save transmitted messages in TEF

bit 2 **SERRLOM:** Transition to Listen Only Mode on System Error bit(1)
1 = Transitions to Listen Only mode
0 = Transitions to Restricted Operation mode

bit 1 **ESIGM:** Transmit ESI in Gateway Mode bit(1)
1 = ESI is transmitted as recessive when ESI of the message is high or CAN controller is error passive
0 = ESI reflects error status of CAN controller

bit 0 **RTXAT:** Restrict Retransmission Attempts bit(1)
1 = Restricted retransmission attempts, uses TXAT<1:0> bits (C1TXQCONH<6:5>)
0 = Unlimited number of retransmission attempts, TXAT<1:0> bits will be ignored

Note 1: These bits can only be modified in Configuration mode (OPMOD<2:0> = 100).

4.2.5 INSTRUCTION ADDRESSING MODES

The addressing modes shown in Table 4-17 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions differ from those in the other instruction types.

4.2.5.1 File Register Instructions

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a Working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire Data Space.

4.2.5.2 MCU Instructions

The three-operand MCU instructions are of the form:

```
Operand 3 = Operand 1 <function> Operand 2
```

where `Operand 1` is always a Working register (that is, the addressing mode can only be Register Direct), which is referred to as Wb. `Operand 2` can be a W register fetched from data memory or a 5-bit literal. The result location can either be a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-Bit or 10-Bit Literal

Note: Not all instructions support all the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

TABLE 4-17: FUNDAMENTAL ADDRESSING MODES SUPPORTED

Addressing Mode	Description
File Register Direct	The address of the file register is specified explicitly.
Register Direct	The contents of a register are accessed directly.
Register Indirect	The contents of Wn form the Effective Address (EA).
Register Indirect Post-Modified	The contents of Wn form the EA. Wn is post-modified (incremented or decremented) by a constant value.
Register Indirect Pre-Modified	Wn is pre-modified (incremented or decremented) by a signed constant value to form the EA.
Register Indirect with Register Offset (Register Indexed)	The sum of Wn and Wb forms the EA.
Register Indirect with Literal Offset	The sum of Wn and a literal forms the EA.

REGISTER 4-102: ADIEL: ADC INTERRUPT ENABLE REGISTER LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IE<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IE<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **IE<15:0>:** Common Interrupt Enable bits
1 = Common and individual interrupts are enabled for the corresponding channel
0 = Common and individual interrupts are disabled for the corresponding channel

REGISTER 4-103: ADIEH: ADC INTERRUPT ENABLE REGISTER HIGH

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	IE<20:16>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4-0 **IE<20:16>:** Common Interrupt Enable bits
1 = Common and individual interrupts are enabled for the corresponding channel
0 = Common and individual interrupts are disabled for the corresponding channel

REGISTER 6-17: APLLFBD1: APLL FEEDBACK DIVIDER REGISTER (SLAVE)

U-0	U-0	U-0	U-0	r-0	r-0	r-0	r-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-1	R/W-0
APLLFBDIV<7:0>							
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **Reserved:** Maintain as '0'

bit 7-0 **APLLFBDIV<7:0>:** APLL Feedback Divider bits

11111111 = Reserved
...
11001000 = 200 maximum(1)
...
10010110 = 150 (default)
...
00010000 = 16 minimum(1)
...
00000010 = Reserved
00000001 = Reserved
00000000 = Reserved

Note 1: The allowed range is 16-200 (decimal). The rest of the values are reserved and should be avoided. The power-on default feedback divider is 150 (decimal) with an 8 MHz FRC input clock; the VCO frequency is 1.2 GHz.

7.6 PMD Control Registers

REGISTER 7-1: PMDCONL: MASTER PMD CONTROL REGISTER LOW

U-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
—	—	—	—	PMDLOCK	—	—	
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as ‘0’

bit 11 **PMDLOCK:** PMD Lock bit
1 = PMD bits can be written
0 = PMD bits are not allowed to be written

bit 10-0 **Unimplemented:** Read as ‘0’

REGISTER 9-6: MPER: MASTER PERIOD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MPER<15:8>(1)							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MPER<7:0>(1)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **MPER<15:0>:** Master Period Register bits(1)

Note 1: Period values less than '0x0010' should not be selected.

REGISTER 9-9: LOGCONy: COMBINATORIAL PWM LOGIC CONTROL REGISTER y(2) (CONTINUED)

bit 6 **S2yPOL:** Combinatorial PWM Logic Source #2 Polarity bit
1 = Input is inverted
0 = Input is positive logic

bit 5-4 **PWMLFy<1:0>:** Combinatorial PWM Logic Function Selection bits
11 = Reserved
10 = PWMS1 ^ PWMS2 (XOR)
01 = PWMS1 & PWMS2 (AND)
00 = PWMS1 | PWMS2 (OR)

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **PWMLFyD<2:0>:** Combinatorial PWM Logic Destination Selection bits
111 = Logic function is assigned to the PWM8H or PWM8L pin
110 = Logic function is assigned to the PWM7H or PWM7L pin
101 = Logic function is assigned to the PWM6H or PWM6L pin
100 = Logic function is assigned to the PWM5H or PWM5Lpin
011 = Logic function is assigned to the PWM4H or PWM4Lpin
010 = Logic function is assigned to the PWM3H or PWM3Lpin
001 = Logic function is assigned to the PWM2H or PWM2Lpin
000 = No assignment, combinatorial PWM logic function is disabled

Note 1: Logic function input will be connected to '0' if the PWM channel is not present.
2: 'y' denotes a common instance (A-F).

TABLE 15-2: I2Cx RESERVED ADDRESSES(1)

Slave Address	R/$\overline{W}$ Bit	Description
0000 000	0	General Call Address(2)
0000 000	1	Start Byte
0000 001	x	Cbus Address
0000 01x	x	Reserved
0000 1xx	x	HS Mode Master Code
1111 0xx	x	10-Bit Slave Upper Byte(3)
1111 1xx	x	Reserved

Note 1: The address bits listed here will never cause an address match independent of address mask settings.

2: This address will be Acknowledged only if GCEN = 1.

3: A match on this address can only occur on the upper byte in 10-Bit Addressing mode.

21.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the dsPIC33CH128MP508 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the *"dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

The dsPIC33CH128MP508 family devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard™ Security
- JTAG Boundary Scan Interface
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Emulation
- Brown-out Reset (BOR)

21.1 Configuration Bits

In dsPIC33CH128MP508 family devices, the Configuration Words are implemented as volatile memory. This means that configuration data will get loaded to volatile memory (from the Flash Configuration Words) each time the device is powered up. Configuration data is stored at the end of the on-chip program memory space, known as the Flash Configuration Words. Their specific locations are shown in Table 21-1. The configuration data is automatically loaded from the Flash Configuration Words to the proper Configuration Shadow registers during device Resets.

Note: Configuration data is reloaded on all types of device Master Resets. Slave Resets do not load the Configuration registers. It is recommended not to change the Slave Configuration register without resetting the Slave along with the Master (S1MSRE = 1).

When creating applications for these devices, users should always specifically allocate the location of the Flash Configuration Words for configuration data in their code for the compiler. This is to make certain that program code is not stored in this address when the code is compiled. Program code executing out of configuration space will cause a device Reset. The Master code, as well as the Slave code, are located in Flash memory. Table 21-1 shows the Master and the Slave Configuration registers and their address locations in Flash memory.

Slave Configuration bits are located in the Master Flash and loaded during a Master Reset.

Note: Performing a page erase operation on the last page of program memory clears the Flash Configuration Words.

TABLE 21-1: CONFIGURATION WORD ADDRESSES

Register	64k Address	128k Address
Master/General Configuration Registers		
FSEC	00AF00	015F00
FBSLIM	00AF10	015F10
FSIGN	00AF14	015F14
FOSCSEL	00AF18	015F18
FOSC	00AF1C	015F1C
FWDT	00AF20	015F20
FPOR	00AF24	015F24
FICD	00AF28	015F28
FDMTIVTL	00AF2C	015F2C
FDMTIVTH	00AF30	015F30
FDMTCNTL	00AF34	015F34
FDMTCNTH	00AF38	015F38
FDMT	00AF3C	015F3C
FDEVOPT	00AF40	015F40
FALTREG	00AF44	015F44
FMBXM	00AF48	015F48
FMBXHS1	00AFC4	015F4C
FMBXHS2	00AF50	015F50
FMBXHSEN	00AF54	015F54
FCFGPRA0	00AF58	015F58
FCFGPRB0	00AF60	015F60
FCFGPRC0	00AF68	015F68
FCFGPRD0	00AF70	015F70
FCFGPRE0	00AF78	015F7C
Slave Configuration Registers		
FS1OSCSEL	00AF80	015F80
FS1OSC	00AF84	015F84
FS1WDT	00AF88	015F88
FS1POR	00AF8C	015F8C
FS1ICD	00AF90	015F90
FS1DEVOPT	00AF94	015F94
FS1ALTREG	00AF98	015F98

REGISTER 21-5: FOSC CONFIGURATION REGISTER

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

U-1	U-1	U-1	R/PO-1	R/PO-1	R/PO-1	U-1	r-1
—	—	—	XTBST	XTCFG1	XTCFG0	—	—
bit 15							bit 8

R/PO-1	R/PO-1	U-1	U-1	U-1	R/PO-1	R/PO-1	R/PO-1
FCKSM1	FCKSM0	—	—	—	OSCIOFNC(1)	POSCMD1	POSCMD0
bit 7							bit 0

Legend:	PO = Program Once bit	r = Reserved bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 23-13 **Unimplemented:** Read as '1'

bit 12 **XTBST:** Oscillator Kick-Start Programmability bit
1 = Boosts the kick-start
0 = Default kick-start

bit 11-10 **XTCFG<1:0>:** Crystal Oscillator Drive Select bits
Current gain programmability for oscillator (output drive).
11 = Gain3 (use for 24-32 MHz crystals)
10 = Gain2 (use for 16-24 MHz crystals)
01 = Gain1 (use for 8-16 MHz crystals)
00 = Gain0 (use for 4-8 MHz crystals)

bit 9 **Unimplemented:** Read as '1'

bit 8 **Reserved:** Maintain as '1'

bit 7-6 **FCKSM<1:0>:** Clock Switching Mode bits
1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled
01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled
00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled

bit 5-3 **Unimplemented:** Read as '1'

bit 2 **OSCIOFNC:** OSCO Pin Function bit (except in XT and HS modes)(1)
1 = OSCO is the clock output
0 = OSCO is the general purpose digital I/O pin

bit 1-0 **POSCMD<1:0>:** Primary Oscillator Mode Select bits
11 = Primary Oscillator is disabled
10 = HS Crystal Oscillator mode (10 MHz-32 MHz)
01 = XT Crystal Oscillator mode (3.5 MHz-10 MHz)
00 = EC (External Clock) mode

Note 1: The OSCO pin function is determined by the S1OSCIOFNC Configuration bit. If both the Master core OSCIOFNC and Slave core S1OSCIOFNC bits are set, the Master core OSCIOFNC bit has priority.

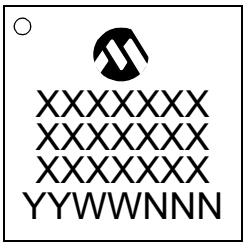
25.1 Package Marking Information (Continued)

48-Lead TQFP (7x7 mm)

Example

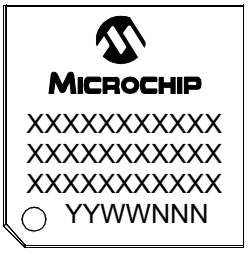
CH64MP
2041810
017

48-Lead UQFN (6x6 mm)

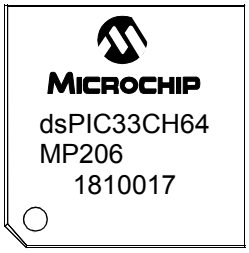


Example

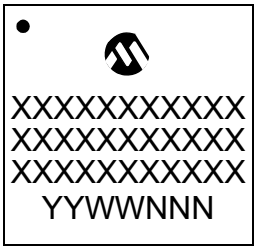
64-Lead TQFP (10x10x1 mm)



Example

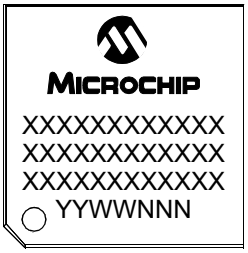


64-Lead QFN (9x9x0.9 mm)



Example

80-Lead TQFP (12x12x1 mm)



Example