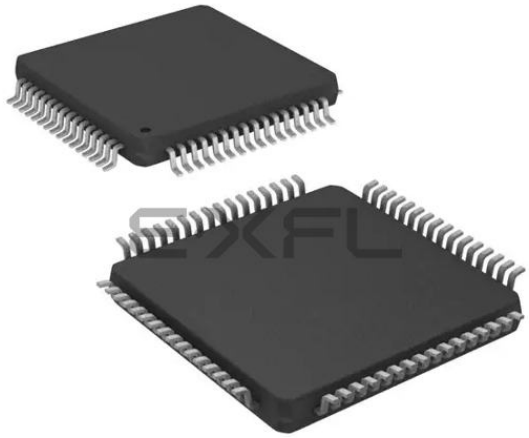
Microchip Technology - DSPIC33CH64MP506-I/PT Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit Dual-Core
Speed	180MHz, 200MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	53
Program Memory Size	88KB (88K x 8)
Program Memory Type	FLASH, PRAM
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 34x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ch64mp506-i-pt

3.1.3 DATA SPACE ADDRESSING

The base Data Space (DS) can be addressed as up to 4K words or 8 Kbytes, and is split into two blocks, referred to as X and Y data memory. Each memory block has its own independent Address Generation Unit (AGU). The MCU class of instructions operates solely through the X memory AGU, which accesses the entire memory map as one linear Data Space. Certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y Data Space boundary is device-specific.

The upper 32 Kbytes of the Data Space memory map can optionally be mapped into Program Space (PS) at any 16K program word boundary. The program-to-Data Space mapping feature, known as Program Space Visibility (PSV), lets any instruction access Program Space as if it were Data Space. Refer to **"Data Memory"** (DS70595) in the *"dsPIC33/PIC24 Family Reference Manual"* for more details on PSV and table accesses.

On dsPIC33CH128MP508 family devices, overhead-free circular buffers (Modulo Addressing) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. The X AGU Circular Addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data re-ordering for radix-2 FFT algorithms.

3.1.4 ADDRESSING MODES

The CPU supports these addressing modes:

- Inherent (no operand)
- Relative
- Literal
- Memory Direct
- Register Direct
- Register Indirect

Each instruction is associated with a predefined addressing mode group, depending upon its functional requirements. As many as six addressing modes are supported for each instruction.

TABLE 3-23: MASTER INTERRUPT VECTOR DETAILS (CONTINUED)

Interrupt Source	Vector #	IRQ #	IVT Address	Interrupt Bit Location		
				Flag	Enable	Priority
ADCAN16 – ADC AN16 Interrupt	115	107	0x0000EA	IFS6<11>	IEC6<11>	IPC26<14:12>
ADCAN17 – ADC AN17 Interrupt	116	108	0x0000EC	IFS6<12>	IEC6<12>	IPC27<2:0>
ADCAN18 – ADC AN18 Interrupt	117	109	0x0000EE	IFS6<13>	IEC6<13>	IPC27<6:4>
ADCAN19 – ADC AN19 Interrupt	118	110	0x0000F0	IFS6<14>	IEC6<14>	IPC27<10:8>
ADCAN20 – ADC AN20 Interrupt	119	111	0x0000F2	IFS6<15>	IEC6<15>	IPC27<14:12>
Reserved	120-122	112-114	0x0000F4-0x0000F8	—	—	—
ADFLT – ADC Fault	123	115	0x0000FA	IFS7<3>	IEC7<3>	IPC28<14:12>
ADCMP0 – ADC Digital Comparator 0	124	116	0x0000FC	IFS7<4>	IEC7<4>	IPC29<2:0>
ADCMP1 – ADC Digital Comparator 1	125	117	0x0000FE	IFS7<5>	IEC7<5>	IPC29<6:4>
ADCMP2 – ADC Digital Comparator 2	126	118	0x000100	IFS7<6>	IEC7<6>	IPC29<10:8>
ADCMP3 – ADC Digital Comparator 3	127	119	0x000102	IFS7<7>	IEC7<7>	IPC29<14:12>
ADFLTR0 – ADC Oversample Filter 0	128	120	0x000104	IFS7<8>	IEC7<8>	IPC30<2:0>
ADFLTR1 – ADC Oversample Filter 1	129	121	0x000106	IFS7<9>	IEC7<9>	IPC30<6:4>
ADFLTR2 – ADC Oversample Filter 2	130	122	0x000108	IFS7<10>	IEC7<10>	IPC30<10:8>
ADFLTR3 – ADC Oversample Filter 3	131	123	0x00010A	IFS7<11>	IEC7<11>	IPC30<14:12>
CLC1P – CLC1 Positive Edge	132	124	0x00010C	IFS7<12>	IEC7<12>	IPC31<2:0>
CLC2P – CLC2 Positive Edge	133	125	0x00010E	IFS7<13>	IEC7<13>	IPC31<6:4>
SPI1G – SPI1 Error	134	126	0x000110	IFS7<14>	IEC7<14>	IPC31<10:8>
SPI2G – SPI2 Error	135	127	0x000112	IFS7<15>	IEC7<15>	IPC31<14:12>
Reserved	136	128	0x000114	—	—	—
MSIS1 – MSI Slave Initiated Interrupt	137	129	0x000116	IFS8<1>	IEC8<1>	IPC32<6:4>
MSIA – MSI Protocol A	138	130	0x000118	IFS8<2>	IEC8<2>	IPC32<10:8>
MSIB – MSI Protocol B	139	131	0x00011A	IFS8<3>	IEC8<3>	IPC32<14:12>
MSIC – MSI Protocol C	140	132	0x00011C	IFS8<4>	IEC8<4>	IPC33<2:0>
MSID – MSI Protocol D	141	133	0x00011E	IFS8<5>	IEC8<5>	IPC33<6:4>
MSIE – MSI Protocol E	142	134	0x000120	IFS8<6>	IEC8<6>	IPC33<10:8>
MSIF – MSI Protocol F	143	135	0x000122	IFS8<7>	IEC8<7>	IPC33<14:12>
MSIG – MSI Protocol G	144	136	0x000124	IFS8<8>	IEC8<8>	IPC34<2:0>
MSIH – MSI Protocol H	145	137	0x000126	IFS8<9>	IEC8<9>	IPC34<6:4>
MSIDT – Master Read FIFO Data Ready	146	138	0x000128	IFS8<10>	IEC8<10>	IPC34<10:8>
MSIWFE – Master Write FIFO Empty	147	139	0x00012A	IFS8<11>	IEC8<11>	IPC34<14:12>
MSIFLT – Read or Write FIFO Fault (Over/Underflow)	148	140	0x00012C	IFS8<12>	IEC8<12>	IPC35<2:0>
S1SRST – MSI Slave Reset	149	141	0x00012E	IFS8<13>	IEC8<13>	IPC35<6:4>
Reserved	150-153	142-145	0x000130-0x000136	—	—	—
S1BRK – Slave Break	154	146	0x000138	IFS9<2>	IEC9<2>	IPC36<10:8>
Reserved	155-156	147-148	0x00013A-0x00013C	—	—	—
CCP7 – Input Capture/Output Compare 7	157	149	0x00013E	IFS9<5>	IEC9<5>	IPC37<6:4>
CCT7 – CCP7 Timer	158	150	0x000140	IFS9<6>	IEC9<6>	IPC37<10:8>
Reserved	159	151	0x000142	—	—	—
CCP8 – Input Capture/Output Compare 8	160	152	0x000144	IFS9<8>	IEC9<8>	IPC38<2:0>
CCT8 – CCP8 Timer	161	153	0x000146	IFS9<9>	IEC9<9>	IPC38<6:4>
Reserved	162-164	154-156	0x000148-0x00014C	—	—	—
S1CLKF – Slave Clock Fail	165	157	0x00014E	IFS9<13>	IEC9<13>	IPC39<6:4>
Reserved	166-175	158-167	0x000150-0x000162	—	—	—
ADFIFO – ADC FIFO Ready	176	168	0x000164	IFS10<8>	IEC10<8>	IPC42<2:0>

REGISTER 3-74: RPOR6: PERIPHERAL PIN SELECT OUTPUT REGISTER 6

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP45R5	RP45R4	RP45R3	RP45R2	RP45R1	RP45R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP44R5	RP44R4	RP44R3	RP44R2	RP44R1	RP44R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP45R<5:0>:** Peripheral Output Function is Assigned to RP45 Output Pin bits (see Table 3-33 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP44R<5:0>:** Peripheral Output Function is Assigned to RP44 Output Pin bits (see Table 3-33 for peripheral function numbers)

REGISTER 3-75: RPOR7: PERIPHERAL PIN SELECT OUTPUT REGISTER 7

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP47R5	RP47R4	RP47R3	RP47R2	RP47R1	RP47R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP46R5	RP46R4	RP46R3	RP46R2	RP46R1	RP46R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP47R<5:0>:** Peripheral Output Function is Assigned to RP47 Output Pin bits (see Table 3-33 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP46R<5:0>:** Peripheral Output Function is Assigned to RP46 Output Pin bits (see Table 3-33 for peripheral function numbers)

REGISTER 3-94: DMTSTAT: DEADMAN TIMER STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

HC/R-0	HC/R-0	HC/R-0	U-0	U-0	U-0	U-0	R-0
BAD1	BAD2	DMTEVENT	—	—	—	—	WINOPN
bit 7							bit 0

Legend:	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **BAD1:** Deadman Timer Bad STEP1<7:0> Value Detect bit
1 = Incorrect STEP1<7:0> value was detected
0 = Incorrect STEP1<7:0> value was not detected

bit 6 **BAD2:** Deadman Timer Bad STEP2<7:0> Value Detect bit
1 = Incorrect STEP2<7:0> value was detected
0 = Incorrect STEP2<7:0> value was not detected

bit 5 **DMTEVENT:** Deadman Timer Event bit
1 = Deadman Timer event was detected (counter expired, or bad STEP1<7:0> or STEP2<7:0> value was entered prior to counter increment)
0 = Deadman Timer event was not detected

bit 4-1 **Unimplemented:** Read as '0'

bit 0 **WINOPN:** Deadman Timer Clear Window bit
1 = Deadman Timer clear window is open
0 = Deadman Timer clear window is not open

REGISTER 3-101: DMTHOLDREG: DMT HOLD REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
UPRCNT<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
UPRCNT<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **UPRCNT<15:0>:** DMTCNTH Register Value when DMTCNTL and DMTCNTH were Last Read bits

Note 1: The DMTHOLDREG register is initialized to '0' on Reset, and is only loaded when the DMTCNTL and DMTCNTH registers are read.

REGISTER 3-174: ADIEL: ADC INTERRUPT ENABLE REGISTER LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IE<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IE<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **IE<15:0>:** Common Interrupt Enable bits
1 = Common and individual interrupts are enabled for the corresponding channel
0 = Common and individual interrupts are disabled for the corresponding channel

REGISTER 3-175: ADIEH: ADC INTERRUPT ENABLE REGISTER HIGH

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	IE<20:16>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4-0 **IE<20:16>:** Common Interrupt Enable bits
1 = Common and individual interrupts are enabled for the corresponding channel
0 = Common and individual interrupts are disabled for the corresponding channel

REGISTER 3-178: ADTRIGnL AND ADTRIGnH: ADC CHANNEL TRIGGER n(x) SELECTION REGISTERS LOW AND HIGH (x = 0 TO 19; n = 0 TO 4)

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	TRGSRC(x+1)4	TRGSRC(x+1)3	TRGSRC(x+1)2	TRGSRC(x+1)1	TRGSRC(x+1)0
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	TRGSRCx4	TRGSRCx3	TRGSRCx2	TRGSRCx1	TRGSRCx0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **TRGSRC(x+1)<4:0>:** Trigger Source Selection for Corresponding Analog Input bits (TRGSRC1 to TRGSRC19 – Odd)

11111 = ADTRG31 (PPS input)
11110 = Master PTG
11101 = Slave CLC1
11100 = Master CLC1
11011 = Slave PWM8 Trigger 2
11010 = Slave PWM5 Trigger 2
11001 = Slave PWM3 Trigger 2
11000 = Slave PWM1 Trigger 2
10111 = Master SCCP4 PWM interrupt
10110 = Master SCCP3 PWM interrupt
10101 = Master SCCP2 PWM interrupt
10100 = Master SCCP1 PWM interrupt
10011 = Reserved
10010 = Reserved
10001 = Reserved
10000 = Reserved
01111 = Reserved
01110 = Reserved
01101 = Reserved
01100 = Reserved
01011 = Master PWM4 Trigger 2
01010 = Master PWM4 Trigger 1
01001 = Master PWM3 Trigger 2
01000 = Master PWM3 Trigger 1
00111 = Master PWM2 Trigger 2
00110 = Master PWM2 Trigger 1
00101 = Master PWM1 Trigger 2
00100 = Master PWM1 Trigger 1
00011 = Reserved
00010 = Level software trigger
00001 = Common software trigger
00000 = No trigger is enabled

bit 7-5 **Unimplemented:** Read as '0'

REGISTER 3-185: PTGBTE: PTG BROADCAST TRIGGER ENABLE LOW REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGBTE<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGBTE<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTGBTE<15:0>:** PTG Broadcast Trigger Enable bits
1 = Generates trigger when the broadcast command is executed
0 = Does not generate trigger when the broadcast command is executed

Note 1: These bits are read-only when the module is executing Step commands.

REGISTER 3-186: PTGBTEH: PTG BROADCAST TRIGGER ENABLE HIGH REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGBTE<31:24>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGBTE<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTGBTE<31:16>:** PTG Broadcast Trigger Enable bits
1 = Generates trigger when the broadcast command is executed
0 = Does not generate trigger when the broadcast command is executed

Note 1: These bits are read-only when the module is executing Step commands.

REGISTER 4-109: ADCMPxENL: ADC DIGITAL COMPARATOR x CHANNEL ENABLE REGISTER LOW (x = 0, 1, 2, 3)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMPEN<15:8>							
bit 15							bit 8

R/W/0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMPEN<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **CMPEN<15:0>:** Comparator Enable for Corresponding Input Channels bits
1 = Conversion result for corresponding channel is used by the comparator
0 = Conversion result for corresponding channel is not used by the comparator

REGISTER 4-110: ADCMPxENH: ADC DIGITAL COMPARATOR x CHANNEL ENABLE REGISTER HIGH (x = 0, 1, 2, 3)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	CMPEN<20:16>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4-0 **CMPEN<20:16>:** Comparator Enable for Corresponding Input Channels bits
1 = Conversion result for corresponding channel is used by the comparator
0 = Conversion result for corresponding channel is not used by the comparator

REGISTER 5-7: MRSWFDATA: MASTER READ (SLAVE WRITE) FIFO DATA REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
MRSWFDATA<15:8>							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
MRSWFDATA<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **MRSWFDATA<15:0>:** Read FIFO Data Out Register bits

REGISTER 5-8: MWSRFDATA: MASTER WRITE (SLAVE READ) FIFO DATA REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
MWSRFDATA<15:8>							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
MWSRFDATA<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **MWSRFDATA<15:0>:** Write FIFO Data Out Register bits

REGISTER 11-2: DACCTRL2H: DAC CONTROL 2 HIGH REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	SSTIME<9:8>(1)	
bit 15							bit 8

R/W-1	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0
SSTIME<7:0>(1)							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **SSTIME<9:0>:** Time from Start of Transition Mode until Steady-State Filter is Enabled bits(1)

Note 1: The value for SSTIME<9:0> should be greater than the TMODTIME<9:0> value.

REGISTER 11-3: DACCTRL2L: DAC CONTROL 2 LOW REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	TMODTIME<9:8>(1)	
bit 15							bit 8

R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-1
TMODTIME<7:0>(1)							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **TMODTIME<9:0>:** Transition Mode Duration bits(1)

Note 1: The value for TMODTIME<9:0> should be less than the SSTIME<9:0> value.

REGISTER 12-4: QEIxSTAT: QEIx STATUS REGISTER

U-0	U-0	HS/R/C-0	R/W-0	HS/R/C-0	R/W-0	HS/R/C-0	R/W-0
—	—	PCHEQIRQ	PCHEQIEN	PCLEQIRQ	PCLEQIEN	POSOVIRQ	POSOVIEN
bit 15							bit 8

HS/R/C-0	R/W-0	HS/R/C-0	R/W-0	HS/R/C-0	R/W-0	HS/R/C-0	R/W-0
PCIIRQ(1)	PCIIEN	VELOVIRQ	VELOVIEN	HOMIRQ	HOMIEN	IDXIRQ	IDXIEN
bit 7							bit 0

Legend:	C = Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **PCHEQIRQ:** Position Counter Greater Than Compare Status bit
1 = POSxCNT ≥ QEIxGEC
0 = POSxCNT < QEIxGEC

bit 12 **PCHEQIEN:** Position Counter Greater Than Compare Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 11 **PCLEQIRQ:** Position Counter Less Than Compare Status bit
1 = POSxCNT ≤ QEIxLEC
0 = POSxCNT > QEIxLEC

bit 10 **PCLEQIEN:** Position Counter Less Than Compare Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 9 **POSOVIRQ:** Position Counter Overflow Status bit
1 = Overflow has occurred
0 = No overflow has occurred

bit 8 **POSOVIEN:** Position Counter Overflow Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 7 **PCIIRQ:** Position Counter (Homing) Initialization Process Complete Status bit(1)
1 = POSxCNT was reinitialized
0 = POSxCNT was not reinitialized

bit 6 **PCIIEN:** Position Counter (Homing) Initialization Process Complete Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 5 **VELOVIRQ:** Velocity Counter Overflow Status bit
1 = Overflow has occurred
0 = No overflow has occurred

bit 4 **VELOVIEN:** Velocity Counter Overflow Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 3 **HOMIRQ:** Status Flag for Home Event Status bit
1 = Home event has occurred
0 = No Home event has occurred

Note 1: This status bit is only applicable to PIMOD<2:0> modes, '011' and '100'.

13.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note 1: This data sheet summarizes the features of the dsPIC33CH128MP508 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Multiprotocol Universal Asynchronous Receiver Transmitter (UART) Module"** (DS70005288) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: The UART is identical for both Master core and Slave core. The x is common for both Master core and Slave core (where the x represents the number of the specific module being addressed). The number of UART modules available on the Master core and Slave core is different and they are located in different SFR locations.

3: All associated register names are the same on the Master core and the Slave core. The Slave code will be developed in a separate project in MPLAB® X IDE with the device selection, dsPIC33CH128MP508**S1**, where the **S1** indicates the Slave device. The Master UART is UART1 and UART2, and the Slave UART is UART1.

Table 13-1 shows an overview of the module.

TABLE 13-1: UART MODULE OVERVIEW

	Number of UART Modules	Identical (Modules)
Master Core	2	Yes
Slave Core	1	Yes

The Universal Asynchronous Receiver Transmitter (UART) is a flexible serial communication peripheral used to interface dsPIC® microcontrollers with other equipment, including computers and peripherals. The UART is a full-duplex, asynchronous communication channel that can be used to implement protocols, such as RS-232 and RS-485. The UART also supports the following hardware extensions:

- LIN/J2602
- IrDA®
- Direct Matrix Architecture (DMX)
- Smart Card

The primary features of the UART are:

- Full or Half-Duplex Operation
- Up to 8-Deep TX and RX First In, First Out (FIFO) Buffers
- 8-Bit or 9-Bit Data Width
- Configurable Stop Bit Length
- Flow Control
- Auto-Baud Calibration
- Parity, Framing and Buffer Overrun Error Detection
- Address Detect
- Break Transmission
- Transmit and Receive Polarity Control
- Manchester Encoder/Decoder
- Operation in Sleep mode
- Wake from Sleep on Sync Break Received Interrupt

16.2 Transmit Mode

By default, the SENTx module is configured for transmit operation. The module can be configured for continuous asynchronous message frame transmission, or alternatively, for Synchronous mode triggered by software. When enabled, the transmitter will send a Sync, followed by the appropriate number of data nibbles, an optional CRC and optional pause pulse. The tick period used by the SENTx transmitter is set by writing a value to the TICKTIME<15:0> (SENTxCON2<15:0>) bits. The tick period calculations are shown in Equation 16-1.

EQUATION 16-1: TICK PERIOD CALCULATION

$$TICKTIME\langle 15:0\rangle = \frac{T_{TICK}}{T_{CLK}} - 1$$

An optional pause pulse can be used in Asynchronous mode to provide a fixed message frame time period. The frame period used by the SENTx transmitter is set by writing a value to the FRAMETIME<15:0> (SENTxCON3<15:0>) bits. The formulas used to calculate the value of frame time are shown in Equation 16-2.

EQUATION 16-2: FRAME TIME CALCULATIONS

$$FRAMETIME\langle 15:0\rangle = T_{TICK}/T_{FRAME}$$

$$FRAMETIME\langle 15:0\rangle \geq 122 + 27N$$

$$FRAMETIME\langle 15:0\rangle \geq 848 + 12N$$

Where:

T_{FRAME} = Total time of the message from ms

N = The number of data nibbles in message, 1-6

Note: The module will not produce a pause period with less than 12 ticks, regardless of the FRAMETIME<15:0> value. FRAMETIME<15:0> values beyond 2047 will have no effect on the length of a data frame.

16.2.1 TRANSMIT MODE CONFIGURATION

16.2.1.1 Initializing the SENTx Module

Perform the following steps to initialize the module:

1. Write RCVEN (SENTxCON1<11>) = 0 for Transmit mode.
2. Write TXM (SENTxCON1<10>) = 0 for Asynchronous Transmit mode or TXM = 1 for Synchronous mode.
3. Write NIBCNT<2:0> (SENTxCON1<2:0>) for the desired data frame length.
4. Write CRCEN (SENTxCON1<8>) for hardware or software CRC calculation.
5. Write PPP (SENTxCON1<7>) for optional pause pulse.
6. If PPP = 1, write TFRAME to SENTxCON3.
7. Write SENTxCON2 with the appropriate value for the desired tick period.
8. Enable interrupts and set interrupt priority.
9. Write initial status and data values to SENTxDATH/L.
10. If CRCEN = 0, calculate CRC and write the value to CRC<3:0> (SENTxDATL<3:0>).
11. Set the SNTEN (SENTxCON1<15>) bit to enable the module.

User software updates to SENTxDATH/L must be performed after the completion of the CRC and before the next message frame's status nibble. The recommended method is to use the message frame completion interrupt to trigger data writes.

REGISTER 21-9: FDMTIVTL CONFIGURATION REGISTER

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
DMTIVT<15:8>							
bit 15							bit 8

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
DMTIVT<7:0>							
bit 7							bit 0

Legend:	PO = Program Once bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-16 **Unimplemented:** Read as ‘1’

bit 15-0 **DMTIVT<15:0>:** DMT Window Interval Lower 16 bits

REGISTER 21-10: FDMTIVTH CONFIGURATION REGISTER

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
DMTIVT<31:24>							
bit 15							bit 8

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
DMTIVT<23:16>							
bit 7							bit 0

Legend:	PO = Program Once bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-16 **Unimplemented:** Read as ‘1’

bit 15-0 **DMTIVT<31:16>:** DMT Window Interval Higher 16 bits

TABLE 22-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles(1)	Status Flags Affected
60	MIN	MIN Acc	If Accumulator A Less than B Load Accumulator with B or vice versa	1	1	N,OV,Z
		MIN.V Acc, Wd	If Accumulator A Less than B Accumulator Force Minimum Data Range Limit with Limit Excess Result	1	1	N,OV,Z
		MINZ Acc	Accumulator Force Minimum Data Range Limit	1	1	N,OV,Z
		MINZ.V Acc, Wd	Accumulator Force Minimum Data Range Limit with Limit Excess Result	1	1	N,OV,Z
61	MOV	MOV f,Wn	Move f to Wn	1	1	None
		MOV f	Move f to f	1	1	None
		MOV f,WREG	Move f to WREG	1	1	None
		MOV #lit16,Wn	Move 16-bit Literal to Wn	1	1	None
		MOV.b #lit8,Wn	Move 8-bit Literal to Wn	1	1	None
		MOV Wn,f	Move Wn to f	1	1	None
		MOV Wso,Wdo	Move Ws to Wd	1	1	None
		MOV WREG,f	Move WREG to f	1	1	None
		MOV.D Wns,Wd	Move Double from W(ns):W(ns + 1) to Wd	1	2	None
		MOV.D Ws,Wnd	Move Double from Ws to W(nd + 1):W(nd)	1	2	None
62	MOVPAG	MOVPAG #lit10,DSRPAG	Move 10-bit Literal to DSRPAG	1	1	None
		MOVPAG #lit8,TBLPAG	Move 8-bit Literal to TBLPAG	1	1	None
		MOVPAG Ws, DSRPAG	Move Ws<9:0> to DSRPAG	1	1	None
		MOVPAG Ws, TBLPAG	Move Ws<7:0> to TBLPAG	1	1	None
64	MOVSAC	MOVSAC Acc,Wx,Wxd,Wy,Wyd,AWB	Prefetch and Store Accumulator	1	1	None
65	MPY	MPY Wm*Wn,Acc,Wx,Wxd,Wy,Wyd	Multiply Wm by Wn to Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
		MPY Wm*Wm,Acc,Wx,Wxd,Wy,Wyd	Square Wm to Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
66	MPY.N	MPY.N Wm*Wn,Acc,Wx,Wxd,Wy,Wyd	-(Multiply Wm by Wn) to Accumulator	1	1	None
67	MSC	MSC Wm*Wm,Acc,Wx,Wxd,Wy,Wyd, AWB	Multiply and Subtract from Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
68	MUL	MUL.SS Wb,Ws,Wnd	{Wnd + 1, Wnd} = Signed(Wb) * Signed(Ws)	1	1	None
		MUL.SS Wb,Ws,Acc	Accumulator = Signed(Wb) * Signed(Ws)	1	1	None
		MUL.SU Wb,Ws,Wnd	{Wnd + 1, Wnd} = Signed(Wb) * Unsigned(Ws)	1	1	None
		MUL.SU Wb,Ws,Acc	Accumulator = Signed(Wb) * Unsigned(Ws)	1	1	None
		MUL.SU Wb,#lit5,Acc	Accumulator = Signed(Wb) * Unsigned(lit5)	1	1	None
		MUL.US Wb,Ws,Wnd	{Wnd + 1, Wnd} = Unsigned(Wb) * Signed(Ws)	1	1	None
		MUL.US Wb,Ws,Acc	Accumulator = Unsigned(Wb) * Signed(Ws)	1	1	None
		MUL.UU Wb,Ws,Wnd	{Wnd + 1, Wnd} = Unsigned(Wb) * Unsigned(Ws)	1	1	None
		MUL.UU Wb,#lit5,Acc	Accumulator = Unsigned(Wb) * Unsigned(lit5)	1	1	None
		MUL.UU Wb,Ws,Acc	Accumulator = Unsigned(Wb) * Unsigned(Ws)	1	1	None
		MULW.SS Wb,Ws,Wnd	Wnd = Signed(Wb) * Signed(Ws)	1	1	None
		MULW.SU Wb,Ws,Wnd	Wnd = Signed(Wb) * Unsigned(Ws)	1	1	None
		MULW.US Wb,Ws,Wnd	Wnd = Unsigned(Wb) * Signed(Ws)	1	1	None
		MULW.UU Wb,Ws,Wnd	Wnd = Unsigned(Wb) * Unsigned(Ws)	1	1	None
		MUL.SU Wb,#lit5,Wnd	{Wnd + 1, Wnd} = Signed(Wb) * Unsigned(lit5)	1	1	None
		MUL.SU Wb,#lit5,Wnd	Wnd = Signed(Wb) * Unsigned(lit5)	1	1	None
		MUL.UU Wb,#lit5,Wnd	{Wnd + 1, Wnd} = Unsigned(Wb) * Unsigned(lit5)	1	1	None
		MUL.UU Wb,#lit5,Wnd	Wnd = Unsigned(Wb) * Unsigned(lit5)	1	1	None
		MUL f	W3:W2 = f * WREG	1	1	None

Note 1: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

2: Cycle times for Slave core are different for Master core, as shown in 2.

3: For dsPIC33CH128MP508 devices, the divide instructions must be preceded with a "REPEAT #5" instruction, such that they are executed six consecutive times

TABLE 24-9: DC CHARACTERISTICS: IDLE CURRENT (IIDLE) (MASTER IDLE/SLAVE SLEEP)

DC CHARACTERISTICS	Master (Idle) + Slave (Sleep)		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Parameter No.	**Typ.**	**Max.**	**Units**	**Conditions**		
Idle Current (IIDLE)(1)						
DC40a	6.6	8.4	mA	-40°C	3.3V	10 MIPS (N = 1, N2 = 5, N3 = 2, M = 50, FVCO = 400 MHz, FPLLO = 40 MHz)
	6.7	11.9	mA	+25°C		
	6.9	17.9	mA	+85°C		
	10.9	24.9	mA	+125°C		
DC41a	7.3	9.2	mA	-40°C	3.3V	20 MIPS (N = 1, N2 = 5, N3 = 1, M = 50, FVCO = 400 MHz, FPLLO = 80 MHz)
	7.5	12.7	mA	+25°C		
	7.7	18.7	mA	+85°C		
	11.7	25.7	mA	+125°C		
DC42a	9.2	11.1	mA	-40°C	3.3V	40 MIPS (N = 1, N2 = 3, N3 = 1, M = 60, FVCO = 480 MHz, FPLLO = 160 MHz)
	9.4	14.8	mA	+25°C		
	9.5	20.7	mA	+85°C		
	13.5	27.5	mA	+125°C		
DC43a	11.8	13.9	mA	-40°C	3.3V	70 MIPS (N = 1, N2 = 2, N3 = 1, M = 70, FVCO = 560 MHz, FPLLO = 280 MHz)
	12.0	17.6	mA	+25°C		
	12.1	23.5	mA	+85°C		
	16.1	30.1	mA	+125°C		
DC44a	14.1	16.3	mA	-40°C	3.3V	90 MIPS (N = 1, N2 = 2, N3 = 1, M = 90, FVCO = 720 MHz, FPLLO = 360 MHz)
	14.2	20	mA	+25°C		
	14.3	25.9	mA	+85°C		
	18.2	32.3	mA	+125°C		

Note 1: Base Idle current (IIDLE) is measured as follows:

- FIN = 8 MHz, FPFD = 8 MHz
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as output low
- $\overline{\text{MCLR}}$ = VDD, WDT and FSCM are disabled
- No peripheral modules are operating or being clocked (all defined PMDx bits are set)
- The NVMSIDL bit (NVMCON<12>) = 1 (i.e., Flash regulator is set to standby while the device is in Idle mode)
- JTAG is disabled

TABLE 24-41: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param No.	**Symbol**	**Characteristic(3)**		**Min.**	**Max.**	**Units**	**Conditions**
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	—	µs	
			400 kHz mode	1.3	—	µs	
			1 MHz mode(1)	0.5	—	µs	
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	µs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	µs	Device must operate at a minimum of 10 MHz
			1 MHz mode(1)	0.28	—	µs	
IS20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 x (VDD/5.5V)	300	ns	
			1 MHz mode(1)	20 x (VDD/5.5V)	120	ns	
IS21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	20 + 0.1 CB	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode		300	ns	
			1 MHz mode(1)	—	120	ns	
IS25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode(1)	50	—	ns	
IS26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	µs	
			400 kHz mode	0	0.9	µs	
			1 MHz mode(1)	0	0.3	µs	
IS30	TSU:STA	Start Condition Setup Time	100 kHz mode	4.7	—	µs	Only relevant for Repeated Start condition
			400 kHz mode	0.6	—	µs	
			1 MHz mode(1)	0.26	—	µs	
IS31	THD:STA	Start Condition Hold Time	100 kHz mode	4.0	—	µs	After this period, the first clock pulse is generated
			400 kHz mode	0.6	—	µs	
			1 MHz mode(1)	0.26	—	µs	
IS33	TSU:STO	Stop Condition Setup Time	100 kHz mode	4	—	µs	
			400 kHz mode	0.6	—	µs	
			1 MHz mode(1)	0.26	—	µs	
IS34	THD:STO	Stop Condition Hold Time	100 kHz mode	> 0	—	µs	
			400 kHz mode	> 0	—	µs	
			1 MHz mode(1)	> 0		µs	
IS40	TAA:SCL	Output Valid from Clock	100 kHz mode	0	3540	ns	
			400 kHz mode	0	900	ns	
			1 MHz mode(1)	0	400	ns	
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode(1)	0.5	—	µs	
IS50	CB	Bus Capacitive Loading		—	400	pF	
IS51	TPGD	Pulse Gobbler Delay		65	390	ns	**(Note 2)**

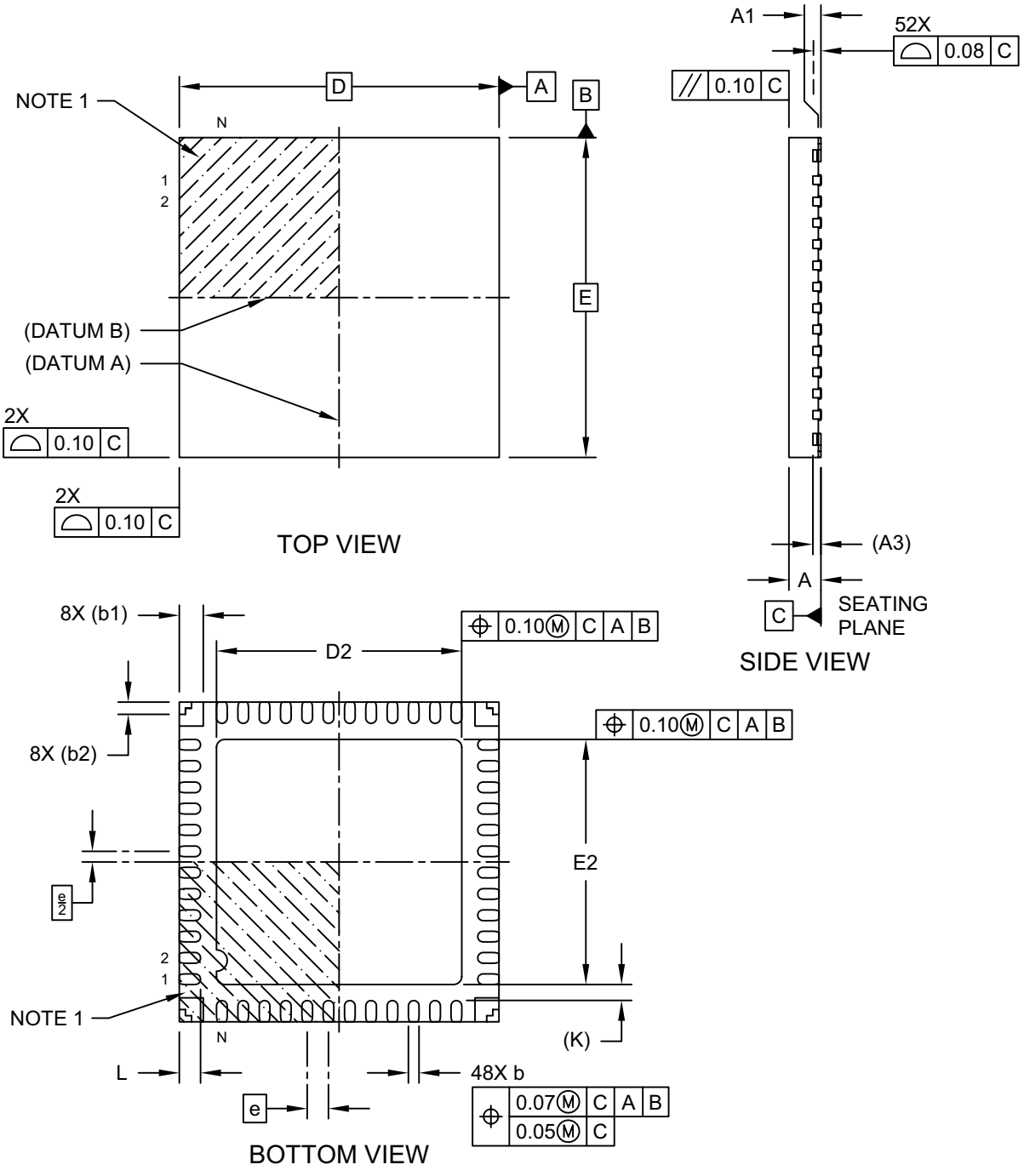
Note 1: Maximum Pin Capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

2: Typical value for this parameter is 130 ns.

3: These parameters are characterized but not tested in manufacturing.

48-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M4) - 6x6 mm Body [UQFN] With Corner Anchors and 4.6x4.6 mm Exposed Pad

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-442A-M4 Sheet 1 of 2

NOTES: