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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit Dual-Core
Speed	180MHz, 200MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	69
Program Memory Size	88KB (88K x 8)
Program Memory Type	FLASH, PRAM
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 34x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ch64mp508-e-pt

3.4.1 RESET RESOURCES

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

3.4.1.1 Key Resources

- **"Reset"** (DS70602) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

3.6 Master I/O Ports

Note 1: This data sheet summarizes the features of the dsPIC33CH128MP508 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"I/O Ports with Edge Detect"** (DS70005322) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: The I/O ports are shared by Master core and Slave core. All input goes to both the Master and Slave. The I/O ownership is defined by the Configuration bits.

3: The TMS pin function may be active multiple times during ICSP™ device erase, programming and debugging. When the TMS function is active, the integrated pull-up resistor will pull the pin to VDD. Proper care should be taken if there are sensitive circuits connected on the TMS pin during programming/erase and debugging.

Many of the device pins are shared among the peripherals and the Parallel I/O ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity. The Master and Slave have the same number of I/O ports and are shared. The Master PORT registers are located in the Master SFR and the Slave PORT registers are located in the Slave SFR, respectively.

Some of the key features of the I/O ports are:

- Individual Output Pin Open-Drain Enable/Disable
- Individual Input Pin Weak Pull-up and Pull-Down
- Monitor Selective Inputs and Generate Interrupt when Change in Pin State is Detected
- Operation during Sleep and Idle modes

Note: The output functionality of the ports is defined by the Configuration registers, FCFGPRA0 to FCFGPRE0. When these Configuration bits are maintained as '1', the Master owns the pin (only the output function); when the bits are '0', the ownership of that specific pin belongs to the Slave.

The input function of the I/O is valid for both Master and Slave. The Configuration registers, FCFGPRA0 to FCFGPRE0, do not have any control over the input function.

3.6.1 PARALLEL I/O (PIO) PORTS

All port pins have 12 registers directly associated with their operation as digital I/Os. The Data Direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input.

All port pins are defined as inputs after a Reset. Reads from the latch (LATx), read the latch. Writes to the latch, write the latch. Reads from the port (PORTx), read the port pins, while writes to the port pins, write the latch. Any bit and its associated data and control registers that are not valid for a particular device are disabled. This means the corresponding LATx and TRISx registers, and the port pin are read as zeros.

When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port because there is no other competing source of outputs. Table 3-27 shows the pin availability. Table 3-28 shows the 5V input tolerant pins across this device.

REGISTER 3-86: RPOR18: PERIPHERAL PIN SELECT OUTPUT REGISTER 18

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP69R5	RP69R4	RP69R3	RP69R2	RP69R1	RP69R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP68R5	RP68R4	RP68R3	RP68R2	RP68R1	RP68R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP69R<5:0>:** Peripheral Output Function is Assigned to RP69 Output Pin bits (see Table 3-33 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP68R<5:0>:** Peripheral Output Function is Assigned to RP68 Output Pin bits (see Table 3-33 for peripheral function numbers)

REGISTER 3-87: RPOR19: PERIPHERAL PIN SELECT OUTPUT REGISTER 19

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP71R5	RP71R4	RP71R3	RP71R2	RP71R1	RP71R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP70R5	RP70R4	RP70R3	RP70R2	RP70R1	RP70R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP71R<5:0>:** Peripheral Output Function is Assigned to RP71 Output Pin bits (see Table 3-33 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP70R<5:0>:** Peripheral Output Function is Assigned to RP70 Output Pin bits (see Table 3-33 for peripheral function numbers)

REGISTER 3-109: C1TDCL: CAN TRANSMITTER DELAY COMPENSATION REGISTER LOW(1)

U-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
—	TDCO<6:0>						
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TDCV<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **TDCO<6:0>:** Transmitter Delay Compensation Offset bits (Secondary Sample Point (SSP))
111 1111 = -64 x TSYS
...
011 1111 = 63 x TSYS
...
000 0000 = 0 x TSYS

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **TDCV<5:0>:** Transmitter Delay Compensation Value bits (Secondary Sample Point (SSP))
11 1111 = FP
...
00 0000 = 0 x FP

Note 1: This register can only be modified in Configuration mode (OPMOD<2:0> = 100).

REGISTER 3-180: ADCMPxENL: ADC DIGITAL COMPARATOR x CHANNEL ENABLE REGISTER LOW (x = 0, 1, 2, 3)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMPEN<15:8>							
bit 15							bit 8

R/W/0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMPEN<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **CMPEN<15:0>:** Comparator Enable for Corresponding Input Channel bits
1 = Conversion result for corresponding channel is used by the comparator
0 = Conversion result for corresponding channel is not used by the comparator

REGISTER 3-181: ADCMPxENH: ADC DIGITAL COMPARATOR x CHANNEL ENABLE REGISTER HIGH (x = 0, 1, 2, 3)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	CMPEN<20:16>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4-0 **CMPEN<20:16>:** Comparator Enable for Corresponding Input Channel bits
1 = Conversion result for corresponding channel is used by the comparator
0 = Conversion result for corresponding channel is not used by the comparator

REGISTER 3-189: PTGT1LIM: PTG TIMER1 LIMIT REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT1LIM<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT1LIM<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTGT1LIM<15:0>:** PTG Timer1 Limit Register bits
General Purpose Timer1 Limit register.

Note 1: These bits are read-only when the module is executing Step commands.

REGISTER 3-190: PTGSDLIM: PTG STEP DELAY LIMIT REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGSDLIM<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGSDLIM<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTGSDLIM<15:0>:** PTG Step Delay Limit Register bits
This register holds a PTG Step delay value representing the number of additional PTG clocks between the start of a Step command and the completion of a Step command.

Note 1: These bits are read-only when the module is executing Step commands.

REGISTER 4-32: CNSTATx: INTERRUPT CHANGE NOTIFICATION STATUS FOR PORTx REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
CNSTATx<15:8>							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
CNSTATx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **CNSTAT<15:0>:** Interrupt Change Notification Status for PORTx bits
When CNSTYLE (CNCONx<11>) = 0:
1 = Change occurred on PORTx[n] since last read of PORTx[n]
0 = Change did not occur on PORTx[n] since last read of PORTx[n]

REGISTER 4-33: CNEN1x: INTERRUPT CHANGE NOTIFICATION EDGE SELECT FOR PORTx REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNEN1x<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNEN1x<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **CNEN1x<15:0>:** Interrupt Change Notification Edge Select for PORTx bits

REGISTER 4-41: RPINR5: PERIPHERAL PIN SELECT INPUT REGISTER 5

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ICM3R7	ICM3R6	ICM3R5	ICM3R4	ICM3R3	ICM3R2	ICM3R1	ICM3R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TCKI3R7	TCKI3R6	TCKI3R5	TCKI3R4	TCKI3R3	TCKI3R2	TCKI3R1	TCKI3R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **ICM3R<7:0>:** Assign SCCP Capture 3 (S1ICM3) to the Corresponding S1RPn Pin bits
See Table 4-27.

bit 7-0 **TCKI3R<7:0>:** Assign SCCP Timer3 (S1TCKI3) to the Corresponding S1RPn Pin bits
See Table 4-27.

REGISTER 4-42: RPINR6: PERIPHERAL PIN SELECT INPUT REGISTER 6

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ICM4R7	ICM4R6	ICM4R5	ICM4R4	ICM4R3	ICM4R2	ICM4R1	ICM4R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TCKI4R7	TCKI4R6	TCKI4R5	TCKI4R4	TCKI4R3	TCKI4R2	TCKI4R1	TCKI4R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **ICM4R<7:0>:** Assign SCCP Capture 4 (S1ICM4) to the Corresponding S1RPn Pin bits
See Table 4-27.

bit 7-0 **TCKI4R<7:0>:** Assign SCCP Timer4 (S1TCKI4) to the Corresponding S1RPn Pin bits
See Table 4-27.

REGISTER 4-49: RPINR20: PERIPHERAL PIN SELECT INPUT REGISTER 20

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SCK1R7	SCK1R6	SCK1R5	SCK1R4	SCK1R3	SCK1R2	SCK1R1	SCK1R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SDI1R7	SDI1R6	SDI1R5	SDI1R4	SDI1R3	SDI1R2	SDI1R1	SDI1R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **SCK1R<7:0>:** Assign SPI1 Clock Input (S1SCK1) to the Corresponding S1RPn Pin bits
See Table 4-27.

bit 7-0 **SDI1R<7:0>:** Assign SPI1 Data Input (S1SDI1) to the Corresponding S1RPn Pin bits
See Table 4-27.

REGISTER 4-50: RPINR21: PERIPHERAL PIN SELECT INPUT REGISTER 21

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
REFOIR7	REFOIR6	REFOIR5	REFOIR4	REFOIR3	REFOIR2	REFOIR1	REFOIR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SS1R7	SS1R6	SS1R5	SS1R4	SS1R3	SS1R2	SS1R1	SS1R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **REFOIR<7:0>:** Assign Reference Clock Input (S1REFOI) to the Corresponding S1RPn Pin bits
See Table 4-27.

bit 7-0 **SS1R<7:0>:** Assign SPI1 Slave Select ($\overline{\text{S1SS1}}$) to the Corresponding S1RPn Pin bits
See Table 4-27.

REGISTER 6-2: CLKDIV: CLOCK DIVIDER REGISTER (MASTER) (CONTINUED)

bit 3-0 **PLLPRE<3:0>:** PLL Phase Detector Input Divider Select bits (also denoted as 'N1', PLL prescaler)(4)
11111 = Reserved
...
1001 = Reserved
1000 = Input divided by 8
0111 = Input divided by 7
0110 = Input divided by 6
0101 = Input divided by 5
0100 = Input divided by 4
0011 = Input divided by 3
0010 = Input divided by 2
0001 = Input divided by 1 (power-on default selection)
0000 = Reserved

Note 1: The DOZE<2:0> bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored.

2: This bit is cleared when the ROI bit is set and an interrupt occurs.

3: The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.

4: PLLPRE<3:0> may be updated while the PLL is operating, but the VCO may overshoot.

REGISTER 6-19: REFOCONL: REFERENCE CLOCK CONTROL LOW REGISTER (SLAVE)

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	HC/R/W-0	HSC/R-0
ROEN	—	ROSIDL	ROOUT	ROSLP	—	ROSWEN	ROACTIV
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	ROSEL3	ROSEL2	ROSEL1	ROSEL0
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ROEN:** Reference Clock Enable bit
1 = Reference Oscillator is enabled on the REFCLKO pin
0 = Reference Oscillator is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **ROSIDL:** Reference Clock Stop in Idle bit
1 = Reference Oscillator is disabled in Idle mode
0 = Reference Oscillator continues to run in Idle mode

bit 12 **ROOUT:** Reference Clock Output Enable bit
1 = Reference clock external output is enabled and available on the REFCLKO pin
0 = Reference clock external output is disabled

bit 11 **ROSLP:** Reference Clock Stop in Sleep bit
1 = Reference Oscillator continues to run in Sleep modes
0 = Reference Oscillator is disabled in Sleep modes

bit 10 **Unimplemented:** Read as '0'

bit 9 **ROSWEN:** Reference Clock Output Enable bit
1 = Clock divider change (requested by changes to RODIVx) is requested or is in progress (set in software, cleared by hardware upon completion)
0 = Clock divider change has completed or is not pending

bit 8 **ROACTIV:** Reference Clock Status bit
1 = Reference clock is active; do not change clock source
0 = Reference clock is stopped; clock source and configuration may be safely changed

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **ROSEL<3:0>:** Reference Clock Source Select bits
1111 =
... = Reserved
1000 = Reserved
0111 = REFI pin
0110 = FVCO/4
0101 = BFRC
0100 = LPRC
0011 = FRC
0010 = Primary Oscillator
0001 = Peripheral clock (FP)
0000 = System clock (FOSC)

REGISTER 7-6: PMD6: MASTER PERIPHERAL MODULE DISABLE 6 CONTROL REGISTER HIGH

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DMA5MD	DMA4MD	DMA3MD	DMA2MD	DMA1MD	DMA0MD
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **DMA5MD:** DMA5 Module Disable bit
1 = DMA5 module is disabled
0 = DMA5 module is enabled

bit 12 **DMA4MD:** DMA4 Module Disable bit
1 = DMA4 module is disabled
0 = DMA4 module is enabled

bit 11 **DMA3MD:** DMA3 Module Disable bit
1 = DMA3 module is disabled
0 = DMA3 module is enabled

bit 10 **DMA2MD:** DMA2 Module Disable bit
1 = DMA2 module is disabled
0 = DMA2 module is enabled

bit 9 **DMA1MD:** DMA1 Module Disable bit
1 = DMA1 module is disabled
0 = DMA1 module is enabled

bit 8 **DMA0MD:** DMA0 Module Disable bit
1 = DMA0 module is disabled
0 = DMA0 module is enabled

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 9-6: MPER: MASTER PERIOD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MPER<15:8>(1)							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MPER<7:0>(1)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **MPER<15:0>:** Master Period Register bits(1)

Note 1: Period values less than '0x0010' should not be selected.

REGISTER 9-14: PGxSTAT: PWM GENERATOR x STATUS REGISTER (CONTINUED)

bit 5 **CAP:** Capture Status bit(1)
1 = PWM Generator time base value has been captured in PGxCAP
0 = No capture has occurred

bit 4 **UPDATE:** PWM Data Register Update Status/Control bit
1 = PWM Data register update is pending – user Data registers are not writable
0 = No PWM Data register update is pending

bit 3 **UPDREQ:** PWM Data Register Update Request bit
User software writes a '1' to this bit location to request a PWM Data register update. The bit location always reads as '0'. The UPDATE status bit will indicate '1' when an update is pending.

bit 2 **STEER:** Output Steering Status bit (Push-Pull Output mode only)
1 = PWM Generator is in 2nd cycle of Push-Pull mode
0 = PWM Generator is in 1st cycle of Push-Pull mode

bit 1 **CAHALF:** Half Cycle Status bit (Center-Aligned modes only)
1 = PWM Generator is in 2nd half of time base cycle
0 = PWM Generator is in 1st half of time base cycle

bit 0 **TRIG:** PWM Trigger Status bit
1 = PWM Generator is triggered and PWM cycle is in progress
0 = No PWM cycle is in progress

Note 1: User software may write a '1' to CAP as a request to initiate a software capture. The CAP status bit will be set when the capture event has occurred. No further captures will occur until CAP is cleared by software.

REGISTER 12-2: QEIxIOCL: QEIx I/O CONTROL LOW REGISTER (CONTINUED)

bit 6 **IDXPOL:** INDXx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

bit 5 **QEBPOL:** QEBx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

bit 4 **QEAPOL:** QEAx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

bit 3 **HOME:** Status of HOMEx Input Pin after Polarity Control bit (read-only)
1 = Pin is at logic '1' if the HOMPOL bit is set to '0'; pin is at logic '0' if the HOMPOL bit is set to '1'
0 = Pin is at logic '0' if the HOMPOL bit is set to '0'; pin is at logic '1' if the HOMPOL bit is set to '1'

bit 2 **INDEX:** Status of INDXx Input Pin After Polarity Control bit (read-only)
1 = Pin is at logic '1' if the IDXPOL bit is set to '0'; pin is at logic '0' if the IDXPOL bit is set to '1'
0 = Pin is at logic '0' if the IDXPOL bit is set to '0'; pin is at logic '1' if the IDXPOL bit is set to '1'

bit 1 **QEB:** Status of QEBx Input Pin After Polarity Control and SWPAB Pin Swapping bit (read-only)
1 = Physical pin, QEBx, is at logic '1' if the QEBPOL bit is set to '0' and the SWPAB bit is set to '0';
physical pin, QEBx, is at logic '0' if the QEBPOL bit is set to '1' and the SWPAB bit is set to '0';
physical pin, QEAx, is at logic '1' if the QEBPOL bit is set to '0' and the SWPAB bit is set to '1';
physical pin, QEAx, is at logic '0' if the QEBPOL bit is set to '1' and the SWPAB bit is set to '1'
0 = Physical pin, QEBx, is at logic '0' if the QEBPOL bit is set to '0' and the SWPAB bit is set to '0';
physical pin, QEBx, is at logic '1' if the QEBPOL bit is set to '1' and the SWPAB bit is set to '0';
physical pin, QEAx, is at logic '0' if the QEBPOL bit is set to '0' and the SWPAB bit is set to '1';
physical pin, QEAx, is at logic '1' if the QEBPOL bit is set to '1' and the SWPAB bit is set to '1'

bit 0 **QEA:** Status of QEAx Input Pin After Polarity Control and SWPAB Pin Swapping bit (read-only)
1 = Physical pin, QEAx, is at logic '1' if the QEAPOL bit is set to '0' and the SWPAB bit is set to '0';
physical pin, QEAx, is at logic '0' if the QEAPOL bit is set to '1' and the SWPAB bit is set to '0';
physical pin, QEBx, is at logic '1' if the QEAPOL bit is set to '0' and the SWPAB bit is set to '1';
physical pin, QEBx, is at logic '0' if the QEAPOL bit is set to '1' and the SWPAB bit is set to '1'
0 = Physical pin, QEAx, is at logic '0' if the QEAPOL bit is set to '0' and the SWPAB bit is set to '0';
physical pin, QEAx, is at logic '1' if the QEAPOL bit is set to '1' and the SWPAB bit is set to '0';
physical pin, QEBx, is at logic '0' if the QEAPOL bit is set to '0' and the SWPAB bit is set to '1'

20.1 Current Bias Generator Control Registers

REGISTER 20-1: BIASCON: CURRENT BIAS GENERATOR CONTROL REGISTER

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
ON	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	I10EN3	I10EN2	I10EN1	I10EN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ON:** Current Bias Module Enable bit
1 = Module is enabled
0 = Module is disabled

bit 14-4 **Unimplemented:** Read as '0'

bit 3 **I10EN3:** 10 µA Enable for Output 3 bit
1 = 10 µA output is enabled
0 = 10 µA output is disabled

bit 2 **I10EN2:** 10 µA Enable for Output 2 bit
1 = 10 µA output is enabled
0 = 10 µA output is disabled

bit 1 **I10EN1:** 10 µA Enable for Output 1 bit
1 = 10 µA output is enabled
0 = 10 µA output is disabled

bit 0 **I10EN0:** 10 µA Enable for Output 0 bit
1 = 10 µA output is enabled
0 = 10 µA output is disabled

TABLE 21-2: MASTER CONFIGURATION REGISTERS MAP

Register Name	Bits 23-16	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FSEC	—	AIVTDIS	—	—	—	CSS2	CSS1	CSS0	CWRP	GSS1	GSS0	GWRP	—	BSEN	BSS1	BSS0	BWRP
FBSLIM	—	—	—	—	BSLIM<12:0>												
FSIGN	—	r(2)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
FOSCSEL	—	—	—	—	—	—	—	—	—	IESO	—	—	—	—	FNOSC2	FNOSC1	FNOSC0
FOSC	—	—	—	—	XTBST	XTCFG1	XTCFG0	—	r(1)	FCKSM1	FCKSM0	—	—	—	OSCIOFNC	POSCMD1	POSCMD0
FWDT	—	FWDTEN	SWDTPS4	SWDTPS3	SWDTPS2	SWDTPS1	SWDTPS0	WDTWIN1	WDTWIN0	WINDIS	RCLKSEL1	RCLKSEL0	RWDTPS4	RWDTPS3	RWDTPS2	RWDTPS1	RWDTPS0
FPOR	—	—	—	—	—	—	—	—	—	—	—	r(1)	r(1)	—	—	—	—
FICD	—	—	—	—	—	—	—	—	—	r(1)	—	JTAGEN	—	—	—	ICS1	ICS0
FDMTIVTL	—	DMTIVT<15:0>															
FDMTIVTH	—	DMTIVT<31:16>															
FDMTCNTL	—	DMTCNT<15:0>															
FDMTCNTH	—	DMTCNT<31:16>															
FDMT	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DMTDIS
FDEVOPT	—	—	—	SPI2PIN	—	—	SMBEN	r(1)	r(1)	r(1)	—	—	ALTI2C2	ALTI2C1	r(1)	—	—
FALTREG	—	—	CTXT4<2:0>			—	CTXT3<2:0>			—	CTXT2<2:0>			—	CTXT1<2:0>		
FMBXM	—	MBXM<15:0>															
FMBXHS1	—	MBXHSD3	MBXHSD2	MBXHSD1	MBXHSD0	MBXHSC3	MBXHSC2	MBXHSC1	MBXHSC0	MBXHSB3	MBXHSB2	MBXHSB1	MBXHSB0	MBXHSA3	MBXHSA2	MBXHSA1	MBXHSA0
FMBXHS2	—	MBXHSH3	MBXHSH2	MBXHSH1	MBXHSH0	MBXHSG3	MBXHSG2	MBXHSG1	MBXHSG0	MBXHSF3	MBXHSF2	MBXHSF1	MBXHSF0	MBXHSE3	MBXHSE2	MBXHSE1	MBXHSE0
FMBXHSEN	—	—	—	—	—	—	—	—	—	HS<H:A>EN							
FCFGPRA0	—	—	—	—	—	—	—	—	—	—	—	—	CPRA<4:0>				
FCFGPRB0	—	CPRB<15:0>															
FCFGPRC0	—	CPRC<15:0>															
FCFGPRD0	—	CPRD<15:0>															
FCFGPRE0	—	CPRE<15:0>															

Legend: — = unimplemented bit, read as '1'; r = reserved bit.

Note 1: Bit is reserved, maintain as '1'.

2: Bit is reserved, maintain as '0'.

TABLE 22-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles(1)	Status Flags Affected
19	CLR	CLR	f	f = 0x0000	1	1	None
		CLR	WREG	WREG = 0x0000	1	1	None
		CLR	Ws	Ws = 0x0000	1	1	None
		CLR	Acc,Wx,Wxd,Wy,Wyd,AWB	Clear Accumulator	1	1	OA,OB,SA,SB
20	CLRWDT	CLRWDT		Clear Watchdog Timer	1	1	WDTO,Sleep
21	COM	COM	f	f = $\bar{f}$	1	1	N,Z
		COM	f,WREG	WREG = $\bar{f}$	1	1	N,Z
		COM	Ws,Wd	Wd = $\overline{Ws}$	1	1	N,Z
22	CP	CP	f	Compare f with WREG	1	1	C,DC,N,OV,Z
		CP	Wb,#lit8	Compare Wb with lit8	1	1	C,DC,N,OV,Z
		CP	Wb,Ws	Compare Wb with Ws (Wb – Ws)	1	1	C,DC,N,OV,Z
23	CP0	CP0	f	Compare f with 0x0000	1	1	C,DC,N,OV,Z
		CP0	Ws	Compare Ws with 0x0000	1	1	C,DC,N,OV,Z
24	CPB	CPB	f	Compare f with WREG, with Borrow	1	1	C,DC,N,OV,Z
		CPB	Wb,#lit8	Compare Wb with lit8, with Borrow	1	1	C,DC,N,OV,Z
		CPB	Wb,Ws	Compare Wb with Ws, with Borrow (Wb – Ws – $\overline{C}$)	1	1	C,DC,N,OV,Z
25	CPSEQ	CPSEQ	Wb,Wn	Compare Wb with Wn, Skip if =	1	1 (2 or 3)	None
	CPBEQ	CPBEQ	Wb,Wn,Expr	Compare Wb with Wn, Branch if =	1	1 (5)	None
26	CPSGT	CPSGT	Wb,Wn	Compare Wb with Wn, Skip if >	1	1 (2 or 3)	None
	CPBGT	CPBGT	Wb,Wn,Expr	Compare Wb with Wn, Branch if >	1	1 (5)	None
27	CPSLT	CPSLT	Wb,Wn	Compare Wb with Wn, Skip if <	1	1 (2 or 3)	None
		CPBLT	Wb,Wn,Expr	Compare Wb with Wn, Branch if <	1	1 (5)	None
28	CPSNE	CPSNE	Wb,Wn	Compare Wb with Wn, Skip if ≠	1	1 (2 or 3)	None
		CPBNE	Wb,Wn,Expr	Compare Wb with Wn, Branch if ≠	1	1 (5)	None
29	CTXTSWP	CTXTSWP	#1it3	Switch CPU Register Context to Context Defined by lit3	1	2	None
30	CTXTSWP	CTXTSWP	Wn	Switch CPU Register Context to Context Defined by Wn	1	2	None
31	DAW.B	DAW.B	Wn	Wn = Decimal Adjust Wn	1	1	C
32	DEC	DEC	f	f = f – 1	1	1	C,DC,N,OV,Z
		DEC	f,WREG	WREG = f – 1	1	1	C,DC,N,OV,Z
		DEC	Ws,Wd	Wd = Ws – 1	1	1	C,DC,N,OV,Z
33	DEC2	DEC2	f	f = f – 2	1	1	C,DC,N,OV,Z
		DEC2	f,WREG	WREG = f – 2	1	1	C,DC,N,OV,Z
		DEC2	Ws,Wd	Wd = Ws – 2	1	1	C,DC,N,OV,Z
34	DISI	DISI	#lit14	Disable Interrupts for k Instruction Cycles	1	1	None
35	DIVF	DIVF	Wm,Wn	Signed 16/16-bit Fractional Divide	1	18/6	N,Z,C,OV
36	DIV.S	DIV.S	Wm,Wn	Signed 16/16-bit Integer Divide	1	18/6	N,Z,C,OV
		DIV.SD	Wm,Wn	Signed 32/16-bit Integer Divide	1	18/6	N,Z,C,OV
37	DIV.U	DIV.U	Wm,Wn	Unsigned 16/16-bit Integer Divide	1	18/6	N,Z,C,OV
		DIV.UD	Wm,Wn	Unsigned 32/16-bit Integer Divide	1	18/6	N,Z,C,OV
38	DIVF2	DIVF2	Wm,Wn	Signed 16/16-bit Fractional Divide (W1:W0 preserved)	1	6	N,Z,C,OV
39	DIV2.S	DIV2.S	Wm,Wn	Signed 16/16-bit Integer Divide (W1:W0 preserved)	1	6	N,Z,C,OV
		DIV2.SD	Wm,Wn	Signed 32/16-bit Integer Divide (W1:W0 preserved)	1	6	N,Z,C,OV

Note 1: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.
2: Cycle times for Slave core are different for Master core, as shown in 2.
3: For dsPIC33CH128MP508 devices, the divide instructions must be preceded with a "REPEAT #5" instruction, such that they are executed six consecutive times

TABLE 24-11: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD})

DC CHARACTERISTICS	Master Sleep + Slave Sleep		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended		
Parameter No.	**Typ.**	**Max.**	**Units**	**Conditions**	
Power-Down Current (I_{PD})(1)					
DC60	3.2	4.8	mA	-40°C	3.3V
	3.4	8.2	mA	+25°C	
	3.7	14.3	mA	+85°C	
	7.6	21.5	mA	+125°C	

Note 1: I_{PD} (Sleep) current is measured as follows:

- CPU core is off, oscillator is configured in EC mode and External Clock is active; OSCI is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as output low
- $\overline{MCLR}$ = V_{DD}, WDT and FSCM are disabled
- All peripheral modules are disabled (PMDx bits are all set)
- The VREGS bit (RCON<8>) = 0 (i.e., core regulator is set to standby while the device is in Sleep mode)
- JTAG is disabled

TABLE 24-12: DC CHARACTERISTICS: WATCHDOG TIMER DELTA CURRENT (ΔI_{WDT})(1)

DC CHARACTERISTICS	Master and Slave		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended		
Parameter No.	**Typ.**	**Max.**	**Units**	**Conditions**	
DC61d	2.9	—	µA	-40°C	3.3V
DC61a	2.7	—	µA	+25°C	
DC61b	3.9	—	µA	+85°C	
DC61c	5.5	—	µA	+125°C	

Note 1: The ΔI_{WDT} current is the additional current consumed when the module is enabled. This current should be added to the base I_{PD} current. All parameters are characterized but not tested during manufacturing.

FIGURE 24-17: UARTx MODULE I/O TIMING CHARACTERISTICS

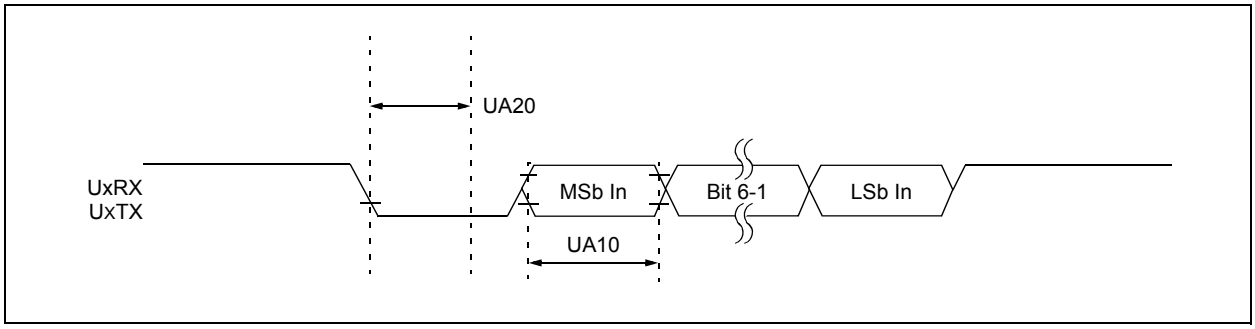

TABLE 24-42: UARTx MODULE I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
UA10	TUABAUD	UARTx Baud Time	66.67	—	—	ns	
UA11	FBAUD	UARTx Baud Frequency	—	—	15	Mbps	
UA20	TCWF	Start Bit Pulse Width to Trigger UARTx Wake-up	500	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in “Typ.” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.