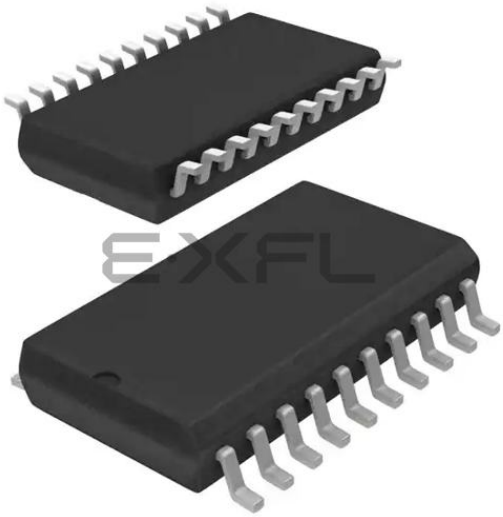

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40MHz
Connectivity	-
Peripherals	POR, PWM, WDT
Number of I/O	11
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89eb5114-tgsil

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
TMOD	89h	Timer/Counter Mode Register	GATE1	C/T1#	M11	M01	GATE0	C/T0#	M10	M00
W0CH	ECh	PWMU0 Counter High Control	W0C15	W0C14	W0C13	W0C12	W0C11	W0C10	W0C9	W0C8
W0CL	EDh	PWMU0 Counter Low Control	W0C7	W0C6	W0C5	W0C4	W0C3	W0C2	W0C1	W0C0
W0CON	E8h	PWMU0 Control Register	W0UP	W0R	-	-	W0OS	W0EN2	W0EN1	W0EN0
W0FH	EAh	PWMU0 Frequency High Control	W0F15	W0F14	W0F13	W0F12	W0F11	W0F10	W0F9	W0F8
W0FL	EBh	PWMU0 Frequency Low Control	W0F7	W0F6	W0F5	W0F4	W0F3	W0F2	W0F1	W0F0
W0IC	EEh	PWMU0 Interrupt Configuration	W0CF	W0CF2	W0CF2	W0CF0	W0ECF	W0ECF2	W0ECF1	W0ECF0
W0MOD	E9h	PWMU0 Counter Mode Register	W0CPS1	W0CPS0	-	-	-	W0INV2	W0INV1	W0INV0
W0R0H	D9h	PWMU0 Module 0 High Toggle	W0R0H15	W0R0H14	W0R0H13	W0R0H12	W0R0H11	W0R0H10	W0R0H9	W0R0H8
W0R0L	DAh	PWMU0 Module 0 Low Toggle	W0R0H7	W0R0H6	W0R0H5	W0R0H4	W0R0H3	W0R0H2	W0R0H1	W0R0H0
W0R1H	DBh	PWMU0 Module 1High Toggle	W0R1H15	W0R1H14	W0R1H13	W0R1H12	W0R1H11	W0R1H10	W0R1H9	W0R1H8
W0R1L	DCh	PWMU0 Module1 Low Toggle	W0R1H7	W0R1H6	W0R1H5	W0R1H4	W0R1H3	W0R1H2	W0R1H1	W0R1H0
W0R2H	DDh	PWMU0 Module 2 High Toggle	W0R2H15	W0R2H14	W0R2H13	W0R2H12	W0R2H11	W0R2H10	W0R2H9	W0R2H8
W0R2L	DEh	PWMU0 Module 2 Low Toggle	W0R2H7	W0R2H6	W0R2H5	W0R2H4	W0R2H3	W0R2H2	W0R2H1	W0R2H0
W1CH	FCh	PWMU1 Counter High Control	W1C15	W1C14	W1C13	W1C12	W1C11	W1C10	W1C9	W1C8
W1CL	FDh	PWMU1 Counter Low Control	W1C7	W1C6	W1C5	W1C4	W1C3	W1C2	W1C1	W1C0
W1CON	F8h	PWMU1 Control Register	W1UP	W1R	-	W1OCLK	W1CPS1	W1CPS0	W1INV0	W1EN0
W1FH	FAh	PWMU1 Frequency High Control	W1F15	W1F14	W1F13	W1F12	W1F11	W1F10	W1F9	W1F8
W1FL	FBh	PWMU1 Frequency Low Control	W1F7	W1F6	W1F5	W1F4	W1F3	W1F2	W1F1	W1F0
W1IC	FEh	PWMU1 Interrupt Configuration	W1CF	-	-	W1CF0	W1ECOF	-	-	W0ECF0
W1R0H	C9h	PWMU1 Module 0 High Toggle	W1R0H15	W1R0H14	W1R0H13	W1R0H12	W1R0H11	W1R0H10	W1R0H9	W1R0H8
W1R0L	CAh	PWMU1 Module 0 Low Toggle	W1R0H7	W1R0H6	W1R0H5	W1R0H4	W1R0H3	W1R0H2	W1R0H1	W1R0H0
WDTRST	A6h	Watchdog Timer enable Register								
WDTPRG	A7h	WatchDog Timer Duration Prg	-	-	-	-	-	S2	S1	S0

Power Monitor

The Power Monitor function supervises the evolution of the voltages feeding the microcontroller, and if needed, suspends its activity when the detected value is out of specification.

It warrants proper startup when AT8xEB5114 is powered up and prevents code execution errors when the power supply becomes lower than the functional threshold.

This chapter describes the functions of the power monitor.

Description

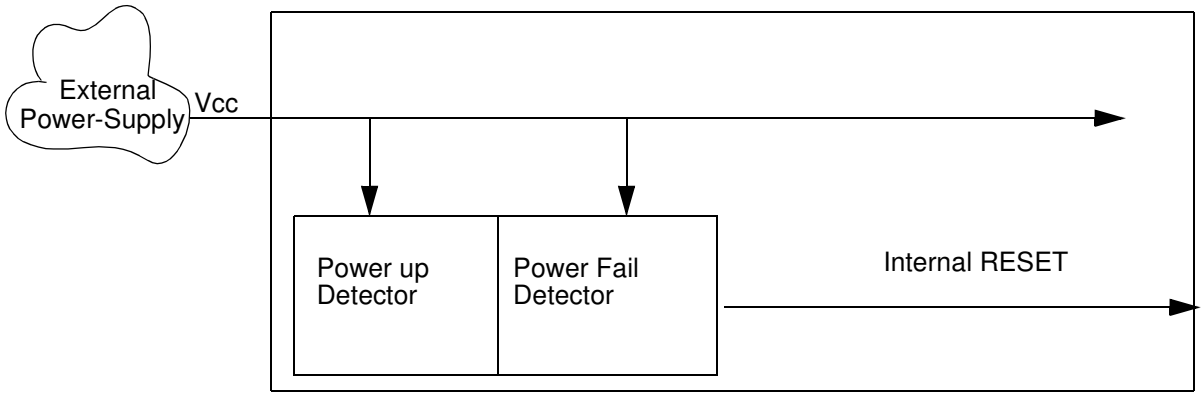
In order to startup and to properly maintain the microcontroller operation, Vcc has to be stabilized in the Vcc operating range and the oscillator has to be stabilized with a nominal amplitude compatible with logic threshold.

In order to be sure the oscillator is stabilized, there is an internal counter which maintains the reset during 1024 clock periods in case the oscillator selected is the OSC A and 64 clock periods in case the oscillator used is OSC B or OSC C.

This control is carried out during three phases: the power-up, normal operation and stop. In accordance with the following requirements:

- it guarantees an operational Reset when the microcontroller is powered-up, and
- a protection if the power supply goes below minimum operating Vcc

Figure 2. Power Monitor Block Diagram



Power Monitor diagram

The Power Monitor monitors the power-supply in order to detect any voltage drops which are not in the target specification. The power monitor block verifies two kinds of situation that may occur:

- during the power-up condition, when Vcc reaches the product specification,
- during a steady-state condition, when Vcc is at nominal value but disturbed by any undesired voltage drops.

Figure 2 shows some configurations which can be handled by the Power Monitor.

Crystal Oscillator: OSCA

The crystal oscillator uses two external pins, XTAL1 for input and XTAL2 for output.

OSCAEN in OSCCON register is an enable signal for the crystal oscillator or for the external oscillator input that can be provided on XTAL1.

High Accurate RC Oscillator: OSCB

The high accuracy RC oscillator needs external R and C components to assure the proper accuracy; its typical frequency is 12 MHz. Frequency accuracy is a function of external R and C accuracy. It is recommended to use 0.5% or better for R and 1% for C components. (Typical values are R = 49.9 K and C = 560 pF)

This oscillator has two modes.

- OSCBEN = 1 and LCKEN = 0: Standard accuracy mode(Typical frequency 12 MHz)
- OSCBEN = 1 and LCKEN = 1: High accuracy mode (Typical frequency 12 MHz).
  The OSCB oscillator is based on a low frequency RC oscillator and a VCO. When locked, the oscillator frequency is defined by the following formula:
  F = 3*[OSCBFA+1]/(R.C). with C including parasitic capacitances.
  Because the oscillator is based on a PLL, it needs several periods to reach its final accuracy. As soon as this accuracy is reached, the OSCBRY bit in OSCCON register is set by hardware.
  The internal frequency is locked on the external RC time constant. So it is possible to adjust frequency by lower than 1% steps with the OSCBFA register. However the frequency adjustment is limited to +/-15% around 12 MHz.
  The frequency can be adjusted until 15% around 12 MHz by OSCBFA Register.

OSCBEN and LCKEN are in the OSCCON register.

Low Power Consumption Oscillator: OSCC

The low power consumption RC oscillator doesn't need any external components. Moreover its consumption is very low. Its typical frequency is 14 MHz. Note that this on-chip oscillator has a +/- 40% frequency tolerance and may not be suitable for use in certain applications.

OSCC is set by OSCCEN bit in OSCCON.

Clock Selector

CKS1 and CKS0 bits in CKSEL register are used to select the clock source.

OSCCEN bit in OSCCON register is used to enable the low power consumption RC oscillator.

OSCBEN bit in OSCCON register is used to enable the high accurate RC oscillator.

OSCAEN bit in OSCCON register is used to enable the crystal oscillator or the external oscillator input.

X2 Feature

The AT8xEB5114 core needs only 6 clock periods per machine cycle. This feature called "X2" provides the following advantages:

- Divides frequency crystals by 2 (cheaper crystals) while keeping same CPU power.
- Saves power consumption while keeping same CPU power (oscillator power saving).
- Saves power consumption by dividing dynamically the operating frequency by 2 in operating and idle modes.
- Increases CPU power by 2 while keeping same crystal frequency.

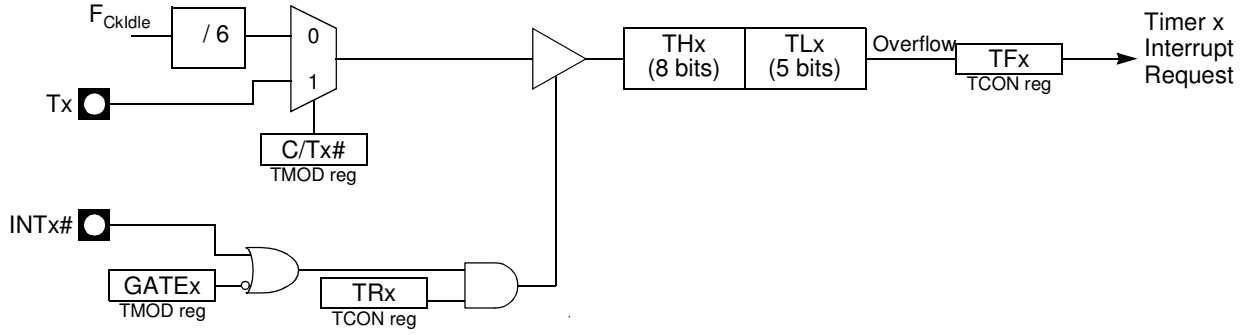
In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be enabled or disabled by software.

operation.
Timer 0 overflow (count rolls over from all 1s to all 0s) sets the TF0 flag and generates an interrupt request.
It is important to stop the Timer/Counter before changing modes.

Mode 0 (13-bit Timer)

Mode 0 configures Timer 0 as a 13-bit Timer which is set up as an 8-bit Timer (TH0 register) with a modulo-32 prescaler implemented with the lower five bits of the TL0 register (see Figure 7). The upper three bits of the TL0 register are indeterminate and should be ignored. Prescaler overflow increments the TH0 register.

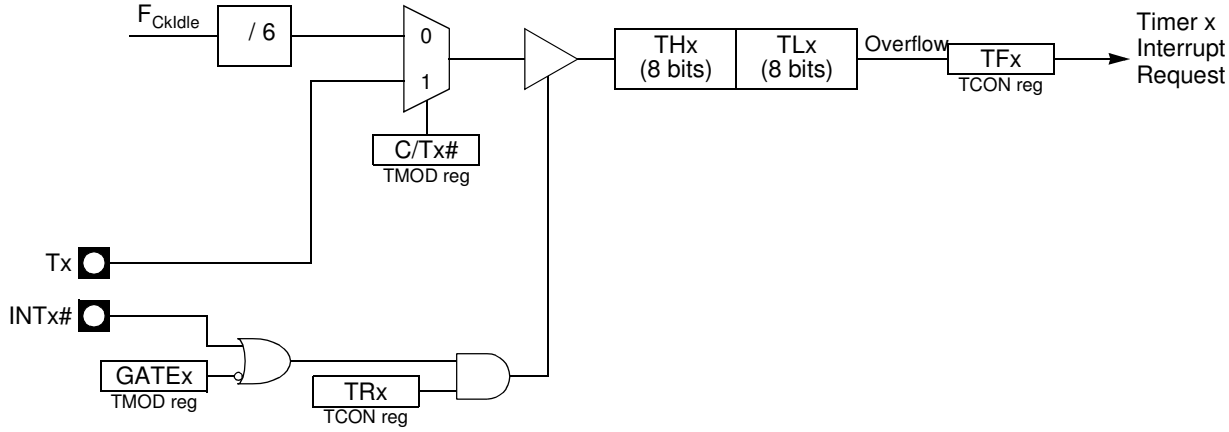
Figure 7. Timer/Counter x (x= 0 or 1) in Mode 0



Mode 1 (16-bit Timer)

Mode 1 configures Timer 0 as a 16-bit Timer with the TH0 and TL0 registers connected in a cascade (see Figure 8). The selected input increments the TL0 register.

Figure 8. Timer/Counter x (x = 0 or 1) in Mode 1



Mode 2 (8-bit Timer with Auto-Reload)

Mode 2 configures Timer 0 as an 8-bit Timer (TL0 register) that automatically reloads from the TH0 register on overflow (see Figure 9). TL0 overflow sets the TF0 flag in the TCON register and reloads TL0 with the contents of TH0, which is preset by the software. When the interrupt request is serviced, the hardware clears TF0. The reload leaves TH0 unchanged. The next reload value may be changed at any time by writing it to the TH0 register.

Table 15. TMOD Register

TMOD (S:89h)

Timer/Counter Mode Control Register.

7	6	5	4	3	2	1	0
GATE1	C/T1#	M11	M01	GATE0	C/T0#	M10	M00

Bit Number	Bit Mnemonic	Description
7	GATE1	**Timer 1 Gating Control bit** Clear to enable Timer counter 1 whenever TR1 bit is set. Set to enable Timer counter 1 only while INT1# pin is high and TR1 bit is set.
6	C/T1#	**Timer 1 Counter/Timer Select bit** Clear for Timer operation: Timer 1 counts the divided-down system clock. Set for Counter operation: Timer 1 counts negative transitions on external pin T1.
5	M11	**Timer 1 Mode Select bits** M11 M01 Operating mode 0 0 Mode 0: 8-bit Timer/Counter (TH1) with 5-bit prescaler (TL1). 0 1 Mode 1: 16-bit Timer/Counter. 1 0 Mode 2: 8-bit auto-reload Timer/Counter (TL1). Reloaded from TH1 at overflow. 1 1 Mode 3:Timer 1 halted. Retains count.
4	M01	
3	GATE0	**Timer 0 Gating Control bit** Clear to enable Timer counter 0 whenever TR0 bit is set. Set to enable Timer counter 0 only while INT0# pin is high and TR0 bit is set.
2	C/T0#	**Timer 0 Counter/Timer Select bit** Clear for Timer operation: Timer 0 counts the divided-down system clock. Set for Counter operation: Timer 0 counts negative transitions on external pin T0.
1	M10	**Timer 0 Mode Select bit** M10 M00 Operating mode 0 0 Mode 0:8-bit Timer/Counter (TH0) with 5-bit prescaler (TL0). 0 1 Mode 1:16-bit Timer/Counter. 1 0 Mode 2:8-bit auto-reload Timer/Counter (TL0). Reloaded from TH0 at overflow 1 1 Mode 3:TL0 is an 8-bit Timer/Counter TH0 is an 8-bit Timer using Timer 1's TR0 and TF0 bits.
0	M00	

Reset Value = 0000 0000b

Table 16. TH0 Register

TH0 (S:8Ch)

Timer 0 High Byte Register.

7	6	5	4	3	2	1	0

Bit Number	Bit Mnemonic	Description
7:0		**High Byte of Timer 0.**

Reset Value = 0000 0000b

Table 17. TL0 Register

TL0 (S:8Ah)

Timer 0 Low Byte Register.

7	6	5	4	3	2	1	0

Bit Number	Bit Mnemonic	Description
7:0		**Low Byte of Timer 0.**

Reset Value = 0000 0000b

Table 18. TH1 Register

TH1 (S:8Dh)
Timer 1 High Byte Register.

7	6	5	4	3	2	1	0

Bit Number	Bit Mnemonic	Description
7:0		**High Byte of Timer 1.**

Reset Value = 0000 0000b

Table 19. TL1 Register

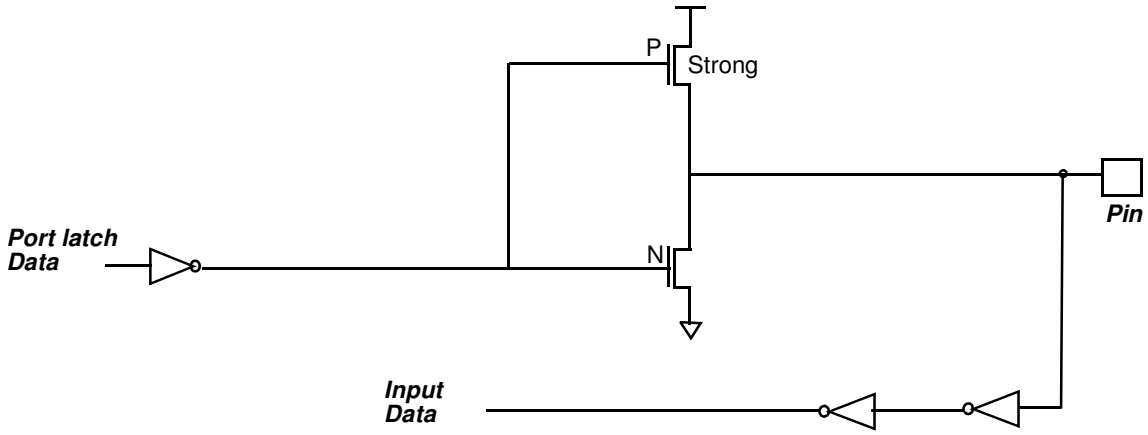
TL1 (S:8Bh)
Timer 1 Low Byte Register.

7	6	5	4	3	2	1	0

Bit Number	Bit Mnemonic	Description
7:0		**Low Byte of Timer 1.**

Reset Value = 0000 0000b

Figure 13. Push-Pull Output

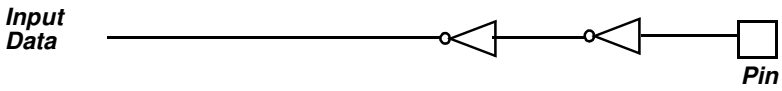


Input only Configuration

The input only configuration is a pure input with neither pull-up nor pull-down.

The input only configuration is shown in Figure 13.

Figure 14. Input only



Ports Description

Ports P3 and P4

The inputs of each I/O port of the AT8xEB5114 are TTL level Schmitt triggers with hysteresis.

Table 36. W1FL: PWMU1 frequency low control register
W1FL - PWMU1 Frequency Control Register (FBh)

7	6	5	4	3	2	1	0
W1F7	W1F6	W1F5	W1F4	W1F3	W1F2	W1F1	W1F0

Bit Number	Bit Mnemonic	Description
7-0	W1F7-0	**PWMU1 low bits counter control frequency** The PWMU1 counter is counting from zero up to W1F15-0 value.

Reset Value = 1111 1111b
Not bit addressable

Table 37. W1CH: PWMU1 counter high control register
W1CH - PWMU1 Counter Control Register (FCh)

7	6	5	4	3	2	1	0
W1C15	W1C14	W1C13	W1C12	W1C11	W1C10	W1C9	W1C8

Bit Number	Bit Mnemonic	Description
7-0	W1C15-8	**PWMU1 high bits counter frequency**

Reset Value = 0000 0000b
Not bit addressable

Table 38. W1CL: PWMU1 counter low control register
W1CL - PWMU1 Counter Control Register (FDh)

7	6	5	4	3	2	1	0
W1C7	W1C6	W1C5	W1C4	W1C3	W1C2	W1C1	W1C0

Bit Number	Bit Mnemonic	Description
7-0	W1F7-0	**PWMU1 low bits counter frequency**

Reset Value = 0000 0000b
Not bit addressable

PWMU1 Output Generation

All the PWMU1 modules have the same frequency determined by the W1F registers. However, each module has is own duty cycle determined by the W1Rn Registers. (n is the module number).

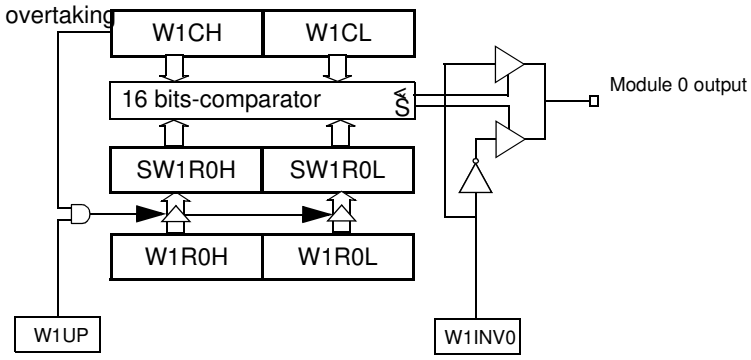
When the W1C content is lower than the value programmed via W1Rn registers, the output is the W1INVn-bit (low if 0, high if 1). When it is equal or higher, the output is the opposite of this W1INVn-bit (high if 0, low if 1).

When the W1C content is higher than SW1F's, an overtaking occurs. The counter value (W1C registers) is automatically reloaded with zero (see Figure 21.). If the W1UP bit is high, the new comparison value is reloaded on the shadow SW1R0 registers with the

content of the W1R0 registers (see Figure 21.). This method allows to change frequency and duty cycle without glitch.

Note: If the PWMU1 is Off (W1R bit in W0CON not set), W1RnH and W1RnL contents are automatically copied on the shadow registers SW1RnH and SW1RnLn and the contents of W1FH and W1FL are automatically copied on the shadow registers SW1FH and SW1FL. This allows to charge the correct comparison values for each PWM module as soon as the PWMU1 timer/counter is turned on.

Figure 21. PWMU1 Interrupt System



The W1INV0 bit that allows output inversion is on the W1CON (W1 Control) register (See Table 34.).

Table 39. W1R0H: PWMU1 module 0 High Toggle Register
W1R0H - PWMU1 Module 0 High Toggle Register (C9h)

7	6	5	4	3	2	1	0
W1R0H15	**W1R0H14**	**W1R0H13**	**W1R0H12**	**W1R0H11**	**W1R0H10**	**W1R0H9**	**W1R0H8**

Bit Number	Bit Mnemonic	Description
7-0	W1R0H 15-8	**PWMU1 Module 0 high toggle register** When the counter exceeds this value, module 0 output toggles.

Reset Value = 0000 0000b
Not bit addressable

Table 40. W1R0L: PWMU1 module 0 Low Toggle Register
W1R0L - PWMU1 Module 0 Low Toggle Register (CAh)

7	6	5	4	3	2	1	0
W1R0L7	**W1R0L6**	**W1R0L5**	**W1R0L4**	**W1R0L3**	**W1R0L2**	**W1R0L1**	**W1R0L0**

Bit Number	Bit Mnemonic	Description
7-0	W1R0L7-0	**PWMU1 Module 0 low toggle register** When the counter exceeds this value, module 0 output toggles.

Reset Value = 0000 0000b
Not bit addressable

Find Hereafter computed Time-Out value for Fosc = 12 MHz

Table 42. Time-Out Computation @12 MHz

S2	S1	S0	Time-Out for F_{OSC}=12 MHz
0	0	0	16.38 ms
0	0	1	32.77 ms
0	1	0	65.54 ms
0	1	1	131.07 ms
1	0	0	262.14 ms
1	0	1	524.29 ms
1	1	0	1.05 s
1	1	1	2.10 s

Table 43. WDTRST Register

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Reset Value = XXXX XXXXb

The WDTRST register is used to reset/enable the WDT by writing 1EH then E1H in sequence.

WatchDog Timer During Power Down Mode and Idle

In Power Down mode the oscillator stops, which means the WDT also stops. While in Power Down mode the user does not need to service the WDT. There are 2 methods of exiting Power Down mode: by a hardware reset or via a level activated external interrupt which is enabled prior to entering Power Down mode. When Power Down is exited with hardware reset, servicing the WDT should occur as it normally does whenever AT8xEB5114 is reset. Exiting Power Down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power Down.

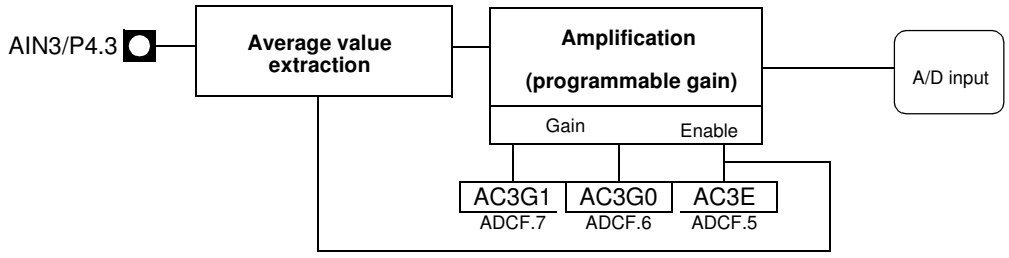
To ensure that the WDT does not overflow within a few states of exiting of power down, it is best to reset the WDT just before entering power down.

In the Idle mode, the oscillator continues to run. To prevent the WDT from resetting while in Idle mode, the user should always set up a timer that will periodically exit Idle, service the WDT, and re-enter Idle mode.

Channel 3 Amplifier and Rectifying Function

If needed, the average value of the rectified signal on channel 3 can be extracted and amplified before A/D conversion as shown on Figure 28.

Figure 28. Channel 3 Amplifier



The main characteristics of this block are the following:

- Input signal level: sine wave centered around Vssa, peak value from 70 to 550 mV depending on gain, Frequency range from 35 to 70KHz. Be sure that the peak value on the amplifier output is lower than voltage supply.
- Gain: x5, x10, x15 and x20, selected using AC3E, AC3G1 and AC3G0 in ADC Amplifier register (See Table 44 and Table 52)
- Max time constant of the average value extraction: 0.5ms. When the gain is changed or when the signal levels changes from the minimum to the maximum value, a new measurement can be done after 10 time constant.
- The amplifier needs 20us to fully load the ADC hold capacitance so the ADC conversion must occurs at least 20us after the amplified channel is sampled.
- Accuracy on amplification and extraction: +/- 5%

Note: The AIN3 direct channel is not equivalent to the other channels. There is a serial resistance of around 100KΩ between the pin and the ADC input. So when the amplifier is bypassed, it is necessary to switch at least 20us the mux on AIN3 input before starting a conversion.

Table 44. ADCF Register

ADCA (S:F7h)
ADC Amplifier Configuration

7	6	5	4	3	2	1	0
-	-	-	-	-	AC3E	AC3G1	AC3G0

Bit Number	Bit Mnemonic	Description
7-3	-	**Not used**
2	AC3E	**Enable Channel 3 amplifier** Set to enable amplifier. Clear for Standby mode
1	AC3G1	**Channel 3 amplifier gain** AC3G1 AC3G0 0 0 gain x5 0 1 gain x10 1 0 gain x15 1 1 gain x20
0	AC3G0	

Reset Value = 0000 0000b

Accuracy improvement on analog to digital conversion using the internal voltage reference

Overview

The internal Vref absolute accuracy is around 4%. This variation is mainly due to the temperature, the process, and the voltage variations. In order to increase the accuracy of the measurements made thanks to the ADC, it is possible to make a software correction of the Vref, in order to calculate the result the ADC should have returned in case the Vref was more accurate.

The idea of this improvement is the following: Because there is an EEPROM stacked on the product, it is possible to store a linear coefficient which allow a correction of the process variations.

Coefficient address

The coefficient is stored at the address 0x00 of the serial data EEPROM stacked on the AT8xEB5114.

Coefficient format

In order to ease the calculation, this coefficient has been stored as a floating decimal number corresponding to Table 46.

Table 46. Calibration coefficient storage format

Bit	Value
7	1,
6	1/2
5	1/4
4	1/8
3	1/16
2	1/32
1	1/64
0	1/128

It means that if the value is 0x80, the coefficient is equal to 1. If the coefficient is 0x7e, the coefficient is equal to 0,111 1110 in binary which is 0,983 in decimal.

During the test, the Vref is measured, and the calibration value calculated is stored at the address 0x00 of the stack die in accordance with the Table 46 format value.

The relation between the coefficient stored, and the true Vref measurement are recorded on the Table 47.

Table 47. Relation between True Vref measurement and coefficient stored into the EEPROM

True Vref Value (V)	Min	2.300	2.316	2.334	2.353	2.372	2.391	2.409	2.428	2.447	2.466	2.484
	Typ	2.306	2.325	2.345	2.362	2.381	2.400	2.419	2.438	2.456	2.475	2.494
	Max	2.316	2.334	2.353	2.372	2.391	2.409	2.428	2.447	2.466	2.484	2.500
Value stored		0x7b	0x7c	0x7d	0x7e	0x7f	0x80	0x81	0x82	0x83	0x84	0x85
decimal value		0.961	0.969	0.977	0.984	0.992	1	1.008	1.016	1.023	1.031	1.039

Table 53. Priority Bit Level Values

IPH.x	IP.x	Interrupt Level Priority
0	0	0 (Lowest)
0	1	1
1	0	2
1	1	3 (Highest)

A low-priority interrupt can be interrupted by a high priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

Interrupt Name	Interrupt Address Vector	Priority Number
external interrupt (INT0)	0003h	1
Timer0 (TF0)	000Bh	2
external interrupt (INT1)	0013h	3
Timer1 (TF1)	001Bh	4
PWM0	0023h	5
PWM1	002Bh	6
ADC	0033h	7

Table 55. IPL0 Register

IPL0 - Interrupt Priority Register (B8h)

7	6	5	4	3	2	1	0
-	PADC	PW1	PW0	PT1	PX1	PT0	PX0

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	PADC	**ADC interrupt Priority bit** Refer to PADCH for priority level
5	PW1	**PWMU1 Priority bit** Refer to PW1H for priority level.
4	PW1	**PWMU0 Priority bit** Refer to PW1H for priority level.
3	PT1	**Timer 1 overflow interrupt Priority bit** Refer to PT1H for priority level.
2	PX1	**External interrupt 1 Priority bit** Refer to PX1H for priority level.
1	PT0	**Timer 0 overflow interrupt Priority bit** Refer to PT0H for priority level.
0	PX0	**External interrupt 0 Priority bit** Refer to PX0H for priority level.

Reset Value = X000 0000b

Bit addressable.

– Launch the programming of the memory spaces
– Get the status of the flash memory (busy/not busy)

Mapping of the Memory Space

By default, the user space is accessed by MOVC instruction for read only. The column latches space is made accessible by setting the FPS bit in FCON register. Writing is possible from 0000h to 0FFFh, address bits 6 to 0 are used to select an address within a page while bits 14 to 7 are used to select the programming address of the page.

The other memory spaces (user, extra row, hardware security) are made accessible in the code segment by programming bits FMOD0 and FMOD1 in FCON register in accordance with Table 57. A MOVC instruction is then used for reading these spaces.

Table 57. .FM0 Blocks Select Bits

FMOD1	FMOD0	FM0 Adressable space
0	0	User (0000h-FFFFh)
0	1	Extra Row(FF80h-FFFFh)
1	0	Hardware Security Byte (0000h)
1	1	reserved

Launching programming

FPL3:0 bits in FCON register are used to secure the launch of programming. A specific sequence must be written in these bits to unlock the write protection and to launch the programming. This sequence is 5xh followed by Axh. Table 33 summarizes the memory spaces to program according to FMOD1:0 bits.

Figure 33. Programming spaces

	Write to FCON				
	FPL3:0	FPS	FMOD1	FMOD0	Operation
User	5	X	0	0	No action
	A	X	0	0	Write the column latches in user space
Extra Row	5	X	0	1	No action
	A	X	0	1	Write the column latches in extra row space
Hardware Security Byte	5	X	1	0	No action
	A	X	1	0	Write the fuse bits space
Reserved	5	X	1	1	No action
	A	X	1	1	No action

Notes: 1. The sequence 5xh and Axh must be executing without instructions between then otherwise the programming is aborted.
2. Interrupts that may occur during programming time must be disable to avoid any spurious exit of the idle mode.

AT8xEB5114 ROM

ROM Structure

The AT8xEB5114 ROM memory is divided in two different arrays:

- the code array: 4 Kbytes.
- the configuration byte:1 byte.

Hardware Configuration Byte

The configuration byte sets the starting microcontroller options and the security levels.

The starting default options are X1 mode, Oscillator A.

Table 60. Hardware Security Byte (HSB)
HSB (S:EFh)
Power configuration Register

7	6	5	4	3	2	1	0
X2	**RST_OSC1**	**RST_OSC0**	**RST_OCLK**	**-**	**-**	**LB1**	**LB0**

Bit Number	Bit Mnemonic	Description
7	X2	**X2 Mode** Clear to force X2 mode (CkOut = OscOut) Set to use the prescaler mode (CkOut = OscOut / (2*(16-M)))
6	RST_OSC1	**Oscillator bit 1 on reset**
5	RST_OSC0	**Oscillator bit 0 on reset** Oscillator bit on reset 11: allow OSCA 10: allow OSCB 01: allow OSCC 00: reserved
4	RST_OCLK	**Output clocking signal after RESET** Clear to start the microcontroller with a low level on P3.5 followed by an output clocking signal on P3.5 as soon as the microcontroller is started. This signal has is a 1/3 high 2/3 low signal. Its frequency is equal to (CKout / 3). Set to start on normal conditions: No signal on P3.5 which is pulled up.
3	CKRLRV	**CKRL Reset Value** If set, the microcontroller starts with the prescaler reset value = XXXX 1000 (OscOut = CkOut/16). If clear, the microcontroller starts with a prescaler reset value = XXXX 1111 (OscOut = CkOut/2).
2	-	**Reserved**
1-0	LB1-0	**User Program Lock Bits** See Table 61 on page 81

HSB = 1111 XX11b

Note: Whatever the value of RST_OSC, the XTAL1 input is always validated in order to enter in test modes.

Stacked EEPROM

Overview

The AT8xEB5114 features a stacked 2-wire serial data EEPROM. The data EEPROM allows to save up to 256 bytes. The EEPROM is internally connected to P3.6 and P3.7 which are respectively connected to the SDA and the SCL pins.

Protocol

In order to access this memory, it is necessary to use software subroutines according to the AT24C02 datasheet. Nevertheless, because the internal pull-up resistors of the AT8xEB5114 is quite high (around 100KΩ), the protocol should be slowed in order to be sure that the SDA pin can rise to the high level before reading it.

Another solution to keep the access to the EEPROM in specification is to work with a software pull-up.

Using a software pull-up, consists of forcing a low level at the output pin of the microcontroller before configuring it as an input (high level).

The C51 the ports are “quasi-bidirectional” ports. It means that the ports can be configured as output low or as input high. In case a port is configured as an output low, it can sink a current and all internal pull-ups are disconnected. In case a port is configured as an input high, it is pulled up with a strong pull-up (a few hundreds Ohms resistor) for 2 clock periods. Then, if the port is externally connected to a low level, it is only kept high with a weak pull up (around 100KΩ), and if not, the high level is latched high thanks to a medium pull (around 10kΩ).

Thus, when the port is configured as an input, and when this input has been read at a low level, there is a pull-up of around 100KΩ, which is quite high, to quickly load the SDA capacitance. So in order to help the reading of a high level just after the reading of a low level, it is possible to force a transition of the SDA port from an input state (1), to an output low state (0), followed by a new transition from this output low state to input state; In this case, the high pull-up has been replaced with a low pull-up which warranties a good reading of the data.

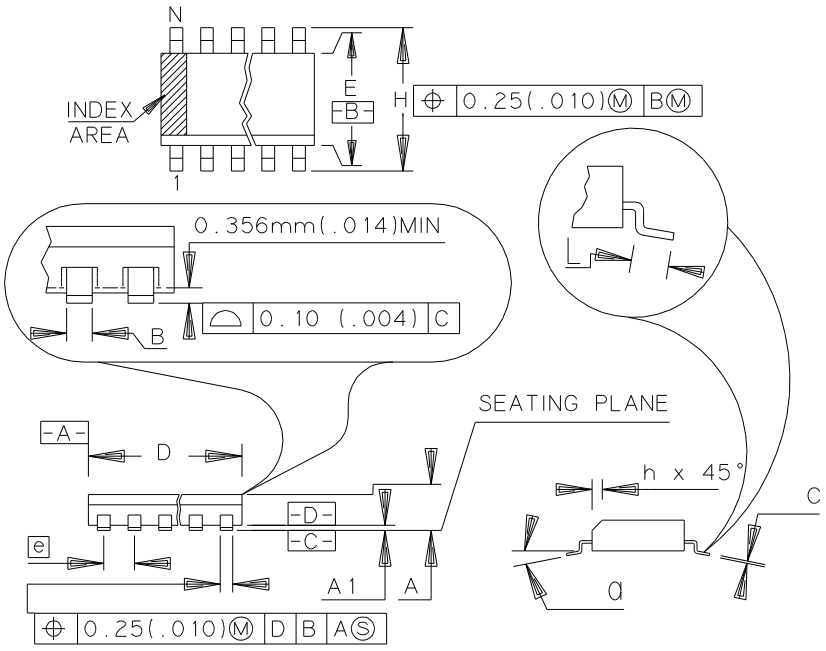
Ordering Information

Table 5. Possible Order Entries

Part Number	Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
AT83EB5114xxxTGRIL	OBSOLETE					
AT89EB5114-TGSIL						
AT83EB5114xxxTGRUL	4Kb ROM	3 to 3.6V	Industrial & Green	40 MHz	S020	Reel
AT89EB5114-TGSUL	4Kb Flash	3 to 3.6V	Industrial & Green	40 MHz	SO20	Stick

Package Drawings

SO20



	MM		INCH	
A	2.35	2.65	.093	.104
A1	0.10	0.30	.004	.012
B	0.35	0.49	.014	.019
C	0.23	0.32	.009	.013
D	12.60	13.00	.496	.512
E	7.40	7.60	.291	.299
e	1.27	BSC	.050	BSC
H	10.00	10.65	.394	.419
h	0.25	0.75	.010	.029
L	0.40	1.27	.016	.050
N	20		20	
a	0°		8°	

Document Revision History

Changes from 4311B to 4311C

1. Removed non-green part numbers from Ordering Information.