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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 14x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f785-e-p

QFN (4x4x0.9) Pin Diagram

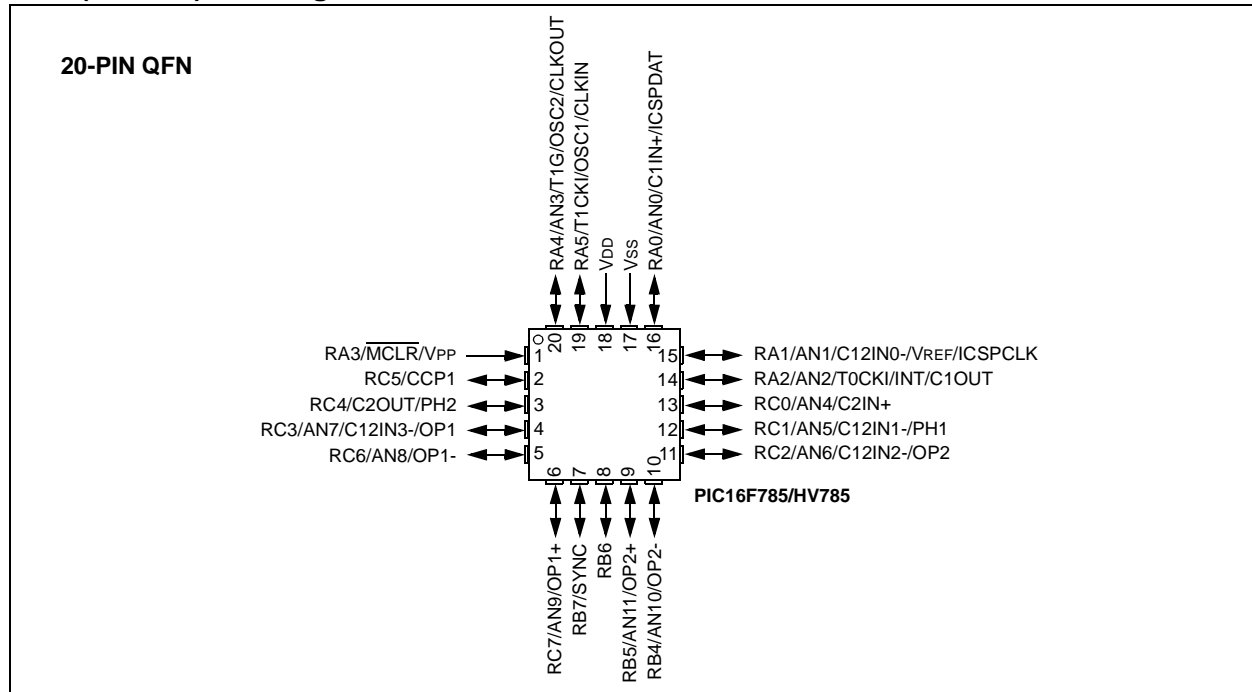


TABLE 2: QFN PIN SUMMARY

I/O	Pin	Analog	Comp.	Op Amps	PWM	Timers	CCP	Interrupt	Pull-ups	Basic
RA0	16	AN0	C1IN+	—	—	—	—	IOC	Y	ICSPDAT
RA1	15	AN1/VREF	C12IN0-	—	—	—	—	IOC	Y	ICSPCLK
RA2	14	AN2	C1OUT	—	—	T0CKI	—	INT/IOC	Y	—
RA3 ⁽¹⁾	1	—	—	—	—	—	—	IOC	Y	MCLR/VPP
RA4	20	AN3	—	—	—	T1G	—	IOC	Y	OSC2/CLKOUT
RA5	19	—	—	—	—	T1CKI	—	IOC	Y	OSC1/CLKIN
RB4	10	AN10	—	OP2-	—	—	—	—	—	—
RB5	9	AN11	—	OP2+	—	—	—	—	—	—
RB6 ⁽²⁾	8	—	—	—	—	—	—	—	—	—
RB7	7	—	—	—	SYNC	—	—	—	—	—
RC0	13	AN4	C2IN+	—	—	—	—	—	—	—
RC1	12	AN5	C12IN1-	—	PH1	—	—	—	—	—
RC2	11	AN6	C12IN2-	OP2	—	—	—	—	—	—
RC3	4	AN7	C12IN3-	OP1	—	—	—	—	—	—
RC4	3	—	C2OUT	—	PH2	—	—	—	—	—
RC5	2	—	—	—	—	—	CCP1	—	—	—
RC6	5	AN8	—	OP1-	—	—	—	—	—	—
RC7	6	AN9	—	OP1+	—	—	—	—	—	—
—	18	—	—	—	—	—	—	—	—	VDD
—	17	—	—	—	—	—	—	—	—	VSS

Note 1: Input only.

2: Open drain.

- General purpose I/O
- Digital input for the capture/compare
- Digital output for the CCP

The diagram illustrates the internal architecture of the CCP1 module. It features two 8-bit shift registers, PORTC and TRISC, which are loaded from the Data Bus via WR PORTC and WR TRISC signals. The TRISC register's output is inverted and connected to the RD TRISC signal. The PORTC register's output is connected to the RD PORTC signal. The RD PORTC signal is also connected to the EN pin of a 16-bit counter (CCP1CON). The counter's output is connected to the CCP1CON register via a multiplexer. The CCP1CON register is also connected to the Data Bus via the CCP out signal. The output of the counter is connected to the I/O Pin, which is also connected to VDD and VSS. The I/O Pin is also connected to the CCP1CON register via a multiplexer.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSEL1	—	—	—	—	ANS11	ANS10	ANS9	ANS8	---- 1111	---- 1111
CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	0000 0000	0000 0000
OPA1CON	OPAON	—	—	—	—	—	—	—	0--- ----	0--- ----
OPA2CON	OPAON	—	—	—	—	—	—	—	0--- ----	0--- ----
PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu
PWMCON0	PRSEN	PASEN	BLANK2	BLANK1	SYNC1	SYNC0	PH2EN	PH1EN	0000 0000	0000 0000
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by PORTC.

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6.5 Timer1 Operation in Asynchronous Counter Mode

If control bit $\overline{T1SYNC}$ of the T1CON Register is set, the external clock input is not synchronized. The timer continues to increment asynchronous to the internal phase clocks. The timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (Section 6.5.1 “Reading and Writing Timer1 in Asynchronous Counter Mode”).

Note: The ANSEL0 (91h) register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read ‘0’.

6.5.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the timer register.

6.6 Timer1 Oscillator

A crystal oscillator circuit is built-in between pins OSC1 (input) and OSC2 (amplifier output). It is enabled by setting control bit T1OSCEN of the T1CON Register. The oscillator is a low power oscillator rated for 32.768 kHz. It will continue to run during Sleep. It is primarily intended for a 32.768 kHz tuning fork crystal.

The Timer1 oscillator is shared with the system LP oscillator. Thus, Timer1 can use this mode only when the primary system clock is also the LP oscillator or is derived from the internal oscillator. As with the system LP oscillator, the user must provide a software time delay to ensure proper oscillator start-up.

Sleep mode will not disable the system clock when the system clock and Timer1 share the LP oscillator.

TRISA<5> and TRISA<4> bits are set when the Timer1 oscillator is enabled. RA5 and RA4 read as ‘0’ and TRISA<5> and TRISA<4> bits read as ‘1’.

Note: The oscillator requires a start-up and stabilization time before use. Thus, T1OSCEN should be set and a suitable delay observed prior to enabling Timer1.

6.7 Timer1 Operation During Sleep

Timer1 can only operate during Sleep when setup in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To setup the timer to wake the device:

- Timer1 of the T1CON Register must be on
- TMR1IE bit of the PIE1 Register must be set
- PEIE bit of the INTCON Register must be set

The device will wake-up on an overflow. If the GIE bit of the INTCON Register is set, the device will wake-up and jump to the Interrupt Service Routine (0004h) on an overflow. If the GIE bit is clear, execution will continue with the next instruction.

TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER1

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSEL0	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111
CM2CON1	MC1OUT	MC2OUT	—	—	—	—	T1GSS	C2SYNC	00-- --10	00-- --10
INTCON	GIE	PEIE	TOIE	INTE	RAIE	TOIF	INTF	RAIF	0000 0000	0000 0000
PIE1	EEIE	ADIE	CCP1IE	C2IE	C1IE	OSFIE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	EEIF	ADIF	CCP1IF	C2IF	C1IF	OSFIF	TMR2IF	TMR1IF	0000 0000	0000 0000
T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	0000 0000	uuuu uuuu
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu

Legend: — x = unknown, u = unchanged, — = unimplemented, read as ‘0’. Shaded cells are not used by the Timer1 module.

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10.0 VOLTAGE REFERENCES

There are two voltage references available in the PIC16F785/HV785: The voltage referred to as the comparator reference (CVREF) is a variable voltage based on VDD; The voltage referred to as the VR reference (VR) is a fixed voltage derived from a stable band gap source. Each source may be individually routed internally to the comparators or output, buffered or unbuffered, on the RA1/AN1/C12IN0-/VREF/ICSPCLK pin.

10.1 Comparator Reference

The comparator module also allows the selection of an internally generated voltage reference for one of the comparator inputs. The VRCON register (Register 10-1) controls the voltage reference module shown in Figure 10-1.

10.1.1 CONFIGURING THE VOLTAGE REFERENCE

The voltage reference can output 32 distinct voltage levels, 16 in a high range and 16 in a low range.

The following equation determines the output voltages:

EQUATION 10-1: CVREF OUTPUT VOLTAGE

$$\begin{aligned} VRR = 1 \text{ (low range):} \\ CVREF &= VR<3:0> \times VDD/24 \\ \\ VRR = 0 \text{ (high range):} \\ CVREF &= (VDD/4) + (VR<3:0> \times VDD/32) \end{aligned}$$

10.1.2 VOLTAGE REFERENCE ACCURACY/ERROR

The full range of VSS to VDD cannot be realized due to the construction of the module. The transistors on the top and bottom of the resistor ladder network (Figure 10-1) keep CVREF from approaching VSS or VDD. The exception is when the module is disabled by clearing all CVROE, C1VREN and C2VREN bits. When disabled with VR<3:0> = 0000 and VRR = 1 the reference voltage will be VSS. This allows the comparators to detect a zero-crossing and not consume CVREF module current.

The voltage reference is VDD derived and therefore, the CVREF output changes with fluctuations in VDD. The tested absolute accuracy of the comparator voltage reference can be found in Table 19-8.

11.3 Effects of a Reset

A device Reset forces all registers to their Reset state. This disables both op amps.

11.4 OPA Module Performance

Common AC and DC performance specifications for the OPA module:

- Common Mode Voltage Range
- Leakage Current
- Input Offset Voltage
- Open Loop Gain
- Gain Bandwidth Product (GBWP)

Common mode voltage range is the specified voltage range for the OPA+ and OPA- inputs, for which the OPA module will perform to within its specifications. The OPA module is designed to operate with input voltages between 0 and $V_{DD}-1.4V$. Behavior for common mode voltages greater than $V_{DD}-1.4V$, or below 0V, are beyond the normal operating range.

Leakage current is a measure of the small source or sink currents on the OPA+ and OPA- inputs. To minimize the effect of leakage currents, the effective impedances connected to the OPA+ and OPA- inputs should be kept as small as possible and equal.

Input offset voltage is a measure of the voltage difference between the OPA+ and OPA- inputs in a closed loop circuit with the OPA in its linear region. The offset voltage will appear as a DC offset in the output equal to the input offset voltage, multiplied by the gain of the circuit. The input offset voltage is also affected by the common mode voltage.

Open loop gain is the ratio of the output voltage to the differential input voltage, (OPA+) - (OPA-). The gain is greatest at DC and falls off with frequency.

Gain Bandwidth Product or GBWP is the frequency at which the open loop gain falls off to 0 dB.

11.5 Effects of Sleep

When enabled, the op amps continue to operate and consume current while the processor is in Sleep mode.

TABLE 11-1: REGISTERS ASSOCIATED WITH THE OPA MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSEL0	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111
ANSEL1	—	—	—	—	ANS11	ANS10	ANS9	ANS8	---- 1111	---- 1111
OPA1CON	OPAON	—	—	—	—	—	—	—	0--- ----	0--- ----
OPA2CON	OPAON	—	—	—	—	—	—	—	0--- ----	0--- ----
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	1111 ----	1111 ----
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for the OPA module.

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REGISTER 12-1: ANSEL0: ANALOG SELECT REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **ANS<7:0>**: Analog Select bits
 Analog select between analog or digital function on pins AN<7:0>, respectively.
 1 = Analog input. Pin is assigned as analog input.⁽¹⁾
 0 = Digital I/O. Pin is assigned to port or special function.

Note 1: Setting a pin to an analog input automatically disables the digital input circuitry, weak pull-ups, and interrupt-on-change, if available. The corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin. Port reads of pins configured assigned as analog inputs will read as '0'.

REGISTER 12-2: ANSEL1: ANALOG SELECT REGISTER

U-0	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	—	ANS11	ANS10	ANS9	ANS8
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-4 **Unimplemented:** Read as '0'
 bit 3-0 **ANS<11:8>**: Analog Select bits
 Analog select between analog or digital function on pins AN<11:8>, respectively.
 1 = Analog input. Pin is assigned as analog input.⁽¹⁾
 0 = Digital I/O. Pin is assigned to port or special function.

Note 1: Setting a pin to an analog input automatically disables the digital input circuitry, weak pull-ups, and interrupt-on-change, if available. The corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin. Port reads of pins assigned as analog inputs will read as '0'.

TABLE 12-2: ANALOG SELECT CROSS REFERENCE

Mode	Reference											
Analog Select	ANS11	ANS10	ANS9	ANS8	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0
Analog Channel	AN11	AN10	AN9	AN8	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
I/O Pin	RB5	RB4	RC7	RC6	RC3	RC2	RC1	RC0	RA4	RA2	RA1	RA0

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REGISTER 12-4: ADCON1: A/D CONTROL REGISTER 1

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	ADCS2	ADCS1	ADCS0	—	—	—	—
bit 7				bit 0			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 7 **Unimplemented:** Read as '0'
- bit 6-4 **ADCS<2:0>:** A/D Conversion Clock Select bits

000 = Fosc/2

001 = Fosc/8

010 = Fosc/32

x11 = FRC (clock derived from a dedicated internal oscillator = 500 kHz max)

100 = Fosc/4

101 = Fosc/16

110 = Fosc/64
- bit 3-0 **Unimplemented:** Read as '0'

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FIGURE 13-6: COMPLEMENTARY OUTPUT PWM TIMING

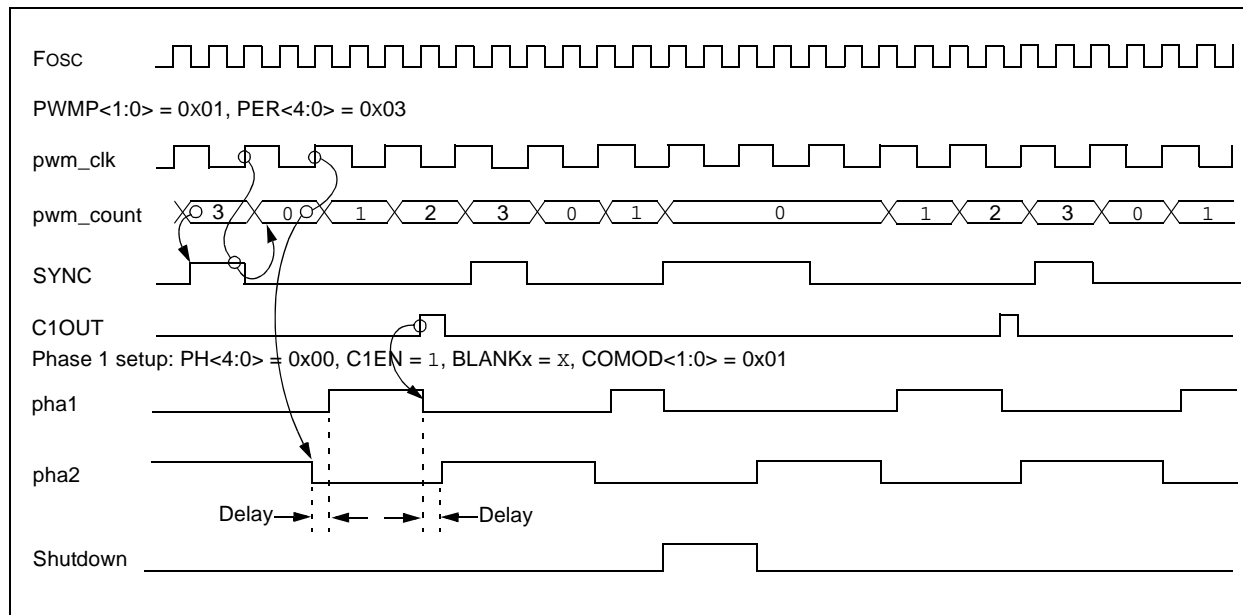


TABLE 13-1: REGISTERS/BITS ASSOCIATED WITH PWM

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CM1CON0	C1ON	C1OUT	C1OE	C1POL	C1SP	C1R	C1CH1	C1CH0	0000 0000	0000 0000
CM2CON0	C2ON	C2OUT	C2OE	C2POL	C2SP	C2R	C2CH1	C2CH0	0000 0000	0000 0000
PWMCLK	PWMASE	PWMP1	PWMP0	PER4	PER3	PER2	PER1	PER0	0000 0000	0000 0000
PWMCON0	PRSEN	PASEN	BLANK2	BLANK1	SYNC1	SYNC0	PH2EN	PH1EN	0000 0000	0000 0000
PWMCON1	—	COMOD1	COMOD0	CMDLY4	CMDLY3	CMDLY2	CMDLY1	CMDLY0	—000 0000	—000 0000
PWMPH1	POL	C2EN	C1EN	PH4	PH3	PH2	PH1	PH0	0000 0000	0000 0000
PWMPH2	POL	C2EN	C1EN	PH4	PH3	PH2	PH1	PH0	0000 0000	0000 0000
REFCON	—	—	BGST	VRBB	VREN	VROE	CVROE	—	—000 000—	—000 000—
VRCON	C1VREN	C2VREN	VRR	—	VR3	VR2	VR1	VR0	000— 0000	000— 0000

Legend: x = unknown, u = unchanged, — = unimplemented read as '0', q = value depends upon condition. Shaded cells are not used by data PWM module.

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15.2.6 TIME-OUT SEQUENCE

On power-up, the time-out sequence is as follows: first, PWRT time out is invoked after POR has expired, then OST is activated after the PWRT time out has expired. The total time out will vary based on oscillator configuration and $\overline{\text{PWRTE}}$ bit status. For example, in EC mode with $\overline{\text{PWRTE}}$ bit equal to '1' (PWRT disabled), there will be no time out at all. Figure 15-4, Figure 15-6 and Figure 15-6 depict time-out sequences. The device can execute code from the INTOSC, while OST is active by enabling Two-Speed Start-up or Fail-Safe Monitor (see Section 3.6.2 "Two-Speed Start-up Sequence" and Section 3.7 "Fail-Safe Clock Monitor").

Since the time outs occur from the POR pulse, if $\overline{\text{MCLR}}$ is kept low long enough, the time outs will expire. Then bringing $\overline{\text{MCLR}}$ high will begin execution immediately (see Figure 15-6). This is useful for testing purposes or to synchronize more than one PIC16F785/HV785 device operating in parallel.

Table 15-5 shows the Reset conditions for some special registers, while Table 15-4 shows the Reset conditions for all the registers.

15.2.7 POWER CONTROL (PCON) REGISTER

The Power Control register (address 8Eh) has two Status bits to indicate what type of Reset that last occurred.

Bit 0 is $\overline{\text{BOR}}$ (Brown-out Reset). $\overline{\text{BOR}}$ is unknown on Power-on Reset. It must then be set by the user and checked on subsequent Resets to see if $\overline{\text{BOR}} = 0$, indicating that a Brown-out has occurred. The BOR Status bit is a "don't care" and is not necessarily predictable if the brown-out circuit is disabled ($\text{BOREN} < 1:0 > = 00$ in the Configuration Word).

Bit 1 is $\overline{\text{POR}}$ (Power-on Reset). It is '0' on Power-on Reset and unaffected otherwise. The user must write a '1' to this bit following a Power-on Reset. On a subsequent Reset, if $\overline{\text{POR}}$ is '0', it will indicate that a Power-on Reset has occurred (i.e., VDD may have gone too low).

For more information, see Section 15.2.4 "Brown-Out Reset (BOR)".

TABLE 15-1: TIME OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Brown-out Reset		Wake-up from Sleep
	$\overline{\text{PWRTE}} = 0$	$\overline{\text{PWRTE}} = 1$	$\overline{\text{PWRTE}} = 0$	$\overline{\text{PWRTE}} = 1$	
XT, HS, LP	$\text{TPWRT} + 1024 \cdot \text{TOSC}$	$1024 \cdot \text{TOSC}$	$\text{TPWRT} + 1024 \cdot \text{TOSC}$	$1024 \cdot \text{TOSC}$	$1024 \cdot \text{TOSC}$
RC, EC, INTOSC	TPWRT	—	TPWRT	—	—

TABLE 15-2: STATUS/PCON BITS AND THEIR SIGNIFICANCE

$\overline{\text{POR}}$	$\overline{\text{BOR}}$	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Condition
0	x	1	1	Power-on Reset
u	0	1	1	Brown-out Reset
u	u	0	u	WDT Reset
u	u	0	0	WDT Wake-up
u	u	u	u	$\overline{\text{MCLR}}$ Reset during normal operation
u	u	1	0	$\overline{\text{MCLR}}$ Reset during Sleep

Legend: u = unchanged, x = unknown

TABLE 15-3: SUMMARY OF REGISTERS ASSOCIATED WITH BROWN-OUT

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
PCON	—	—	—	SBOREN	—	—	POR	BOR	---1 --pq	---1 --pq
STATUS	IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	0001 1xxx

Legend: u = unchanged, x = unknown, — = unimplemented bit, reads as '0', q = value depends on condition. Shaded cells are not used by BOR.

Note 1: Other (non Power-up) Resets include $\overline{\text{MCLR}}$ Reset and Watchdog Timer Reset during normal operation.

15.3 Interrupts

The PIC16F785/HV785 has 11 sources of interrupt:

- External Interrupt RA2/INT
- TMR0 Overflow Interrupt
- PORTA Change Interrupt
- 2 Comparator Interrupts
- A/D Interrupt
- Timer1 Overflow Interrupt
- Timer2 Match Interrupt
- EEPROM Data Write Interrupt
- Fail-Safe Clock Monitor Interrupt
- CCP Interrupt

The Interrupt Control register (INTCON) and Peripheral Interrupt register (PIR1) record individual interrupt requests in flag bits. The INTCON register also has individual and global interrupt enable bits.

A Global Interrupt Enable bit, GIE of the INTCON Register enables (if set) all unmasked interrupts, or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in INTCON register and PIE1 register. GIE is cleared on Reset.

The Return from Interrupt instruction, `RETFIE`, exits interrupt routine, as well as sets the GIE bit, which re-enables unmasked interrupts.

The following interrupt flags are contained in the INTCON register:

- INT Pin Interrupt
- PORTA Change Interrupt
- TMR0 Overflow Interrupt

The peripheral interrupt flags are contained in the special register PIR1. The corresponding interrupt enable bit is contained in special register PIE1.

The following interrupt flags are contained in the PIR1 register:

- EEPROM Data Write Interrupt
- A/D Interrupt
- 2 Comparator Interrupts
- Timer1 Overflow Interrupt
- Timer2 Match Interrupt
- Fail-Safe Clock Monitor Interrupt
- CCP Interrupt

When an interrupt is serviced:

- The GIE is cleared to disable any further interrupt
- The return address is PUSHed onto the stack
- The PC is loaded with 0004h

For external interrupt events, such as the INT pin or PORTA change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends upon when the interrupt event occurs (see Figure 15-8). The latency is the same for one or two-cycle instructions. Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid multiple interrupt requests.

Note 1: Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.

2: When an instruction that clears the GIE bit is executed, any interrupts that were pending for execution in the next cycle are ignored. The interrupts, which were ignored, are still pending to be serviced when the GIE bit is set again.

For additional information on Timer1, Timer2, comparators, A/D, Data EEPROM or CCP modules, refer to the respective peripheral section.

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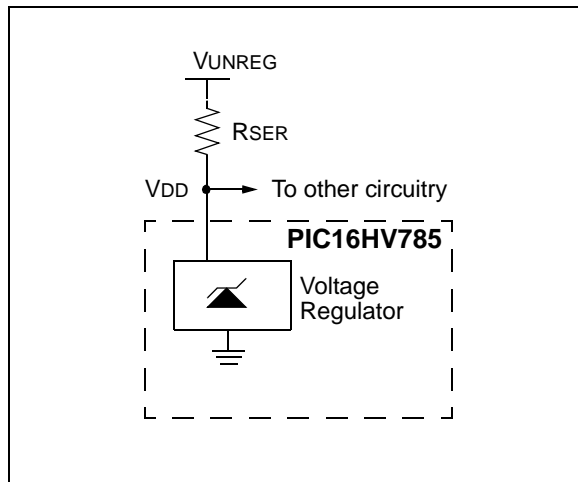
16.0 VOLTAGE REGULATOR

The PIC16HV785 includes a permanent internal 5 volt (nominal) shunt regulator in parallel with the VDD pin. This eliminates the need for an external voltage regulator in systems sourced by an unregulated supply. All external devices connected directly to the VDD pin will share the regulated supply voltage and contribute to the total VDD supply current (I_{LOAD}).

16.1 Regulator Operation

The regulator operates by maintaining a constant voltage at the VDD pin by adjusting the regulator shunt current in response to variations of the VDD supply load and the unregulated supply voltage. The regulator behaves like a fully compensated Zener diode. (See Figure 16-1).

FIGURE 16-1: REGULATOR



An external current limiting resistor, R_{SER}, located between the unregulated supply, V_{UNREG}, and the VDD pin, drops the difference in voltage between V_{UNREG} and VDD. R_{SER} must be between R_{MAX} and R_{MIN} as defined by Equation 16-1.

EQUATION 16-1: R_{SER} LIMITING RESISTOR

$$R_{MAX} = \frac{(V_{UMIN} - V_{DD}) \cdot 1000}{1.05 \cdot (4 \text{ mA} + I_{LOAD})}$$

$$R_{MIN} = \frac{(V_{UMIN} - V_{DD}) \cdot 1000}{0.95 \cdot (50 \text{ mA})}$$

Where:

R_{MAX} = maximum value of R_{SER} (ohms)

R_{MIN} = minimum value of R_{SER} (ohms)

V_{UMIN} = minimum value of V_{UNREG}

V_{UMAX} = maximum value of V_{UNREG}

VDD = regulated voltage (5V nominal)

I_{LOAD} = maximum expected load current in mA including I/O pin currents and external circuits connected to VDD.

1.05 = compensation for +5% tolerance of R_{SER}

0.95 = compensation for -5% tolerance of R_{SER}

16.2 Regulator Precautions

The total VDD load current variation must be less than 46 mA so that it falls within the voltage regulator shunt current dynamic range. If the load current rises above the expected maximum, the regulator will be starved for current and go out of regulation causing VDD to drop.

Since the regulator uses the band gap voltage as the regulated voltage reference, the VR voltage reference is permanently enabled in the PIC16HV785 device.

(used on blank pages to make page count even)

18.11 PICSTART Plus Development Programmer

The PICSTART Plus Development Programmer is an easy-to-use, low-cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. The PICSTART Plus Development Programmer supports most PIC devices in DIP packages up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus Development Programmer is CE compliant.

18.12 PICkit 2 Development Programmer

The PICkit™ 2 Development Programmer is a low-cost programmer and selected Flash device debugger with an easy-to-use interface for programming many of Microchip's baseline, mid-range and PIC18F families of Flash memory microcontrollers. The PICkit 2 Starter Kit includes a prototyping development board, twelve sequential lessons, software and HI-TECH's PICC™ Lite C compiler, and is designed to help get up to speed quickly using PIC® microcontrollers. The kit provides everything needed to program, evaluate and develop applications using Microchip's powerful, mid-range Flash memory family of microcontrollers.

18.13 Demonstration, Development and Evaluation Boards

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

20.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

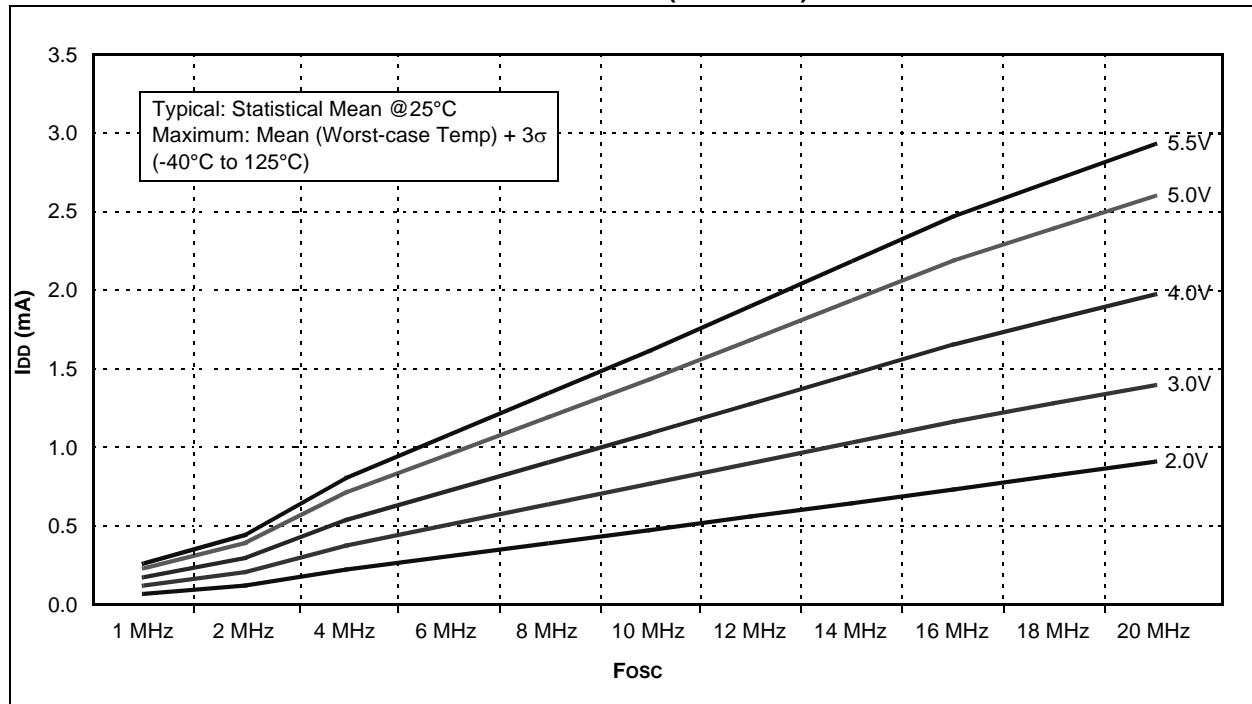
The graphs and tables provided in this section are for **design guidance** and are **not tested**.

In some graphs or tables, the data presented are **outside specified operating range** (i.e., outside specified V_{DD} range). This is for **information only** and devices are ensured to operate properly only within the specified range.

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

“Typical” represents the mean of the distribution at 25°C. “Maximum” or “minimum” represents (mean + 3 σ) or (mean - 3 σ) respectively, where σ is a standard deviation, over each temperature range.

FIGURE 20-1: TYPICAL I_{DD} vs. F_{osc} OVER V_{DD} (EC MODE)



PIC16F785/HV785

FIGURE 20-2: MAXIMUM I_{DD} vs. F_{osc} OVER V_{DD} (EC MODE)

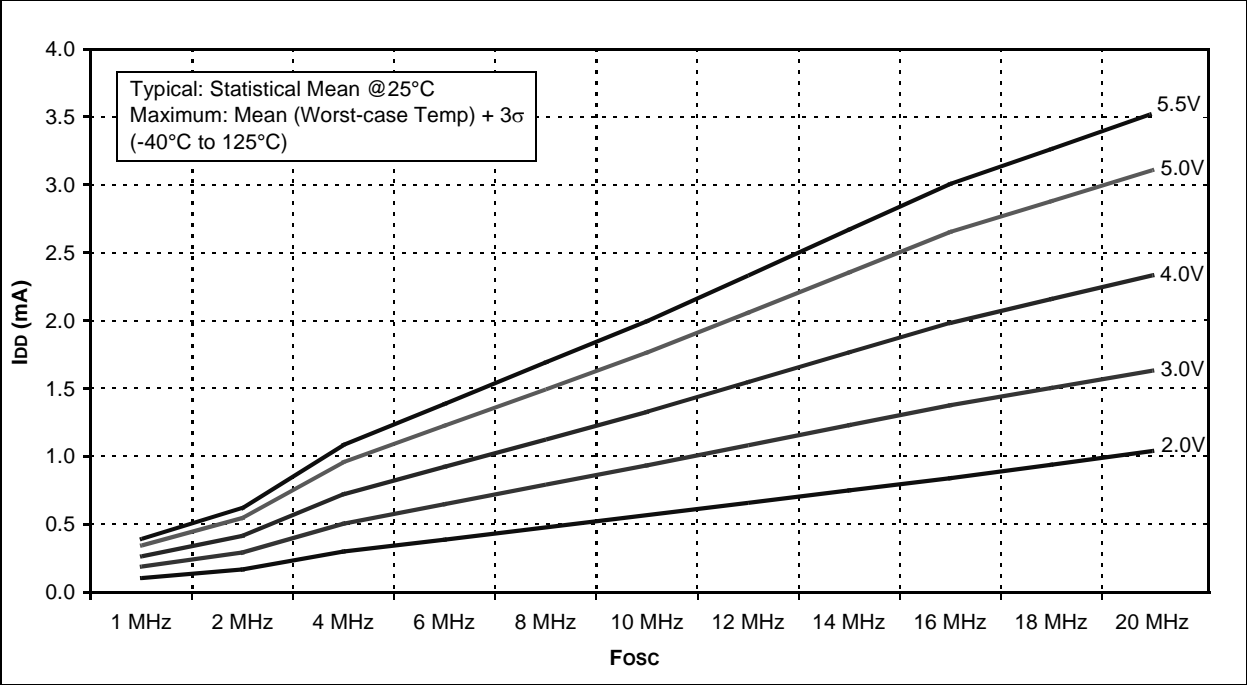
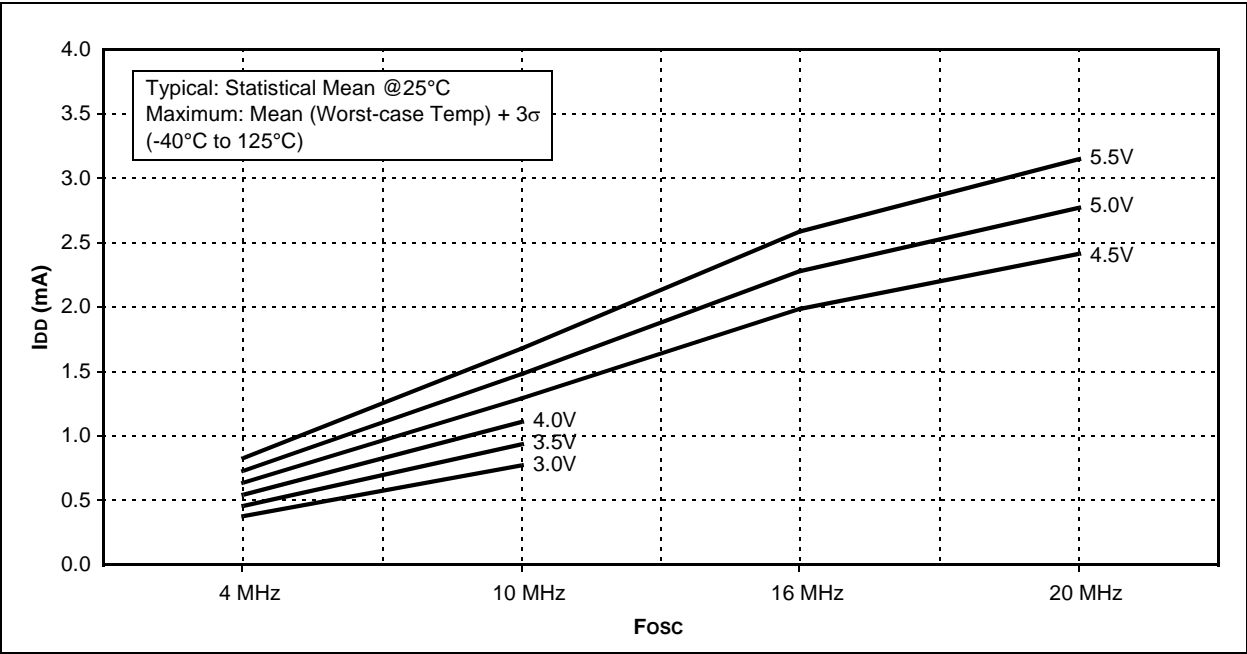


FIGURE 20-3: TYPICAL I_{DD} vs. F_{osc} OVER V_{DD} (HS MODE)



PIC16F785/HV785

FIGURE 20-6: MAXIMUM I_{DD} vs. V_{DD} OVER F_{osc} (XT MODE)

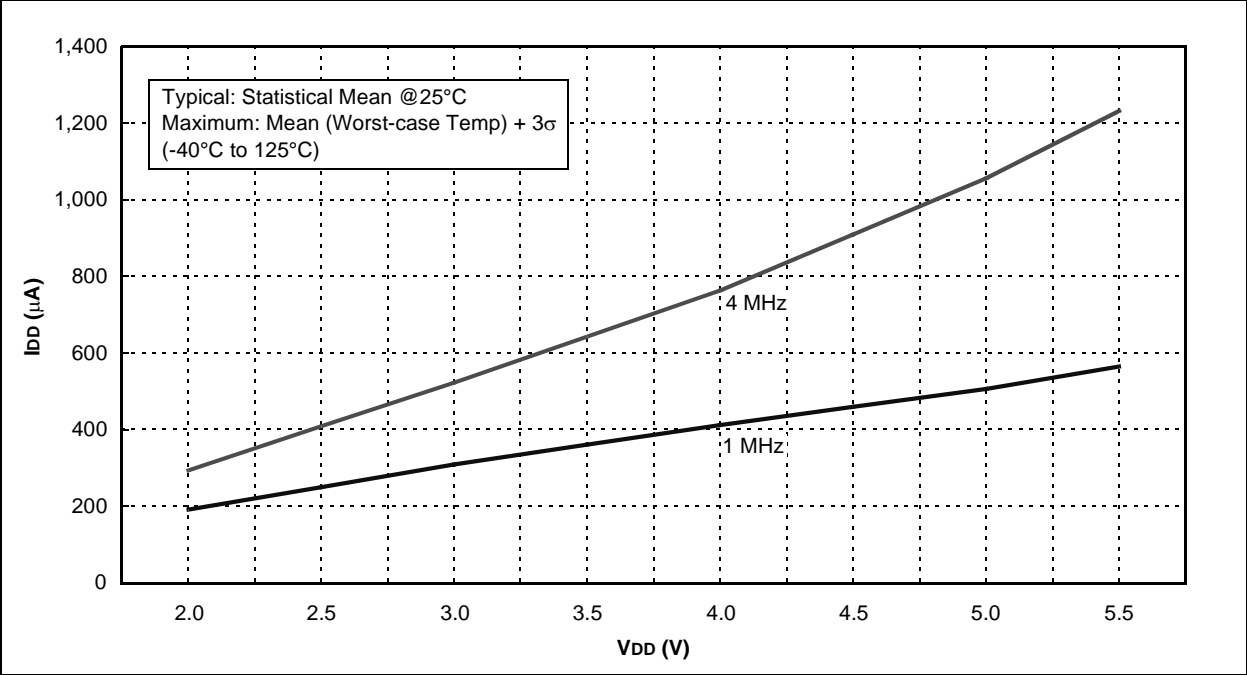
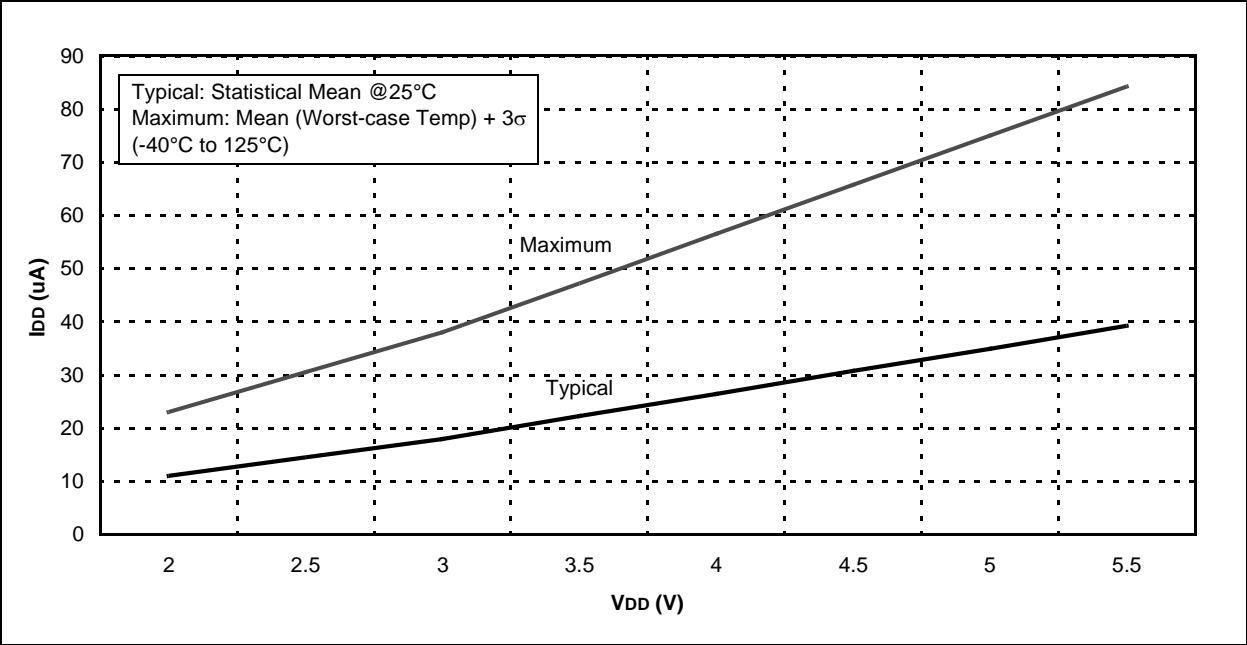


FIGURE 20-7: I_{DD} vs. V_{DD} (LP MODE)



PIC16F785/HV785

FIGURE 20-14: MAXIMUM I_{PD} vs. V_{DD} (SLEEP MODE, ALL PERIPHERALS DISABLED)

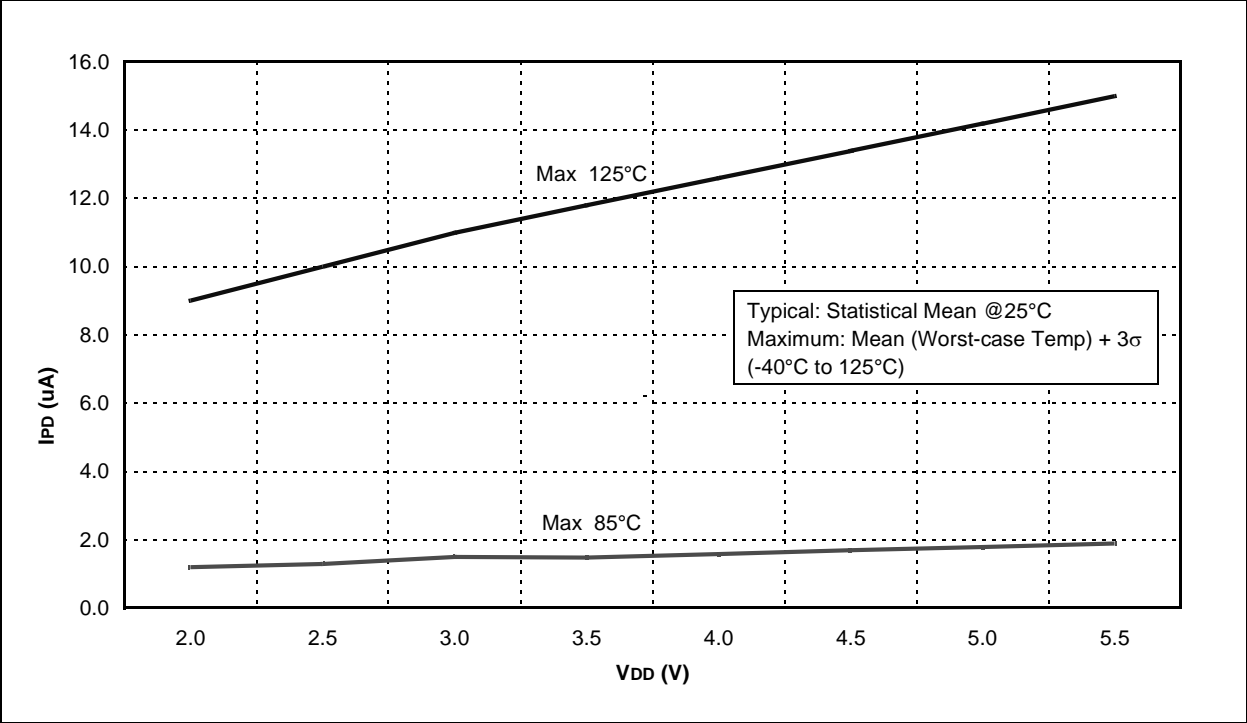
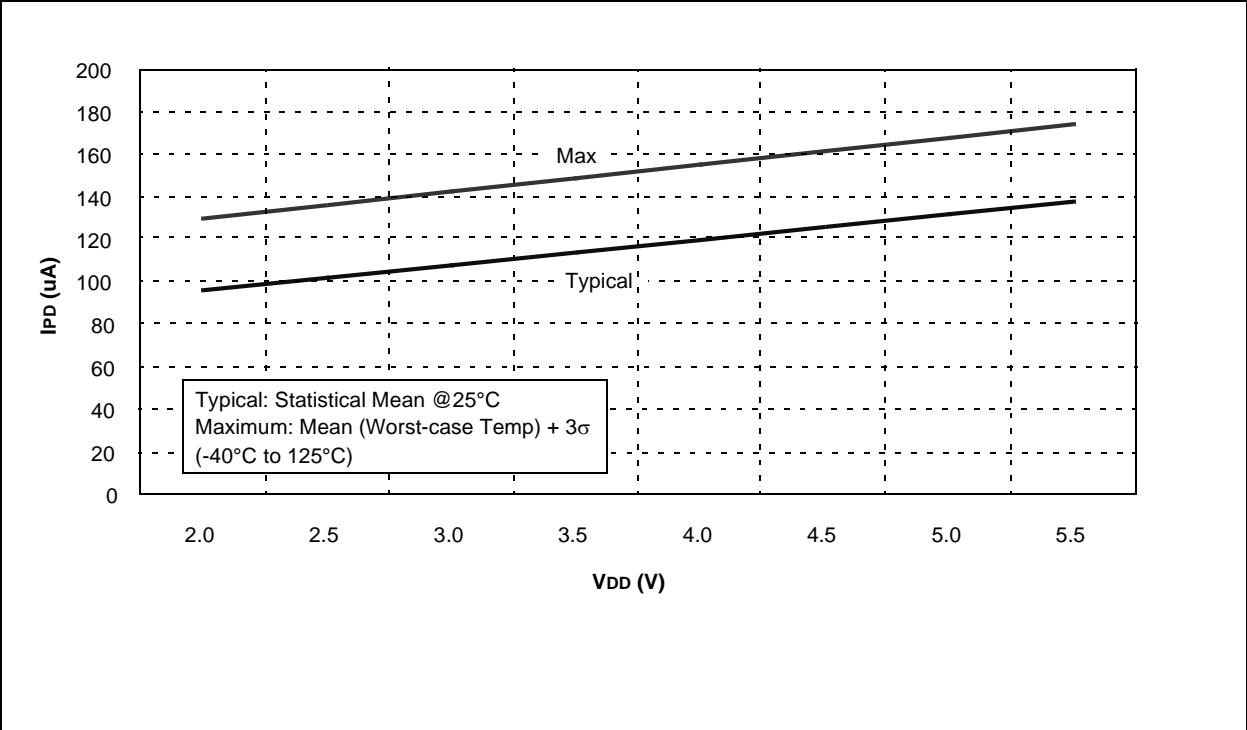


FIGURE 20-15: COMPARATOR I_{PD} vs. V_{DD} (BOTH COMPARATORS ENABLED)



21.0 PACKAGING INFORMATION

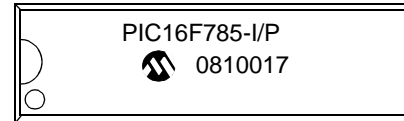
21.1 Package Marking Information

The following sections give the technical details of the packages.

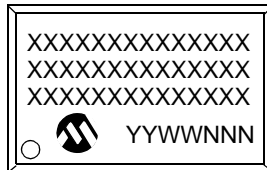
20-Lead PDIP



Example



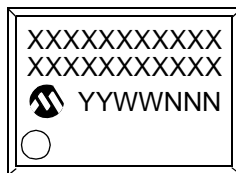
20-Lead SOIC (.300")



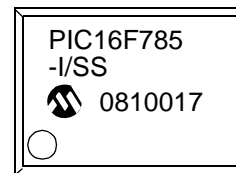
Example



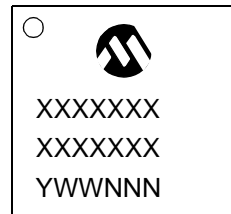
20-Lead SSOP



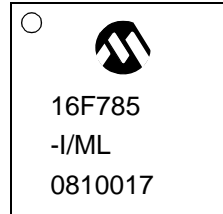
Example



20-Lead QFN



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

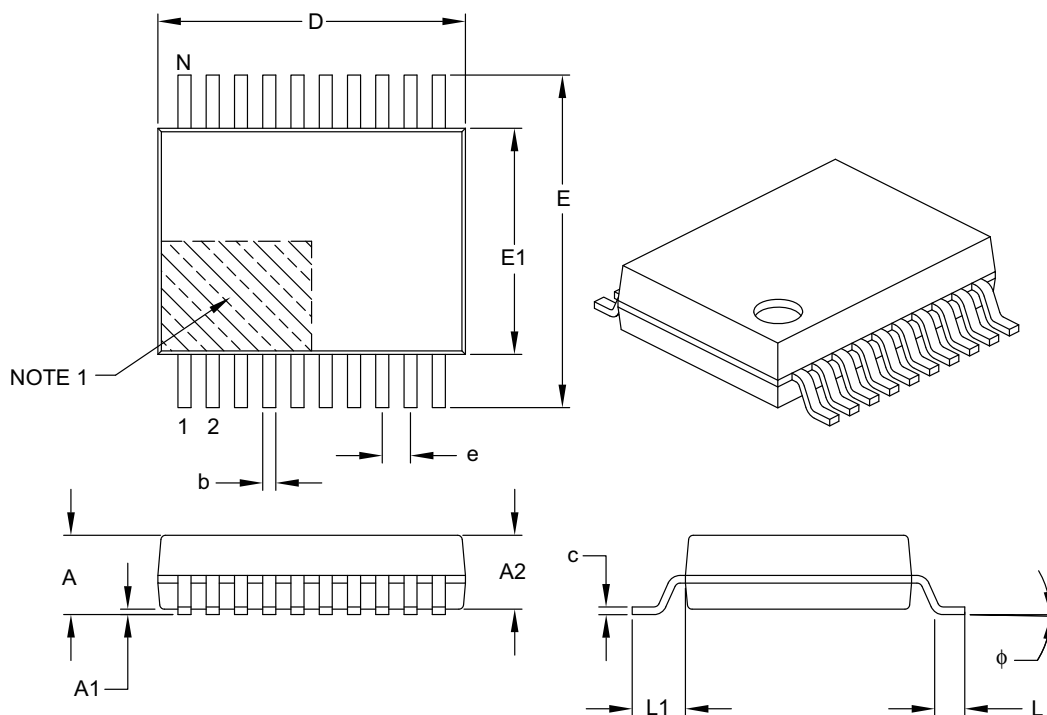
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

* Standard PIC® device marking consists of Microchip part number, year code, week code, and traceability code. For PIC device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

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20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N		20		
Pitch	e		0.65 BSC		
Overall Height	A		–	–	2.00
Molded Package Thickness	A2		1.65	1.75	1.85
Standoff	A1		0.05	–	–
Overall Width	E		7.40	7.80	8.20
Molded Package Width	E1		5.00	5.30	5.60
Overall Length	D		6.90	7.20	7.50
Foot Length	L		0.55	0.75	0.95
Footprint	L1		1.25 REF		
Lead Thickness	c		0.09	–	0.25
Foot Angle	φ		0°	4°	8°
Lead Width	b		0.22	–	0.38

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B

PIC16F785/HV785

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>/XX</u>	<u>XXX</u>
Device	Temperature Range	Package	Pattern
Device:	PIC16F785 ⁽¹⁾ , PIC16HV785 ⁽¹⁾ , PIC16F785T ⁽²⁾ , PIC16HV785T ⁽²⁾ ; VDD range 4.2V to 5.5V PIC16F785 ⁽¹⁾ , PIC16HV785 ⁽¹⁾ , PIC16F785T ⁽²⁾ , PIC16HV785T ⁽²⁾ ; VDD range 2.0V to 5.5V		
Temperature Range:	I = -40°C to +85°C Industrial) E = -40°C to +125°C Extended)		
Package:	ML = QFN P = PDIP SO = SOIC SS = SSOP		
Pattern:	QTP, SQTP, Code or Special Requirements (blank otherwise)		

Examples:
a) PIC16F785 - E/SO 301 = Extended temp., SOIC package.
b) PIC16F785 - I/ML = Industrial temp., QFN package.

Note 1: F = Standard Voltage Range
LF = Wide Voltage Range
2: T = in tape and reel PLCC, and TQFP packages only.