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Applications of "Embedded - Microcontrollers"

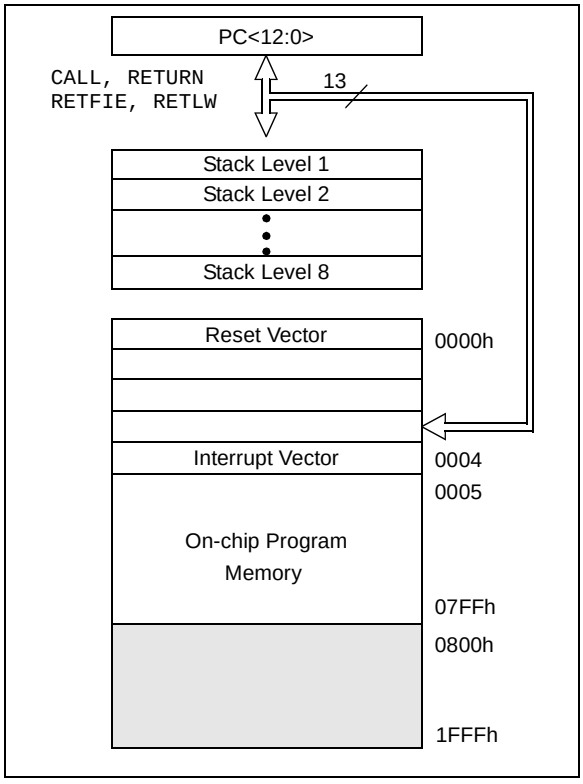
Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 14x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f785-e-so

2.0 MEMORY ORGANIZATION

2.1 Program Memory Organization

The PIC16F785/HV785 has a 13-bit program counter capable of addressing an 8k x 14 program memory space. Only the first 2k x 14 (0000h-07FFh) for the PIC16F785/HV785 is physically implemented. Accessing a location above these boundaries will cause a wrap around within the first 2k x 14 space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 2-1).

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK FOR THE PIC16F785/HV785



2.2 Data Memory Organization

The data memory (see Figure 2-2) is partitioned into four banks, which contain the General Purpose Registers (GPR) and the Special Function Registers (SFR). The Special Function Registers are located in the first 32 locations of each bank. Register locations 20h-7Fh in Bank 0 and A0h-BFh in Bank 1 are General Purpose Registers, implemented as static RAM. The last sixteen register locations in Bank 1 (F0h-FFh), Bank 2 (170h-17Fh), and Bank 3 (1F0h-1FFh) point to addresses 70h-7Fh in Bank 0. All other RAM is unimplemented and returns '0' when read.

Seven address bits are required to access any location in a data memory bank. Two additional bits are required to access the four banks. When data memory is accessed directly, the seven Least Significant address bits are contained within the opcode and the two Most Significant bits are contained in the STATUS register. RP0 and RP1 bits of the STATUS register are the two Most Significant data memory address bits and are also known as the bank select bits. Table 2-1 lists how to access the four banks of registers.

TABLE 2-1: BANK SELECTION

	RP1	RP0
Bank 0	0	0
Bank 1	0	1
Bank 2	1	0
Bank 3	1	1

2.2.1 GENERAL PURPOSE REGISTER FILE

The register file banks are organized as 128 x 8 in the PIC16F785/HV785. Each register is accessed, either directly, by seven address bits within the opcode, or indirectly, through the File Select Register (FSR). When the FSR is used to access data memory, the eight Least Significant data memory address bits are contained in the FSR and the ninth Most Significant address bit is contained in the IRP bit in the STATUS Register. (see **Section 2.4 "Indirect Addressing, INDF and FSR Registers"**).

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (see Table 2-2). These registers are static RAM.

The special registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the "core" are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

REGISTER 6-1: T1CON: TIMER1 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T1GINV(1)	TMR1GE(2)	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **T1GINV:** Timer1 Gate Invert bit (1)
1 = Timer1 gate is high true (see bit 6)
0 = Timer1 gate is low true (see bit 6)

bit 6 **TMR1GE:** Timer1 Gate Enable bit (2)
If TMR1ON = 0:
This bit is ignored
If TMR1ON = 1:
1 = Timer1 is on if Timer1 gate is true (see bit 7)
0 = Timer1 is on independent of Timer1 gate

bit 5-4 **T1CKPS<1:0>:** Timer1 Input Clock Prescale Select bits
11 = 1:8 Prescale Value
10 = 1:4 Prescale Value
01 = 1:2 Prescale Value
00 = 1:1 Prescale Value

bit 3 **T1OSCEN:** LP Oscillator Enable Control bit
If System Clock is INTOSC without CLKOUT or LP mode:
1 = LP oscillator is enabled for Timer1 clock
0 = LP oscillator is off
Else:
This bit is ignored

bit 2 **$\overline{\text{T1SYNC}}$:** Timer1 External Clock Input Synchronization Control bit
TMR1CS = 1:
1 = Do not synchronize external clock input
0 = Synchronize external clock input
TMR1CS = 0:
This bit is ignored. Timer1 uses the internal clock.

bit 1 **TMR1CS:** Timer1 Clock Source Select bit
1 = External clock from T1CKI pin (on the rising edge)
0 = Internal clock (FOSC/4)

bit 0 **TMR1ON:** Timer1 On bit
1 = Enables Timer1
0 = Stops Timer1

Note 1: T1GINV bit inverts the Timer1 gate logic, regardless of source.

2: TMR1GE bit must be set to use either T1G pin or C2OUT, as selected by T1GSS bit (CM2CON1<1>), as a Timer1 gate source.

9.0 COMPARATOR MODULE

The Comparator module has two separate voltage comparators: Comparator 1 (C1) and Comparator 2 (C2).

Each comparator offers the following list of features:

- Control and Configuration register
- Comparator output available externally
- Programmable output polarity
- Interrupt-on-change flags
- Wake-up from Sleep
- Configurable as feedback input to the PWM
- Programmable four input multiplexer
- Programmable two input reference selections
- Programmable speed/power
- Output synchronization to Timer1 clock input (Comparator C2 only)

9.1 Control Registers

Both comparators have separate control and Configuration registers: CM1CON0 for C1 and CM2CON0 for C2. In addition, Comparator C2 has a second control register, CM2CON1, for synchronization control and simultaneous reading of both comparator outputs.

9.1.1 COMPARATOR C1 CONTROL REGISTER

The CM1CON0 register (shown in Register 9-1) contains the control and Status bits for the following:

- Comparator enable
- Comparator input selection
- Comparator reference selection
- Output mode
- Comparator speed

Setting C1ON (CM1CON0<7>) enables Comparator C1 for operation.

Bits C1CH<1:0> of the CM1CON0 Register select the comparator input from the four analog pins AN<7:5,1>.

Note:	To use AN<7:5,1> as analog inputs the appropriate bits must be programmed to '1' in the ANSEL0 register.

Setting C1R of the CM1CON0 Register selects the C1VREF output of the comparator voltage reference module as the reference voltage for the comparator. Clearing C1R selects the C1IN+ input on the RA0/AN0/C1IN+/ICSPDAT pin.

The output of the comparator is available internally via the C1OUT flag of the CM1CON0 Register. To make the output available for an external connection, the C1OE bit of the CM1CON0 Register must be set.

The polarity of the comparator output can be inverted by setting the C1POL bit of the CM1CON0 Register. Clearing C1POL results in a non-inverted output.

A complete table showing the output state versus input conditions and the polarity bit is shown in Table 9-1.

TABLE 9-1: C1 OUTPUT STATE VERSUS INPUT CONDITIONS

Input Condition	C1POL	C1OUT
C1VN > C1VP	0	0
C1VN < C1VP	0	1
C1VN > C1VP	1	1
C1VN < C1VP	1	0

Note 1:	The internal output of the comparator is latched at the end of each instruction cycle. External outputs are not latched.
2:	The C1 interrupt will operate correctly with C1OE set or cleared.
3:	To output C1 on RA2/AN2/T0CKI/INT/C1OUT:(C1OE = 1) and (C1ON = 1) and (TRISA<2> = 0).

C1SP of the CM1CON0 Register configures the speed of the comparator. When C1SP is set, the comparator operates at its normal speed. Clearing C1SP operates the comparator in a slower, low-power mode.

9.1.2.2 Control Register CM2CON1

Comparator C2 has one additional feature: its output can be synchronized to the Timer1 clock input. Setting C2SYNC of the CM2CON1 Register synchronizes the output of Comparator 2 to the falling edge of the Timer1 clock input (see Figure 9-2 and Register 9-3).

The CM2CON1 register also contains mirror copies of both comparator outputs, MC1OUT and MC2OUT of the CM2CON1 Register. The ability to read both outputs simultaneously from a single register eliminates the timing skew of reading separate registers.

Note:	Obtaining the status of C1OUT or C2OUT by reading CM2CON1 does not affect the comparator interrupt mismatch registers.

REGISTER 9-3: CM2CON1: COMPARATOR C2 CONTROL REGISTER 1

R-0	R-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0
MC1OUT	MC2OUT	—	—	—	—	T1GSS	C2SYNC
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **MC1OUT**: Mirror Copy of C1OUT bit (CM1CON0<6>)

bit 6 **MC2OUT**: Mirror Copy of C2OUT bit (CM2CON0<6>)

bit 5-2 **Unimplemented:** Read as ‘0’

bit 1 **T1GSS**: Timer1 Gate Source Select bit
1 = Timer1 gate source is RA4/AN3/T1G/OSC2/CLKOUT
0 = Timer1 gate source is SYNCC2OUT.

bit 0 **C2SYNC**: C2 Output Synchronous Mode bit
1 = C2 output is synchronous to falling edge of TMR1 clock
0 = C2 output is asynchronous

9.2 Comparator Outputs

The comparator outputs are read through the CM1CON0, COM2CON0 or CM2CON1 registers. CM1CON0 and CM2CON0 each contain the individual comparator output of Comparator 1 and Comparator 2, respectively. CM2CON2 contains a mirror copy of both comparator outputs facilitating a simultaneous read of both comparators. These bits are read-only. The comparator outputs may also be directly output to the RA2/AN2/T0CKI/INT/C1OUT and RC4/C2OUT/PH2 I/O pins. When enabled, multiplexers in the output path of the RA2 and RC4 pins will switch and the output of each pin will be the unsynchronized output of the comparator. The uncertainty of each of the comparators is related to the input offset voltage and the response time given in the specifications. Figure 9-1 and Figure 9-2 show the output block diagrams for Comparators 1 and 2, respectively.

The TRIS bits will still function as an output enable/ disable for the RA2/AN2/T0CKI/INT/C1OUT and RC4/ C2OUT/PH2 pins while in this mode.

The polarity of the comparator outputs can be changed using the C1POL and C2POL bits of the CMxCON0 Register.

Timer1 gate source can be configured to use the T1G pin or Comparator 2 output as selected by the T1GSS bit of the CM2CON1 Register. The Timer1 gate feature can be used to time the duration or interval of analog events. The output of Comparator 2 can also be synchronized with Timer1 by setting the C2SYNC bit of the CM2CON1 Register. When enabled, the output of Comparator 2 is latched on the falling edge of the Timer1 clock source. If a prescaler is used with Timer1, Comparator 2 is latched after the prescaler. To prevent a race condition, the Comparator 2 output is latched on the falling edge of the Timer1 clock source and Timer1 increments on the rising edge of its clock source. See the Comparator 2 Block Diagram (Figure 9-2) and the Timer1 Block Diagram (Figure 6-1) for more information.

It is recommended to synchronize Comparator 2 with Timer1 by setting the C2SYNC bit when Comparator 2 is used as the Timer1 gate source. This ensures Timer1 does not miss an increment if Comparator 2 changes during an increment.

9.3 Comparator Interrupts

The comparator interrupt flags are set whenever there is a change in the output value of its respective comparator. Software will need to maintain information about the status of the output bits, as read from CM2CON0<7:6>, to determine the actual change that has occurred. The CxIF bits, PIR1<4:3>, are the Comparator Interrupt Flags. Each comparator interrupt bit must be reset in software by clearing it to '0'. Since it is also possible to write a '1' to this register, a simulated interrupt may be initiated.

The CxIE bits of the PIE1 Register and the PEIE bit of the INTCON Register must be set to enable the interrupts. In addition, the GIE bit must also be set. If any of these bits are cleared, the interrupt is not enabled, though the CxIF bits will still be set if an interrupt condition occurs.

The comparator interrupt of the PIC16F785/HV785 differs from previous designs in that the interrupt flag is set by the mismatch edge and not the mismatch level. This means that the interrupt flag can be reset without the additional step of reading or writing the CMxCON0 register to clear the mismatch registers. When the mismatch registers are not cleared, an interrupt will not occur when the comparator output returns to the previous state. When the mismatch registers are cleared, an interrupt will occur when the comparator returns to the previous state.

Note 1: If a change in the CMxCON0 register (CxOUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CxIF of the PIR1 Register interrupt flag may not get set.

2: When either comparator is first enabled, bias circuitry in the Comparator module may cause an invalid output from the comparator until the bias circuitry is stable. Allow about 1 μs for bias settling then clear the mismatch condition and interrupt flags before enabling comparator interrupts.

9.4 Effects of Reset

A Reset forces all registers to their Reset state. This disables both comparators.

REGISTER 13-4: PWMPH2: PWM PHASE 2 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POL	C2EN	C1EN	PH4	PH3	PH2	PH1	PH0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **POL:** PH2 Output Polarity bit
1 = PH2 Pin is active low
0 = PH2 Pin is active high

bit 6 **C2EN:** Comparator 2 Enable bit
When COMOD<1:0> = 00(1)
1 = PH2 is reset when C2OUT goes high
0 = PH2 ignores Comparator 2
When COMOD<1:0> = 1X or X1(1)
C2EN has no effect

bit 5 **C1EN:** Comparator 1 Enable bit
When COMOD<1:0> = 00(1)
1 = PH2 is reset when C1OUT goes high
0 = PH2 ignores Comparator 1
When COMOD<1:0> = 1X or X1(1)
C1EN has no effect

bit 4-0 **PH<4:0>:** PWM Phase bits
When COMOD<1:0> = 00(1)
00000 = PH2 starts 1 pwm_clk period after falling edge of SYNC pulse. All other PH2 delays are expressed relative to this time.
00001 = PH2 is delayed by 1 pwm_clk pulse
••••• = •••
11111 = PH2 is delayed by 31 pwm_clk pulses
When COMOD<1:0> = 1X(1)
00000 = Complementary drive terminates 1 pwm_clk period after falling edge of SYNC pulse. All other PH2 delays are expressed relative to this time.
00001 = Complementary drive termination is delayed by 1 pwm_clk pulse
••••• = •••
11111 = Complementary drive termination is delayed by 31 pwm_clk pulses
When COMOD<1:0> = 01(1)
PH<4:0> has no effect.

Note 1: See PWMCON1 register (Register 13-5).

REGISTER 13-5: PWMCON1: PWM CONTROL REGISTER 1

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	COMOD1	COMOD0	CMDLY4	CMDLY3	CMDLY2	CMDLY1	CMDLY0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

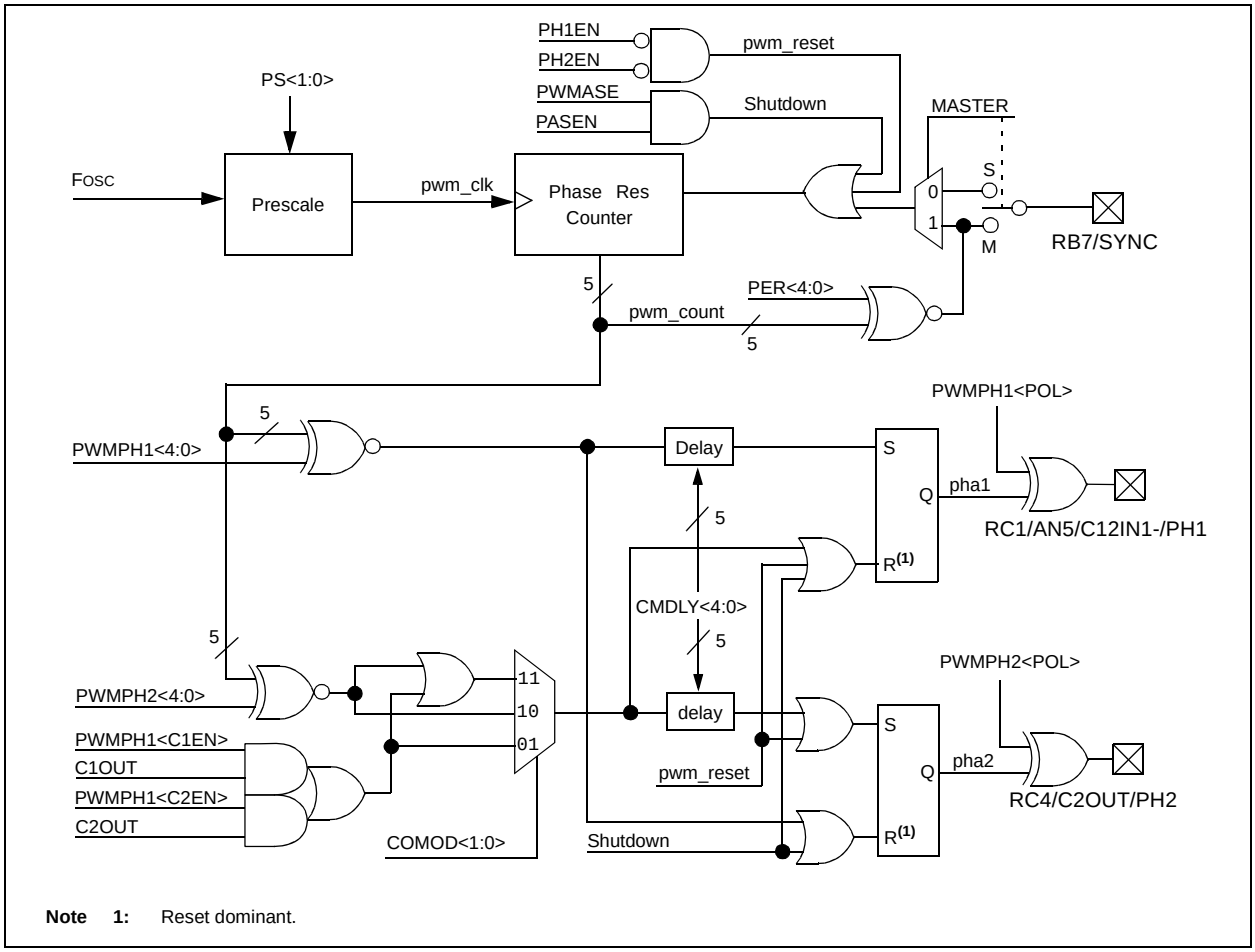
bit 7 **Unimplemented:** Read as '0'

bit 6-5 **COMOD<1:0>:** Complementary Mode Select bits(1)
- 00 = Normal two-phase operation. Complementary mode is disabled.
- 01 = Complementary operation. Duty cycle is terminated by C1OUT or C2OUT.
- 10 = Complementary operation. Duty cycle is terminated by PWMPH2<4:0> = pwm_count.
- 11 = Complementary operation. Duty cycle is terminated by PWMPH2<4:0> = pwm_count or C1OUT or C2OUT.

bit 4-0 **CMDLY<4:0>:** Complementary Drive Dead Time bits (typical)
- 00000 = Delay = 0
- 00001 = Delay = 5 ns
- 00010 = Delay = 10 ns
- ••••• = •••
- 11111 = Delay = 155 ns

Note 1: PWMCON0<1:0> must be set to '11' for Complementary mode operation.

FIGURE 13-5: COMPLEMENTARY OUTPUT PWM BLOCK DIAGRAM



Note 1: Reset dominant.

14.1 EECON1 and EECON2 Registers

EECON1 is the control register with four low-order bits physically implemented. The upper four bits are non-implemented and read as '0's.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set in software. They are cleared in hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental, premature termination of a write operation.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a $\overline{\text{MCLR}}$ Reset, or a WDT Time-out Reset during normal operation. In these situations, following Reset, the user can check the WRERR bit, clear it and rewrite the location. The EEDAT and EEADR registers are cleared by a Reset. Therefore, the EEDAT and EEADR registers will need to be re-initialized.

Interrupt flag EEIF bit of the PIR1 Register is set when write is complete. This bit must be cleared in software.

EECON2 is not a physical register. Reading EECON2 will read all '0's. The EECON2 register is used exclusively in the data EEPROM write sequence.

Note:	The EECON1, EEDAT and EEADR registers should not be modified during a data EEPROM write (WR bit = 1).

REGISTER 14-3: EECON1: EEPROM CONTROL REGISTER

U-0	U-0	U-0	U-0	R/W-x	R/W-0	R/S-0	R/S-0
—	—	—	—	WRERR	WREN	WR	RD
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **IUnimplemented:** Read as '0'

bit 3 **WRERR:** EEPROM Error Flag bit
- 1 = A write operation is prematurely terminated (any $\overline{\text{MCLR}}$ Reset, any WDT Reset during normal operation or BOR reset)
- 0 = The write operation completed

bit 2 **WREN:** EEPROM Write Enable bit
- 1 = Allows write cycles
- 0 = Inhibits write to the data EEPROM

bit 1 **WR:** Write Control bit
- 1 = Initiates a write cycle (The bit is cleared by hardware once write is complete. The WR bit can only be set, not cleared, in software.)
- 0 = Write cycle to the data EEPROM is complete

bit 0 **RD:** Read Control bit
- 1 = Initiates an EEPROM read (Read takes one cycle. RD is cleared in hardware. The RD bit can only be set, not cleared, in software.)
- 0 = Does not initiate an EEPROM read

15.2 Reset

The PIC16F785/HV785 differentiates between various kinds of Reset:

- Power-on Reset (POR)
- WDT Reset during normal operation
- WDT Reset during Sleep
- $\overline{\text{MCLR}}$ Reset during normal operation
- $\overline{\text{MCLR}}$ Reset during Sleep
- Brown-out Reset (BOR)

Some registers are not affected in any Reset condition; their status is unknown on POR and unchanged in any other Reset. Most other registers are reset to a "Reset state" on:

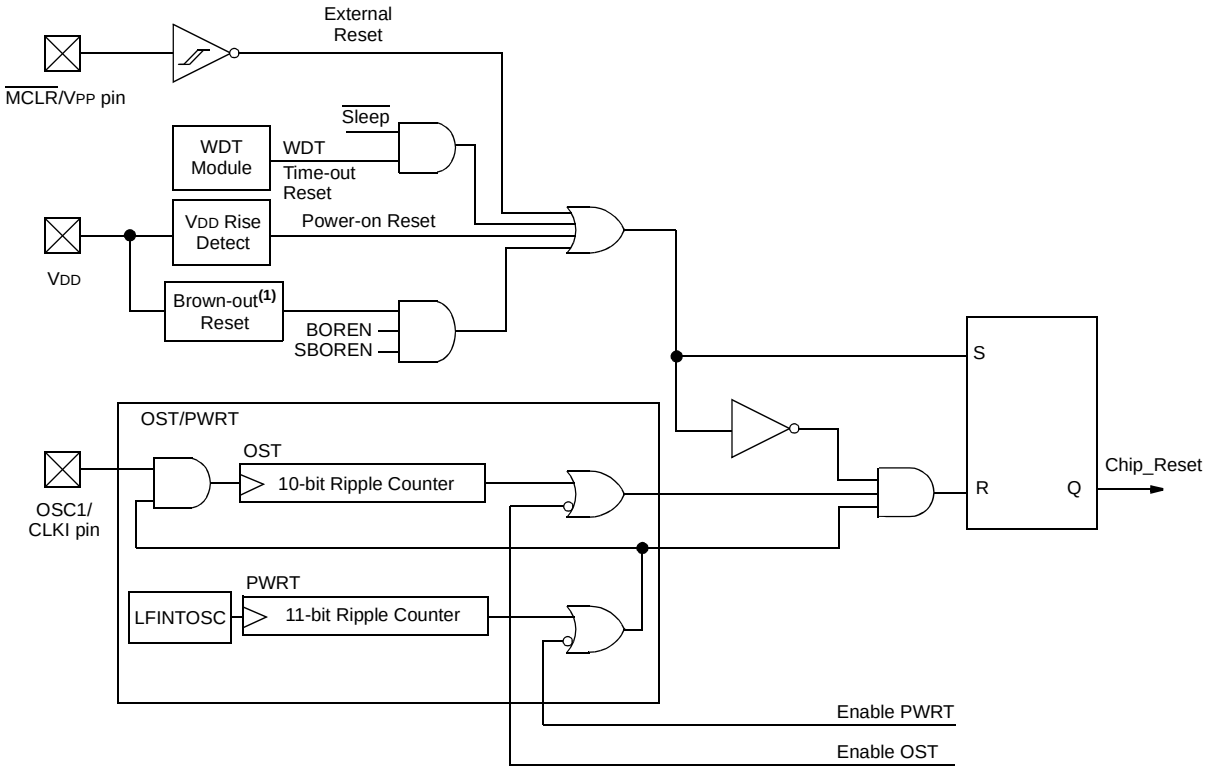
- Power-on Reset
- $\overline{\text{MCLR}}$ Reset
- $\overline{\text{MCLR}}$ Reset during Sleep
- WDT Reset
- Brown-out Reset (BOR)

They are not affected by a WDT wake-up since this is viewed as the resumption of normal operation. $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are set or cleared differently in different Reset situations, as indicated in Table 15-2. These bits are used in software to determine the nature of the Reset. See Table 15-4 for a full description of Reset states of all registers.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 15-1.

The $\overline{\text{MCLR}}$ Reset path has a noise filter to detect and ignore small pulses. See **Section 19.0 "Electrical Specifications"** for pulse width specifications.

FIGURE 15-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



Note 1: Refer to the Configuration Word register (Register 15.2).

TABLE 15-4: INITIALIZATION CONDITION FOR REGISTERS

Register	Address	Power-on Reset	$\overline{\text{MCLR}}$ Reset WDT Reset Brown-out Reset(1)	Wake-up from Sleep through interrupt Wake-up from Sleep through WDT Time-out
W	—	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h/80h	xxxx xxxx	xxxx xxxx	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h/82h	0000 0000	0000 0000	PC + 1(3)
STATUS	03h/83h	0001 1xxx	000q quuu(4)	uuuq quuu(4)
FSR	04h/84h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	05h	--x0 x000(6)	--u0 u000(7)	--uu uuuu
PORTB	06h	xx00 ----(6)	uu00 ----(7)	uuuu ----
PORTC	07h	00xx 0000(6)	00uu uuuu(7)	uuuu uuuu
PCLATH	0Ah/8Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh/8Bh	0000 0000	0000 0000	uuuu uuuu(2)
PIR1	0Ch	0000 0000	0000 0000	uuuu uuuu(2)
TMR1L	0Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	0Fh	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	10h	0000 0000	uuuu uuuu	uuuu uuuu
TMR2	11h	0000 0000	0000 0000	uuuu uuuu
T2CON	12h	-000 0000	-000 0000	-uuu uuuu
CCPR1L	13h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR1H	14h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CON	15h	--00 0000	--00 0000	--uu uuuu
WDTCON	18h	---0 1000	---0 1000	---u uuuu
ADRESH	1Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON0	1Fh	0000 0000	0000 0000	uuuu uuuu
OPTION_REG	81h	1111 1111	1111 1111	uuuu uuuu
TRISA	85h	--11 1111	--11 1111	--uu uuuu
TRISB	86h	1111 ----	1111 ----	uuuu ----
TRISC	87h	1111 1111	1111 1111	uuuu uuuu
PIE1	8Ch	0000 0000	0000 0000	uuuu uuuu
PCON	8Eh	---1 --0x	---u --uq(1,5)	---u --uu
OSCCON	8Fh	-110 q000	-110 q000	-uuu uuuu
OSCTUNE	90h	---0 0000	---u uuuu	---u uuuu
ANSEL0	91h	1111 1111	1111 1111	uuuu uuuu
PR2	92h	1111 1111	1111 1111	1111 1111
ANSEL1	93h	---- 1111	---- 1111	---- uuuu
WPUA	95h	--11 1111	--11 1111	--uu uuuu
IOCA	96h	--00 0000	--00 0000	--uu uuuu
REFCON	98h	--00 000-	--00 000-	--uu uuu-

Legend: u = unchanged, x = unknown, – = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

2: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

4: See Table 15-5 for Reset value for specific condition.

5: If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

6: Analog channels read 0 but data latches are unknown.

7: Analog channels read 0 but data latches are unchanged.

TABLE 15-5: INITIALIZATION CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	0001 1xxx	---1 --0x
$\overline{MCLR}$ Reset during normal operation	000h	000u uuuu	---u --uu
$\overline{MCLR}$ Reset during Sleep	000h	0001 0uuu	---u --uu
WDT Reset	000h	0000 uuuu	---u --uu
WDT Wake-up	PC + 1	uuu0 0uuu	---u --uu
Brown-out Reset	000h	0001 1uuu	---1 --u0
Interrupt Wake-up from Sleep	PC + 1(1)	uuu1 0uuu	---u --uu

Legend: u = unchanged, x = unknown, – = unimplemented bit, reads as '0'.

Note 1: When the wake-up is due to an interrupt and global enable bit GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

17.0 INSTRUCTION SET SUMMARY

The PIC16F785/HV785 instruction set is highly orthogonal and is comprised of three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

Each PIC16 instruction is a 14-bit word divided into an **opcode,** which specifies the instruction type and one or more **operands,** which further specify the operation of the instruction. The format for each of the categories is presented in Figure 17-1, while the various opcode fields are summarized in Table 17-1.

Table 17-2 lists the instructions recognized by the MPASM™ assembler.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator, which selects the bit affected by the operation, while 'f' represents the address of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8-bit or 11-bit constant, or literal value.

One instruction cycle consists of four oscillator periods; for an oscillator frequency of 4 MHz, this gives a normal instruction execution time of 1 μs. All instructions are executed within a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of an instruction. When this occurs, the execution takes two instruction cycles, with the second cycle executed as a NOP.

Note:	To maintain upward compatibility with future products, do not use the OPTION and TRIS instructions.

All instruction examples use the format '0xhh' to represent a hexadecimal number, where 'h' signifies a hexadecimal digit.

17.1 Read-Modify-Write Operations

Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (RMW) operation. The register is read, the data is modified, and the result is stored according to either the instruction, or the destination designator 'd'. A read operation is always performed, even if the instruction is a Write command.

For example, a CLRF PORTA instruction will read PORTA, clear all the data bits, then write the result back to PORTA. This example would have the unintended result of clearing the condition that set the RAIF flag.

TABLE 17-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1). The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1.
PC	Program Counter
TO	Time-out bit
PD	Power-down bit

FIGURE 17-1: GENERAL FORMAT FOR INSTRUCTIONS

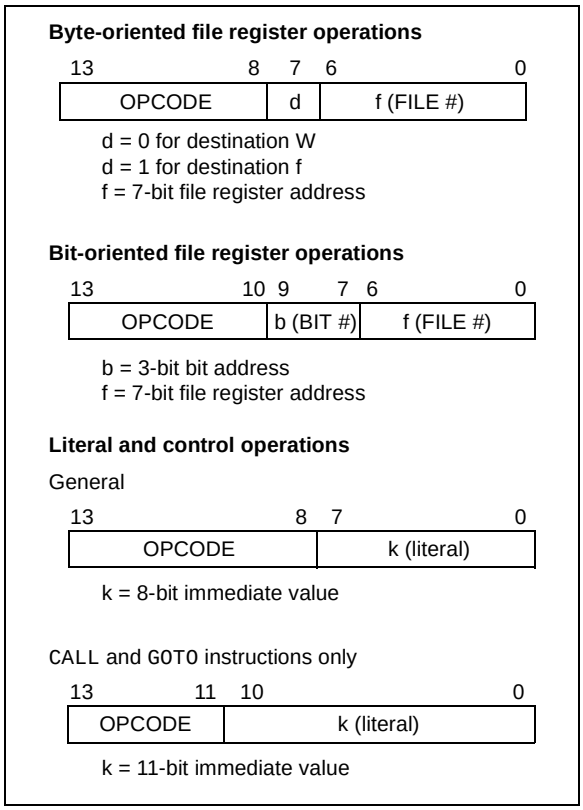


FIGURE 19-4: CLKOUT AND I/O TIMING

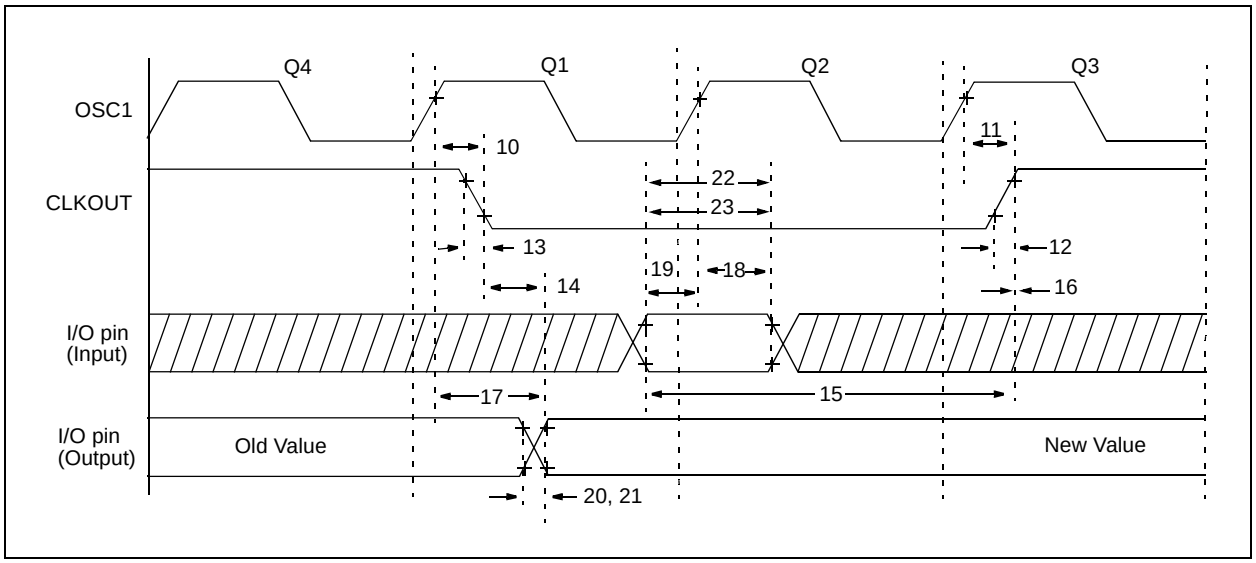


TABLE 19-2: CLKOUT AND I/O TIMING REQUIREMENTS

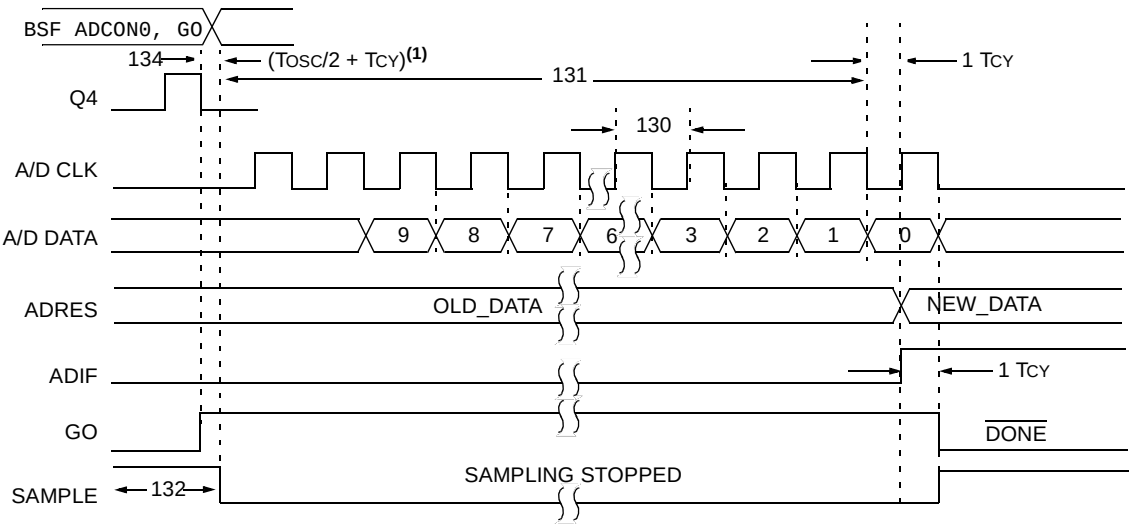
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
10	TOSH2CKL	OSC1↑ to CLKOUT↓	—	75	200	ns	**(Note 1)**
11	TOSH2CKH	OSC1↑ to CLKOUT↑	—	75	200	ns	**(Note 1)**
12	TCKR	CLKOUT rise time	—	35	100	ns	**(Note 1)**
13	TCKF	CLKOUT fall time	—	35	100	ns	**(Note 1)**
14	TCKL2IOV	CLKOUT↓ to Port out valid	—	—	20	ns	**(Note 1)**
15	TIOV2CKH	Port input valid before CLKOUT↑	TOSC + 200 ns	—	—	ns	**(Note 1)**
16	TCKH2IOI	Port input hold after CLKOUT↑	0	—	—	ns	**(Note 1)**
17	TOSH2IOV	OSC1↑ (Q1 cycle) to Port out valid	—	50	150 *	ns	
			—	—	300	ns	
18	TOSH2IOI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	100	—	—	ns	
19	TIOV2OSH	Port input valid to OSC1↑ (I/O in setup time)	0	—	—	ns	
20	TIOR	Port output rise time	—	10	40	ns	
21	TIOF	Port output fall time	—	10	40	ns	
22	TINP	INT pin high or low time	25	—	—	ns	
23	TRBP	PORTA interrupt-on-change high or low time	TCY	—	—	ns	

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated.

Note 1: Measurements are taken in RC mode where CLKOUT output is 4 x TOSC.

FIGURE 19-10: PIC16F785/HV785 A/D CONVERSION TIMING (SLEEP MODE)



Note 1: If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

TABLE 19-17: PIC16F785/HV785 A/D CONVERSION REQUIREMENTS (SLEEP MODE)

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
130	TAD	A/D Internal RC Oscillator Period	3.0*	6.0	9.0*	µs	ADCS<1:0> = 11 (RC mode) At VDD = 2.5V
			2.0*	4.0	6.0*	µs	At VDD = 5.0V
131	TCNV	Conversion Time (not including Acquisition Time)(1)	—	11	—	TAD	
132	TACQ	Acquisition Time	**(Note 2)**	11.5	—	µs	
			5*	—	—	µs	The minimum time is the amplifier settling time. This may be used if the "new" input voltage has not changed by more than 1 LSb (i.e., 4.1 mV @ 4.096V) from the last sampled voltage (as stored on CHOLD).
134	TGO	Q4 to A/D Clock Start	—	TOSC/2 + TCY	—	—	If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRES register may be read on the following TCY cycle.

2: See Table 12-1 for minimum conditions.

FIGURE 20-6: MAXIMUM IDD vs. VDD OVER FOSC (XT MODE)

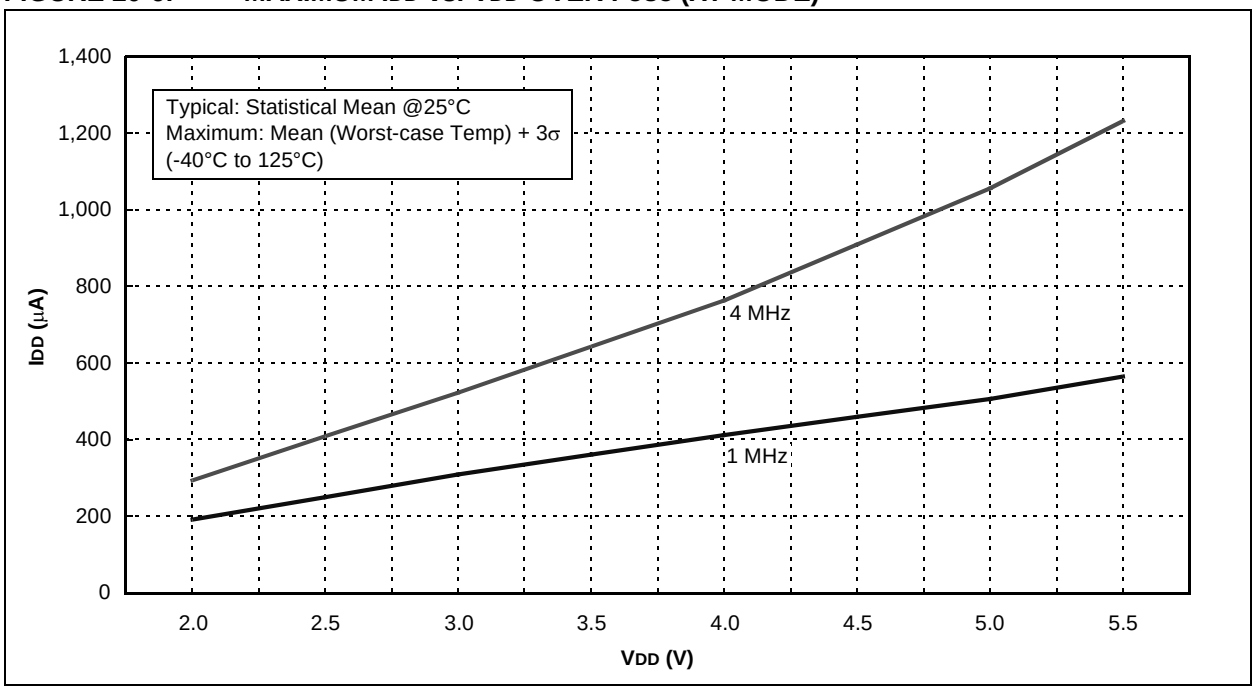


FIGURE 20-7: IDD vs. VDD (LP MODE)

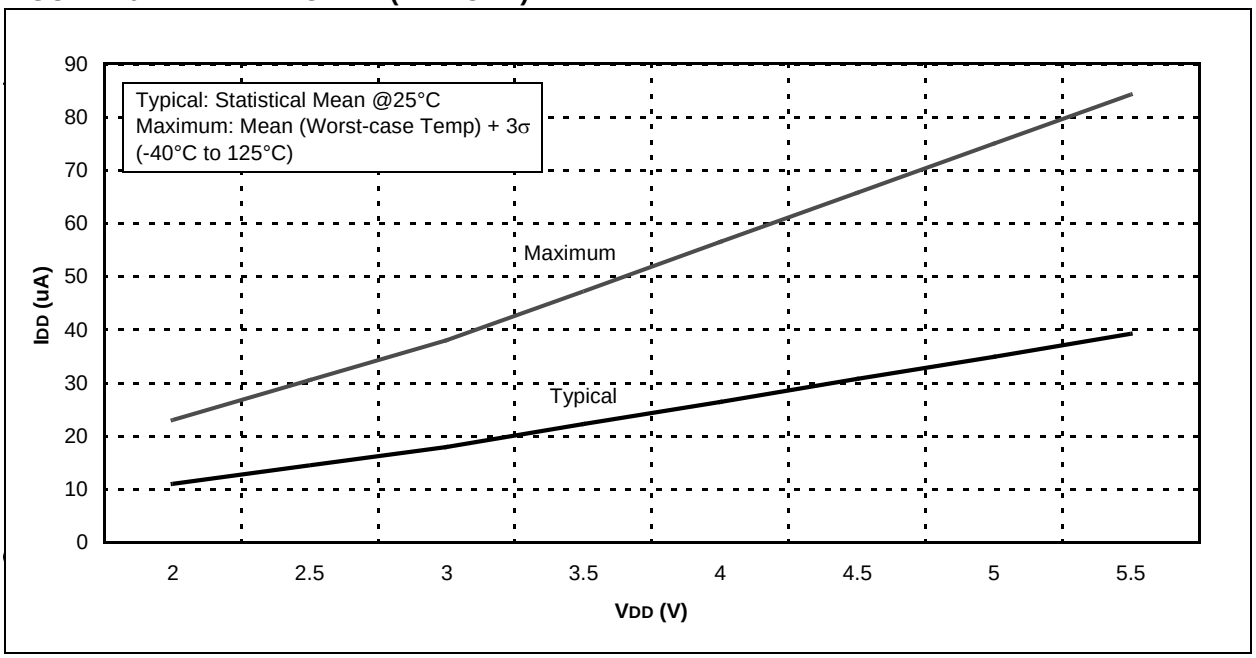


FIGURE 20-16: COMPARATOR IPD vs. VDD (BOTH COMPARATORS ENABLED) CXSP=1

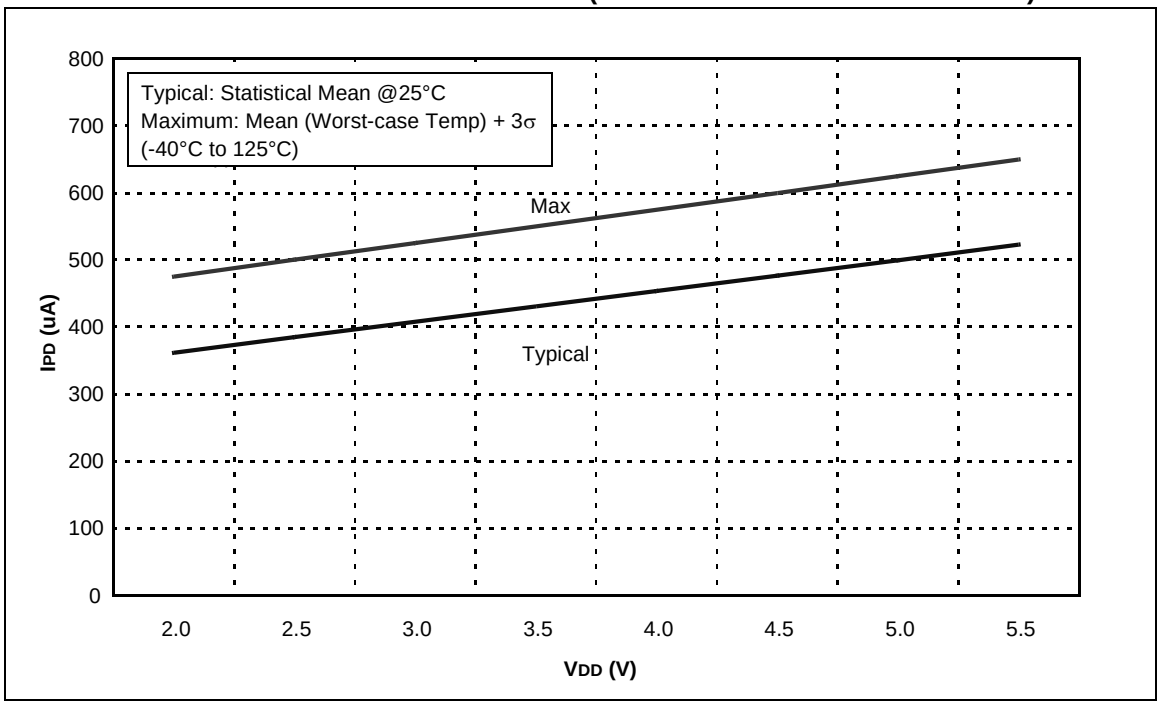


FIGURE 20-17: BOR IPD vs. VDD OVER TEMPERATURE

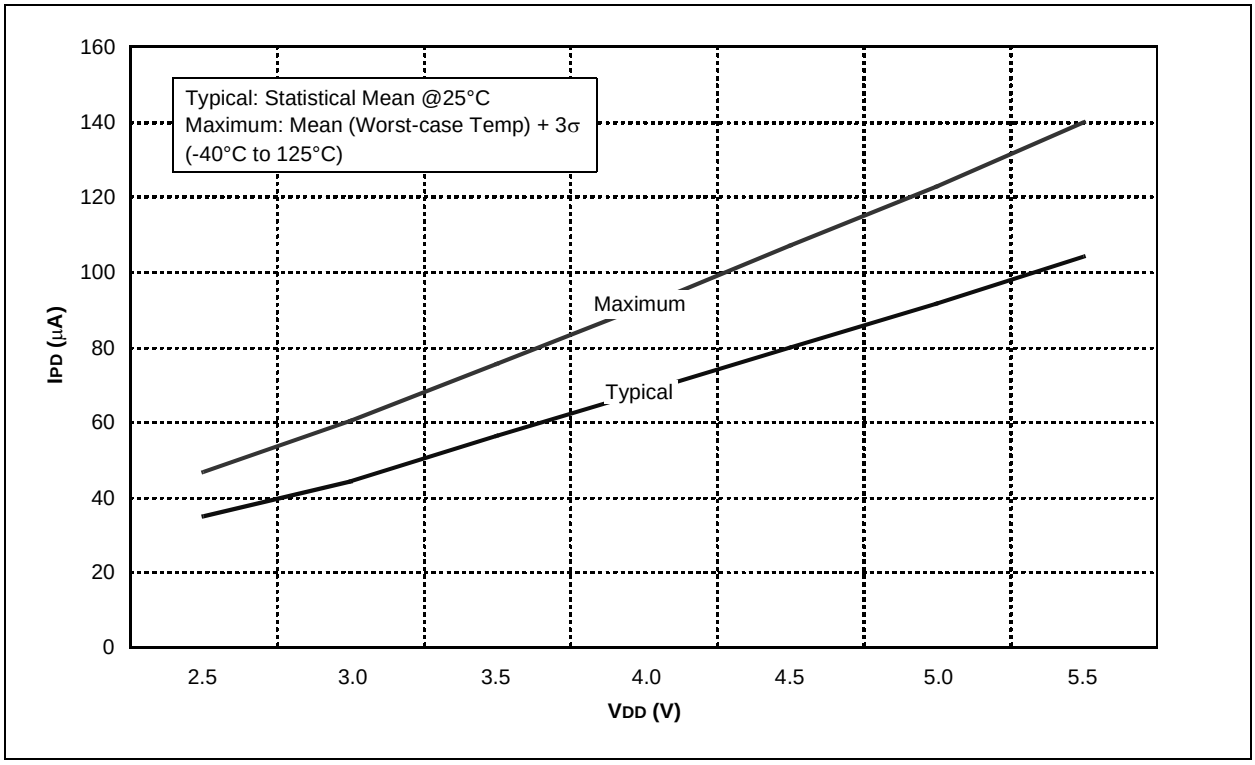


FIGURE 20-30: ADC CLOCK PERIOD vs. VDD OVER TEMPERATURE

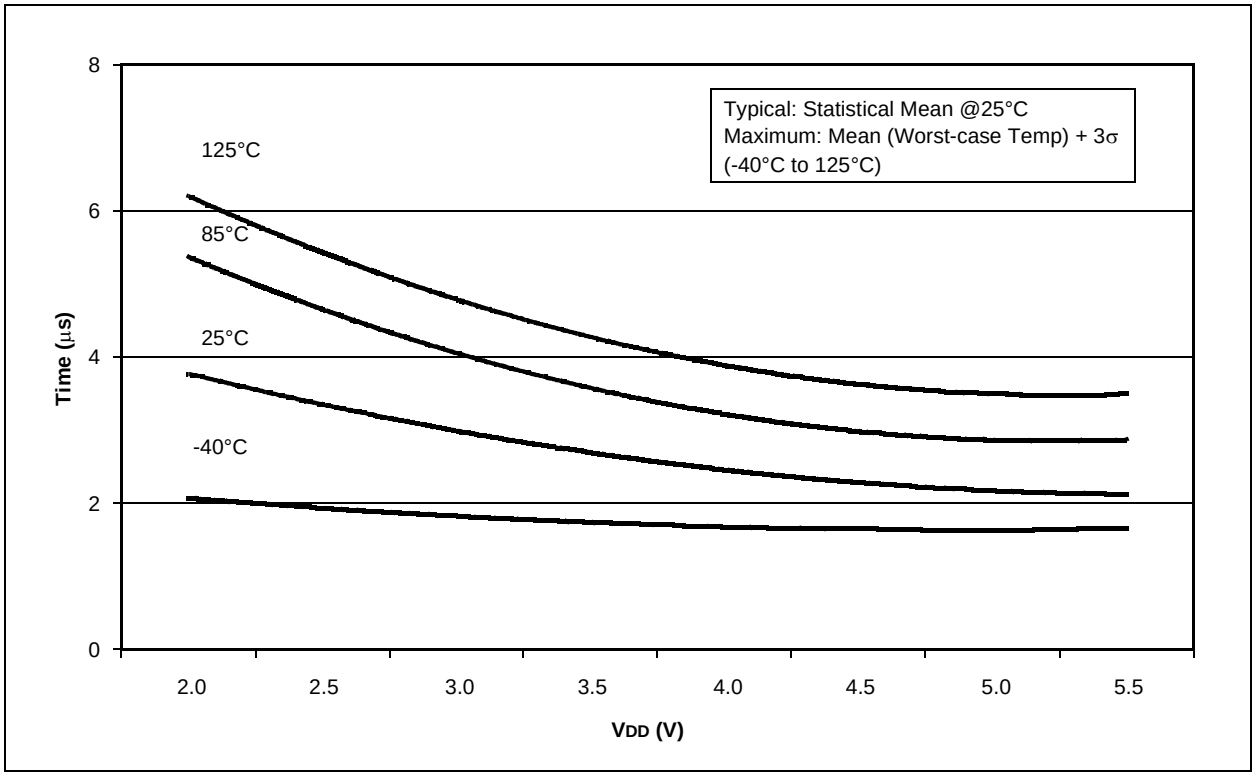


FIGURE 20-31: TYPICAL HFINTOSC START-UP TIMES vs. VDD OVER TEMPERATURE

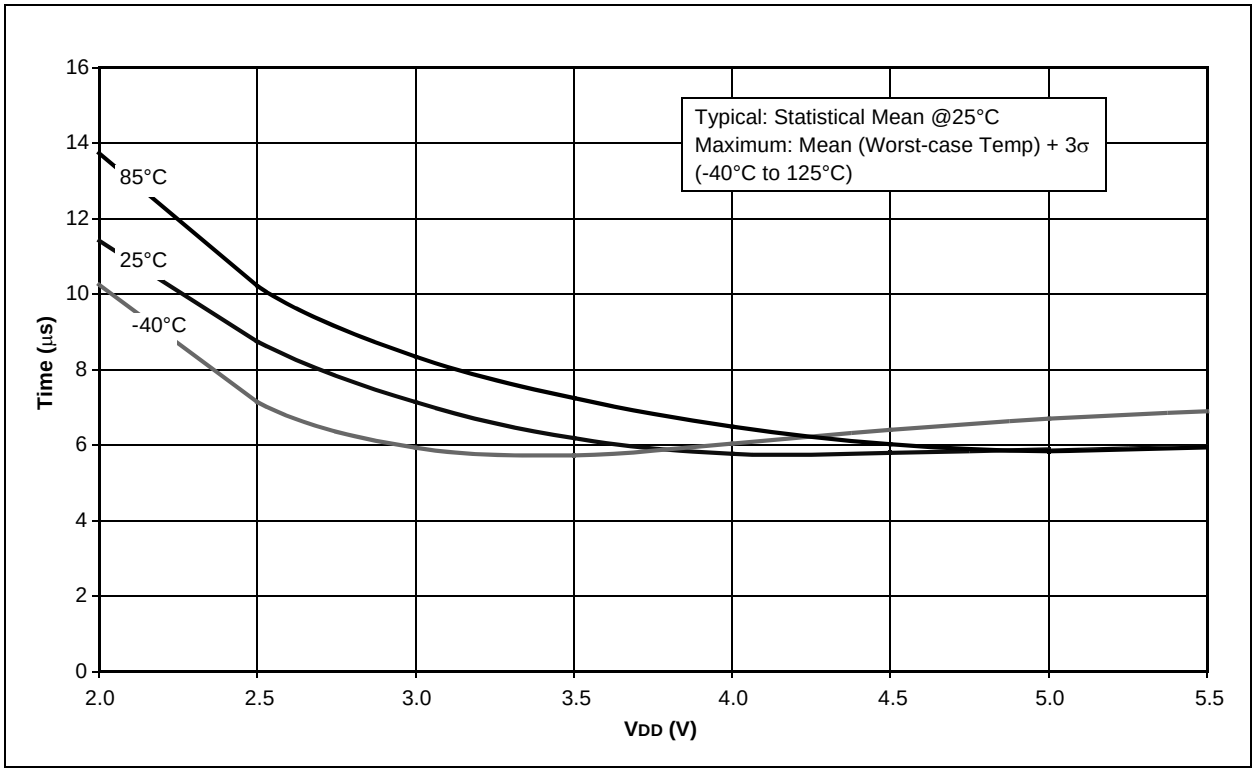


FIGURE 20-44: TYPICAL VP6 REFERENCE VOLTAGE DISTRIBUTION (3V, 25°C)

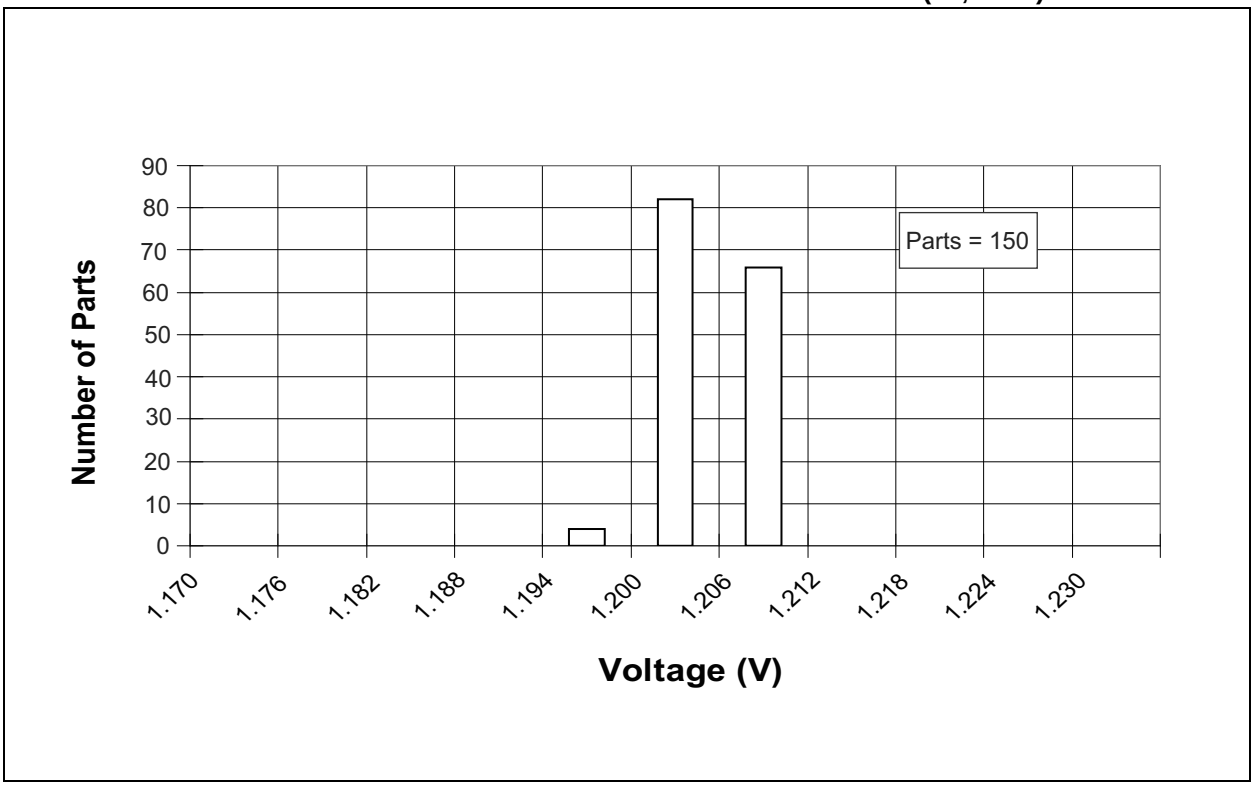
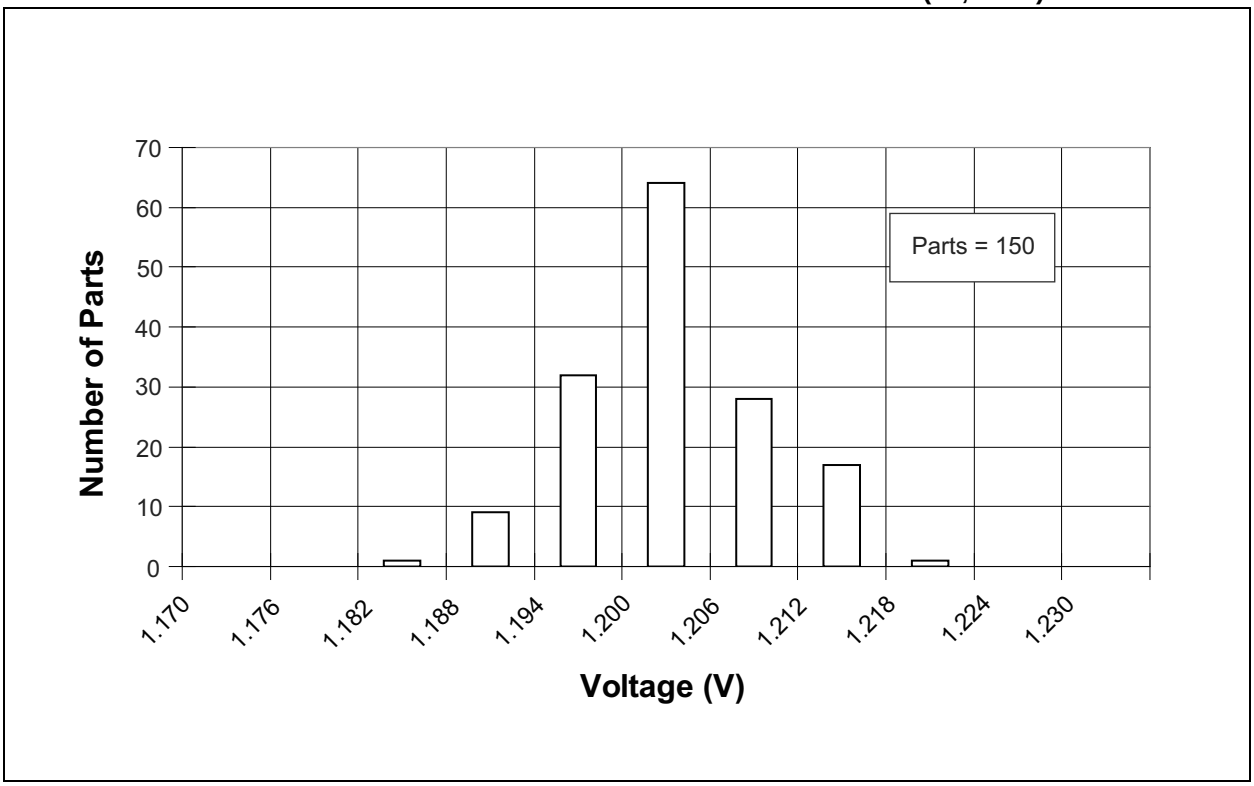
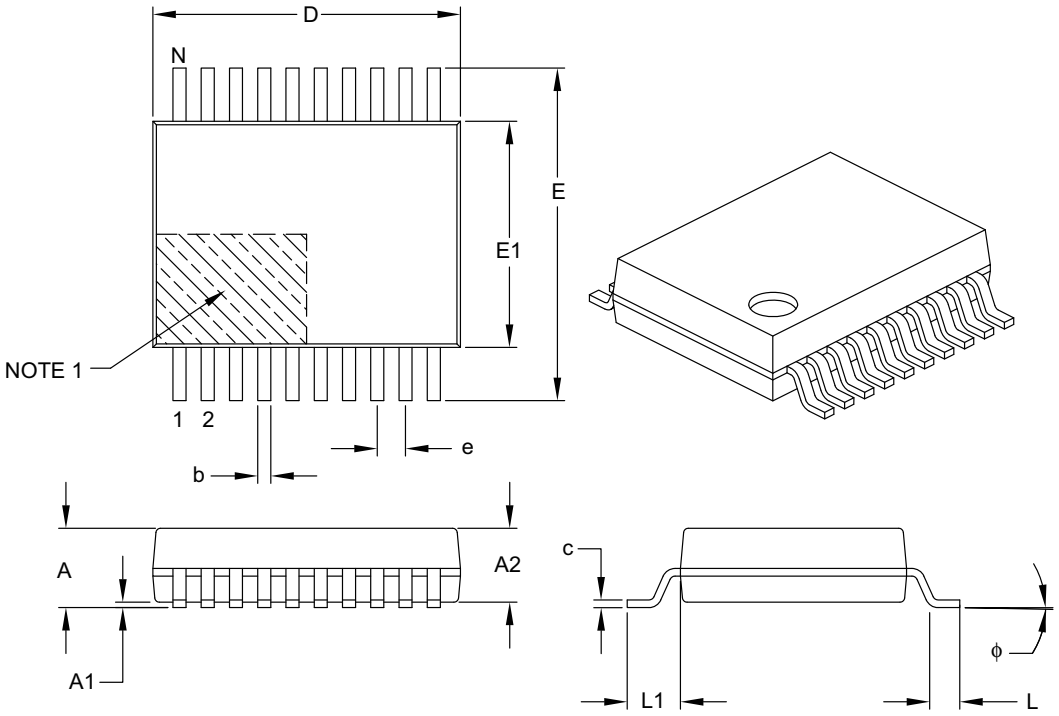


FIGURE 20-45: TYPICAL VP6 REFERENCE VOLTAGE DISTRIBUTION (3V, 85°C)



20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	6.90	7.20	7.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

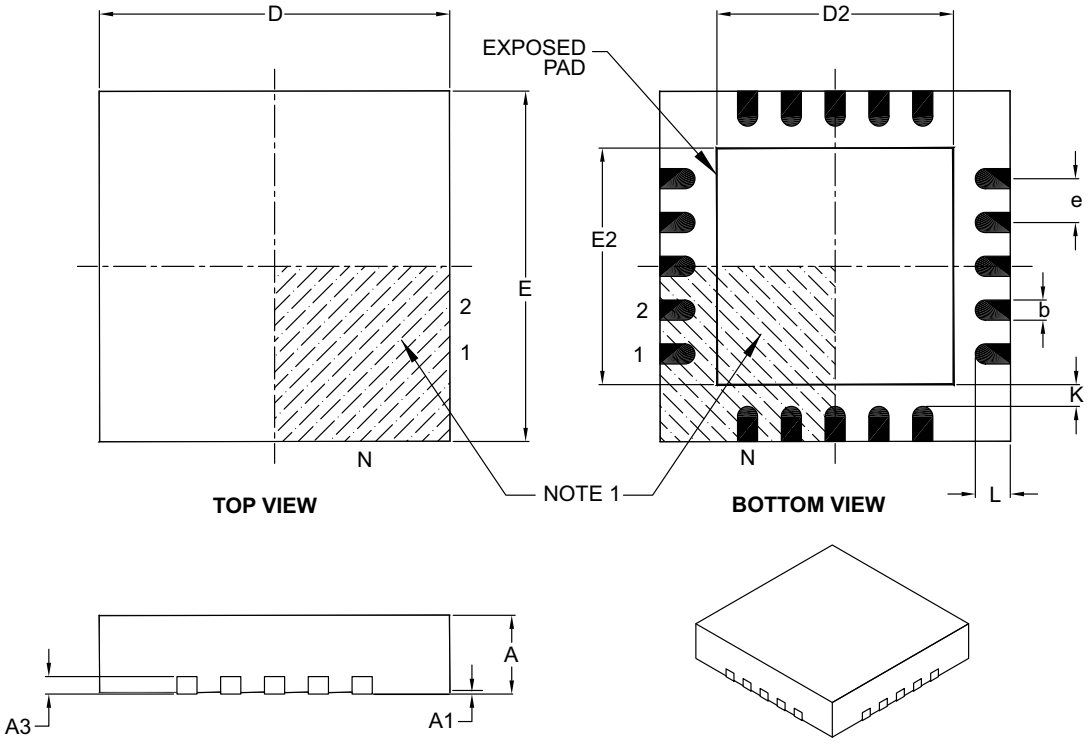
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B

20-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.60	2.70	2.80
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.60	2.70	2.80
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-126B