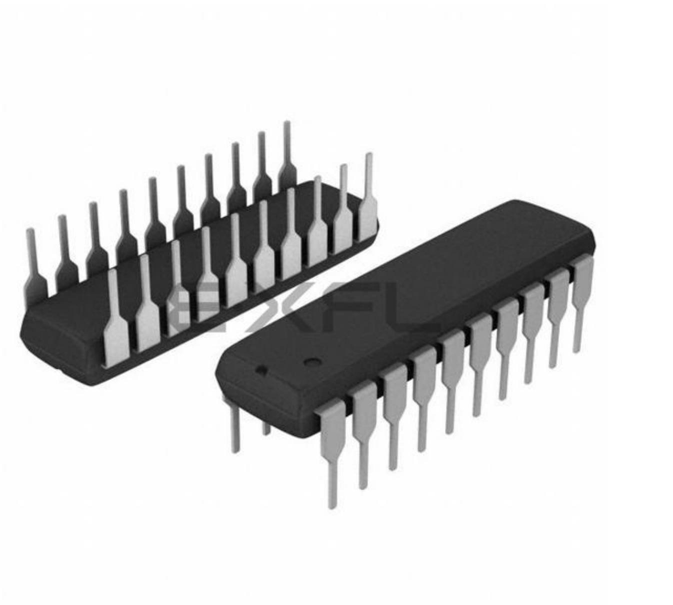

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 14x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f785-i-p

2.2.2.6 PCON Register

The Power Control register contains flag bits to allow differentiation between a Power-on Reset ($\overline{\text{POR}}$), a Brown-out Reset ($\overline{\text{BOR}}$), a Watchdog Timer (WDT) Reset (WDT) and an external $\overline{\text{MCLR}}$ Reset.

REGISTER 2-6: PCON: POWER CONTROL REGISTER

U-0	U-0	U-0	R/W-1	U-0	U-0	R/W-0	R/W-x
	—	—	—	SBOREN[1]	—	—	$\overline{\text{POR}}$
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4 **SBOREN:** Software BOR Enable bit[1]
1 = BOR enabled
0 = BOR disabled

bit 3-2 **Unimplemented:** Read as ‘0’

bit 1 **$\overline{\text{POR}}$:** Power-on Reset Status bit
1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{\text{BOR}}$:** Brown-out Reset Status bit
1 = No Brown-out Reset occurred
0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

Note 1: BOREN<1:0> = 01 in Configuration Word for this bit to control the $\overline{\text{BOR}}$.

3.4.2.2 OSCTUNE Register

The HFINTOSC is factory calibrated but can be adjusted in software by writing to the OSCTUNE register (Register 3-1).

The OSCTUNE register has a nominal tuning range of ±12%. The default value of the OSCTUNE register is '0'. The value is a 5-bit two's complement number. Due to process variation, the monotonicity and frequency step cannot be specified.

When the OSCTUNE register is modified, the HFINTOSC frequency will begin shifting to the new frequency. The HFINTOSC clock will stabilize within 1 ms. Code execution continues during this shift. There is no indication that the shift has occurred.

OSCTUNE does not affect the LFINTOSC frequency. Operation of features that depend on the LFINTOSC clock source frequency, such as the Power-up Timer (PWRT), Watchdog Timer (WDT), Fail-Safe Clock Monitor (FSCM) and peripherals, are *not* affected by the change in frequency.

REGISTER 3-1: OSCTUNE: OSCILLATOR TUNING REGISTER

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **TUN<4:0>:** Frequency Tuning bits
01111 = Maximum frequency
01110 =
•
•
•
00001 =
00000 = Center frequency. Oscillator module is running at the calibrated frequency.
11111 =
•
•
•
10000 = Minimum frequency

4.4.1.8 RC5/CCP1

The RC5 is configurable to function as one of the following:

- General purpose I/O
- Digital input for the capture/compare
- Digital output for the CCP

FIGURE 4-14: BLOCK DIAGRAM OF RC5

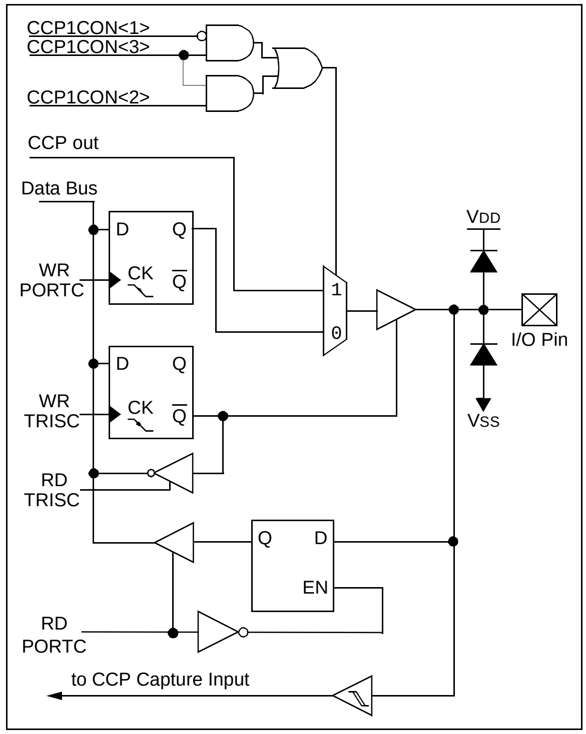


TABLE 4-3: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSEL1	—	—	—	—	ANS11	ANS10	ANS9	ANS8	---- 1111	---- 1111
CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	0000 0000	0000 0000
OPA1CON	OPAON	—	—	—	—	—	—	—	0--- ----	0--- ----
OPA2CON	OPAON	—	—	—	—	—	—	—	0--- ----	0--- ----
PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu
PWMCON0	PRSEN	PASEN	BLANK2	BLANK1	SYNC1	SYNC0	PH2EN	PH1EN	0000 0000	0000 0000
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged, – = unimplemented locations read as ‘0’. Shaded cells are not used by PORTC.

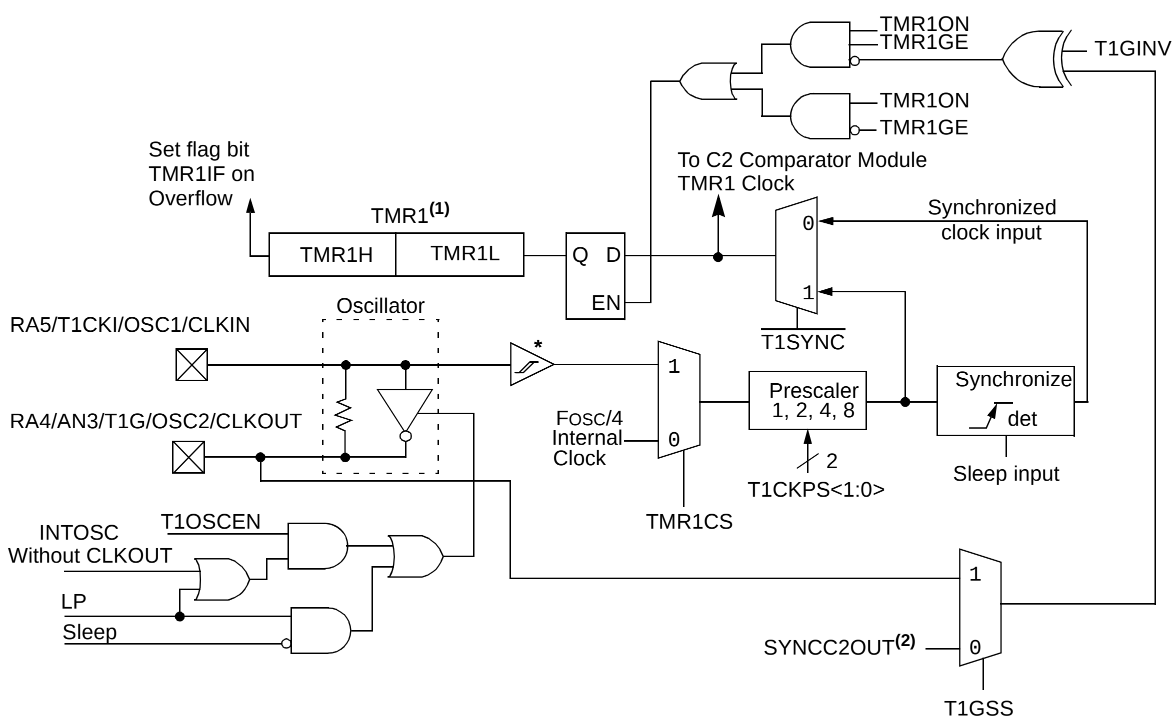
6.0 TIMER1 MODULE WITH GATE CONTROL

The Timer1 module is the 16-bit counter of the PIC16F785/HV785. Figure 6-1 shows the basic block diagram of the Timer1 module. Timer1 has the following features:

- 16-bit timer/counter (TMR1H:TMR1L)
- Readable and writable
- Internal or external clock selection
- Synchronous or asynchronous operation
- Interrupt on overflow from FFFFh to 0000h
- Wake-up upon overflow (Asynchronous mode)
- Optional external enable input:
  - Selectable gate source; T1G or C2 output (T1GSS)
  - Selectable gate polarity (T1GINV)
- Optional LP oscillator

The Timer1 Control register (T1CON), shown in Register 6-1, is used to enable/disable Timer1 and select the various features of the Timer1 module.

FIGURE 6-1: TIMER1 ON THE PIC16F785/HV785 BLOCK DIAGRAM



* ST Buffer is low power type when using LP OSC, or high-speed type when using T1CKI.

Note 1: Timer1 increments on the rising edge.

2: SYNCC2OUT is the synchronized output from Comparator 2 (See Figure 9-2 on 66).

6.5 Timer1 Operation in Asynchronous Counter Mode

If control bit $\overline{\text{T1SYNC}}$ of the T1CON Register is set, the external clock input is not synchronized. The timer continues to increment asynchronous to the internal phase clocks. The timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (**Section 6.5.1 "Reading and Writing Timer1 in Asynchronous Counter Mode"**).

> **Note:** The ANSEL0 (91h) register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.

6.5.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the timer register.

6.6 Timer1 Oscillator

A crystal oscillator circuit is built-in between pins OSC1 (input) and OSC2 (amplifier output). It is enabled by setting control bit T1OSCEN of the T1CON Register. The oscillator is a low power oscillator rated for 32.768 kHz. It will continue to run during Sleep. It is primarily intended for a 32.768 kHz tuning fork crystal.

The Timer1 oscillator is shared with the system LP oscillator. Thus, Timer1 can use this mode only when the primary system clock is also the LP oscillator or is derived from the internal oscillator. As with the system LP oscillator, the user must provide a software time delay to ensure proper oscillator start-up.

Sleep mode will not disable the system clock when the system clock and Timer1 share the LP oscillator.

TRISA<5> and TRISA<4> bits are set when the Timer1 oscillator is enabled. RA5 and RA4 read as '0' and TRISA<5> and TRISA<4> bits read as '1'.

> **Note:** The oscillator requires a start-up and stabilization time before use. Thus, T1OSCEN should be set and a suitable delay observed prior to enabling Timer1.

6.7 Timer1 Operation During Sleep

Timer1 can only operate during Sleep when setup in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To setup the timer to wake the device:

- Timer1 of the T1CON Register must be on
- TMR1IE bit of the PIE1 Register must be set
- PEIE bit of the INTCON Register must be set

The device will wake-up on an overflow. If the GIE bit of the INTCON Register is set, the device will wake-up and jump to the Interrupt Service Routine (0004h) on an overflow. If the GIE bit is clear, execution will continue with the next instruction.

TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER1

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSEL0	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111
CM2CON1	MC1OUT	MC2OUT	—	—	—	—	T1GSS	C2SYNC	00-- --10	00-- --10
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
PIE1	EEIE	ADIE	CCP1IE	C2IE	C1IE	OSFIE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	EEIF	ADIF	CCP1IF	C2IF	C1IF	OSFIF	TMR2IF	TMR1IF	0000 0000	0000 0000
T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	0000 0000	uuuu uuuu
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu

Legend: – x = unknown, u = unchanged, – = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.

7.2 Timer2 Interrupt

The Timer2 module has an 8-bit period register, PR2. Timer2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle. PR2 is a readable and writable register. The PR2 register is initialized to FFh upon Reset.

FIGURE 7-1: TIMER2 BLOCK DIAGRAM

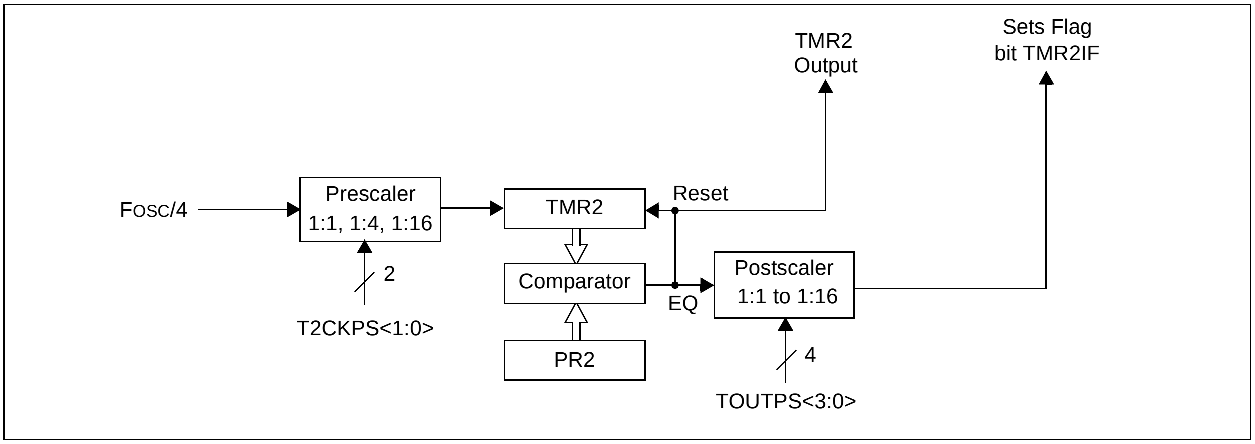


TABLE 7-1: REGISTERS ASSOCIATED WITH TIMER2

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
PIE1	EEIE	ADIE	CCP1IE	C2IE	C1IE	OSFIE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	EEIF	ADIF	CCP1IF	C2IF	C1IF	OSFIF	TMR2IF	TMR1IF	0000 0000	0000 0000
PR2	Timer2 Module Period register								1111 1111	1111 1111
T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
TMR2	Holding Register for the 8-bit TMR2 Register								0000 0000	0000 0000

Legend: – x = unknown, u = unchanged, – = unimplemented, read as ‘0’. Shaded cells are not used by the Timer2 module.

8.3 CCP PWM Mode

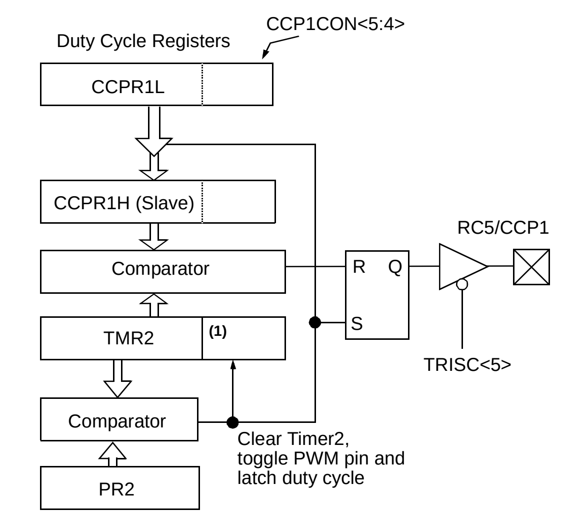
In Pulse Width Modulation (PWM) mode, the CCP module produces up to a 10-bit resolution PWM output on the RC5/CCP1 pin. Since the RC5/CCP1 pin is multiplexed with the PORTC data latch, the TRISC<5> must be cleared to make the RC5/CCP1 pin an output.

> **Note:** Clearing the CCP1CON register will force the PWM output latch to the default inactive levels. This is not the PORTC I/O data latch.

Figure 8-3 shows a simplified block diagram of PWM operation.

For a step by step procedure on how to set up the CCP module for PWM operation, see **Section 8.3.5 "Setup for PWM Operation"**.

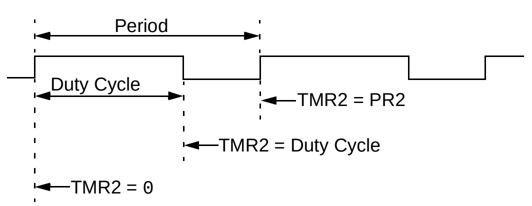
FIGURE 8-3: SIMPLIFIED PWM BLOCK DIAGRAM



Note 1: The 8-bit timer TMR2 register is concatenated with the 2-bit internal Q clock, or 2 bits of the prescaler, to create the 10-bit time base.

The PWM output (Figure 8-4) has a time base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/period).

FIGURE 8-4: CCP PWM OUTPUT



8.3.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the formula of Equation 8-1.

EQUATION 8-1: PWM PERIOD

$$PWM\ period = [(PR2) + 1] \bullet 4 \bullet T_{OSC} \bullet (TMR2\ prescale\ value)$$

PWM frequency is defined as 1/[PWM period].

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The RC5/CCP1 pin is set. (exception: if PWM duty cycle = 0%, the pin will not be set)
- The PWM duty cycle is latched from CCPR1L into CCPR1H

> **Note:** The Timer2 postscaler (see **Section 7.1 "Timer2 Operation"**) is not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

9.1.2.2 Control Register CM2CON1

Comparator C2 has one additional feature: its output can be synchronized to the Timer1 clock input. Setting C2SYNC of the CM2CON1 Register synchronizes the output of Comparator 2 to the falling edge of the Timer1 clock input (see Figure 9-2 and Register 9-3).

The CM2CON1 register also contains mirror copies of both comparator outputs, MC1OUT and MC2OUT of the CM2CON1 Register. The ability to read both outputs simultaneously from a single register eliminates the timing skew of reading separate registers.

Note:	Obtaining the status of C1OUT or C2OUT by reading CM2CON1 does not affect the comparator interrupt mismatch registers.

REGISTER 9-3: CM2CON1: COMPARATOR C2 CONTROL REGISTER 1

R-0	R-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0
MC1OUT	MC2OUT	—	—	—	—	T1GSS	C2SYNC
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7	**MC1OUT**: Mirror Copy of C1OUT bit (CM1CON0<6>)
bit 6	**MC2OUT**: Mirror Copy of C2OUT bit (CM2CON0<6>)
bit 5-2	**Unimplemented:** Read as ‘0’
bit 1	**T1GSS**: Timer1 Gate Source Select bit 1 = Timer1 gate source is RA4/AN3/T1G/OSC2/CLKOUT 0 = Timer1 gate source is SYNCC2OUT.
bit 0	**C2SYNC**: C2 Output Synchronous Mode bit 1 = C2 output is synchronous to falling edge of TMR1 clock 0 = C2 output is asynchronous

9.2 Comparator Outputs

The comparator outputs are read through the CM1CON0, COM2CON0 or CM2CON1 registers. CM1CON0 and CM2CON0 each contain the individual comparator output of Comparator 1 and Comparator 2, respectively. CM2CON2 contains a mirror copy of both comparator outputs facilitating a simultaneous read of both comparators. These bits are read-only. The comparator outputs may also be directly output to the RA2/AN2/T0CKI/INT/C1OUT and RC4/C2OUT/PH2 I/O pins. When enabled, multiplexers in the output path of the RA2 and RC4 pins will switch and the output of each pin will be the unsynchronized output of the comparator. The uncertainty of each of the comparators is related to the input offset voltage and the response time given in the specifications. Figure 9-1 and Figure 9-2 show the output block diagrams for Comparators 1 and 2, respectively.

The TRIS bits will still function as an output enable/disable for the RA2/AN2/T0CKI/INT/C1OUT and RC4/C2OUT/PH2 pins while in this mode.

The polarity of the comparator outputs can be changed using the C1POL and C2POL bits of the CMxCON0 Register.

Timer1 gate source can be configured to use the T1G pin or Comparator 2 output as selected by the T1GSS bit of the CM2CON1 Register. The Timer1 gate feature can be used to time the duration or interval of analog events. The output of Comparator 2 can also be synchronized with Timer1 by setting the C2SYNC bit of the CM2CON1 Register. When enabled, the output of Comparator 2 is latched on the falling edge of the Timer1 clock source. If a prescaler is used with Timer1, Comparator 2 is latched after the prescaler. To prevent a race condition, the Comparator 2 output is latched on the falling edge of the Timer1 clock source and Timer1 increments on the rising edge of its clock source. See the Comparator 2 Block Diagram (Figure 9-2) and the Timer1 Block Diagram (Figure 6-1) for more information.

It is recommended to synchronize Comparator 2 with Timer1 by setting the C2SYNC bit when Comparator 2 is used as the Timer1 gate source. This ensures Timer1 does not miss an increment if Comparator 2 changes during an increment.

9.3 Comparator Interrupts

The comparator interrupt flags are set whenever there is a change in the output value of its respective comparator. Software will need to maintain information about the status of the output bits, as read from CM2CON0<7:6>, to determine the actual change that has occurred. The CxIF bits, PIR1<4:3>, are the Comparator Interrupt Flags. Each comparator interrupt bit must be reset in software by clearing it to ‘0’. Since it is also possible to write a ‘1’ to this register, a simulated interrupt may be initiated.

The CxIE bits of the PIE1 Register and the PEIE bit of the INTCON Register must be set to enable the interrupts. In addition, the GIE bit must also be set. If any of these bits are cleared, the interrupt is not enabled, though the CxIF bits will still be set if an interrupt condition occurs.

The comparator interrupt of the PIC16F785/HV785 differs from previous designs in that the interrupt flag is set by the mismatch edge and not the mismatch level. This means that the interrupt flag can be reset without the additional step of reading or writing the CMxCON0 register to clear the mismatch registers. When the mismatch registers are not cleared, an interrupt will not occur when the comparator output returns to the previous state. When the mismatch registers are cleared, an interrupt will occur when the comparator returns to the previous state.

Note 1: If a change in the CMxCON0 register (CxOUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CxIF of the PIR1 Register interrupt flag may not get set.

2: When either comparator is first enabled, bias circuitry in the Comparator module may cause an invalid output from the comparator until the bias circuitry is stable. Allow about 1 μs for bias settling then clear the mismatch condition and interrupt flags before enabling comparator interrupts.

9.4 Effects of Reset

A Reset forces all registers to their Reset state. This disables both comparators.

10.2 VR Reference Module

The VR Reference module generates a 1.2V nominal output voltage for use by the ADC and comparators. The output voltage can also be brought out to the VREF pin for user applications. This module uses a bandgap as a reference. See Table 19-9 for detailed specifications. Register 10-2 shows the control register for the VR module.

REGISTER 10-2: REFCON: VOLTAGE REFERENCE CONTROL REGISTER

U-0	U-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
—	—	BGST	VRBB	VREN	VROE	CVROE	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5 **BGST:** Band Gap Reference Voltage Stable Flag bit
1 = Reference is stable
0 = Reference is not stable

bit 4 **VRBB:** Voltage Reference Buffer Bypass bit
1 = VREF output is not buffered. Power is removed from buffer amplifier.
0 = VREF output is buffered(1)

bit 3 **VREN:** Voltage Reference Enable bit (VR = 1.2V nominal)(2)
1 = VR reference is enabled
0 = VR reference is disabled and does not consume any current

bit 2 **VROE:** Voltage Reference Output Enable bit
If CVROE = 0:
1 = VREF output on RA1/AN1/C12IN0-/VREF/ICSPCLK pin is 1.2 volt VR analog reference
0 = Disabled, 1.2 volt VR analog reference is used internally only
If CVROE = 1:
VROE has no effect.

bit 1 **CVROE**: Comparator Voltage Reference Output Enable bit (see Figure 10-2)
1 = VREF output on RA1/AN1/C12IN0-/VREF/ICSPCLK pin is CVREF voltage
0 = VREF output on RA1/AN1/C12IN0-/VREF/ICSPCLK pin is controlled by VROE

bit 0 **Unimplemented:** Read as ‘0’

Note 1: Buffer amplifier common mode limitations require VREF ≤ (VDD - 1.4)V for buffered output.
2: VREN is fixed high for PIC16HV785 device.

12.2 A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (C_{HOLD}) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 12-4. The source impedance (R_S) and the internal sampling switch (R_{SS}) impedance directly affect the time required to charge the capacitor C_{HOLD}. The sampling switch (R_{SS}) impedance varies over the device voltage (V_{DD}), see Figure 12-4. **The maximum recommended impedance for analog sources is 10 kΩ**. As the impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (changed), this acquisition must be done before the conversion can be started.

To calculate the minimum acquisition time, Equation 12-1 may be used. This equation assumes that 1/2 LSb error is used (1024 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

EQUATION 12-1: ACQUISITION TIME EXAMPLE

Assumptions: $Temperature = 50°C$ *and external impedance of* $10k\Omega$ $5.0V$ V_{DD}

$$T_{ACQ} = \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient}$$
$$= T_{AMP} + T_C + T_{COFF}$$
$$= 5\mu s + T_C + [(Temperature - 25°C)(0.05\mu s/°C)]$$

The value for T_C *can be approximated with the following equations:*

$$V_{APPLIED}\left(1 - \frac{1}{2047}\right) = V_{CHOLD} \quad \text{;[1] Vchold charged to within 1/2 lsb}$$

$$V_{APPLIED}\left(1 - e^{\frac{-T_C}{RC}}\right) = V_{CHOLD} \quad \text{;[2] Vchold charge response to Vapplied}$$

$$V_{APPLIED}\left(1 - e^{\frac{-T_C}{RC}}\right) = V_{APPLIED}\left(1 - \frac{1}{2047}\right) \quad \text{;Combining [1] and [2]}$$

Solving for T_C:

$$T_C = -C_{HOLD}(R_{IC} + R_{SS} + R_S)\ ln(1/2047)$$
$$= -10pF(1k\Omega + 7k\Omega + 10k\Omega)\ ln(0.0004885)$$
$$= 1.37\mu s$$

Therefore:

$$T_{ACQ} = 5\mu s + 1.37\mu s + [(50°C - 25°C)(0.05\mu s/°C)]$$
$$= 7.62\mu s$$

Note 1:	The reference voltage (V_{REF}) has no effect on the equation, since it cancels itself out.
2:	The charge holding capacitor (C_{HOLD}) is not discharged after each conversion.
3:	The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.

REGISTER 13-4: PWMPH2: PWM PHASE 2 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POL	C2EN	C1EN	PH4	PH3	PH2	PH1	PH0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **POL:** PH2 Output Polarity bit
- 1 = PH2 Pin is active low
- 0 = PH2 Pin is active high

bit 6 **C2EN:** Comparator 2 Enable bit

When COMOD<1:0> = 00[(1)]
- 1 = PH2 is reset when C2OUT goes high
- 0 = PH2 ignores Comparator 2

When COMOD<1:0> = 1X or X1[(1)]
- C2EN has no effect

bit 5 **C1EN:** Comparator 1 Enable bit

When COMOD<1:0> = 00[(1)]
- 1 = PH2 is reset when C1OUT goes high
- 0 = PH2 ignores Comparator 1

When COMOD<1:0> = 1X or X1[(1)]
- C1EN has no effect

bit 4-0 **PH<4:0>:** PWM Phase bits

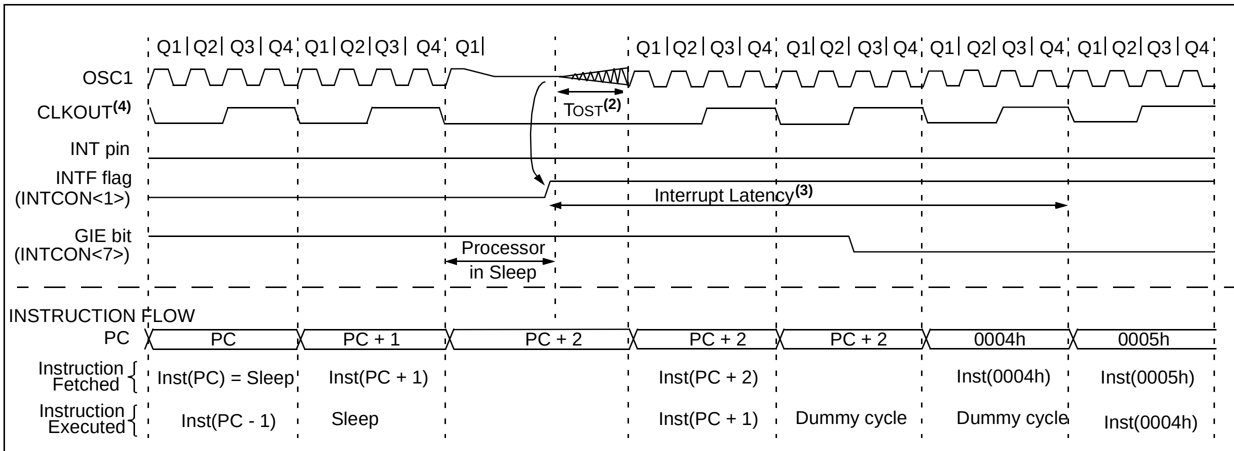
When COMOD<1:0> = 00[(1)]
- 00000 = PH2 starts 1 pwm_clk period after falling edge of SYNC pulse. All other PH2 delays are expressed relative to this time.
- 00001 = PH2 is delayed by 1 pwm_clk pulse
- ••••• = •••
- 11111 = PH2 is delayed by 31 pwm_clk pulses

When COMOD<1:0> = 1X[(1)]
- 00000 = Complementary drive terminates 1 pwm_clk period after falling edge of SYNC pulse. All other PH2 delays are expressed relative to this time.
- 00001 = Complementary drive termination is delayed by 1 pwm_clk pulse
- ••••• = •••
- 11111 = Complementary drive termination is delayed by 31 pwm_clk pulses

When COMOD<1:0> = 01[(1)]
- PH<4:0> has no effect.

Note 1: See PWMCON1 register (Register 13-5).

FIGURE 15-10: WAKE-UP FROM SLEEP THROUGH INTERRUPT(1)



Note 1: XT, HS or LP Oscillator mode assumed.

2: TOST = 1024TOSC (drawing not to scale). This delay does not apply to EC, RC and INTOSC Oscillator modes or Two-Speed Start-up (see **Section 3.6 "Two-Speed Clock Start-up Mode"**).

3: GIE = `1` assumed. In this case after wake-up, the processor jumps to 0004h. If GIE = `0`, execution will continue in-line.

4: CLKOUT is not available in XT, HS, LP or EC Oscillator modes, but shown here for timing reference.

15.7 Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out using ICSP™ for verification purposes.

Note:	If the code protection is turned off, the entire data EEPROM and Flash program memory will be erased by performing a bulk erase command. See the "PIC16F785/HV785 *Memory Programming Specification*" (DS41237) for more information.

15.8 ID Locations

Four memory locations (2000h-2003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution, but are readable and writable during Program/Verify. Only the Least Significant 7 bits of the ID locations are used.

15.9 In-Circuit Serial Programming™ (ICSP™)

The PIC16F785/HV785 microcontrollers can be serially programmed while in the end application circuit. This is simply done with five lines:

- Clock
- Data
- Power
- Ground
- Programming voltage

This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware, or a custom firmware, to be programmed.

The device is placed into a Program/Verify mode by holding the RA0 and RA1 pins low, while raising the MCLR (VPP) pin from VIL to VIHH. See the "PIC16F785/HV785 *Memory Programming Specification*" (DS41237) for more information. RA0 becomes the programming data and RA1 becomes the programming clock. Both RA0 and RA1 are Schmitt Trigger inputs in this mode.

After Reset, to place the device into Program/Verify mode, the Program Counter (PC) is at location 00h. A 6-bit command is then supplied to the device. Depending on the command, 14 bits of program data are then supplied to or from the device, depending on whether the command was a load or a read. For complete details of serial programming, please refer to the "PIC16F785/HV785 *Memory Programming Specification*" (DS41237).

A typical In-Circuit Serial Programming connection is shown in Figure 15-11.

BTFSC	Bit Test f, Skip if Clear
Syntax:	[*label*] BTFSC f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	skip if (f<b>) = `0`
Status Affected:	None
Description:	If bit ‘b’ in register ‘f’ is ‘`1`’, the next instruction is executed. If bit ‘b’, in register ‘f’, is ‘`0`’, the next instruction is discarded, and a `NOP` is executed instead, making this a two-cycle instruction.

BTFSS	Bit Test f, Skip if Set
Syntax:	[*label*] BTFSS f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b < 7
Operation:	skip if (f<b>) = `1`
Status Affected:	None
Description:	If bit ‘b’ in register ‘f’ is ‘`0`’, the next instruction is executed. If bit ‘b’ is ‘`1`’, then the next instruction is discarded and a `NOP` is executed instead, making this a two-cycle instruction.

CALL	Call Subroutine
Syntax:	[*label*] CALL k
Operands:	0 ≤ k ≤ 2047
Operation:	(PC)+ 1→ TOS, k → PC<10:0>, (PCLATH<4:3>) → PC<12:11>
Status Affected:	None
Description:	Call Subroutine. First, return address (PC + 1) is pushed onto the stack. The eleven-bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. `CALL` is a two-cycle instruction.

CLRF	Clear f
Syntax:	[*label*] CLRF f
Operands:	0 ≤ f ≤ 127
Operation:	00h → (f) 1 → Z
Status Affected:	Z
Description:	The contents of register ‘f’ are cleared and the Z bit is set.

CLRW	Clear W
Syntax:	[*label*] CLRW
Operands:	None
Operation:	00h → (W) 1 → Z
Status Affected:	Z
Description:	W register is cleared. Zero bit (Z) is set.

CLRWDT	Clear Watchdog Timer
Syntax:	[*label*] CLRWDT
Operands:	None
Operation:	00h → WDT 0 → WDT prescaler, 1 → $\overline{TO}$ 1 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	`CLRWDT` instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits $\overline{TO}$ and $\overline{PD}$ are set.

XORWF	Exclusive OR W with f			
Syntax:	[*label*] XORWF f,d			
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$			
Operation:	(W) .XOR. (f) → (dest)			
Status Affected:	Z			
Encoding:	`00`	`0110`	`dfff`	`ffff`
Description:	Exclusive OR the contents of the W register with register ‘f’. If ‘d’ is ‘0’, the result is stored in the W register. If ‘d’ is ‘1’ the result is stored back in register ‘f’.			

FIGURE 19-4: CLKOUT AND I/O TIMING

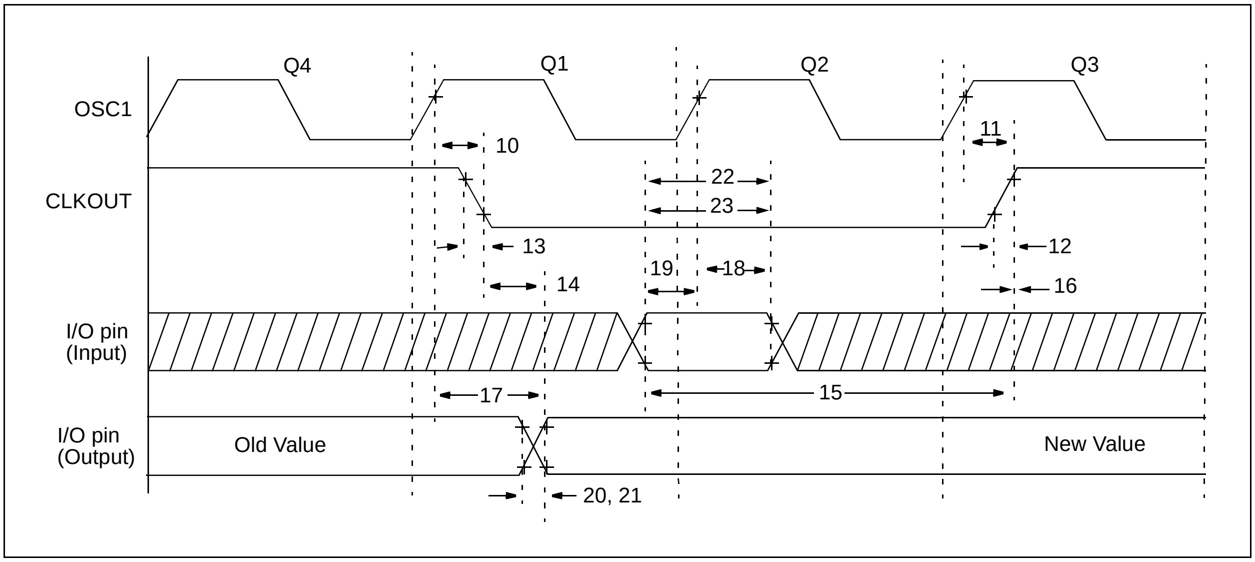


TABLE 19-2: CLKOUT AND I/O TIMING REQUIREMENTS

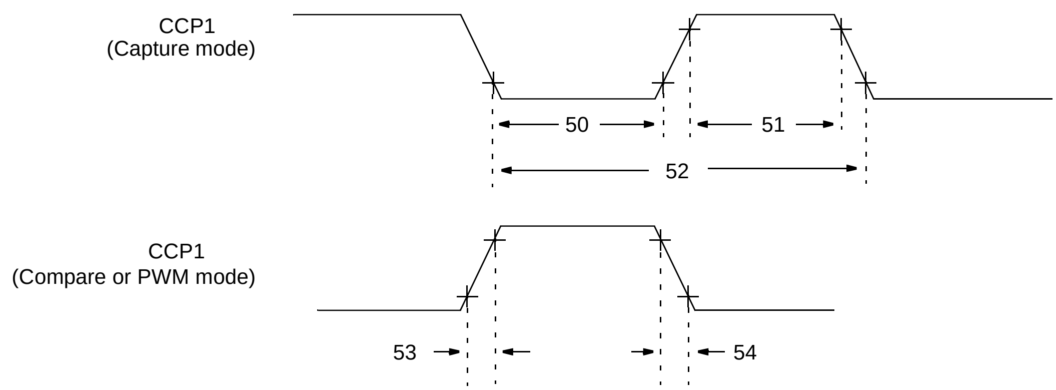
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
10	TOSH2CKL	OSC1↑ to CLKOUT↓	—	75	200	ns	**(Note 1)**
11	TOSH2CKH	OSC1↑ to CLKOUT↑	—	75	200	ns	**(Note 1)**
12	TCKR	CLKOUT rise time	—	35	100	ns	**(Note 1)**
13	TCKF	CLKOUT fall time	—	35	100	ns	**(Note 1)**
14	TCKL2IOV	CLKOUT↓ to Port out valid	—	—	20	ns	**(Note 1)**
15	TIOV2CKH	Port input valid before CLKOUT↑	TOSC + 200 ns	—	—	ns	**(Note 1)**
16	TCKH2IOI	Port input hold after CLKOUT↑	0	—	—	ns	**(Note 1)**
17	TOSH2IOV	OSC1↑ (Q1 cycle) to Port out valid	—	50	150 *	ns	
			—	—	300	ns	
18	TOSH2IOI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	100	—	—	ns	
19	TIOV2OSH	Port input valid to OSC1↑ (I/O in setup time)	0	—	—	ns	
20	TIOR	Port output rise time	—	10	40	ns	
21	TIOF	Port output fall time	—	10	40	ns	
22	TINP	INT pin high or low time	25	—	—	ns	
23	TRBP	PORTA interrupt-on-change high or low time	TCY	—	—	ns	

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated.

Note 1: Measurements are taken in RC mode where CLKOUT output is 4 x TOSC.

FIGURE 19-8: CAPTURE/COMPARE/PWM TIMINGS (CCP)



Note: Refer to Figure 19-2 for load conditions.

TABLE 19-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP)

Param No.	Symbol	Characteristic		Min	Typ†	Max	Units	Conditions
50*	TCCL	CCP1 input low time	No Prescaler	0.5TCY + 20	—	—	ns	
			With Prescaler	20	—	—	ns	
51*	TCCH	CCP1 input high time	No Prescaler	0.5TCY + 20	—	—	ns	
			With Prescaler	20	—	—	ns	
52*	TCCP	CCP1 input period		$\frac{3T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1,4 or 16)
53*	TCCR	CCP1 output rise time		—	25	50	ns	
54*	TCCF	CCP1 output fall time		—	25	45	ns	

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 19-7: COMPARATOR SPECIFICATIONS

Comparator Specifications			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C				
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
C01	VOS	Input Offset Voltage	—	±5	±10	mV	
C02	VCM	Input Common Mode Voltage	0	—	VDD – 1.5	V	
C03	ILC	Input Leakage Current	—	—	200*	nA	
C04	CMRR	Common Mode Rejection Ratio	+70*	—	—	dB	
C05	TRT	Response Time(1)	— —	— —	20* 40*	ns ns	Internal Output to pin

* These parameters are characterized but not tested.

Note 1: Response time measured with one comparator input at (VDD – 1.5)/2, while the other input transitions from VSS to VDD – 1.5V.

TABLE 19-8: COMPARATOR VOLTAGE REFERENCE (CVREF) SPECIFICATIONS

Comparator Voltage Reference Specifications			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C				
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
CV01	CVRES	Resolution	— —	VDD/24* VDD/32	— —	LSb LSb	Low Range (VRR = 1) High Range (VRR = 0)
CV02		Absolute Accuracy	— —	— —	±1/4* ±1/2*	LSb LSb	Low Range (VRR = 1) High Range (VRR = 0)
CV03		Unit Resistor Value (R)	—	2K*	—	Ω	
CV04		Settling Time(1)	—	—	10*	μs	

* These parameters are characterized but not tested.

Note 1: Settling time measured while VRR = 1 and VR<3:0> transitions from '0000' to '1111'.

TABLE 19-9: VOLTAGE REFERENCE (VR) SPECIFICATIONS

VR Voltage Reference Specifications			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C Operating Voltage 3.0V ≤ VDD ≤ 5.5V				
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
VR01	VROUT	VR voltage output	1.188 1.176 1.164	1.200 1.200 1.200	1.212 1.224 1.236	V V V	TA = 25°C 0°C ≤ TA ≤ +85°C -40°C ≤ TA ≤ +125°C

TABLE 19-10: VOLTAGE REFERENCE OUTPUT (VREF) BUFFER SPECIFICATIONS

Voltage Reference Output Buffer Specifications			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C Operating voltage 3.0V ≤ VDD ≤ 5.5V				
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
VB01*	CL	External capacitor load	—	—	200	pF	

* These parameters are characterized but not tested.

FIGURE 20-24: V_{OL} vs. I_{OL} OVER TEMPERATURE (V_{DD} = 5.0V)

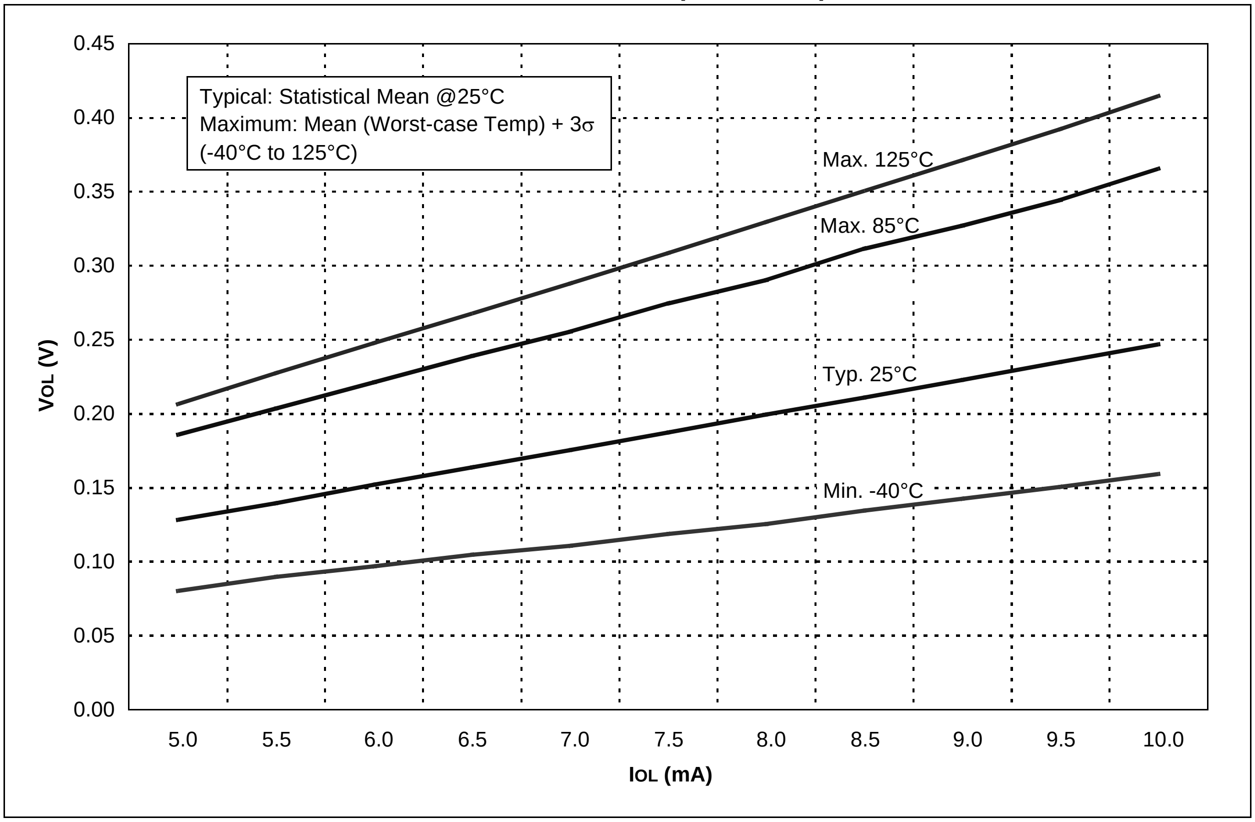


FIGURE 20-25: V_{OH} vs. I_{OH} OVER TEMPERATURE (V_{DD} = 3.0V)