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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 14x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f785-i-so

QFN (4x4x0.9) Pin Diagram

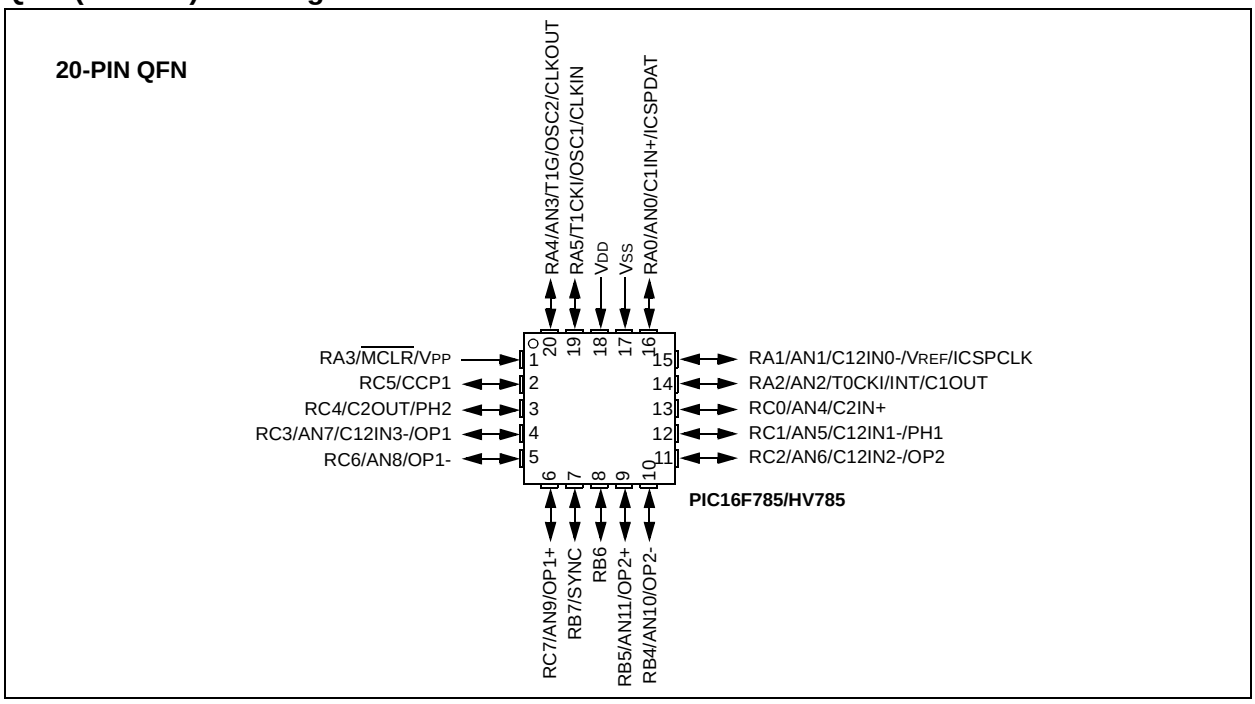


TABLE 2: QFN PIN SUMMARY

I/O	Pin	Analog	Comp.	Op Amps	PWM	Timers	CCP	Interrupt	Pull-ups	Basic
RA0	16	AN0	C1IN+	—	—	—	—	IOC	Y	ICSPDAT
RA1	15	AN1/VREF	C12IN0-	—	—	—	—	IOC	Y	ICSPCLK
RA2	14	AN2	C1OUT	—	—	T0CKI	—	INT/IOC	Y	—
RA3(1)	1	—	—	—	—	—	—	IOC	Y	$\overline{\text{MCLR}}$/VPP
RA4	20	AN3	—	—	—	T1G	—	IOC	Y	OSC2/CLKOUT
RA5	19	—	—	—	—	T1CKI	—	IOC	Y	OSC1/CLKIN
RB4	10	AN10	—	OP2-	—	—	—	—	—	—
RB5	9	AN11	—	OP2+	—	—	—	—	—	—
RB6(2)	8	—	—	—	—	—	—	—	—	—
RB7	7	—	—	—	SYNC	—	—	—	—	—
RC0	13	AN4	C2IN+	—	—	—	—	—	—	—
RC1	12	AN5	C12IN1-	—	PH1	—	—	—	—	—
RC2	11	AN6	C12IN2-	OP2	—	—	—	—	—	—
RC3	4	AN7	C12IN3-	OP1	—	—	—	—	—	—
RC4	3	—	C2OUT	—	PH2	—	—	—	—	—
RC5	2	—	—	—	—	—	CCP1	—	—	—
RC6	5	AN8	—	OP1-	—	—	—	—	—	—
RC7	6	AN9	—	OP1+	—	—	—	—	—	—
—	18	—	—	—	—	—	—	—	—	VDD
—	17	—	—	—	—	—	—	—	—	VSS

Note 1: Input only.

2: Open drain.

TABLE 1-1: PIC16F785/HV785 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/C1IN+/ICSPDAT	RA0	TTL	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	AN0	AN	—	A/D Channel 0 input
	C1IN+	AN	—	Comparator 1 non-inverting input
	ICSPDAT	ST	CMOS	Serial Programming Data I/O
RA1/AN1/C12IN0-/VREF/ ICSPCLK	RA1	TTL	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	AN1	AN	—	A/D Channel 1 input
	C12IN0-	AN	—	Comparator 1 and 2 inverting input
	VREF	AN	AN	External Voltage Reference for A/D, buffered reference output
	ICSPCLK	ST	—	Serial Programming Clock
RA2/AN2/T0CKI/INT/C1OUT	RA2	ST	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	AN2	AN	—	A/D Channel 2 input
	T0CKI	ST	—	Timer0 clock input
	INT	ST	—	External Interrupt
	C1OUT	—	CMOS	Comparator 1 output
RA3/$\overline{\text{MCLR}}$/Vpp	RA3	TTL	—	PORTA input with prog. pull-up and interrupt-on-change
	$\overline{\text{MCLR}}$	ST	—	Master Clear with internal pull-up
	VPP	HV	—	Programming voltage
RA4/AN3/T1G/OSC2/ CLKOUT	RA4	TTL	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	AN3	AN	—	A/D Channel 3 input
	T1G	ST	—	Timer1 gate
	OSC2	—	XTAL	Crystal/Resonator
	CLKOUT	—	CMOS	FOSC/4 output
RA5/T1CKI/OSC1/CLKIN	RA5	TTL	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	T1CKI	ST	—	Timer1 clock
	OSC1	XTAL	—	Crystal/Resonator
	CLKIN	ST	—	External clock input/RC oscillator connection
RB4/AN10/OP2-	RB4	TTL	CMOS	PORTB I/O
	AN10	AN	—	A/D Channel 10 input
	OP2-	—	AN	Op Amp 2 inverting input
RB5/AN11/OP2+	RB5	TTL	CMOS	PORTB I/O
	AN11	AN	—	A/D Channel 11 input
	OP2+	—	AN	Op Amp 2 non-inverting input
RB6	RB6	TTL	OD	PORTB I/O. Open drain output
RB7/SYNC	RB7	TTL	CMOS	PORTB I/O
	SYNC	ST	CMOS	Master PWM Sync output or slave PWM Sync input
RC0/AN4/C2IN+	RC0	TTL	CMOS	PORTC I/O
	AN4	AN	—	A/D Channel 4 input
	C2IN+	AN	—	Comparator 2 non-inverting input

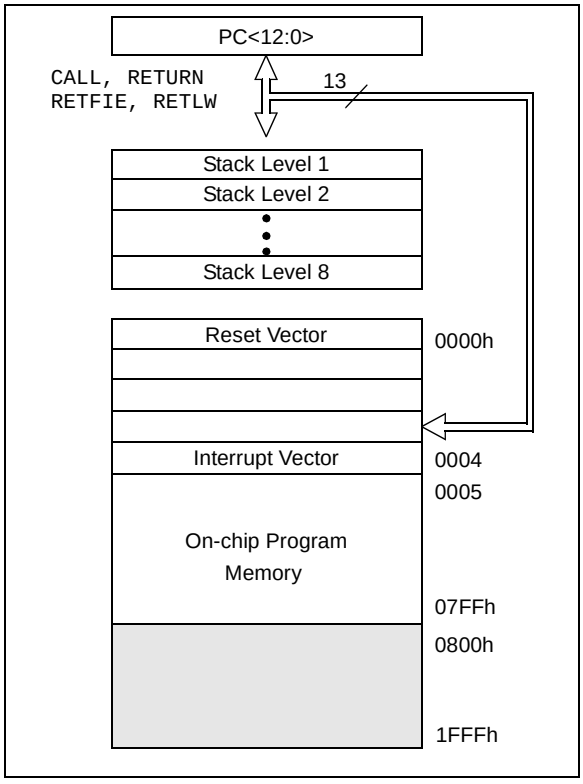
Legend: TTL = TTL input buffer, ST = Schmitt Trigger input buffer, AN = Analog, OD = Open Drain output, HV = High Voltage

2.0 MEMORY ORGANIZATION

2.1 Program Memory Organization

The PIC16F785/HV785 has a 13-bit program counter capable of addressing an 8k x 14 program memory space. Only the first 2k x 14 (0000h-07FFh) for the PIC16F785/HV785 is physically implemented. Accessing a location above these boundaries will cause a wrap around within the first 2k x 14 space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 2-1).

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK FOR THE PIC16F785/HV785



2.2 Data Memory Organization

The data memory (see Figure 2-2) is partitioned into four banks, which contain the General Purpose Registers (GPR) and the Special Function Registers (SFR). The Special Function Registers are located in the first 32 locations of each bank. Register locations 20h-7Fh in Bank 0 and A0h-BFh in Bank 1 are General Purpose Registers, implemented as static RAM. The last sixteen register locations in Bank 1 (F0h-FFh), Bank 2 (170h-17Fh), and Bank 3 (1F0h-1FFh) point to addresses 70h-7Fh in Bank 0. All other RAM is unimplemented and returns '0' when read.

Seven address bits are required to access any location in a data memory bank. Two additional bits are required to access the four banks. When data memory is accessed directly, the seven Least Significant address bits are contained within the opcode and the two Most Significant bits are contained in the STATUS register. RP0 and RP1 bits of the STATUS register are the two Most Significant data memory address bits and are also known as the bank select bits. Table 2-1 lists how to access the four banks of registers.

TABLE 2-1: BANK SELECTION

	RP1	RP0
Bank 0	0	0
Bank 1	0	1
Bank 2	1	0
Bank 3	1	1

2.2.1 GENERAL PURPOSE REGISTER FILE

The register file banks are organized as 128 x 8 in the PIC16F785/HV785. Each register is accessed, either directly, by seven address bits within the opcode, or indirectly, through the File Select Register (FSR). When the FSR is used to access data memory, the eight Least Significant data memory address bits are contained in the FSR and the ninth Most Significant address bit is contained in the IRP bit in the STATUS Register. (see **Section 2.4 "Indirect Addressing, INDF and FSR Registers"**).

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (see Table 2-2). These registers are static RAM.

The special registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the "core" are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

2.2.2.5 PIR1 Register

The Peripheral Interrupt Register 1 contains the interrupt flag bits.

Note:	Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE, in the INTCON Register). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-5: PIR1: PERIPHERAL INTERRUPT REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EEIF	ADIF	CCP1IF	C2IF	C1IF	OSFIF	TMR2IF	TMR1IF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EEIF:** EEPROM Write Operation Interrupt Flag bit
1 = The write operation completed (must be cleared in software)
0 = The write operation has not completed or has not been started

bit 6 **ADIF:** A/D Interrupt Flag bit
1 = A/D conversion complete
0 = A/D conversion has not completed or has not been started

bit 5 **CCP1IF:** CCP1 Interrupt Flag bit
Capture mode:
1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred
Compare mode:
1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred
PWM mode:
Unused in this mode

bit 4 **C2IF:** Comparator 2 Interrupt Flag bit
1 = Comparator 2 output has changed (must be cleared in software)
0 = Comparator 2 output has not changed

bit 3 **C1IF:** Comparator 1 Interrupt Flag bit
1 = Comparator 1 output has changed (must be cleared in software)
0 = Comparator 1 output has not changed

bit 2 **OSFIF:** Oscillator Fail Interrupt Flag bit
1 = System oscillator failed, clock input has changed to INTOSC (must be cleared in software)
0 = System clock operating

bit 1 **TMR2IF:** Timer2 to PR2 Match Interrupt Flag bit
1 = Timer2 to PR2 match occurred (must be cleared in software)
0 = Timer2 to PR2 match has not occurred

bit 0 **TMR1IF:** Timer1 Overflow Interrupt Flag bit
1 = Timer1 register overflowed (must be cleared in software)
0 = Timer1 has not overflowed

3.3.3 LP, XT, HS MODES

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to the OSC1 and OSC2 pins (Figure 3-1). The mode selects a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

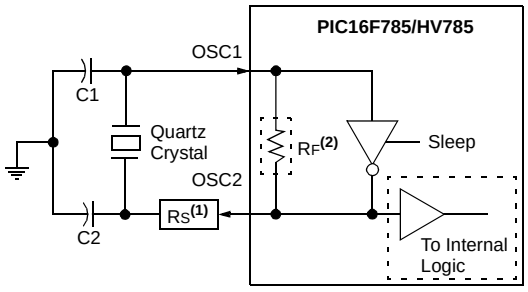
LP Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is best suited to drive resonators with a low drive level specification, for example, tuning fork type crystals.

XT Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive resonators with a medium drive level specification, for example, AT-cut quartz crystal resonators.

HS Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require a high drive setting, for example, AT-cut quartz crystal resonators or ceramic resonators.

Figure 3-3 and Figure 3-4 show typical circuits for quartz crystal and ceramic resonators, respectively.

FIGURE 3-3: QUARTZ CRYSTAL OPERATION (LP, XT OR HS MODE)

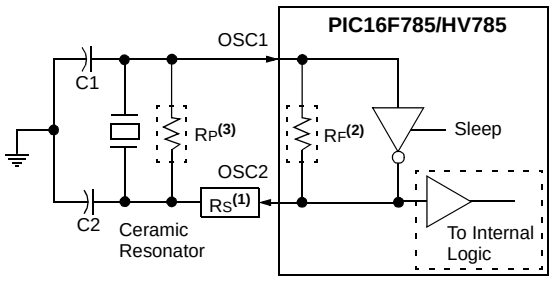


Note 1: A series resistor (R_S) may be required for quartz crystals with low drive level.

2: The value of R_F varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

Note 1:	Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.
2:	Always verify oscillator performance over the V_{DD} and temperature range that is expected for the application.

FIGURE 3-4: CERAMIC RESONATOR OPERATION (XT OR HS MODE)



Note 1: A series resistor (R_S) may be required for ceramic resonators with low drive level.

2: The value of R_F varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

3: An additional parallel feedback resistor (R_P) may be required for proper ceramic resonator operation (typical value 1 MΩ).

TABLE 3-2: CERAMIC RESONATORS

Mode	Freq.	OSC1 (C1)	OSC2 (C2)
XT	455 kHz	68-100 pF	68-100 pF
	2.0 MHz	15-68 pF	15-68 pF
HS	4.0 MHz	10-68 pF	10-68 pF
	8.0 MHz	15-68 pF	15-68 pF
	16.0 MHz	10-22 pF	10-22 pF

Note: These values are for design guidance only. See notes following this table.

4.2.2 INTERRUPT-ON-CHANGE

Each of the PORTA pins is individually configurable as an interrupt-on-change pin. Control bits IOCAx enable or disable the interrupt function for each pin. Refer to Register 4-4. The interrupt-on-change is disabled on a Power-on Reset.

For enabled interrupt-on-change pins, the values are compared with the old value latched on the last read of PORTA. The 'mismatch' outputs of the last read are OR'd together to set, the PORTA Change Interrupt flag bit (RAIF) in the INTCON register (Register 2-3).

This interrupt can wake the device from Sleep. The user, in the Interrupt Service Routine, clears the interrupt by:

a) Any read or write of PORTA. This will end the mismatch condition, then,

b) Clear the flag bit RAIF.

A mismatch condition will continue to set flag bit RAIF. Reading PORTA will end the mismatch condition and allow flag bit RAIF to be cleared. The latch holding the last read value is neither affected by an $\overline{MCLR}$ nor BOR Reset. After these resets, the RAIF flag will continue to be set if a mismatch is present.

Note:	If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the RAIF interrupt flag may not get set.

REGISTER 4-4: IOCA: INTERRUPT-ON-CHANGE PORTA REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	IOCA5(2)	IOCA4(2)	IOCA3	IOCA2	IOCA1	IOCA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **IOCA<5:0>:** Interrupt-on-change PORTA Control bits(2)

1 = Interrupt-on-change enabled
0 = Interrupt-on-change disabled

Note 1: Global interrupt enable (GIE) must be enabled for individual interrupts to be recognized.

2: IOCA<5:4> always reads '1' in XT, HS and LP OSC modes.

5.3 Using Timer0 with an External Clock

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI, with the internal phase clocks, is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks. Therefore, it is necessary for T0CKI to be high for at least 2TOSC (and a small RC delay of 20 ns) and low for at least 2TOSC (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

5.4 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer. For simplicity, this counter will be referred to as "prescaler" throughout this Data Sheet. The prescaler assignment is controlled in software by the control bit PSA of the OPTION Register. Clearing the PSA bit will assign the prescaler to Timer0. Prescale values are selectable via the PS<2:0> bits of the OPTION Register.

The prescaler is not readable or writable. When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., `CLRF 1, MOVWF 1, BSF 1,x....etc.`) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the Watchdog Timer.

5.4.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed "on the fly" during program execution). To avoid an unintended device Reset, the following instruction sequence (Example 5-1 and Example 5-2) must be executed when changing the prescaler assignment between Timer0 and WDT.

EXAMPLE 5-1: CHANGING PRESCALER (TIMER0→WDT)

```
BCF     STATUS,RP0      ;Bank 0
BCF     STATUS,RP1      ;
CLRWDT                  ;Clear WDT
CLRF    TMR0            ;Clear TMR0 and
                        ; prescaler
BSF     STATUS,RP0      ;Bank 1

MOVLW   b'00101111'     ;Required if desired
MOVWF   OPTION_REG      ; PS2:PS0 is
CLRWDT                  ; 000 or 001
                        ;
MOVLW   b'00101xxx'     ;Set postscaler to
MOVWF   OPTION_REG      ; desired WDT rate
BCF     STATUS,RP0      ;Bank 0
```

To change prescaler from the WDT to the TMR0 module, use the sequence shown in Example 5-2. This precaution must be taken even if the WDT is disabled.

EXAMPLE 5-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT                  ;Clear WDT and
                        ; prescaler
BSF     STATUS,RP0      ;Bank 1
BCF     STATUS,RP1      ;

MOVLW   b'xxxx0xxx'     ;Select TMR0,
                        ; prescale, and
                        ; clock source
MOVWF   OPTION_REG      ;
BCF     STATUS,RP0      ;Bank 0
```

TABLE 5-1: REGISTERS ASSOCIATED WITH TIMER0

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSEL0	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
OPTION_REG	$\overline{\text{RAPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
TMR0	Timer0 Module Register								xxxx xxxx	uuuu uuuu
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111

Legend: – = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Timer0 module.

9.1.2 COMPARATOR C2 CONTROL REGISTERS

The CM2CON0 register is a functional copy of the CM1CON0 register described in **Section 9.1.1 "Comparator C1 Control Register"**. A second control register, CM2CON1, is also present for control of an additional synchronizing feature, as well as mirrors of both comparator outputs.

9.1.2.1 Control Register CM2CON0

The CM2CON0 register, shown in Register 9-2, contains the control and Status bits for Comparator C2.

Setting C2ON of the CM2CON0 Register enables Comparator C2 for operation.

Bits C2CH<1:0> of the CM2CON0 Register select the comparator input from the four analog pins, AN<7:5,1>.

Note:	To use AN<7:5,1> as analog inputs, the appropriate bits must be programmed to 1 in the ANSEL0 register.

C2R of the CM2CON0 Register selects the reference to be used with the comparator. Setting C2R of the CM2CON0 Register selects the C2VREF output of the comparator voltage reference module as the reference voltage for the comparator. Clearing C2R selects the C2IN+ input on the RC0/AN4/C2IN+ pin.

The output of the comparator is available internally via the C2OUT bit of the CM2CON0 Register. To make the output available for an external connection, the C2OE bit of the CM2CON0 Register must be set.

The comparator output, C2OUT, can be inverted by setting the C2POL bit of the CM2CON0 Register. Clearing C2POL results in a non-inverted output.

A complete table showing the output state versus input conditions and the polarity bit is shown in Table 9-2.

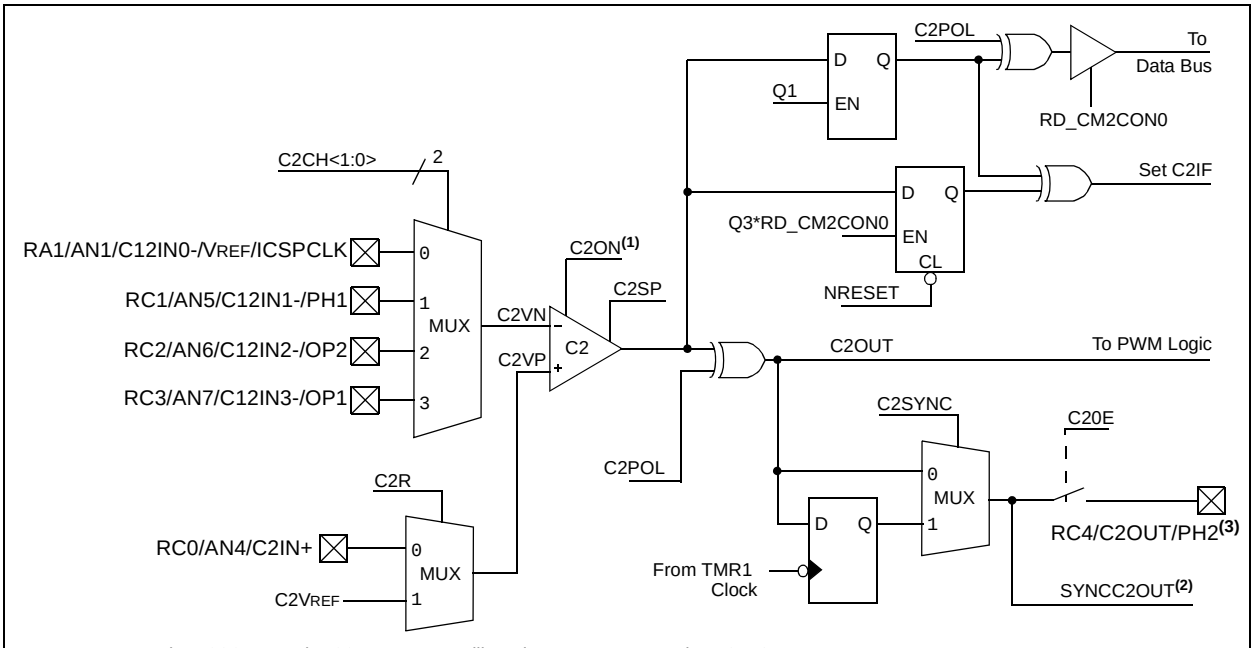
TABLE 9-2: C2 OUTPUT STATE VERSUS INPUT CONDITIONS

Input Condition	C2POL	C2OUT
C2VN > C2VP	0	0
C2VN < C2VP	0	1
C2VN > C2VP	1	1
C2VN < C2VP	1	0

Note 1:	The internal output of the comparator is latched at the end of each instruction cycle. External outputs are not latched.
2:	The C2 interrupt will operate correctly with C2OE set or cleared. An external output is not required for the C2 interrupt.
3:	For C2 output on RC4/C2OUT/PH2: (C2OE = 1) and (C2ON = 1) and (TRISA<4> = 0).

C2SP of the CM2CON0 Register configures the speed of the comparator. When C2SP is set, the comparator operates at its normal speed. Clearing C2SP operates the comparator in low-power mode.

FIGURE 9-2: COMPARATOR C2 SIMPLIFIED BLOCK DIAGRAM



Note 1: When C2ON = 0, the C2 comparator will produce a '0' output to the XOR Gate.
2: Timer1 gate control (see Figure 6-1).
3: Output shown for reference only. For more detail, see Figure 4-13.

10.2 VR Reference Module

The VR Reference module generates a 1.2V nominal output voltage for use by the ADC and comparators. The output voltage can also be brought out to the VREF pin for user applications. This module uses a bandgap as a reference. See Table 19-9 for detailed specifications. Register 10-2 shows the control register for the VR module.

REGISTER 10-2: REFCON: VOLTAGE REFERENCE CONTROL REGISTER

U-0	U-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
—	—	BGST	VRBB	VREN	VROE	CVROE	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **BGST:** Band Gap Reference Voltage Stable Flag bit
1 = Reference is stable
0 = Reference is not stable

bit 4 **VRBB:** Voltage Reference Buffer Bypass bit
1 = VREF output is not buffered. Power is removed from buffer amplifier.
0 = VREF output is buffered **(1)**

bit 3 **VREN:** Voltage Reference Enable bit (VR = 1.2V nominal) **(2)**
1 = VR reference is enabled
0 = VR reference is disabled and does not consume any current

bit 2 **VROE:** Voltage Reference Output Enable bit
If CVROE = 0:
1 = VREF output on RA1/AN1/C12IN0-/VREF/ICSPCLK pin is 1.2 volt VR analog reference
0 = Disabled, 1.2 volt VR analog reference is used internally only
If CVROE = 1:
VROE has no effect.

bit 1 **CVROE**: Comparator Voltage Reference Output Enable bit (see Figure 10-2)
1 = VREF output on RA1/AN1/C12IN0-/VREF/ICSPCLK pin is CVREF voltage
0 = VREF output on RA1/AN1/C12IN0-/VREF/ICSPCLK pin is controlled by VROE

bit 0 **Unimplemented:** Read as '0'

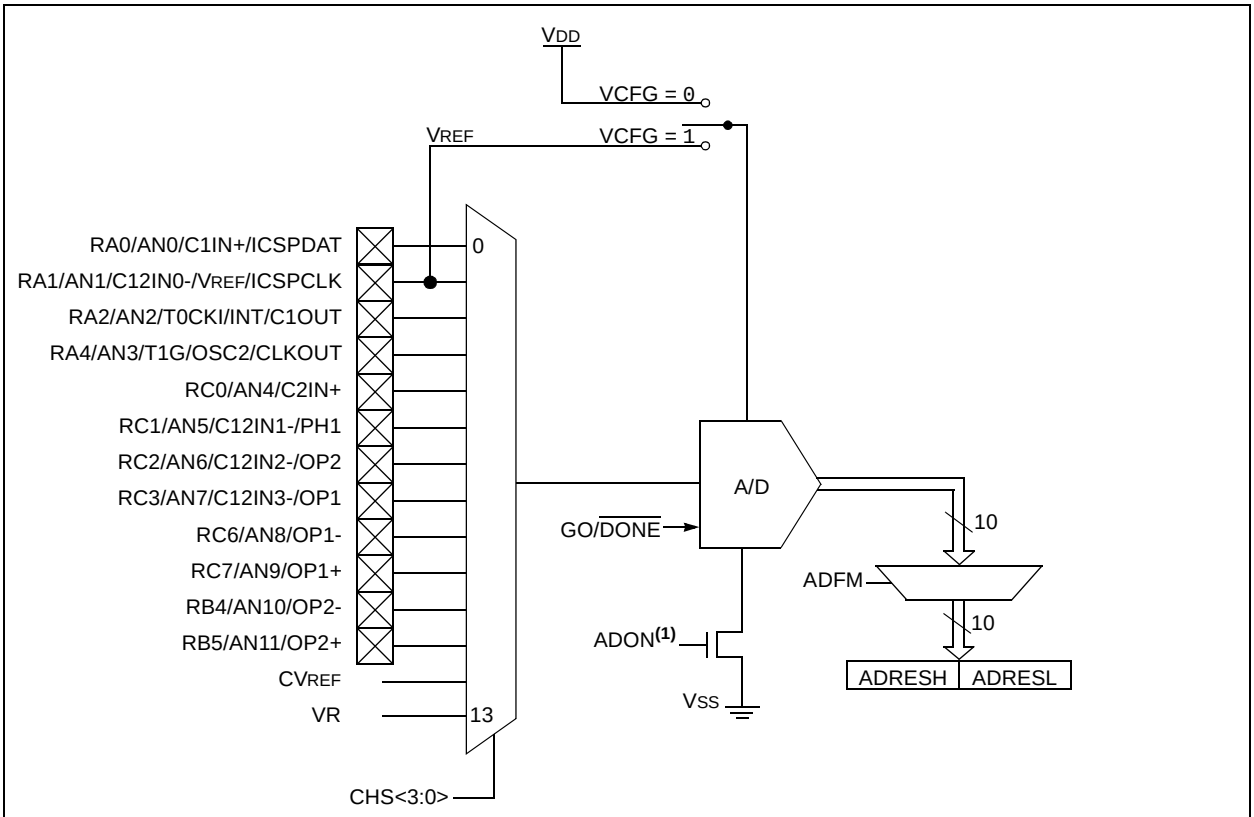
Note 1: Buffer amplifier common mode limitations require $V_{REF} \leq (V_{DD} - 1.4)V$ for buffered output.

2: VREN is fixed high for PIC16HV785 device.

12.0 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The analog-to-digital converter (A/D) allows conversion of an analog input signal to a 10-bit binary representation of that signal. The PIC16F785/HV785 has twelve analog I/O inputs, plus two internal inputs, multiplexed into one sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a binary result via successive approximation and stores the result in a 10-bit register. The voltage reference used in the conversion is software selectable to either VDD or a voltage applied by the VREF pin. Figure 12-1 shows the block diagram of the A/D on the PIC16F785/HV785.

FIGURE 12-1: A/D BLOCK DIAGRAM



Note 1: When ADON = 0 all input channels are disconnected from ADC (no loading).

12.1.5 STARTING A CONVERSION

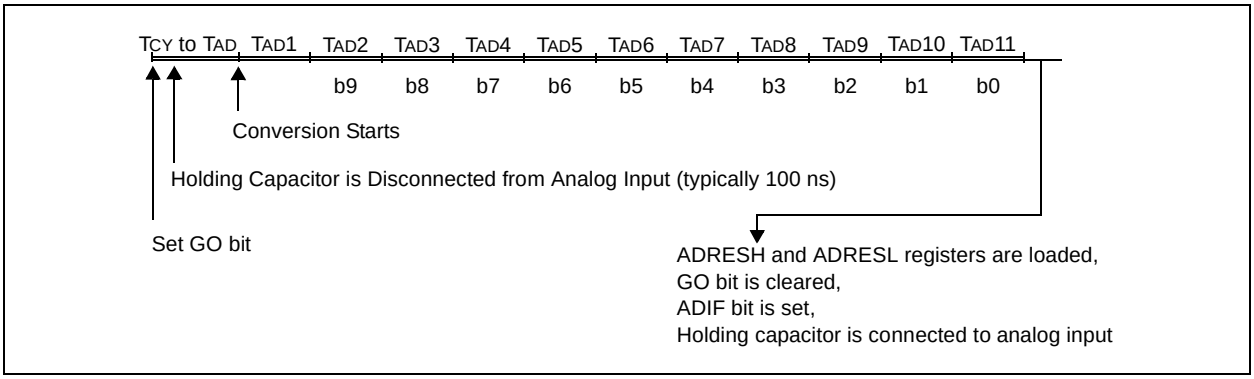
The A/D conversion is initiated by setting the GO/$\overline{\text{DONE}}$ bit (ADCON0<1>). When the conversion is complete, the A/D module:

- Clears the GO/$\overline{\text{DONE}}$ bit
- Sets the ADIF flag (PIR1<6>)
- Generates an interrupt (if enabled)

If the conversion must be aborted, the GO/$\overline{\text{DONE}}$ bit can be cleared in software. The ADRESH:ADRESL registers will not be updated with the partially complete A/D conversion sample. Instead, the ADRESH:ADRESL registers will retain the value of the previous conversion. After an aborted conversion, a 2 TAD delay is required before another acquisition can be initiated. Following the delay, an input acquisition is automatically started on the selected channel.

Note:	The GO/$\overline{\text{DONE}}$ bit should not be set in the same instruction that turns on the A/D.

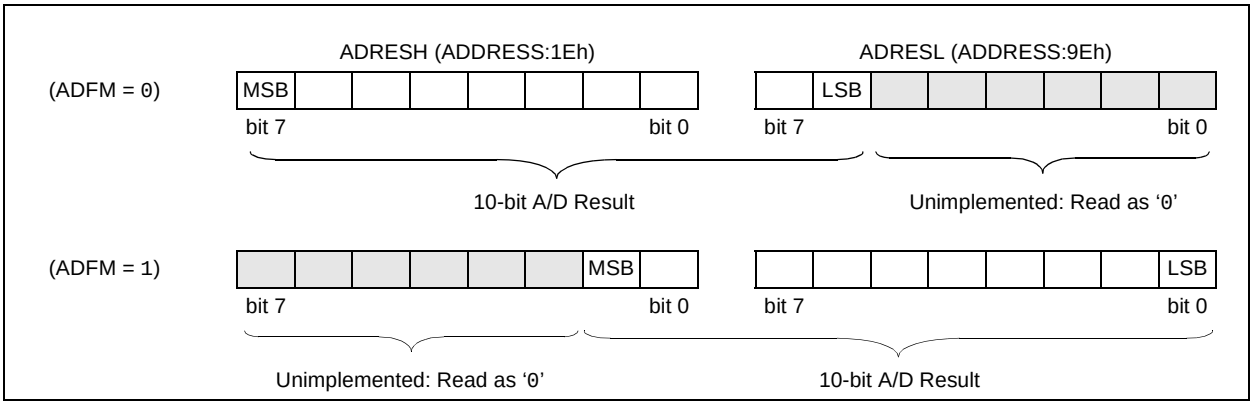
FIGURE 12-2: A/D CONVERSION TAD CYCLES



12.1.6 CONVERSION OUTPUT

The A/D conversion can be supplied in two formats: left or right justified. The ADFM bit of the ADCON0 register controls the output format. Figure 12-3 shows the output formats.

FIGURE 12-3: 10-BIT A/D RESULT FORMAT

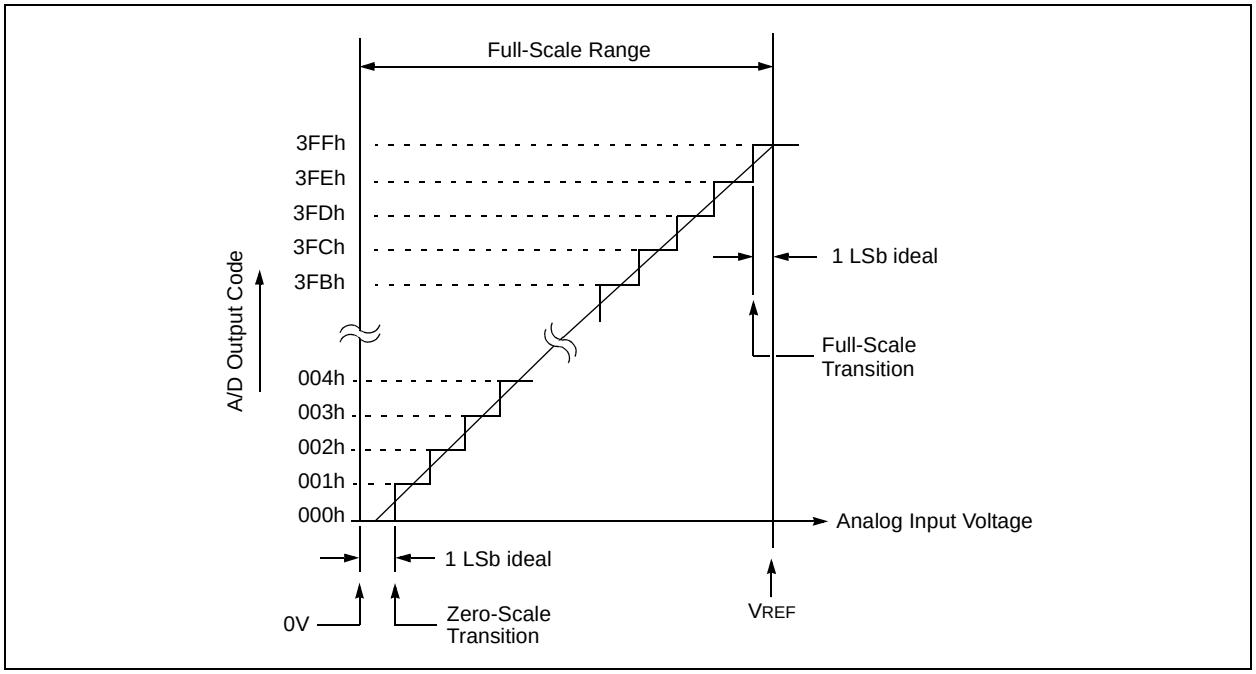


12.3 A/D Operation During Sleep

The A/D Converter module can operate during Sleep. This requires the A/D clock source to be set to the FRC option. When the RC clock source is selected, the A/D waits one instruction before starting the conversion. This allows the SLEEP instruction to be executed, thus eliminating much of the switching noise from the conversion. When the conversion is complete, the GO/DONE bit is cleared and the result is loaded into the ADRESH:ADRESL registers. If the A/D interrupt is enabled (ADIE and PEIE bits set), the device awakens from Sleep. If the GIE bit of the INTCON Register is set, the program counter is set to the interrupt vector (0004h). If GIE is clear, the next instruction is executed. If the A/D interrupt is not enabled, the A/D module is turned off, although the ADON bit remains set.

When the A/D clock source is something other than RC, a SLEEP instruction causes the present conversion to be aborted and the A/D module is turned off. The ADON bit remains set.

FIGURE 12-5: A/D TRANSFER FUNCTION



NOTES:

14.1 EECON1 and EECON2 Registers

EECON1 is the control register with four low-order bits physically implemented. The upper four bits are non-implemented and read as '0's.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set in software. They are cleared in hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental, premature termination of a write operation.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a $\overline{\text{MCLR}}$ Reset, or a WDT Time-out Reset during normal operation. In these situations, following Reset, the user can check the WRERR bit, clear it and rewrite the location. The EEDAT and EEADR registers are cleared by a Reset. Therefore, the EEDAT and EEADR registers will need to be re-initialized.

Interrupt flag EEIF bit of the PIR1 Register is set when write is complete. This bit must be cleared in software.

EECON2 is not a physical register. Reading EECON2 will read all '0's. The EECON2 register is used exclusively in the data EEPROM write sequence.

Note:	The EECON1, EEDAT and EEADR registers should not be modified during a data EEPROM write (WR bit = 1).

REGISTER 14-3: EECON1: EEPROM CONTROL REGISTER

U-0	U-0	U-0	U-0	R/W-x	R/W-0	R/S-0	R/S-0
—	—	—	—	WRERR	WREN	WR	RD
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **IUnimplemented:** Read as '0'

bit 3 **WRERR:** EEPROM Error Flag bit
- 1 = A write operation is prematurely terminated (any $\overline{\text{MCLR}}$ Reset, any WDT Reset during normal operation or BOR reset)
- 0 = The write operation completed

bit 2 **WREN:** EEPROM Write Enable bit
- 1 = Allows write cycles
- 0 = Inhibits write to the data EEPROM

bit 1 **WR:** Write Control bit
- 1 = Initiates a write cycle (The bit is cleared by hardware once write is complete. The WR bit can only be set, not cleared, in software.)
- 0 = Write cycle to the data EEPROM is complete

bit 0 **RD:** Read Control bit
- 1 = Initiates an EEPROM read (Read takes one cycle. RD is cleared in hardware. The RD bit can only be set, not cleared, in software.)
- 0 = Does not initiate an EEPROM read

15.0 SPECIAL FEATURES OF THE CPU

The PIC16F785/HV785 has a host of features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving features and offer code protection.

These features are:

- Reset:
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Brown-out Reset (BOR)
- Interrupts
- Watchdog Timer (WDT)
- Oscillator selection
- Sleep
- Code protection
- ID Locations
- In-Circuit Serial Programming™ (ICSP™)

The PIC16F785/HV785 has two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 64 ms (nominal) on power-up only, designed to keep the part in Reset while the power supply stabilizes. There is also circuitry to reset the device if a brown-out occurs, which can use the Power-up Timer to provide at least a 64 ms Reset. With these three functions on-chip, most applications need no external Reset circuitry.

The Sleep mode is designed to offer a very low-current Power-down mode. The user can wake-up from Sleep through an external Reset, Watchdog Timer Wake-up or interrupt.

Several oscillator options are also made available to allow the part to fit the application. The INTOSC option saves system cost, while the LP crystal option saves power. A set of configuration bits are used to select various options (see Register 15.2).

15.1 Configuration Bits

The configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1') to select various device configurations as shown in Register 15.2. These bits are mapped in program memory location 2007h.

Note:	Address 2007h is beyond the user program memory space. It belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming. See "*PIC16F785/HV785 Memory Programming Specification*" (DS41237) for more information.

FIGURE 15-4: TIME-OUT SEQUENCE ON POWER-UP (DELAYED $\overline{MCLR}$): CASE 1

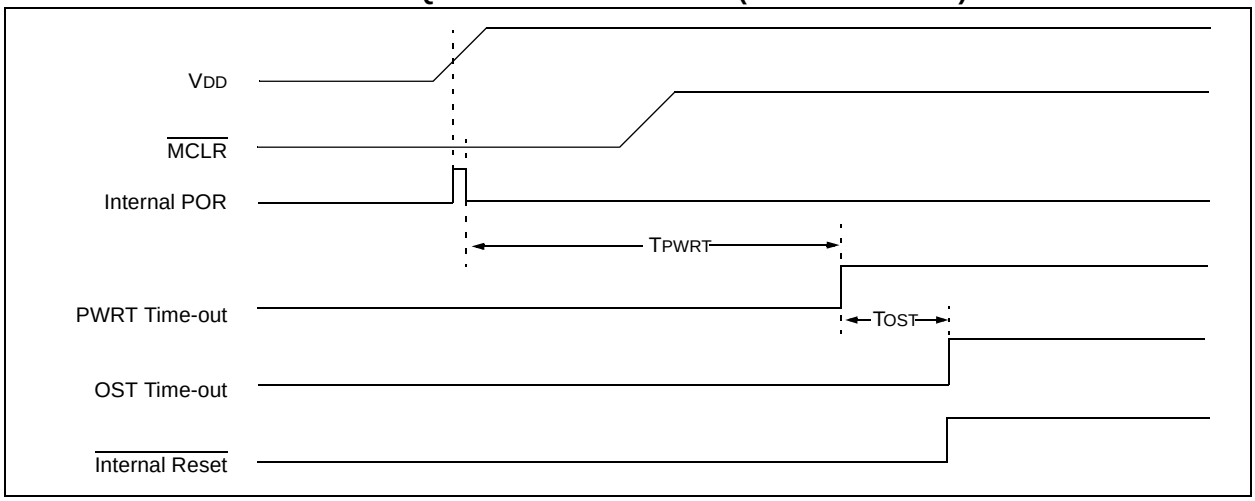


FIGURE 15-5: TIME-OUT SEQUENCE ON POWER-UP (DELAYED $\overline{MCLR}$): CASE 2

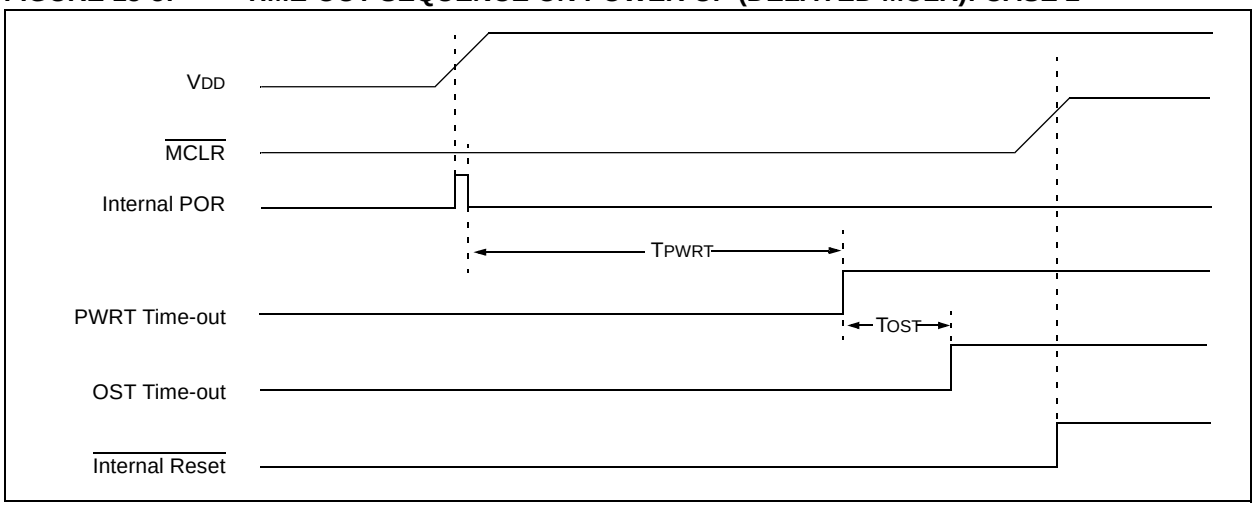
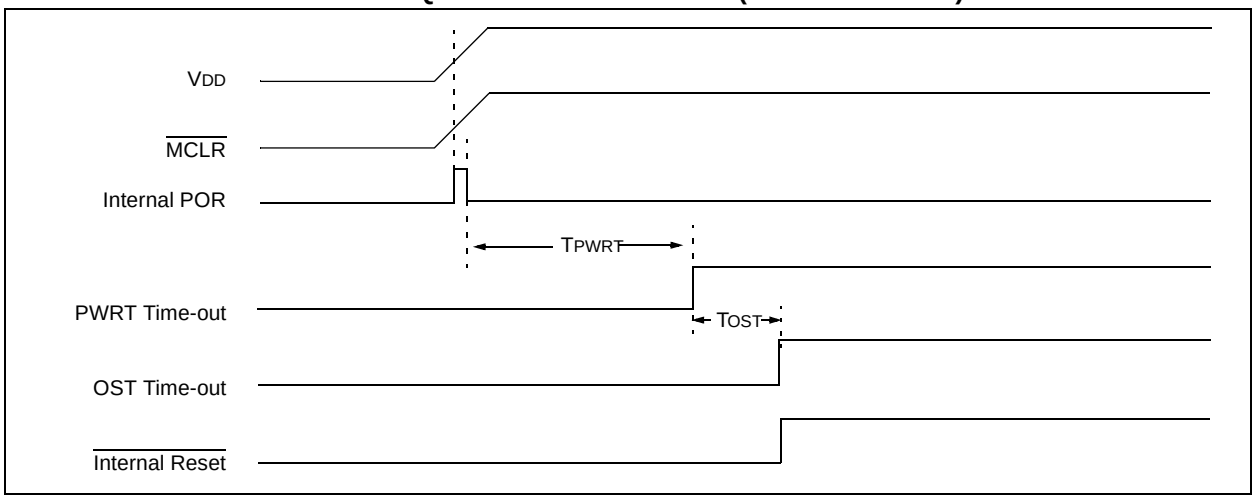


FIGURE 15-6: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ WITH VDD)



15.4 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt (e.g., W and STATUS registers). This must be implemented in software.

Since the last 16 bytes of all banks are common in the PIC16F785/HV785 (see Figure 2-2), temporary holding registers W_TEMP and STATUS_TEMP should be placed in here. These 16 locations do not require banking, therefore, making it easier to save and restore context. The same code shown in Example 15-1 can be used to:

- Store the W register
- Store the STATUS register
- Execute the ISR code
- Restore the Status (and Bank Select Bit register)
- Restore the W register

Note:	The PIC16F785/HV785 normally does not require saving the PCLATH. However, if computed GOTO's are used in the ISR and the main code, the PCLATH must be saved and restored in the ISR.

EXAMPLE 15-1: SAVING STATUS AND W REGISTERS IN RAM

```
MOVWF   W_TEMP              ;Copy W to TEMP register
SWAPF   STATUS,W            ;Swap status to be saved into W (swap does not affect status)
CLRF    STATUS              ;bank 0, regardless of current bank, Clears IRP,RP1,RP0
MOVWF   STATUS_TEMP         ;Save status to bank zero STATUS_TEMP register
:
:(ISR)                      ;Insert user code here
:
SWAPF   STATUS_TEMP,W       ;Swap STATUS_TEMP register into W
                            ;(sets bank to original state)
MOVWF   STATUS              ;Move W into Status register
SWAPF   W_TEMP,F            ;Swap W_TEMP
SWAPF   W_TEMP,W            ;Swap W_TEMP into W
```

FIGURE 20-6: MAXIMUM IDD vs. VDD OVER FOSC (XT MODE)

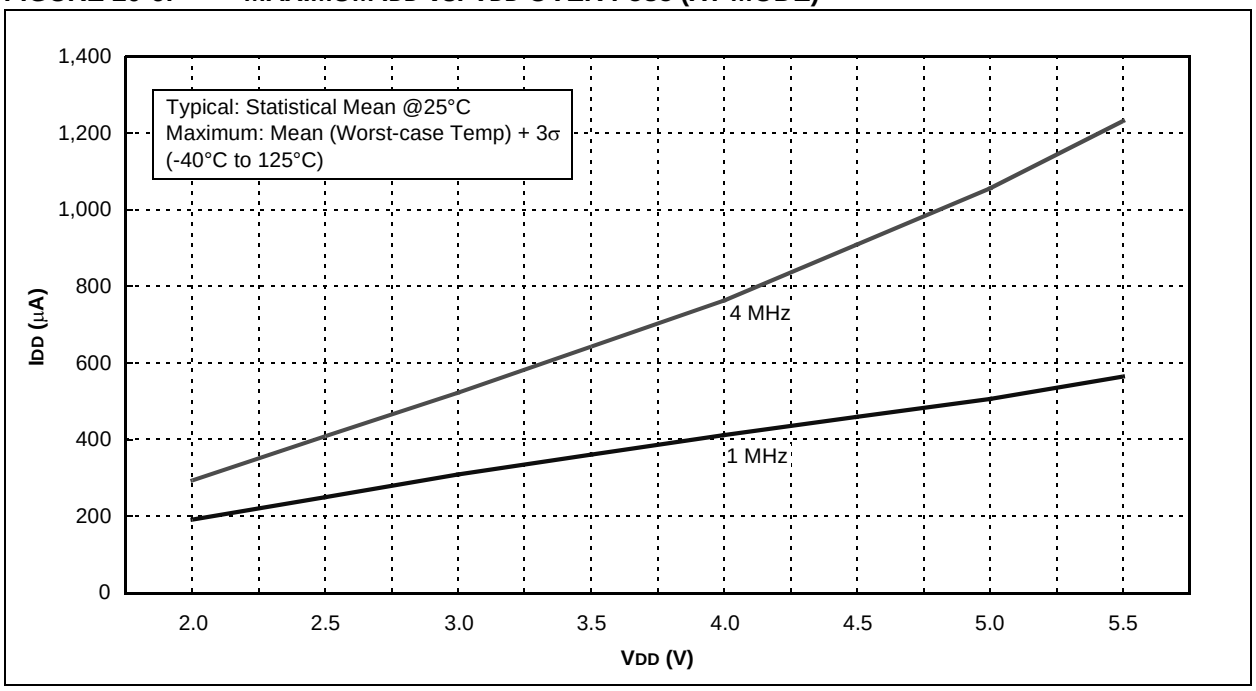


FIGURE 20-7: IDD vs. VDD (LP MODE)

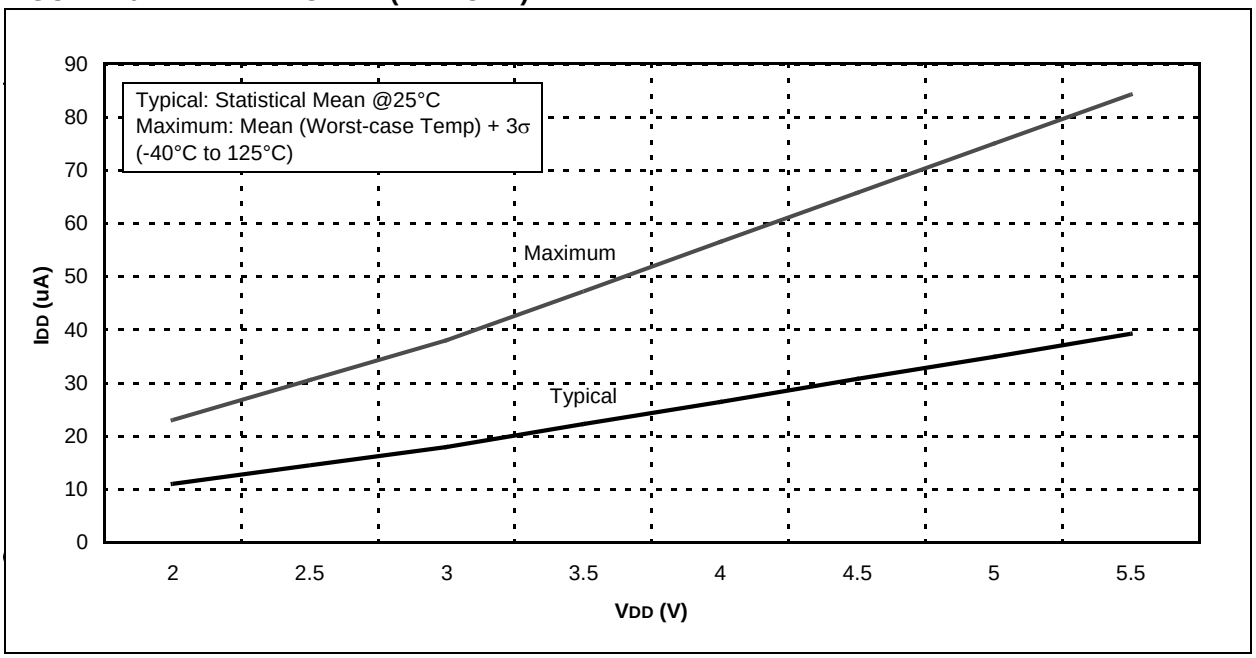


FIGURE 20-30: ADC CLOCK PERIOD vs. VDD OVER TEMPERATURE

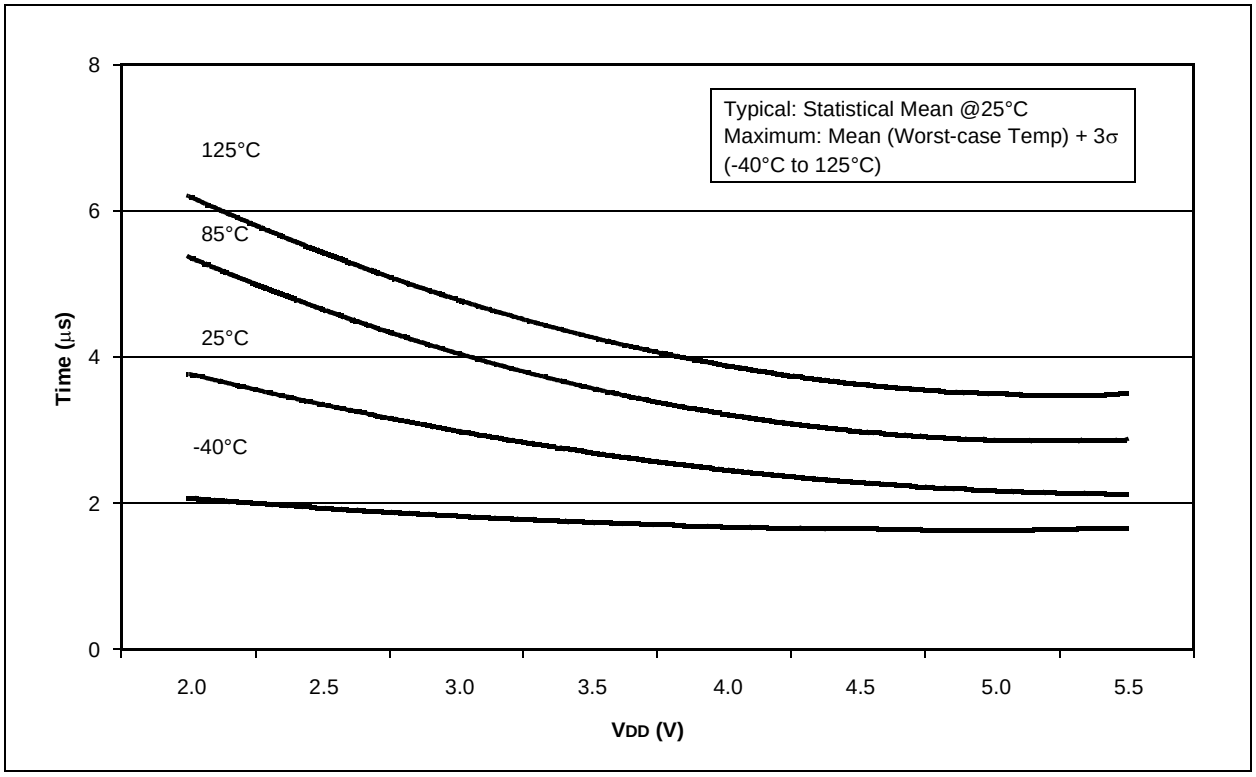
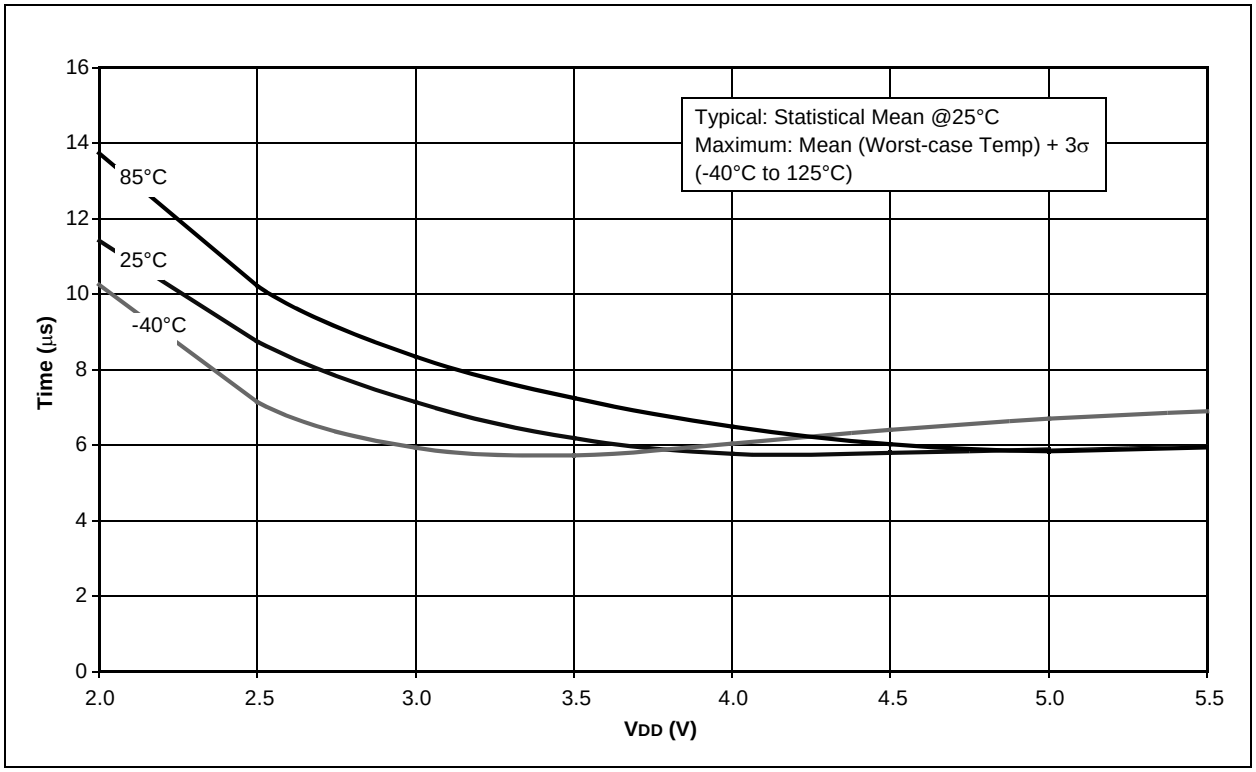
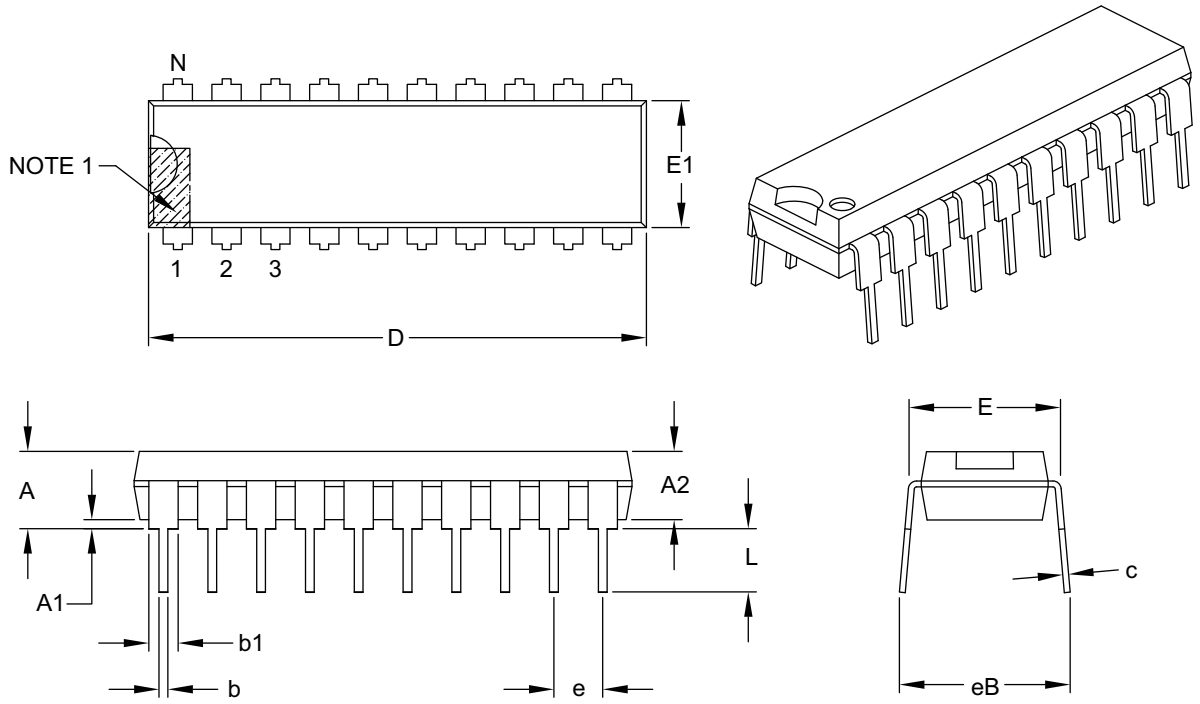


FIGURE 20-31: TYPICAL HFINTOSC START-UP TIMES vs. VDD OVER TEMPERATURE



20-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.300	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.980	1.030	1.060
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-019B