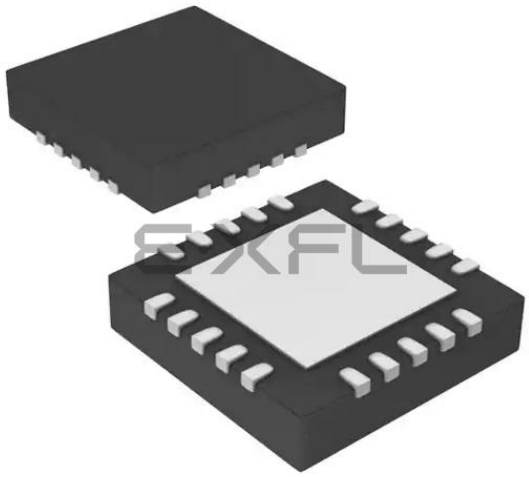

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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 14x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	20-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f785t-i-ml

QFN (4x4x0.9) Pin Diagram

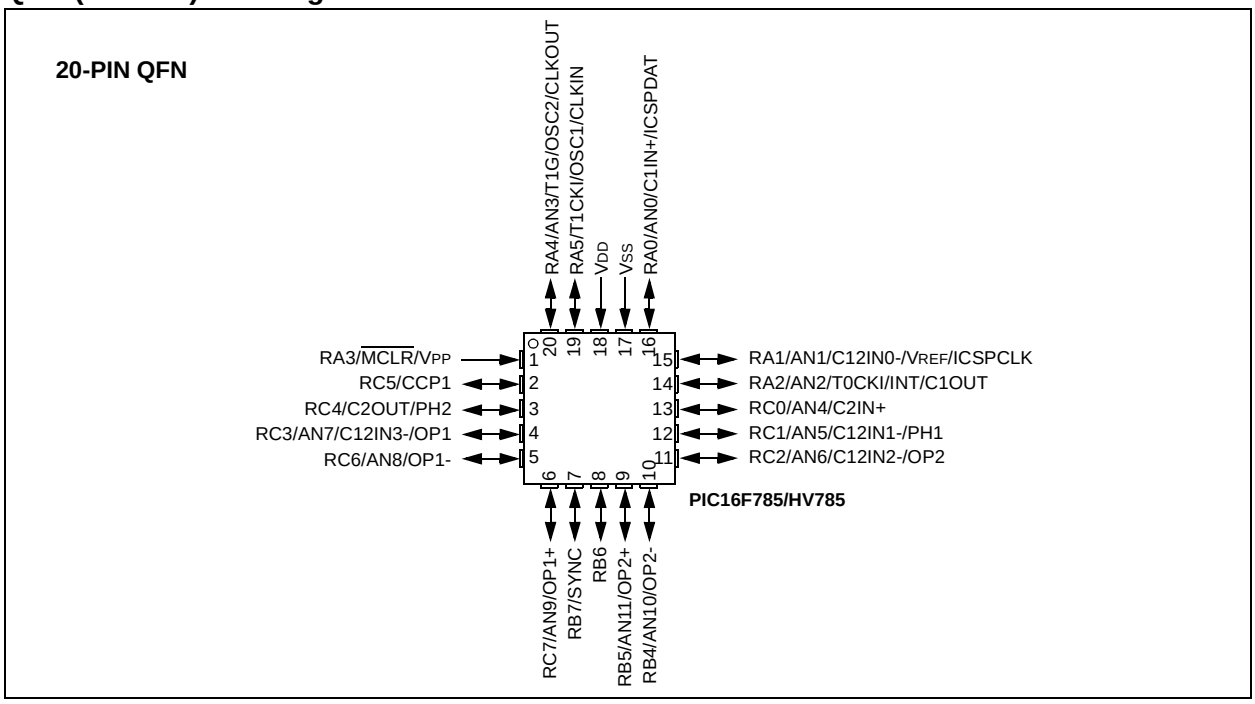

TABLE 2: QFN PIN SUMMARY

I/O	Pin	Analog	Comp.	Op Amps	PWM	Timers	CCP	Interrupt	Pull-ups	Basic
RA0	16	AN0	C1IN+	—	—	—	—	IOC	Y	ICSPDAT
RA1	15	AN1/VREF	C12IN0-	—	—	—	—	IOC	Y	ICSPCLK
RA2	14	AN2	C1OUT	—	—	T0CKI	—	INT/IOC	Y	—
RA3(1)	1	—	—	—	—	—	—	IOC	Y	$\overline{\text{MCLR}}$/VPP
RA4	20	AN3	—	—	—	T1G	—	IOC	Y	OSC2/CLKOUT
RA5	19	—	—	—	—	T1CKI	—	IOC	Y	OSC1/CLKIN
RB4	10	AN10	—	OP2-	—	—	—	—	—	—
RB5	9	AN11	—	OP2+	—	—	—	—	—	—
RB6(2)	8	—	—	—	—	—	—	—	—	—
RB7	7	—	—	—	SYNC	—	—	—	—	—
RC0	13	AN4	C2IN+	—	—	—	—	—	—	—
RC1	12	AN5	C12IN1-	—	PH1	—	—	—	—	—
RC2	11	AN6	C12IN2-	OP2	—	—	—	—	—	—
RC3	4	AN7	C12IN3-	OP1	—	—	—	—	—	—
RC4	3	—	C2OUT	—	PH2	—	—	—	—	—
RC5	2	—	—	—	—	—	CCP1	—	—	—
RC6	5	AN8	—	OP1-	—	—	—	—	—	—
RC7	6	AN9	—	OP1+	—	—	—	—	—	—
—	18	—	—	—	—	—	—	—	—	VDD
—	17	—	—	—	—	—	—	—	—	VSS

Note 1: Input only.

2: Open drain.

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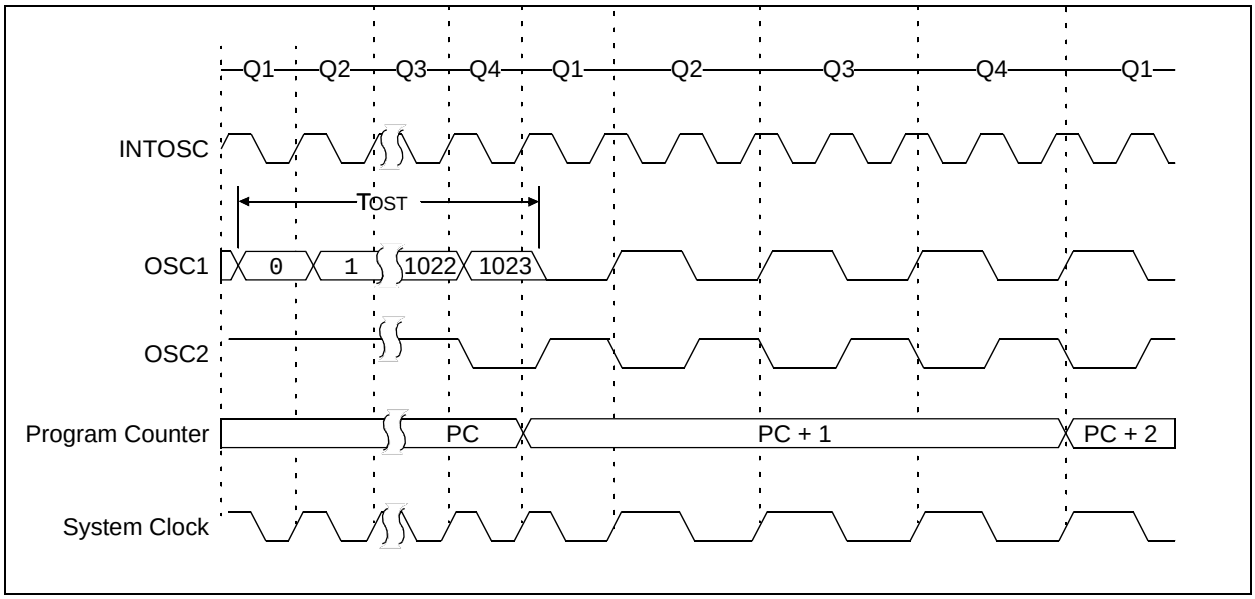
NOTES:

TABLE 2-4: PIC16F785/HV785 SPECIAL FUNCTION REGISTERS SUMMARY BANK 2

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Page
Bank 2											
100h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	22,114
101h	TMR0	Timer0 Module's Register								xxxx xxxx	49,114
102h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	21,114
103h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	15,114
104h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	22,114
105h	PORTA(1)	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--x0 x000	35,114
106h	PORTB(1)	RB7	RB6	RB5	RB4	—	—	—	—	xx00 ----	42,114
107h	PORTC(1)	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	00xx 0000	45,114
108h	—	Unimplemented								—	—
109h	—	Unimplemented								—	—
10Ah	PCLATH	—	—	—	Write Buffer for Upper 5 bits of Program Counter					---0 0000	21,114
10Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	17,114
10Ch	—	Unimplemented								—	—
10Dh	—	Unimplemented								—	—
10Eh	—	Unimplemented								—	—
10Fh	—	Unimplemented								—	—
110h	PWMCON1	—	COMOD1	COMOD0	CMDLY4	CMDLY3	CMDLY2	CMDLY1	CMDLY0	-000 0000	101,114
111h	PWMCON0	PRSEN	PASEN	BLANK2	BLANK1	SYNC1	SYNC0	PH2EN	PH1EN	0000 0000	93,114
112h	PWMCLK	PWMASE	PWMP1	PWMP0	PER4	PER3	PER2	PER1	PER0	0000 0000	94,114
113h	PWMPH1	POL	C2EN	C1EN	PH4	PH3	PH2	PH1	PH0	0000 0000	95,114
114h	PWMPH2	POL	C2EN	C1EN	PH4	PH3	PH2	PH1	PH0	0000 0000	96,114
115h	—	Unimplemented								—	—
116h	—	Unimplemented								—	—
117h	—	Unimplemented								—	—
118h	—	Unimplemented								—	—
119h	CM1CON0	C1ON	C1OUT	C1OE	C1POL	C1SP	C1R	C1CH1	C1CH0	0000 0000	65,114
11Ah	CM2CON0	C2ON	C2OUT	C2OE	C2POL	C2SP	C2R	C2CH1	C2CH0	0000 0000	67,114
11Bh	CM2CON1	MC1OUT	MC2OUT	—	—	—	—	T1GSS	C2SYNC	00-- --10	68,114
11Ch	OPA1CON	OPAON	—	—	—	—	—	—	—	0--- ----	76,114
11Dh	OPA2CON	OPAON	—	—	—	—	—	—	—	0--- ----	76,114
11Eh	—	Unimplemented								—	—
11Fh	—	Unimplemented								—	—

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented
Note 1: Port pins with analog functions controlled by the ANSEL0 and ANSEL1 registers will read '0' immediately after a Reset even though the data latches are either undefined (POR) or unchanged (other Resets).

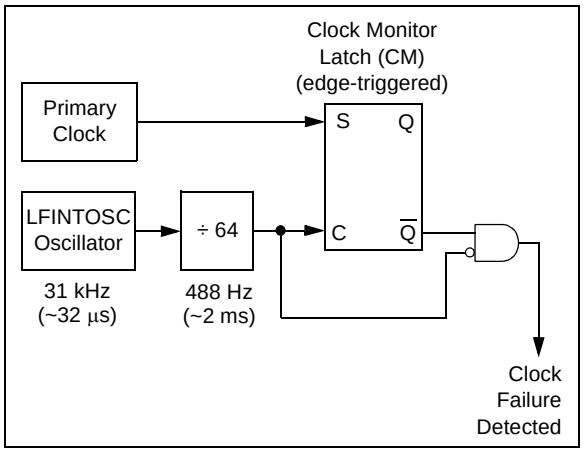
FIGURE 3-7: TWO-SPEED START-UP



3.7 Fail-Safe Clock Monitor

The Fail-Safe Clock Monitor (FSCM) is designed to allow the device to continue to operate in the event of an oscillator failure. The FSCM can detect oscillator failure at any point after the device has exited a Reset or Sleep condition and the Oscillator Start-up Timer (OST) has expired.

FIGURE 3-8: FSCM BLOCK DIAGRAM



The FSCM function is enabled by setting the FCMEN bit in Configuration Word (CONFIG). It is applicable to all external clock options (LP, XT, HS, EC, RC or I/O modes).

In the event of an external clock failure, the FSCM will set the OSFIF bit in the PIR1 Register and generate an oscillator fail interrupt if the OSFIE bit in the PIE1 Register is set. The device will then switch the system clock to the internal oscillator. The system clock will continue to come from the internal oscillator unless the external clock recovers and the Fail-Safe condition is exited.

The frequency of the internal oscillator will depend upon the value contained in the IRCF bits (OSCCON<6:4>). Upon entering the Fail-Safe condition, the OSTS bit in the OSCCON Register is automatically cleared to reflect that the internal oscillator is active and the WDT is cleared. The SCS bit in the OSCCON Register is not updated. Enabling FSCM does not affect the LTS bit.

The FSCM sample clock is generated by dividing the LFINTOSC clock by 64. This will allow enough time between FSCM sample clocks for a system clock edge to occur. Figure 3-8 shows the FSCM block diagram.

On the rising edge of the sample clock, the monitoring latch (CM = 0) will be cleared. On a falling edge of the primary system clock, the monitoring latch will be set (CM = 1). In the event that a falling edge of the sample clock occurs, and the monitoring latch is not set, a clock failure has been detected. The assigned internal oscillator is enabled when FSCM is enabled as reflected by the IRCF bits.

Note:	Two-Speed Start-up is automatically enabled when the Fail-Safe Clock Monitor mode is enabled.

REGISTER 3-2: OSCCON: OSCILLATOR CONTROL REGISTER

U-0	R/W-1	R/W-1	R/W-0	R-q	R-0	R-0	R/W-0
—	IRCF2	IRCF1	IRCF0	OSTS(1)	HTS	LTS	SCS
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **IRCF<2:0>:** Internal Oscillator Frequency Select bits

000 = 31 kHz
001 = 125 kHz
010 = 250 kHz
011 = 500 kHz
100 = 1 MHz
101 = 2 MHz
110 = 4 MHz
111 = 8 MHz

bit 3 **OSTS:** Oscillator Start-up Time-out Status bit(1)

1 = Device is running from the external system clock defined by FOSC<2:0>
0 = Device is running from the internal system clock (HFINTOSC or LFINTOSC)

bit 3 **PD:** Power-down bit

1 = After power-up or by the CLRWDT instruction
0 = By execution of the SLEEP instruction

bit 2 **HTS:** HFINTOSC (High Frequency – 8 MHz to 125 kHz) Status bit

1 = HFINTOSC is stable
0 = HFINTOSC is not stable

bit 1 **LTS:** LFINTOSC (Low Frequency – 31 kHz) Stable bit

1 = LFINTOSC is stable
0 = LFINTOSC is not stable

bit 0 **SCS:** System Clock Select bit

1 = Internal oscillator is used for system clock
0 = Clock source defined by FOSC<2:0>

Note 1: Bit resets to '0' with Two-Speed Start-up and LP, XT or HS selected as the Oscillator mode or Fail-Safe mode is enabled, otherwise this bit resets to '1'

TABLE 4-1: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSEL0	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111
CM1CON0	C1ON	C1OUT	C1OE	C1POL	C1SP	C1R	C1CH1	C1CH0	0000 0000	0000 0000
CM2CON1	MC1OUT	MC2OUT	—	—	—	—	T1GSS	C2SYNC	00-- --10	00-- --10
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
IOCA	—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0	--00 0000	--00 0000
OPTION_REG	$\overline{\text{RAPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--xx xxxx	--uu uuuu
REFCON	—	—	BGST	VRBB	VREN	VROE	CVROE	—	--00 000-	--00 000-
T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	0000 0000	0000 0000
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
WPUA	—	—	WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0	--11 1111	--11 1111

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

4.4.1.5 RC2/AN6/C12IN2-/OP2

The RC2 is configurable to function as one of the following:

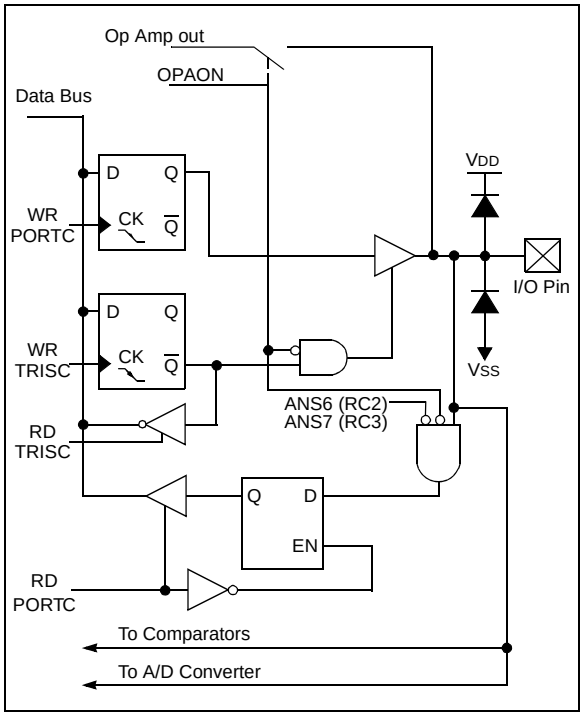
- General purpose I/O
- Analog input for the A/D Converter
- Analog input to Comparators 1 and 2
- Analog output from Op Amp 2

4.4.1.6 RC3/AN7/C12IN3-/OP1

The RC3 is configurable to function as one of the following:

- General purpose I/O
- Analog input for the A/D Converter
- Analog input to Comparators 1 and 2
- Analog output for Op Amp 1

FIGURE 4-12: BLOCK DIAGRAM OF RC2 AND RC3



4.4.1.7 RC4/C2OUT/PH2

The RC4 is configurable to function as one of the following:

- General purpose I/O
- Digital output from Comparator 2
- Digital output from the Two-Phase PWM

FIGURE 4-13: BLOCK DIAGRAM OF RC4

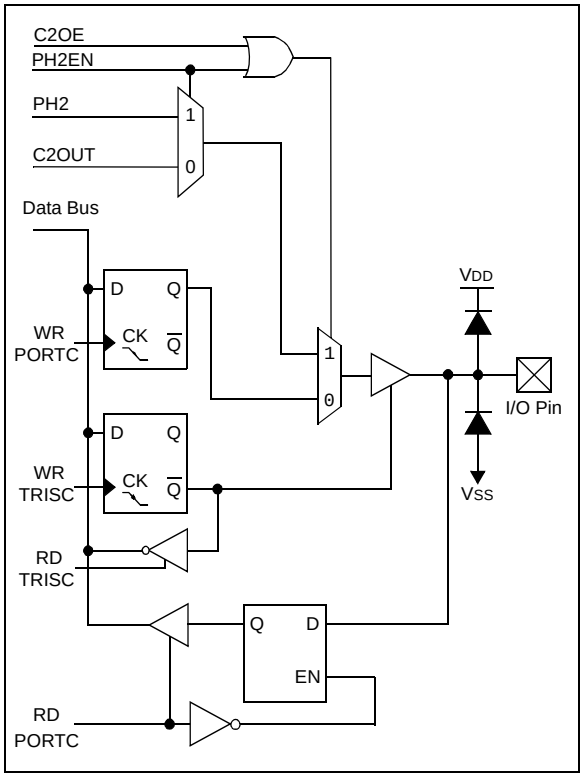
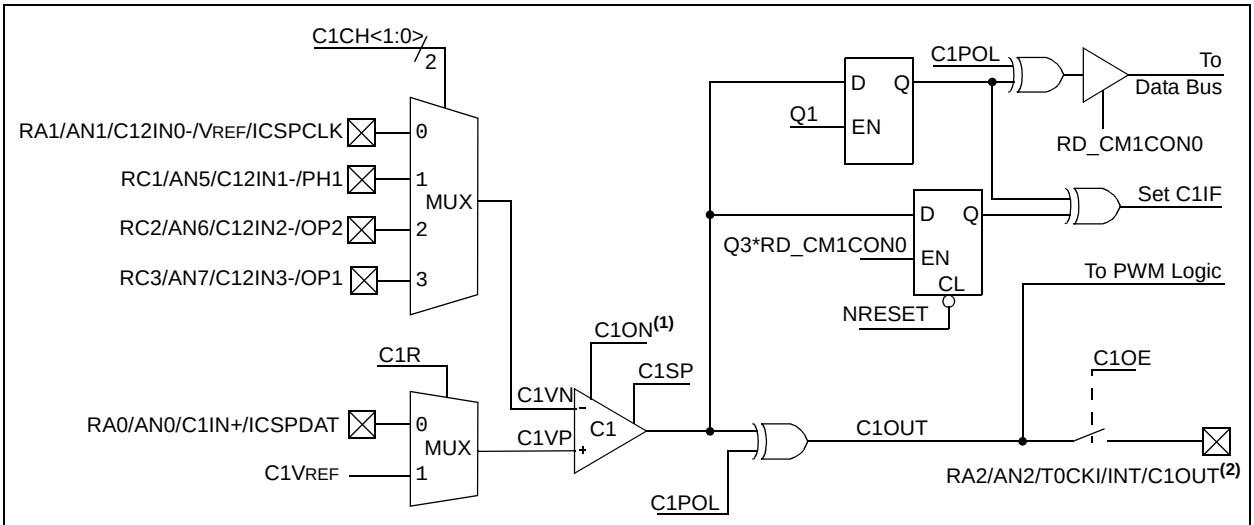


FIGURE 9-1: COMPARATOR C1 SIMPLIFIED BLOCK DIAGRAM



Note 1: When C1ON = 0, the C1 comparator will produce a '0' output to the XOR Gate.
2: Output shown for reference only. For more detail, see Figure 4-3.

REGISTER 9-2: CM2CON0: COMPARATOR C2 CONTROL REGISTER 0

R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
C2ON	C2OUT	C2OE	C2POL	C2SP	C2R	C2CH1	C2CH0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **C2ON:** Comparator C2 Enable bit
1 = C2 Comparator is enabled
0 = C2 Comparator is disabled

bit 6 **C2OUT:** Comparator C2 Output bit
If C2POL = 1 (inverted polarity):
C2OUT = 1, C2VP < C2VN
C2OUT = 0, C2VP > C2VN
If C2POL = 0 (non-inverted polarity):
C2OUT = 1, C2VP > C2VN
C2OUT = 0, C2VP < C2VN

bit 5 **C2OE:** Comparator C2 Output Enable bit
1 = C2OUT is present on RC4/C2OUT/PH2**(1)**
0 = C2OUT is internal only

bit 4 **C2POL:** Comparator C2 Output Polarity Select bit
1 = C2OUT logic is inverted
0 = C2OUT logic is not inverted

bit 3 **C2SP:** Comparator C2 Speed Select bit
1 = C2 operates in normal speed mode
0 = C2 operates in low power, slow speed mode.

bit 2 **C2R:** Comparator C2 Reference Select bits (non-inverting input)
1 = C2VP connects to $C2V_{REF}$
0 = C2VP connects to RC0/AN4/C2IN+

bit 1-0 **C2CH<1:0>:** Comparator C2 Channel Select bits
00 = C2VN of C2 connects to RA1/AN1/C12IN0-/V_{REF}/ICSPCLK
01 = C2VN of C2 connects to RC1/AN5/C12IN1-/PH1
10 = C2VN of C2 connects to RC2/AN6/C12IN2-/OP2
11 = C2VN of C2 connects to RC3/AN7/C12IN3-/OP1

Note 1: C2OUT will only drive RC4/C2OUT/PH2 if: (C2OE = 1) and (C2ON = 1) and (TRISC<4> = 0).

REGISTER 10-1: VRCON: VOLTAGE REFERENCE CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
C1VREN(1)	C2VREN(1)	VRR	—	VR3	VR2	VR1	VR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **C1VREN**: Comparator 1 Voltage Reference Enable bit(1)
1 = CVREF circuit powered on and routed to C1VREF input of comparator 1
0 = 1.2 Volt VR routed to C1VREF input of comparator 1

bit 6 **C2VREN**: Comparator 2 Voltage Reference Enable bit(1)
1 = CVREF circuit powered on and routed to C2VREF input of comparator 2
0 = 1.2 Volt VR routed to C2VREF input of comparator 2

bit 5 **VRR**: Comparator Voltage Reference CVREF Range Selection bit
1 = Low Range
0 = High Range

bit 4 **Unimplemented**: Read as '0'

bit 3-0 **VR<3:0>**: Comparator Voltage Reference CVREF Value Selection $0 \leq VR<3:0> \leq 15$
When VRR = 1 and CVREN = 1: $CV_{REF} = (VR<3:0> \times V_{DD}/24)$
When VRR = 0 and CVREN = 1: $CV_{REF} = (V_{DD}/4) + (VR<3:0> \times V_{DD}/32)$
When CxVREN = 0 and VREN = 1: CxVREF = 1.2V from VR module

Note 1: When C1VREN, C2VREN and CVROE (Register 10-2) are all low, the CVREF circuit is powered down and does not contribute to IDD current.

11.3 Effects of a Reset

A device Reset forces all registers to their Reset state. This disables both op amps.

11.4 OPA Module Performance

Common AC and DC performance specifications for the OPA module:

- Common Mode Voltage Range
- Leakage Current
- Input Offset Voltage
- Open Loop Gain
- Gain Bandwidth Product (GBWP)

Common mode voltage range is the specified voltage range for the OPA+ and OPA- inputs, for which the OPA module will perform to within its specifications. The OPA module is designed to operate with input voltages between 0 and V_{DD}-1.4V. Behavior for common mode voltages greater than V_{DD}-1.4V, or below 0V, are beyond the normal operating range.

Leakage current is a measure of the small source or sink currents on the OPA+ and OPA- inputs. To minimize the effect of leakage currents, the effective impedances connected to the OPA+ and OPA- inputs should be kept as small as possible and equal.

Input offset voltage is a measure of the voltage difference between the OPA+ and OPA- inputs in a closed loop circuit with the OPA in its linear region. The offset voltage will appear as a DC offset in the output equal to the input offset voltage, multiplied by the gain of the circuit. The input offset voltage is also affected by the common mode voltage.

Open loop gain is the ratio of the output voltage to the differential input voltage, (OPA+) - (OPA-). The gain is greatest at DC and falls off with frequency.

Gain Bandwidth Product or GBWP is the frequency at which the open loop gain falls off to 0 dB.

11.5 Effects of Sleep

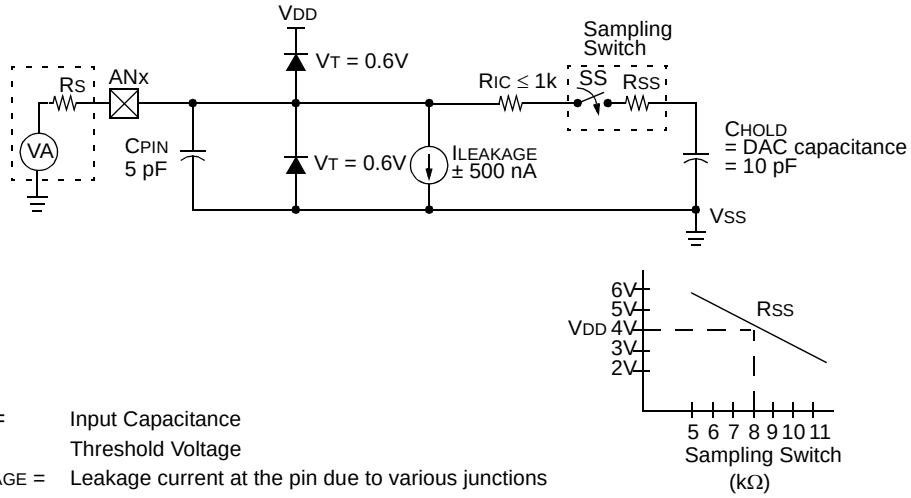
When enabled, the op amps continue to operate and consume current while the processor is in Sleep mode.

TABLE 11-1: REGISTERS ASSOCIATED WITH THE OPA MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSEL0	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111
ANSEL1	—	—	—	—	ANS11	ANS10	ANS9	ANS8	---- 1111	---- 1111
OPA1CON	OPAON	—	—	—	—	—	—	—	0--- ----	0--- ----
OPA2CON	OPAON	—	—	—	—	—	—	—	0--- ----	0--- ----
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	1111 ----	1111 ----
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for the OPA module.

FIGURE 12-4: ANALOG INPUT MODEL



Legend:

CPIN =	Input Capacitance
VT =	Threshold Voltage
I LEAKAGE =	Leakage current at the pin due to various junctions
RIC =	Interconnect Resistance
SS =	Sampling Switch
CHOLD =	Sample/Hold Capacitance (from DAC)

NOTES:

13.8 PWM Configuration

When configuring the Two-Phase PWM, care must be taken to avoid active output levels from the PH1 and PH2 pins before the PWM is fully configured. The following sequence is suggested before the TRISC register or any of the Two-Phase PWM control registers are first configured:

- Output inactive (OFF) levels to the PORTC RC1/AN5/C12IN1-/PH1 and RC4/C2OUT/PH2 pins.
- Clear TRISC bits 1 and 4 to configure the PH1 and PH2 pins as outputs.
- Configure the PWMCLK, PWMPH1, PWMPH2, and PWMCON1 registers.
- Configure the PWMCON0 register.

EXAMPLE 13-1: PWM SETUP EXAMPLE

```
;Example to configure PH1 as a free running PWM output using the SYNC output as the duty cycle
;termination feedback.
;This requires an external connection between the SYNC output and the comparator input.
;SYNC out = RB7 on pin 10
;C1 inverting input = RC2/AN6 on pin 14

;Configure PH1, PH2 and SYNC pins as outputs
;First, ensure output latches are low
    BCF     PORTC,1         ;PH1 low
    BCF     PORTC,4         ;PH2 low
    BCF     PORTB,7         ;SYNC low
;Configure the I/Os as outputs
    BANKSEL  TRISB
    BCF     TRISC,1         ;PH1 output
    BCF     TRISC,4         ;PH2 output
    BCF     TRISB,7         ;SYNC output
;PH1 shares its function with AN5
;Configure AN5 as digital I/O
    BCF     ANSEL0,5        ;AN5 is digital, all others default as analog
;Configure the PWM but don't enable PH1 or PH2 yet
    BANKSEL  PWMCLK
;PWM control setup
    MOVLW   B'00001100'     ;auto shutdown off, no blanking, SYNC on, PH1 and PH2 off
    MOVWF   PWMCON0         ;see data sheet page 93
;PWM clock setup
    MOVLW   B'00111101'     ;pwm_clk = Fosc, 30 clocks in PWM period
    MOVWF   PWMCLK          ;see data sheet page 94
;PH1 setup
    MOVLW   B'00101111'     ;non-inverted, terminate on C1, Start on clock 15
    MOVWF   PWMPH1          ;see data sheet page 95
;PH2 setup
    MOVLW   B'00110101'     ;non-inverted, terminate on C1, Start on clock 21
    MOVWF   PWMPH2          ;see data sheet page 96
;Configure Comparator 1
    MOVLW   B'10011110'     ;C1 on, internal, inverted, normal speed, +:C1VREF, -:AN6
    MOVWF   CM1CON0         ;see data sheet page 68
;Configure comparator voltage reference
    BANKSEL  VRCON
    MOVLW   B'10101100'     ;C1VREN on, low range, CVREF= VDD/2
    MOVWF   VRCON           ;see data sheet page 72
;Everything is setup at this point so now it is time to enable PH1
    BANKSEL  PWMCON0
    BSF     PWMCON0,PH1EN  ;enable PH1
;Module is running autonomously at this point
```

FIGURE 20-16: COMPARATOR IPD vs. VDD (BOTH COMPARATORS ENABLED) CXSP=1

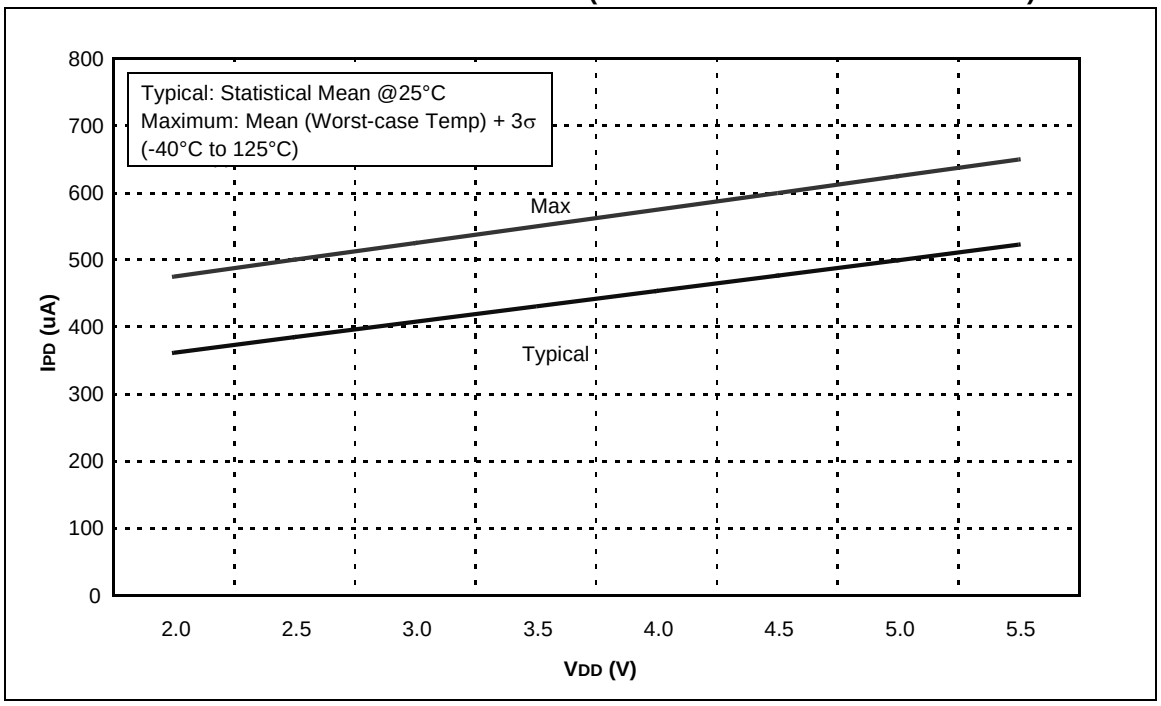


FIGURE 20-17: BOR IPD vs. VDD OVER TEMPERATURE

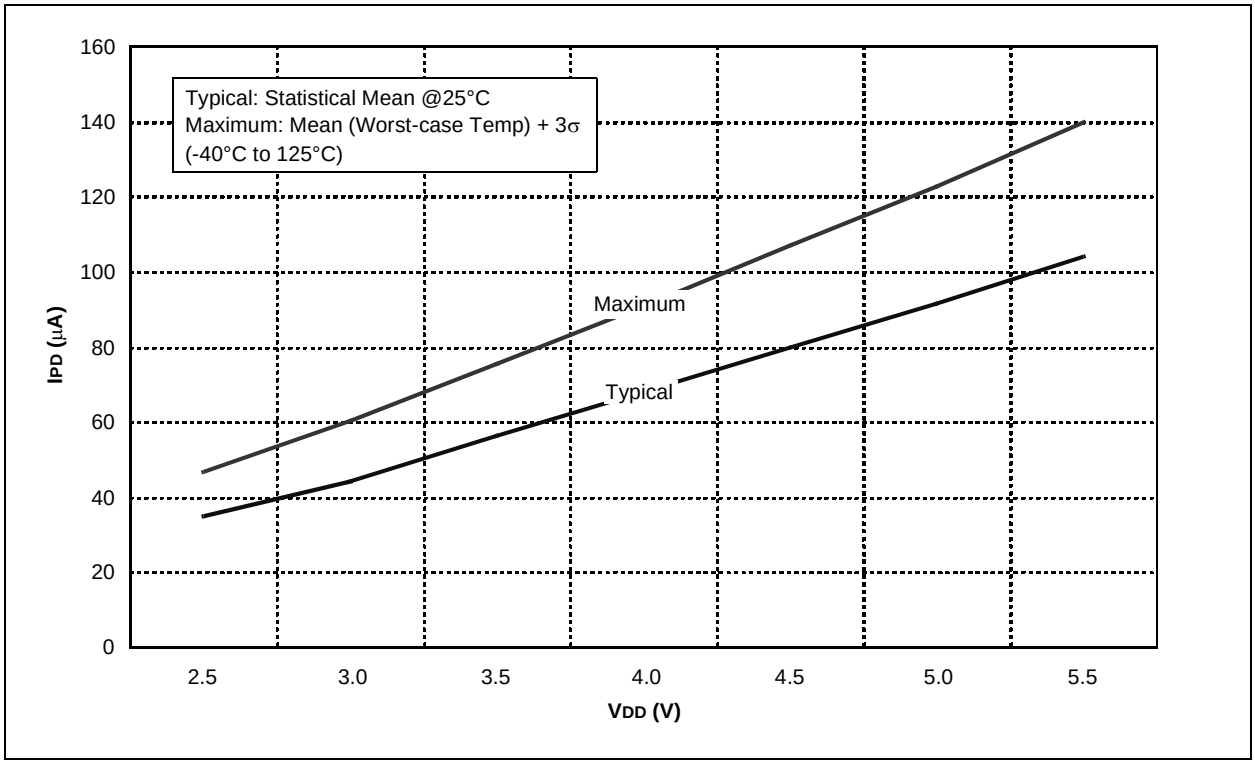


FIGURE 20-30: ADC CLOCK PERIOD vs. VDD OVER TEMPERATURE

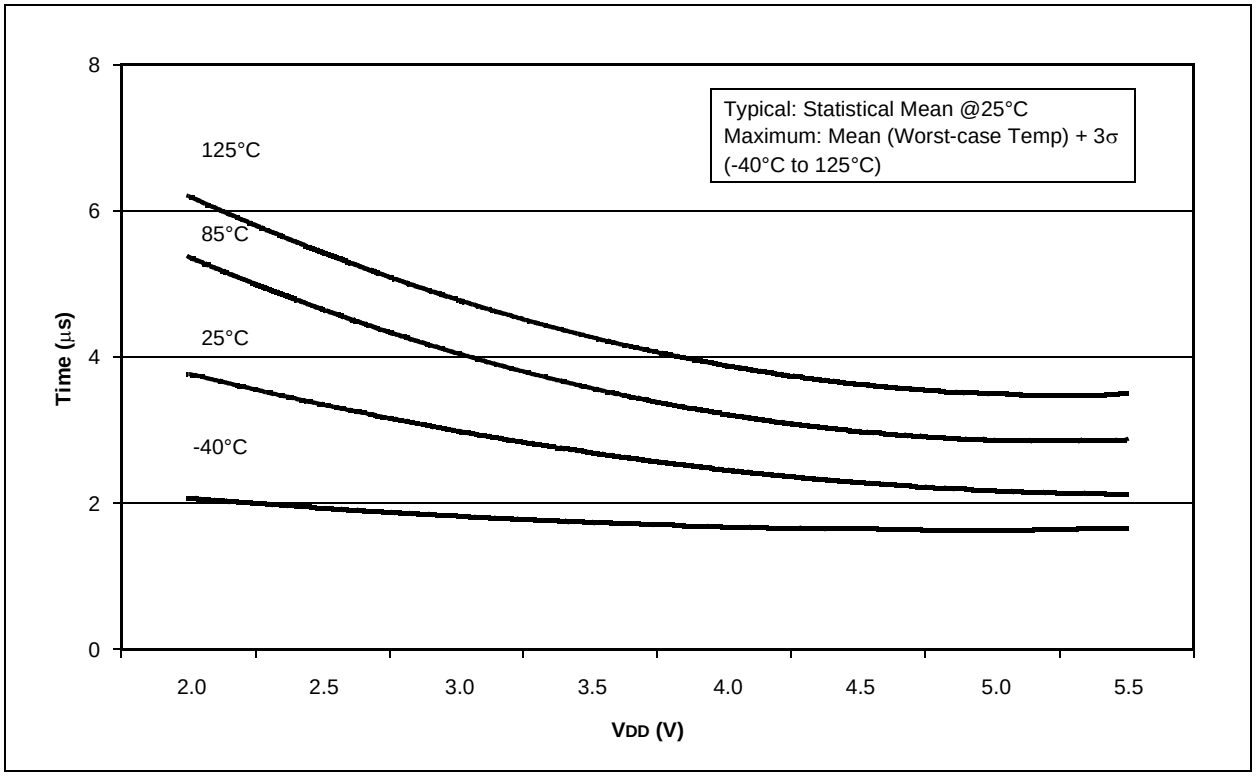
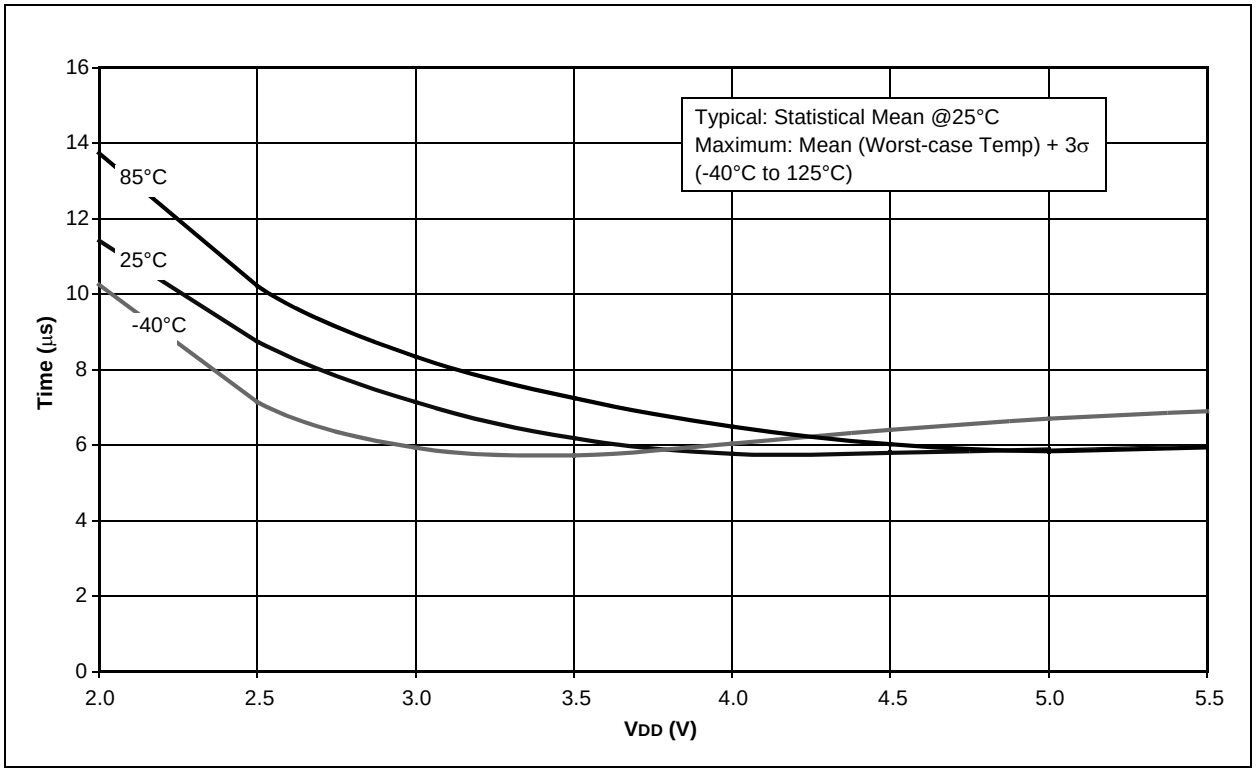
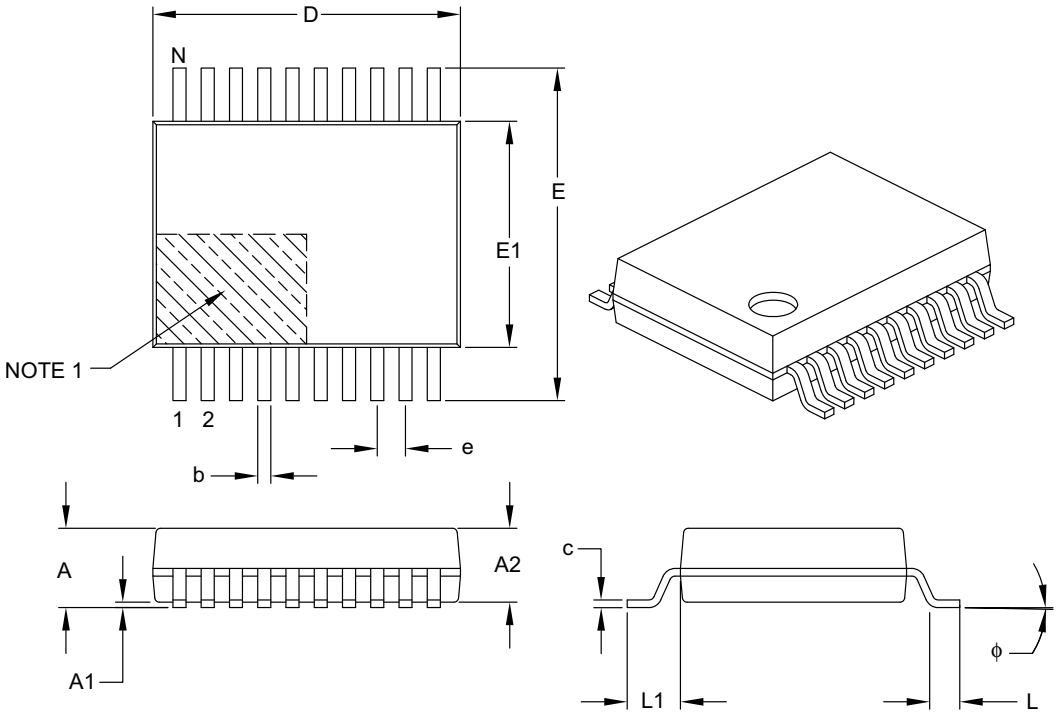


FIGURE 20-31: TYPICAL HFINTOSC START-UP TIMES vs. VDD OVER TEMPERATURE



20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	6.90	7.20	7.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B

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