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Core Processor	PIC
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Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 14x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
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2.2.2.6 PCON Register

The Power Control register contains flag bits to allow differentiation between a Power-on Reset ($\overline{POR}$), a Brown-out Reset ($\overline{BOR}$), a Watchdog Timer (WDT) Reset (WDT) and an external $\overline{MCLR}$ Reset.

REGISTER 2-6: PCON: POWER CONTROL REGISTER

U-0	U-0	U-0	R/W-1	U-0	U-0	R/W-0	R/W-x
	—	—	—	SBOREN(1)	—	—	$\overline{POR}$
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **SBOREN:** Software BOR Enable bit(1)
1 = BOR enabled
0 = BOR disabled

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **$\overline{POR}$:** Power-on Reset Status bit
1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{BOR}$:** Brown-out Reset Status bit
1 = No Brown-out Reset occurred
0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

Note 1: BOREN<1:0> = 01 in Configuration Word for this bit to control the $\overline{BOR}$.

3.4.2.2 OSCTUNE Register

The HFINTOSC is factory calibrated but can be adjusted in software by writing to the OSCTUNE register (Register 3-1).

The OSCTUNE register has a nominal tuning range of ±12%. The default value of the OSCTUNE register is '0'. The value is a 5-bit two's complement number. Due to process variation, the monotonicity and frequency step cannot be specified.

When the OSCTUNE register is modified, the HFINTOSC frequency will begin shifting to the new frequency. The HFINTOSC clock will stabilize within 1 ms. Code execution continues during this shift. There is no indication that the shift has occurred.

OSCTUNE does not affect the LFINTOSC frequency. Operation of features that depend on the LFINTOSC clock source frequency, such as the Power-up Timer (PWRT), Watchdog Timer (WDT), Fail-Safe Clock Monitor (FSCM) and peripherals, are *not* affected by the change in frequency.

REGISTER 3-1: OSCTUNE: OSCILLATOR TUNING REGISTER

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **TUN<4:0>:** Frequency Tuning bits

01111 = Maximum frequency
01110 =
•
•
•
00001 =
00000 = Center frequency. Oscillator module is running at the calibrated frequency.
11111 =
•
•
•
10000 = Minimum frequency

3.5 Clock Switching

The system clock source can be switched between external and internal clock sources via software using the System Clock Select (SCS) bit.

3.5.1 SYSTEM CLOCK SELECT (SCS) BIT

The System Clock Select (SCS) bit, in the OSCCON Register, selects the system clock source that is used for the CPU and peripherals.

- When SCS = 0, the system clock source is determined by configuration of the FOSC<2:0> bits in Configuration Word (CONFIG).
- When SCS = 1, the system clock source is chosen by the internal oscillator frequency selected by the IRCF bits. After a Reset, SCS is always cleared.

Note:	Any automatic clock switch, which may occur from Two-Speed Start-up or Fail-Safe Clock Monitor, does not update the SCS bit. The user can monitor the OSTS (OSCCON<3>) to determine the current system clock source.

3.5.2 OSCILLATOR START-UP TIME-OUT STATUS BIT

The Oscillator Start-up Time-out Status (OSTS) bit, (OSCCON<3>), indicates whether the system clock is running from the external clock source as defined by the FOSC bits, or from internal clock source. In particular, OSTS indicates that the Oscillator Start-up Timer (OST) has timed out for LP, XT or HS modes.

3.6 Two-Speed Clock Start-up Mode

Two-Speed Start-up mode provides additional power savings by minimizing the latency between external oscillator start-up and code execution. In applications that make heavy use of the Sleep mode, Two-Speed Start-up will remove the external oscillator start-up time from the time spent awake and can reduce the overall power consumption of the device.

This mode allows the application to wake-up from Sleep, perform a few instructions using the INTOSC as the clock source and go back to Sleep without waiting for the primary oscillator to become stable.

Note:	Executing a SLEEP instruction will abort the Oscillator Start-up Time and will cause the OSTS bit in the OSCCON Register to remain clear.

When the PIC16F785/HV785 is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) is enabled (see **Section 3.3.1 "Oscillator Start-up Timer (OST)"**). The OST timer will suspend program execution until 1024 oscillations are counted. Two-Speed Start-up mode minimizes the delay in code execution by operating from the internal oscillator as the OST is counting. When the OST count reaches 1024 and the OSTS bit in the OSCCON Register is set, program execution switches to the external oscillator.

3.6.1 TWO-SPEED START-UP MODE CONFIGURATION

Two-Speed Start-up mode is configured by the following settings:

- IESO = 1 (CONFIG<10>) Internal/External Switch Over bit.
- SCS = 0.
- FOSC configured for LP, XT or HS mode.

Two-Speed Start-up mode is entered after:

- Power-on Reset (POR) and, if enabled, after PWRT has expired, or
- Wake-up from Sleep.

If the external clock oscillator is configured to be anything other than LP, XT or HS mode, then Two-Speed Start-up is disabled. This is because the external clock oscillator does not require any stabilization time after POR or an exit from Sleep.

3.6.2 TWO-SPEED START-UP SEQUENCE

1. Wake-up from Power-on Reset or Sleep.
2. Instructions begin execution by the internal oscillator at the frequency set in the IRCF bits (in the OSCCON Register.
3. OST enabled to count 1024 clock cycles.
4. OST timed out, wait for falling edge of the internal oscillator.
5. OSTS is set.
6. System clock held low until the next falling edge of new clock (LP, XT or HS mode).
7. System clock is switched to external clock source.

3.6.3 CHECKING EXTERNAL/INTERNAL CLOCK STATUS

Checking the state of the OSTS bit in the OSCCON Register) will confirm if the PIC16F785/HV785 is running from the external clock source as defined by the FOSC bits in the Configuration Word (CONFIG) or the internal oscillator.

REGISTER 4-2: TRISA: PORTA TRI-STATE REGISTER

U-0	U-0	R/W-1	R/W-1	R-1	R/W-1	R/W-1	R/W-1
—	—	TRISA5(2)	TRISA4(2)	TRISA3(1)	TRISA2	TRISA1	TRISA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **TRISA<5:0>:** PORTA Tri-State Control bit(1), (2)
1 = PORTA pin configured as an input (tri-stated)
0 = PORTA pin configured as an output

bit 0 **C:** Carry/$\overline{\text{Borrow}}$ bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)(1)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: TRISA<3> always reads '1'.

2: TRISA<5:4> always reads '1' in XT, HS and LP OSC modes.

4.2 Additional Pin Functions

Every PORTA pin on the PIC16F785/HV785 has an interrupt-on-change option and a weak pull-up option. The next three sections describe these functions.

4.2.1 WEAK PULL-UPS

Each of the PORTA pins has an individually configurable internal weak pull-up. Control bits WPUAx enable or disable each pull-up. Refer to Register 4-3. Each weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset by the $\overline{\text{RAPU}}$ bit in the (OPTION Register. The weak pull-up on RA3 is automatically enabled when RA3 is configured as $\overline{\text{MCLR}}$.

REGISTER 4-3: WPUA: WEAK PULL-UP REGISTER

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	WPUA5(4)	WPUA4(4)	WPUA3(3)	WPUA2	WPUA1	WPUA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **WPUA<5:0>:** Weak Pull-up Register bits
1 = Pull-up enabled
0 = Pull-up disabled

Note 1: Global $\overline{\text{RAPU}}$ must be enabled for individual pull-ups to be enabled.

2: The weak pull-up device is automatically disabled if the pin is in Output mode (TRISA = 0).

3: The RA3 pull-up is automatically enabled when configured as $\overline{\text{MCLR}}$ in the Configuration Word.

4: WPUA<5:4> always reads '1' in XT, HS and LP OSC modes.

4.4.1.8 RC5/CCP1

The RC5 is configurable to function as one of the following:

- General purpose I/O
- Digital input for the capture/compare
- Digital output for the CCP

FIGURE 4-14: BLOCK DIAGRAM OF RC5

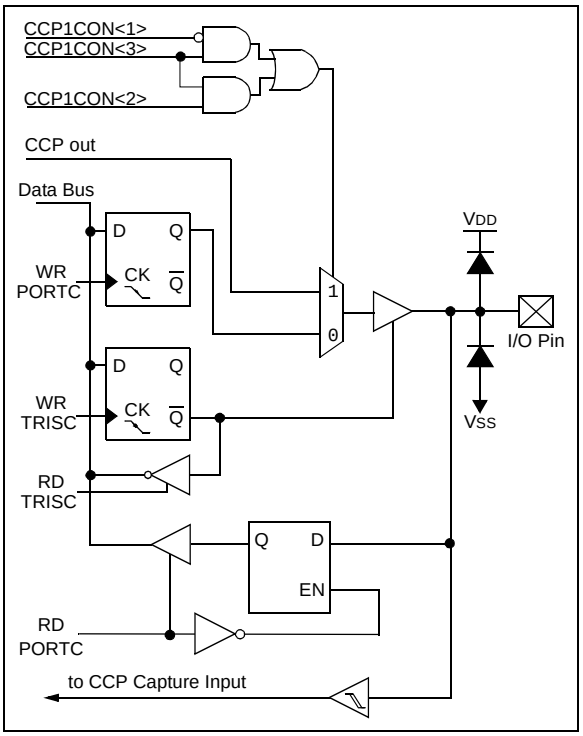


TABLE 4-3: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSEL1	—	—	—	—	ANS11	ANS10	ANS9	ANS8	---- 1111	---- 1111
CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	0000 0000	0000 0000
OPA1CON	OPAON	—	—	—	—	—	—	—	0--- ----	0--- ----
OPA2CON	OPAON	—	—	—	—	—	—	—	0--- ----	0--- ----
PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu
PWMCON0	PRSEN	PASEN	BLANK2	BLANK1	SYNC1	SYNC0	PH2EN	PH1EN	0000 0000	0000 0000
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by PORTC.

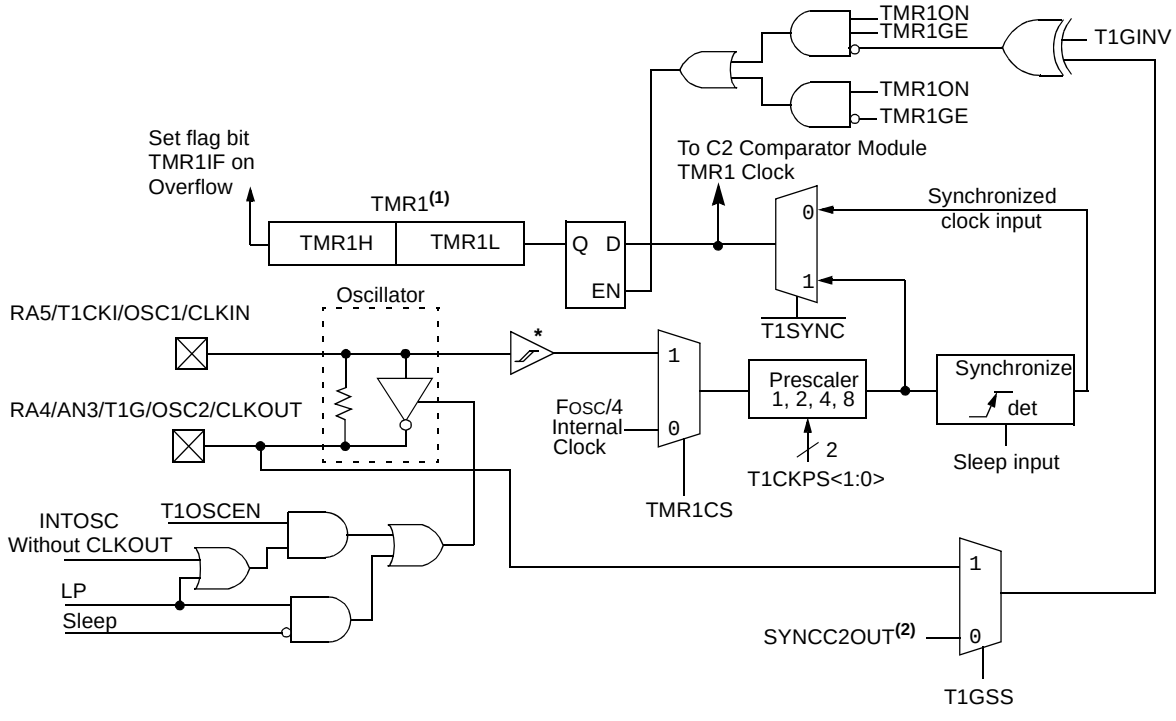
6.0 TIMER1 MODULE WITH GATE CONTROL

The Timer1 module is the 16-bit counter of the PIC16F785/HV785. Figure 6-1 shows the basic block diagram of the Timer1 module. Timer1 has the following features:

- 16-bit timer/counter (TMR1H:TMR1L)
- Readable and writable
- Internal or external clock selection
- Synchronous or asynchronous operation
- Interrupt on overflow from FFFFh to 0000h
- Wake-up upon overflow (Asynchronous mode)
- Optional external enable input:
  - Selectable gate source; T1G or C2 output (T1GSS)
  - Selectable gate polarity (T1GINV)
- Optional LP oscillator

The Timer1 Control register (T1CON), shown in Register 6-1, is used to enable/disable Timer1 and select the various features of the Timer1 module.

FIGURE 6-1: TIMER1 ON THE PIC16F785/HV785 BLOCK DIAGRAM



* ST Buffer is low power type when using LP OSC, or high-speed type when using T1CKI.

Note 1: Timer1 increments on the rising edge.

2: SYNCC2OUT is the synchronized output from Comparator 2 (See Figure 9-2 on 66).

6.1 Timer1 Modes of Operation

Timer1 can operate in one of three modes:

- 16-bit Timer with prescaler
- 16-bit Synchronous counter
- 16-bit Asynchronous counter

In Timer mode, Timer1 is incremented on every instruction cycle. In Counter mode, Timer1 is incremented on the rising edge of the external clock input T1CKI. In addition, the Counter mode clock can be synchronized to the microcontroller system clock or run asynchronously.

In Counter and Timer modules, the counter/timer clock can be gated by the Timer1 gate, which can be selected as either the T1G pin or Comparator 2 output.

If an external clock oscillator is needed (and the microcontroller is using the LP oscillator or INTOSC without CLKOUT), Timer1 can use the LP oscillator as a clock source.

Note:	In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge after any one or more of the following conditions. • Timer1 enabled after POR Reset • Write to TMR1H or TMR1L • Timer1 is disabled (TMR1ON = 0) when T1CKI is high then Timer1 is enabled (TMR1ON = 1) when T1CKI is low. See Figure 6-2.

6.2 Timer1 Interrupt

The Timer1 register pair (TMR1H:TMR1L) increments to FFFFh and rolls over to 0000h. When Timer1 rolls over, the Timer1 interrupt flag bit of the PIR1 Register is set. To enable the interrupt on rollover, you must set these bits:

- Timer1 Interrupt Enable bit of the PIE1 Register
- PEIE bit of the INTCON Register
- GIE bit of the INTCON Register

The interrupt is cleared by clearing the TMR1IF in the Interrupt Service Routine.

Note:	The TMR1H:TMR1L register pair and the TMR1IF bit should be cleared before enabling interrupts.

6.3 Timer1 Prescaler

Timer1 has four prescaler options allowing 1, 2, 4 or 8 divisions of the clock input. The T1CKPS bits, of the T1CON Register, control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

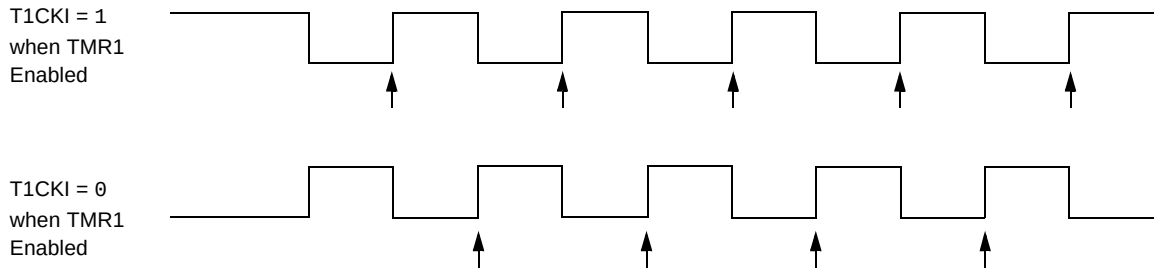
6.4 Timer1 Gate

Timer1 gate source is software configurable to be T1G pin or the output of Comparator 2. This allows the device to directly time external events using T1G or analog events using Comparator 2. See CM2CON1 (Register 9-3) for selecting the Timer1 gate source. This feature can simplify the software for a Delta-Sigma A/D Converter and many other applications. For more information on Delta-Sigma A/D Converters, see the Microchip web site (www.microchip.com).

Note:	TMR1GE bit, of the T1CON Register, must be set to use either T1G or C2OUT as the Timer1 gate source. See Register 9-3 for more information on selecting the Timer1 gate source.

Timer1 gate can be inverted using the T1GINV bit of the T1CON Register, whether it originates from the T1G pin or Comparator 2 output. This configures Timer1 to measure either the active high or active low time between events.

FIGURE 6-2: TIMER1 INCREMENTING EDGE



Note 1: Arrows indicate counter increments.
2: See note box in **Section 6.1 "Timer1 Modes of Operation"**.

7.2 Timer2 Interrupt

The Timer2 module has an 8-bit period register, PR2. Timer2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle. PR2 is a readable and writable register. The PR2 register is initialized to FFh upon Reset.

FIGURE 7-1: TIMER2 BLOCK DIAGRAM

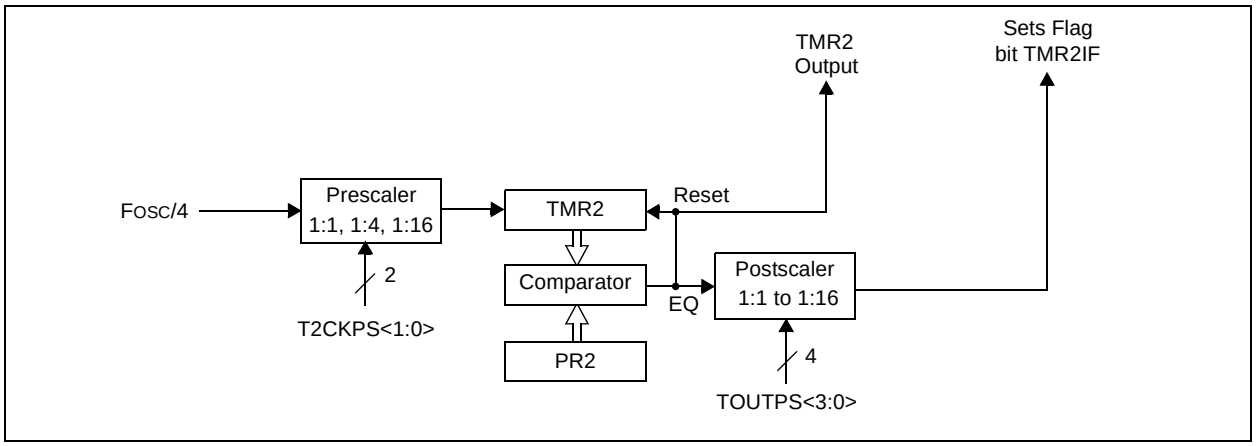


TABLE 7-1: REGISTERS ASSOCIATED WITH TIMER2

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
PIE1	EEIE	ADIE	CCP1IE	C2IE	C1IE	OSFIE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	EEIF	ADIF	CCP1IF	C2IF	C1IF	OSFIF	TMR2IF	TMR1IF	0000 0000	0000 0000
PR2	Timer2 Module Period register								1111 1111	1111 1111
T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
TMR2	Holding Register for the 8-bit TMR2 Register								0000 0000	0000 0000

Legend: – x = unknown, u = unchanged, – = unimplemented, read as '0'. Shaded cells are not used by the Timer2 module.

9.1.2 COMPARATOR C2 CONTROL REGISTERS

The CM2CON0 register is a functional copy of the CM1CON0 register described in **Section 9.1.1 "Comparator C1 Control Register"**. A second control register, CM2CON1, is also present for control of an additional synchronizing feature, as well as mirrors of both comparator outputs.

9.1.2.1 Control Register CM2CON0

The CM2CON0 register, shown in Register 9-2, contains the control and Status bits for Comparator C2.

Setting C2ON of the CM2CON0 Register enables Comparator C2 for operation.

Bits C2CH<1:0> of the CM2CON0 Register select the comparator input from the four analog pins, AN<7:5,1>.

Note:	To use AN<7:5,1> as analog inputs, the appropriate bits must be programmed to 1 in the ANSEL0 register.

C2R of the CM2CON0 Register selects the reference to be used with the comparator. Setting C2R of the CM2CON0 Register selects the C2VREF output of the comparator voltage reference module as the reference voltage for the comparator. Clearing C2R selects the C2IN+ input on the RC0/AN4/C2IN+ pin.

The output of the comparator is available internally via the C2OUT bit of the CM2CON0 Register. To make the output available for an external connection, the C2OE bit of the CM2CON0 Register must be set.

The comparator output, C2OUT, can be inverted by setting the C2POL bit of the CM2CON0 Register. Clearing C2POL results in a non-inverted output.

A complete table showing the output state versus input conditions and the polarity bit is shown in Table 9-2.

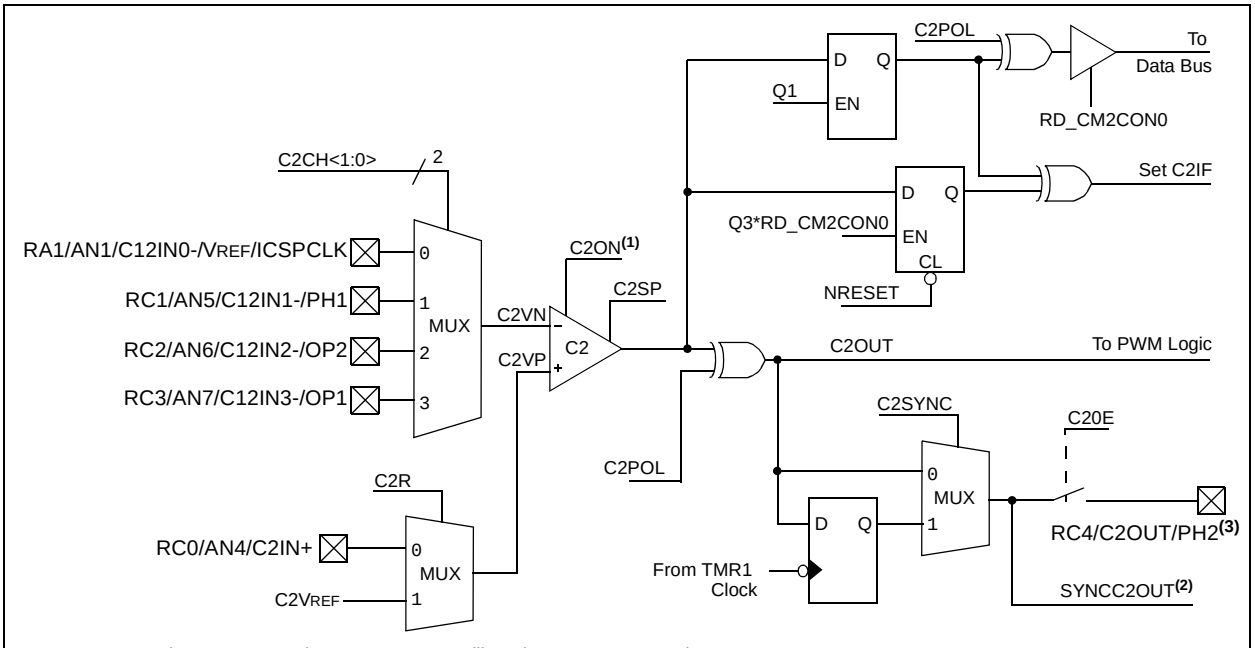
TABLE 9-2: C2 OUTPUT STATE VERSUS INPUT CONDITIONS

Input Condition	C2POL	C2OUT
C2VN > C2VP	0	0
C2VN < C2VP	0	1
C2VN > C2VP	1	1
C2VN < C2VP	1	0

Note 1:	The internal output of the comparator is latched at the end of each instruction cycle. External outputs are not latched.
2:	The C2 interrupt will operate correctly with C2OE set or cleared. An external output is not required for the C2 interrupt.
3:	For C2 output on RC4/C2OUT/PH2: (C2OE = 1) and (C2ON = 1) and (TRISA<4> = 0).

C2SP of the CM2CON0 Register configures the speed of the comparator. When C2SP is set, the comparator operates at its normal speed. Clearing C2SP operates the comparator in low-power mode.

FIGURE 9-2: COMPARATOR C2 SIMPLIFIED BLOCK DIAGRAM



Note 1: When C2ON = 0, the C2 comparator will produce a '0' output to the XOR Gate.
2: Timer1 gate control (see Figure 6-1).
3: Output shown for reference only. For more detail, see Figure 4-13.

REGISTER 13-5: PWMCON1: PWM CONTROL REGISTER 1

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	COMOD1	COMOD0	CMDLY4	CMDLY3	CMDLY2	CMDLY1	CMDLY0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

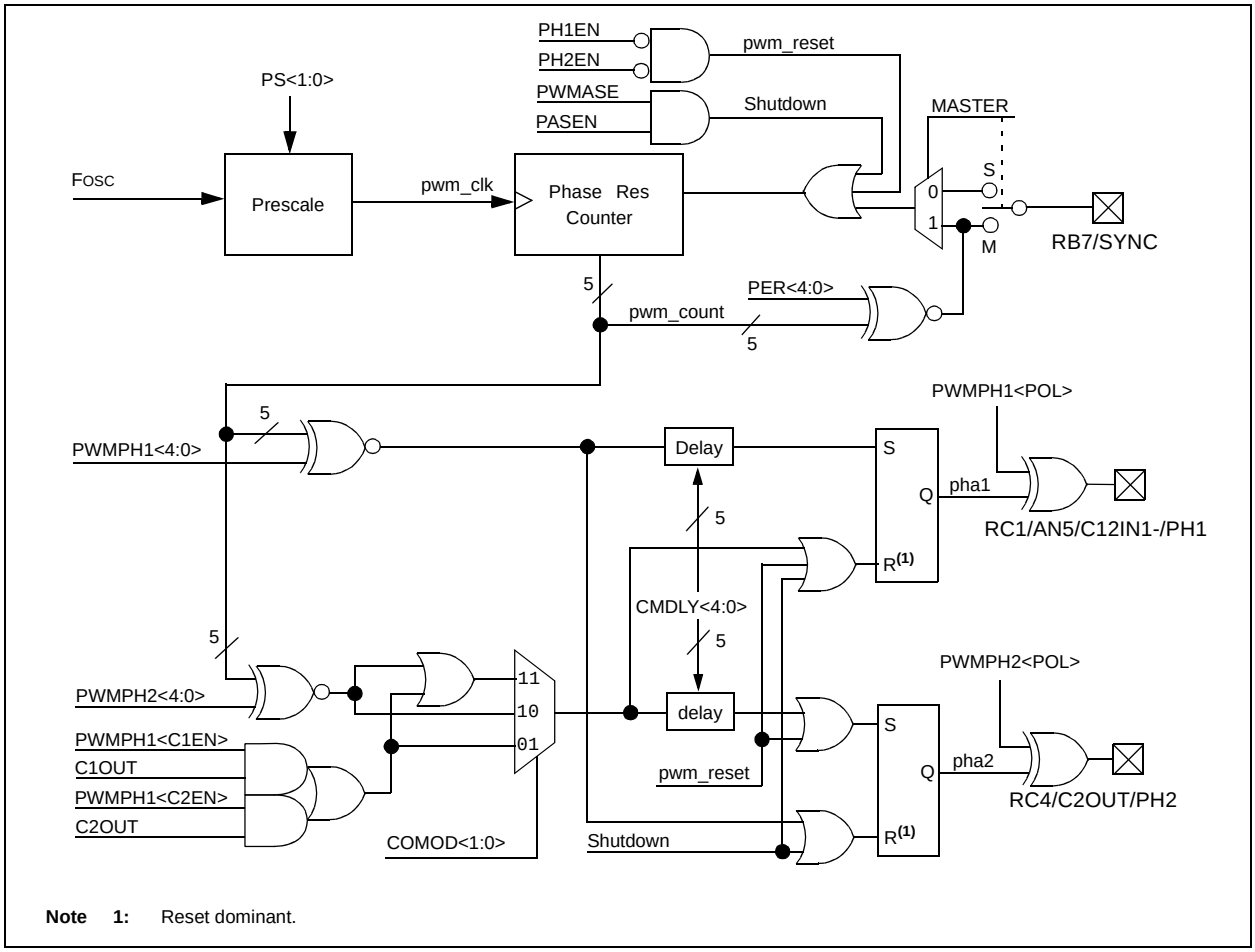
bit 7 **Unimplemented:** Read as '0'

bit 6-5 **COMOD<1:0>:** Complementary Mode Select bits(1)
- 00 = Normal two-phase operation. Complementary mode is disabled.
- 01 = Complementary operation. Duty cycle is terminated by C1OUT or C2OUT.
- 10 = Complementary operation. Duty cycle is terminated by PWMPH2<4:0> = pwm_count.
- 11 = Complementary operation. Duty cycle is terminated by PWMPH2<4:0> = pwm_count or C1OUT or C2OUT.

bit 4-0 **CMDLY<4:0>:** Complementary Drive Dead Time bits (typical)
- 00000 = Delay = 0
- 00001 = Delay = 5 ns
- 00010 = Delay = 10 ns
- ••••• = •••
- 11111 = Delay = 155 ns

Note 1: PWMCON0<1:0> must be set to '11' for Complementary mode operation.

FIGURE 13-5: COMPLEMENTARY OUTPUT PWM BLOCK DIAGRAM



Note 1: Reset dominant.

15.4 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt (e.g., W and STATUS registers). This must be implemented in software.

Since the last 16 bytes of all banks are common in the PIC16F785/HV785 (see Figure 2-2), temporary holding registers W_TEMP and STATUS_TEMP should be placed in here. These 16 locations do not require banking, therefore, making it easier to save and restore context. The same code shown in Example 15-1 can be used to:

- Store the W register
- Store the STATUS register
- Execute the ISR code
- Restore the Status (and Bank Select Bit register)
- Restore the W register

Note:	The PIC16F785/HV785 normally does not require saving the PCLATH. However, if computed GOTO's are used in the ISR and the main code, the PCLATH must be saved and restored in the ISR.

EXAMPLE 15-1: SAVING STATUS AND W REGISTERS IN RAM

```
MOVWF   W_TEMP              ;Copy W to TEMP register
SWAPF   STATUS,W            ;Swap status to be saved into W (swap does not affect status)
CLRF    STATUS              ;bank 0, regardless of current bank, Clears IRP,RP1,RP0
MOVWF   STATUS_TEMP         ;Save status to bank zero STATUS_TEMP register
:
:(ISR)                      ;Insert user code here
:
SWAPF   STATUS_TEMP,W       ;Swap STATUS_TEMP register into W
                            ;(sets bank to original state)
MOVWF   STATUS              ;Move W into Status register
SWAPF   W_TEMP,F            ;Swap W_TEMP
SWAPF   W_TEMP,W            ;Swap W_TEMP into W
```

COMF	Complement f
Syntax:	[*label*] COMF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	$(\bar{f}) \rightarrow$ (destination)
Status Affected:	Z
Description:	The contents of register 'f' are complemented. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f'.

DECF	Decrement f
Syntax:	[*label*] DECF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) - 1 $\rightarrow$ (destination)
Status Affected:	Z
Description:	Decrement register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

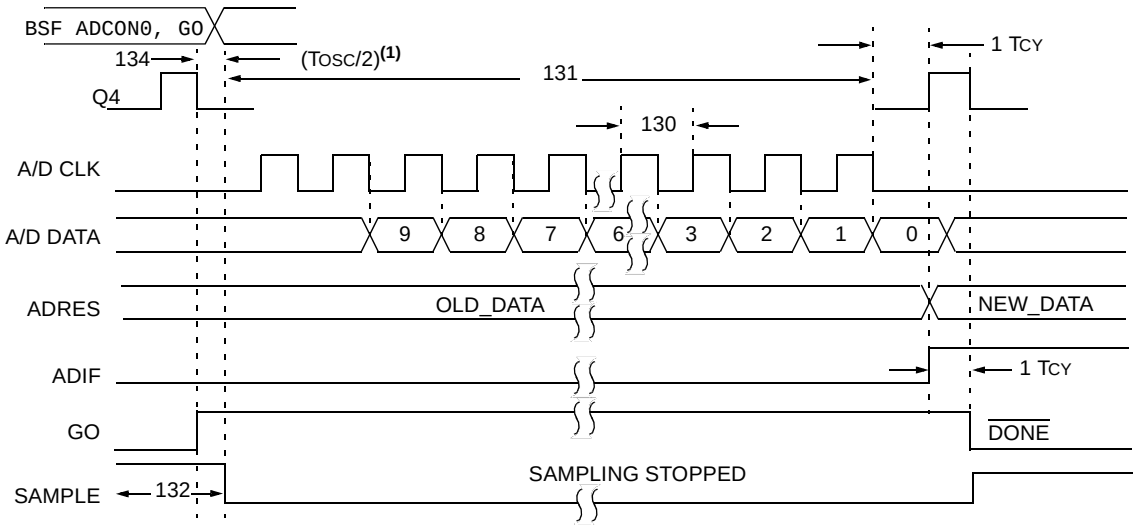
DECFSZ	Decrement f, Skip if 0
Syntax:	[*label*] DECFSZ f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) - 1 $\rightarrow$ (destination); skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are decremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', then a NOP is executed instead, making it a two-cycle instruction.

GOTO	Unconditional Branch
Syntax:	[*label*] GOTO k
Operands:	$0 \le k \le 2047$
Operation:	k $\rightarrow$ PC<10:0> PCLATH<4:3> $\rightarrow$ PC<12:11>
Status Affected:	None
Description:	GOTO is an unconditional branch. The eleven-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two-cycle instruction.

INCF	Increment f
Syntax:	[*label*] INCF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) + 1 $\rightarrow$ (destination)
Status Affected:	Z
Description:	The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

INCFSZ	Increment f, Skip if 0
Syntax:	[*label*] INCFSZ f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) + 1 $\rightarrow$ (destination), skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', a NOP is executed instead, making it a two-cycle instruction.

FIGURE 19-9: PIC16F785/HV785 A/D CONVERSION TIMING (NORMAL MODE)



Note 1: If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

TABLE 19-16: PIC16F785/HV785 A/D CONVERSION REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
130	TAD	A/D Clock Period	1.6	—	—	µs	TOSC-based, VREF ≥ 3.0V
			3.0*	—	—	µs	TOSC-based, VREF full range
130	TAD	A/D Internal RC Oscillator Period					ADCS<1:0> = 11 (RC mode)
			3.0*	6.0	9.0*	µs	At VDD = 2.5V
			2.0*	4.0	6.0*	µs	At VDD = 5.0V
131	TCNV	Conversion Time (not including Acquisition Time)(1)	—	11	—	TAD	Set GO bit to new data in A/D result register
132	TACQ	Acquisition Time	**(Note 2)**	11.5	—	µs	
			5*	—	—	µs	The minimum time is the amplifier settling time. This may be used if the "new" input voltage has not changed by more than 1 LSb (i.e., 4.1 mV @ 4.096V) from the last sampled voltage (as stored on CHOLD).
134	TGO	Q4 to A/D Clock Start	—	TOSC/2	—	—	If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRESH and ADRESL registers may be read on the following TCY cycle.

2: See **Section 12.2 "A/D Acquisition Requirements"** for minimum conditions.

FIGURE 20-6: MAXIMUM IDD vs. VDD OVER FOSC (XT MODE)

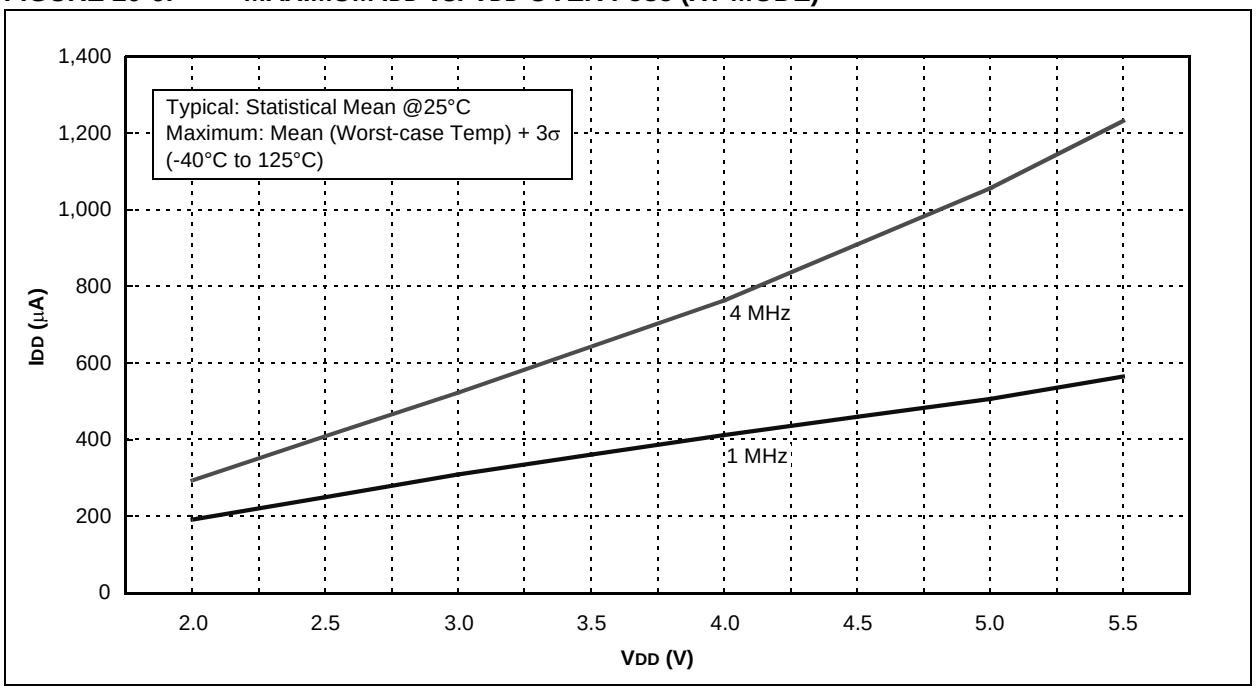


FIGURE 20-7: IDD vs. VDD (LP MODE)

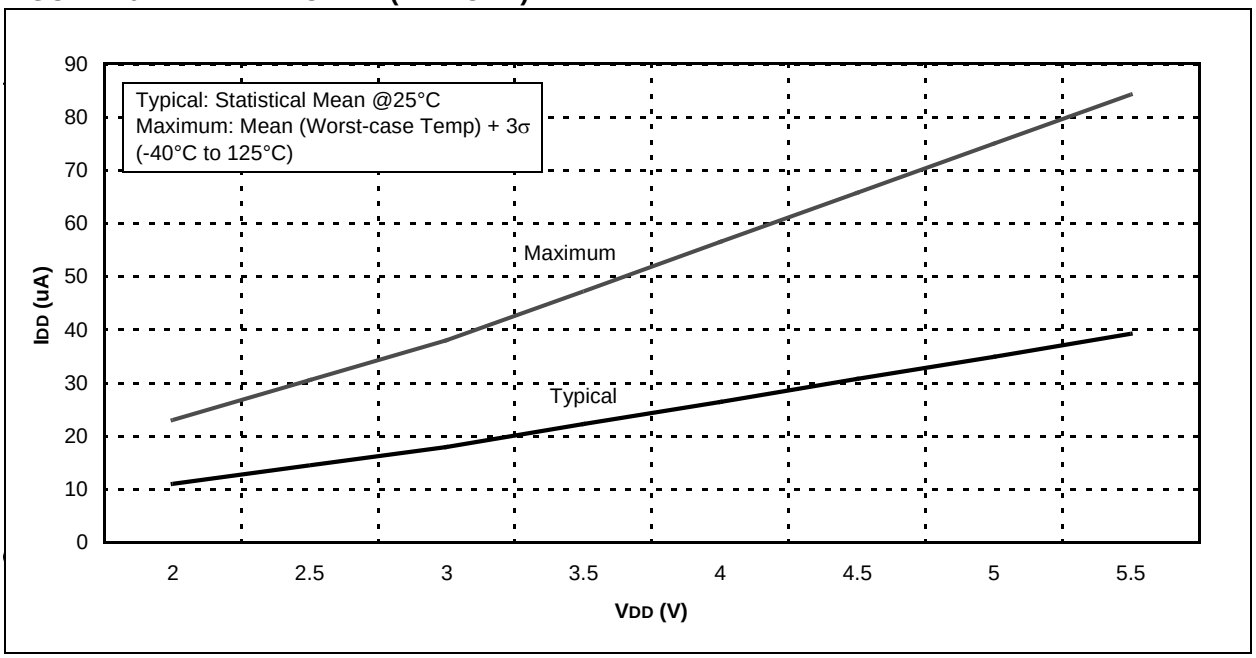


FIGURE 20-12: MAXIMUM IDD vs. FOSC OVER VDD (HFINTOSC MODE)

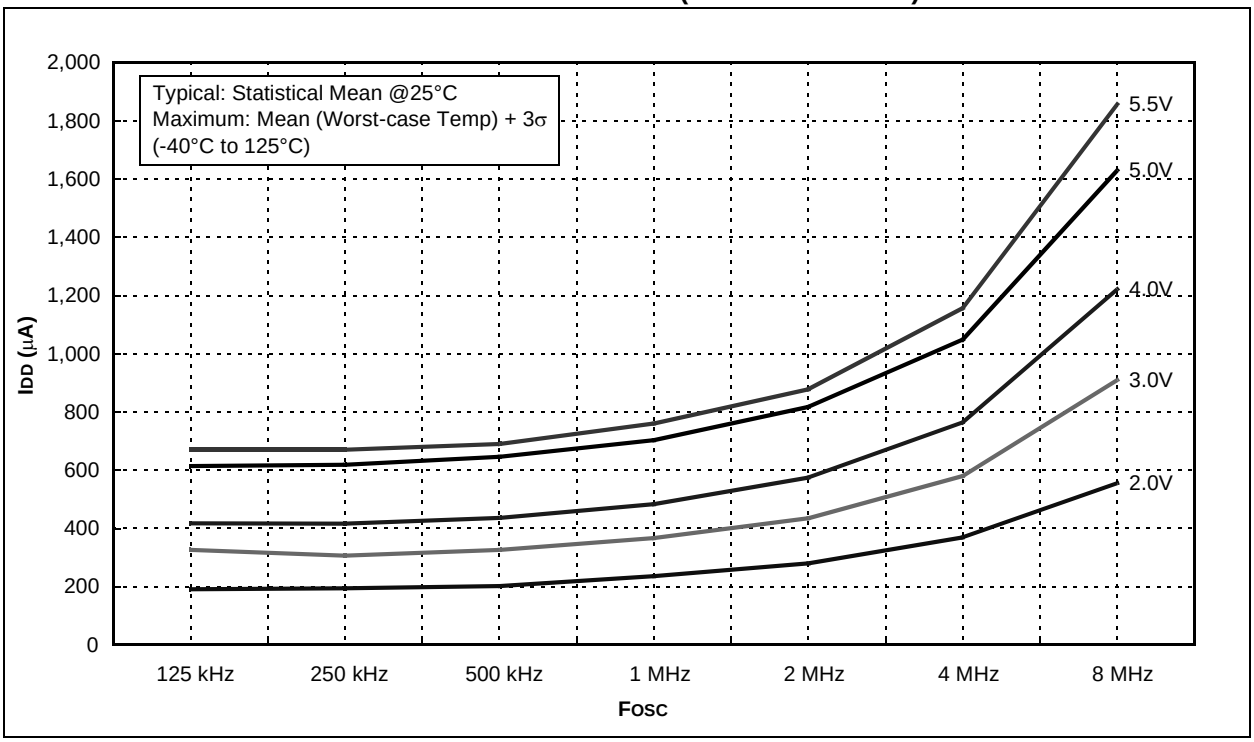


FIGURE 20-13: TYPICAL IPD vs. VDD (SLEEP MODE, ALL PERIPHERALS DISABLED)

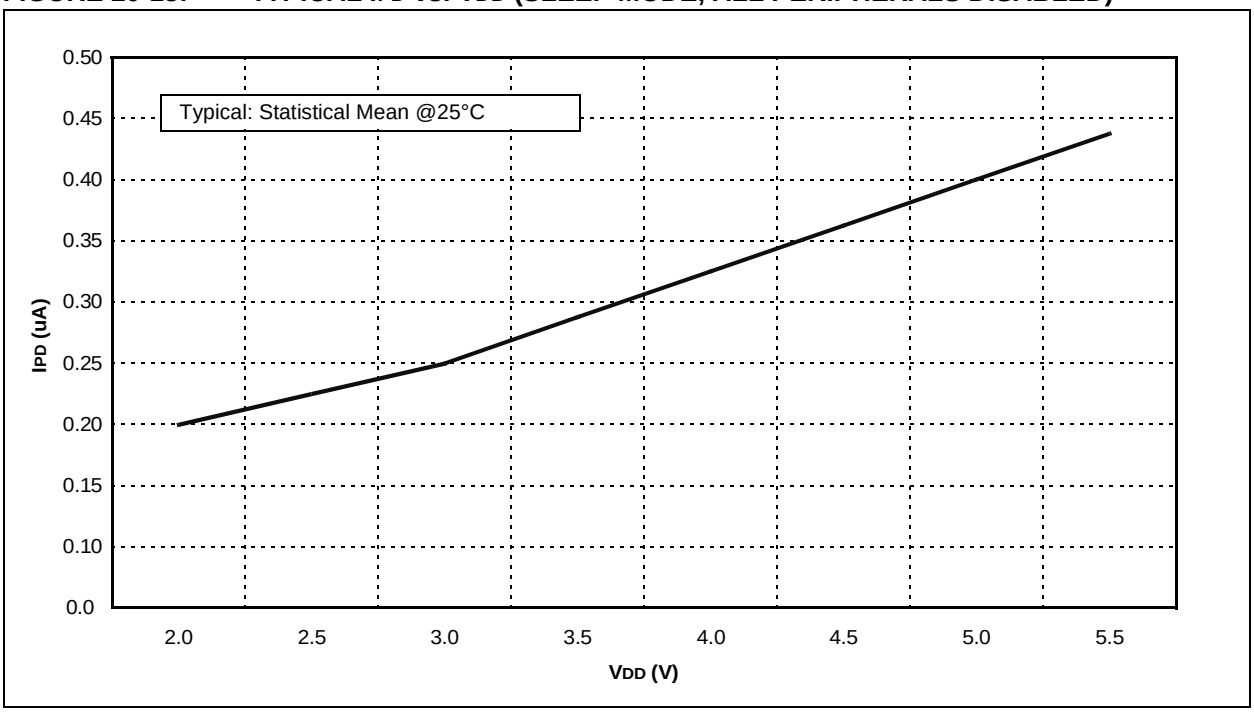


FIGURE 20-16: COMPARATOR IPD vs. VDD (BOTH COMPARATORS ENABLED) CXSP=1

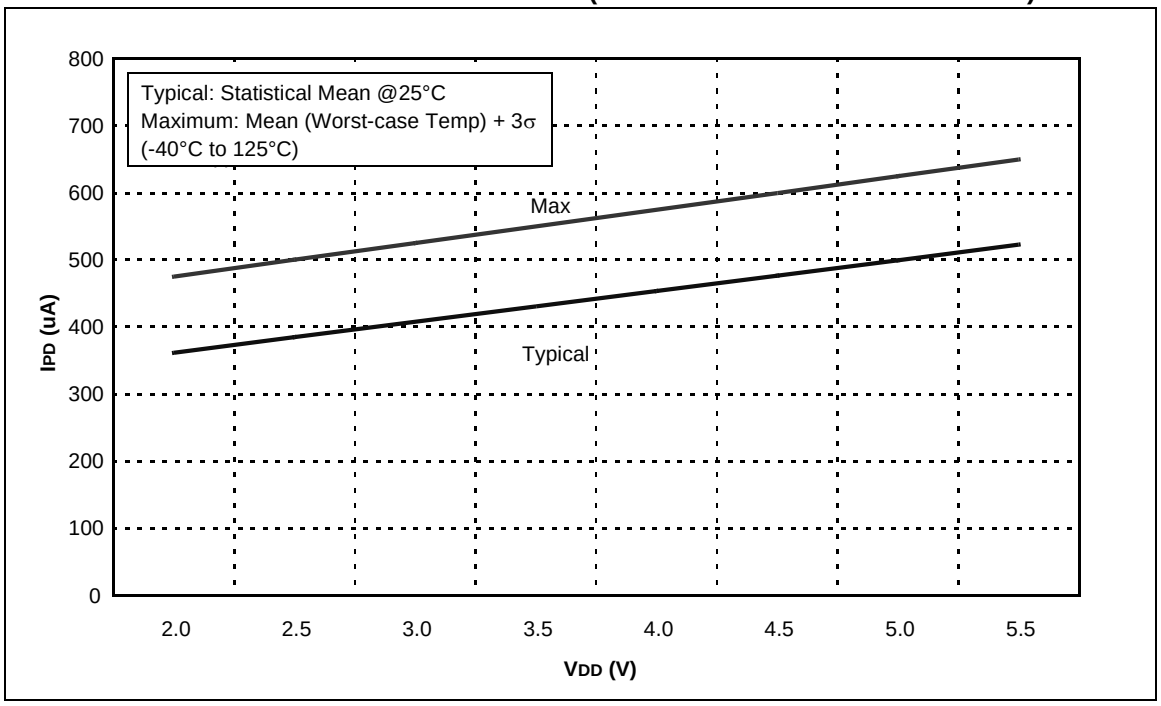


FIGURE 20-17: BOR IPD vs. VDD OVER TEMPERATURE

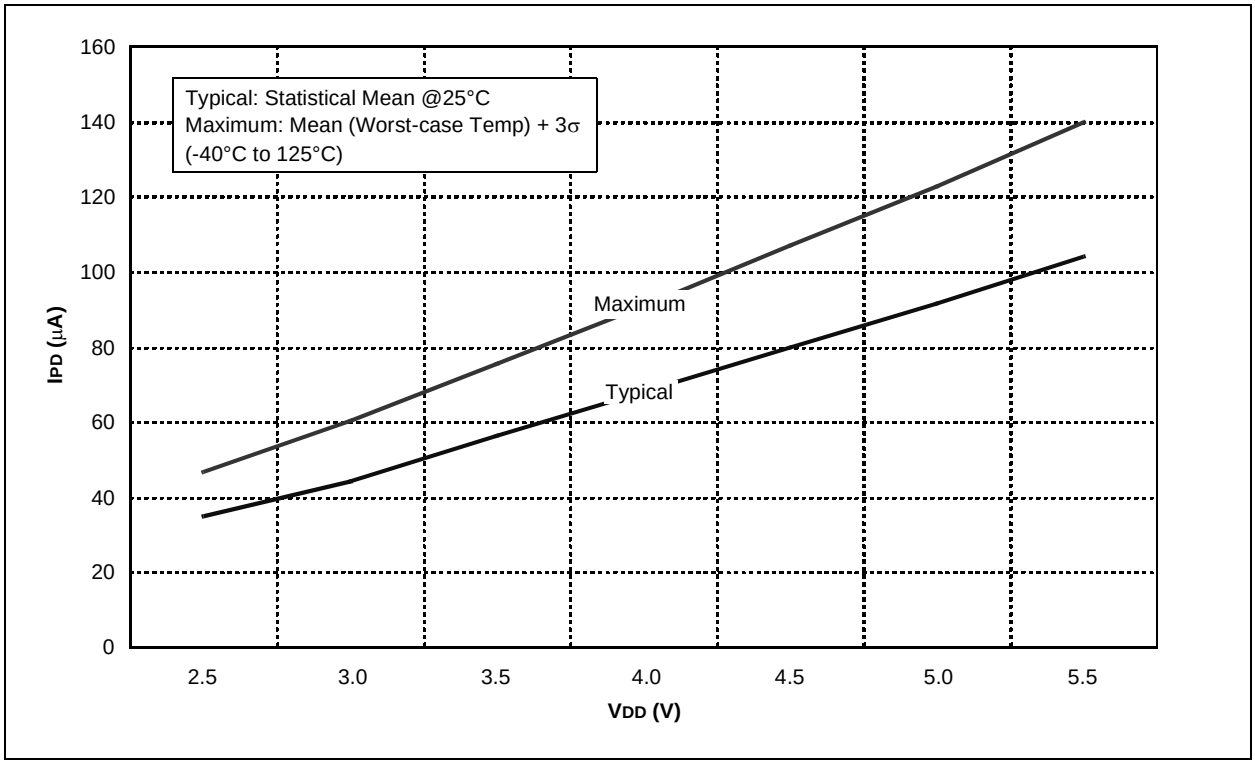


FIGURE 20-34: TYPICAL HFINTOSC FREQUENCY CHANGE vs. VDD (25°C)

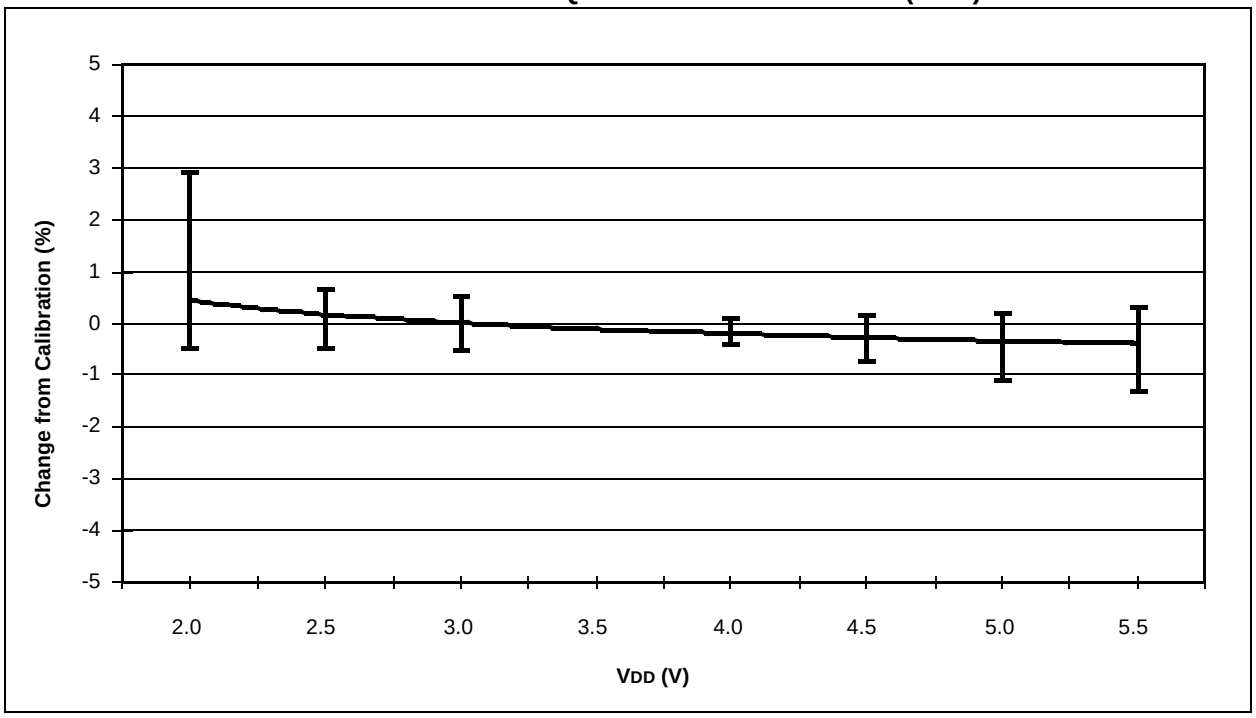
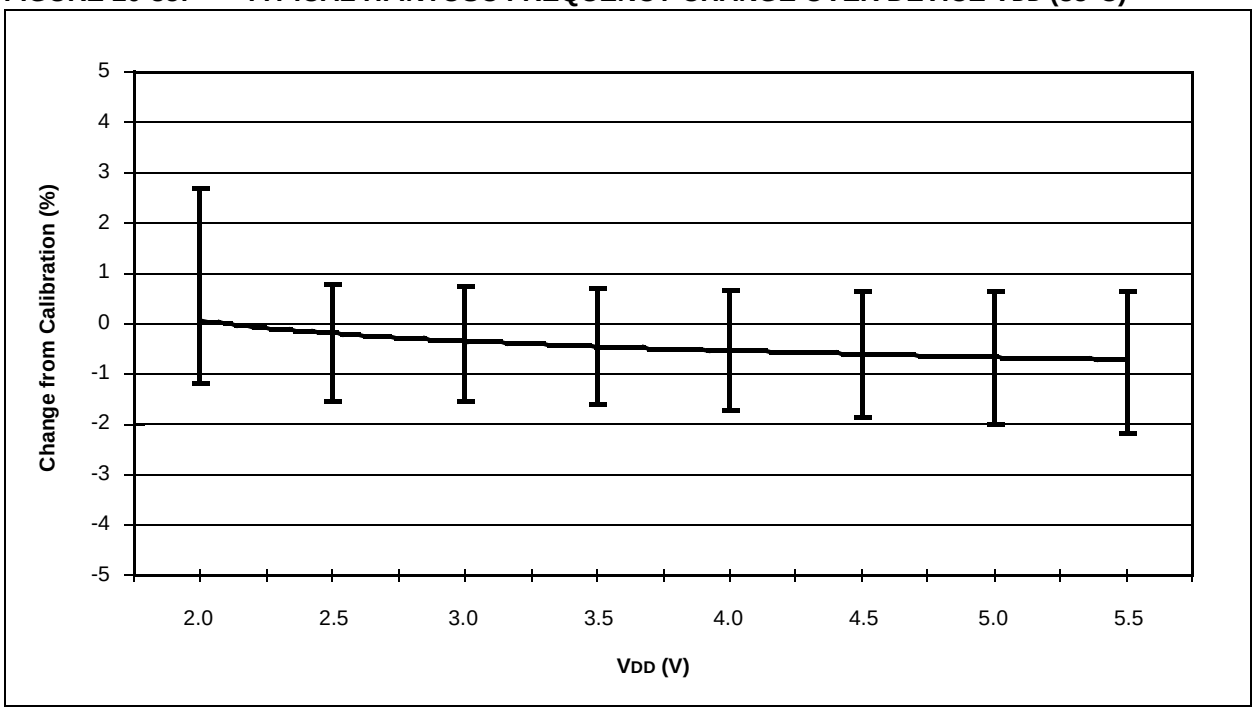


FIGURE 20-35: TYPICAL HFINTOSC FREQUENCY CHANGE OVER DEVICE VDD (85°C)



PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device:	PIC16F785[(1)], PIC16HV785[(1)], PIC16F785T[(2)], PIC16HV785T[(2)]; VDD range 4.2V to 5.5V PIC16F785[(1)], PIC16HV785[(1)], PIC16F785T[(2)], PIC16HV785T[(2)]; VDD range 2.0V to 5.5V
Temperature Range:	I = -40°C to +85°C Industrial) E = -40°C to +125°C Extended)
Package:	ML = QFN P = PDIP SO = SOIC SS = SSOP
Pattern:	QTP, SQTP, Code or Special Requirements (blank otherwise)

Examples:

a) PIC16F785 - E/SO 301 = Extended temp., SOIC package.

b) PIC16F785 - I/ML = Industrial temp., QFN package.

Note 1: F = Standard Voltage Range
LF = Wide Voltage Range

2: T = in tape and reel PLCC, and TQFP packages only.

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