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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 14x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f785t-i-ss

QFN (4x4x0.9) Pin Diagram

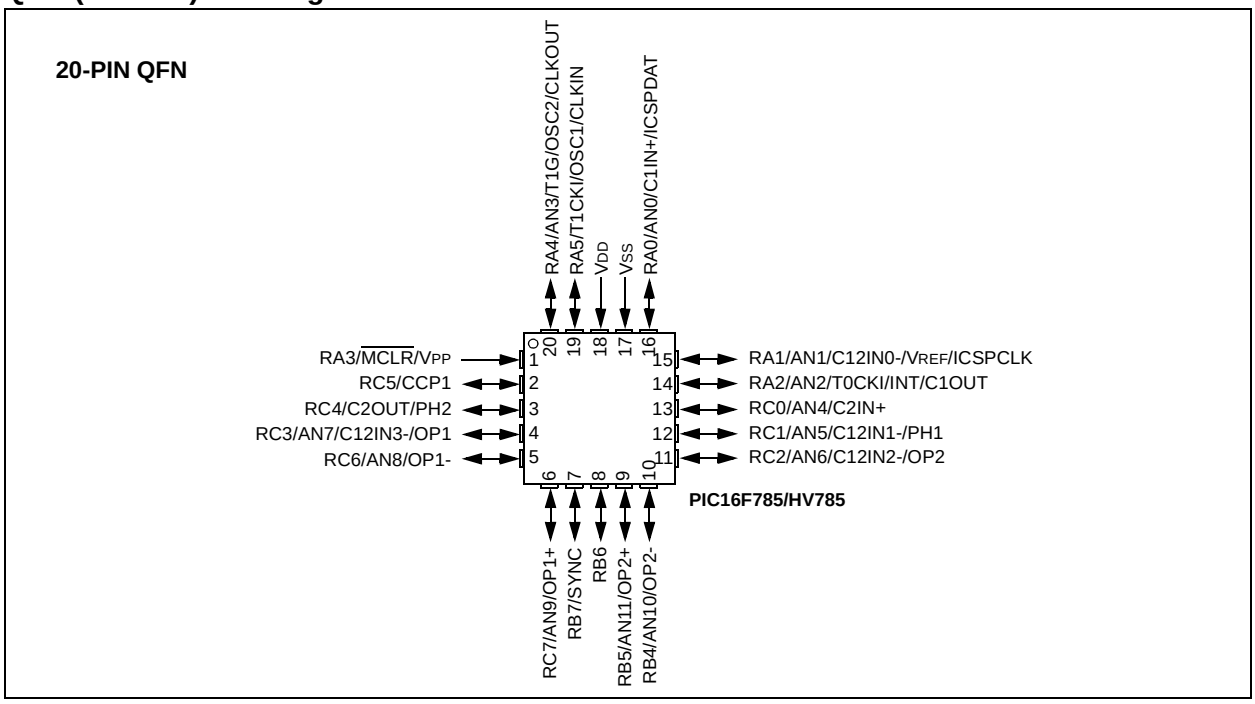


TABLE 2: QFN PIN SUMMARY

I/O	Pin	Analog	Comp.	Op Amps	PWM	Timers	CCP	Interrupt	Pull-ups	Basic
RA0	16	AN0	C1IN+	—	—	—	—	IOC	Y	ICSPDAT
RA1	15	AN1/VREF	C12IN0-	—	—	—	—	IOC	Y	ICSPCLK
RA2	14	AN2	C1OUT	—	—	T0CKI	—	INT/IOC	Y	—
RA3(1)	1	—	—	—	—	—	—	IOC	Y	$\overline{\text{MCLR}}$/VPP
RA4	20	AN3	—	—	—	T1G	—	IOC	Y	OSC2/CLKOUT
RA5	19	—	—	—	—	T1CKI	—	IOC	Y	OSC1/CLKIN
RB4	10	AN10	—	OP2-	—	—	—	—	—	—
RB5	9	AN11	—	OP2+	—	—	—	—	—	—
RB6(2)	8	—	—	—	—	—	—	—	—	—
RB7	7	—	—	—	SYNC	—	—	—	—	—
RC0	13	AN4	C2IN+	—	—	—	—	—	—	—
RC1	12	AN5	C12IN1-	—	PH1	—	—	—	—	—
RC2	11	AN6	C12IN2-	OP2	—	—	—	—	—	—
RC3	4	AN7	C12IN3-	OP1	—	—	—	—	—	—
RC4	3	—	C2OUT	—	PH2	—	—	—	—	—
RC5	2	—	—	—	—	—	CCP1	—	—	—
RC6	5	AN8	—	OP1-	—	—	—	—	—	—
RC7	6	AN9	—	OP1+	—	—	—	—	—	—
—	18	—	—	—	—	—	—	—	—	VDD
—	17	—	—	—	—	—	—	—	—	VSS

Note 1: Input only.

2: Open drain.

TABLE 3-4: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CONFIG	$\overline{CPD}$	$\overline{CP}$	MCLRE	$\overline{PWRTE}$	WDTE	FOSC2	FOSC1	FOSC0	—	—
OSCCON	—	IRCF2	IRCF1	IRCF0	OSTS	HTS	LTS	SCS	-110 q000	-110 q000
OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	---0 0000	---u uuuu
PIE1	EEIE	ADIE	CCP1IE	C2IE	C1IE	OSFIE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	EEIF	ADIF	CCP1IF	C2IF	C1IF	OSFIF	TMR2IF	TMR1IF	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0', q = value depends on condition. Shaded cells are not used by oscillators.

Note 1: See Register 15.2 for operation of all Configuration Word bits.

4.3.1 PORTB PIN DESCRIPTIONS AND DIAGRAMS

Each PORTB pin is multiplexed with other functions. The pins and their combined functions are briefly described here. For specific information about individual functions such as the PWM, operational amplifier, or the A/D, refer to the appropriate section in this Data Sheet.

4.3.1.1 RB4/AN10/OP2-

The RB4/AN10/OP2- pin is configurable to function as one of the following:

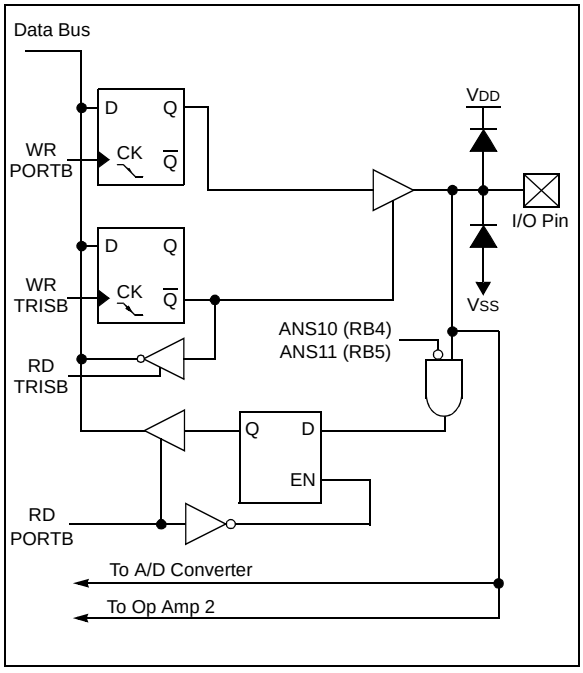
- General purpose I/O
- Analog input to the A/D
- Analog input to Op Amp 2

4.3.1.2 RB5/AN11/OP2+

The RB5/AN11/OP2+ pin is configurable to function as one of the following:

- General purpose I/O
- Analog input to the A/D
- Analog input to Op Amp 2

FIGURE 4-7: BLOCK DIAGRAM OF RB4 AND RB5

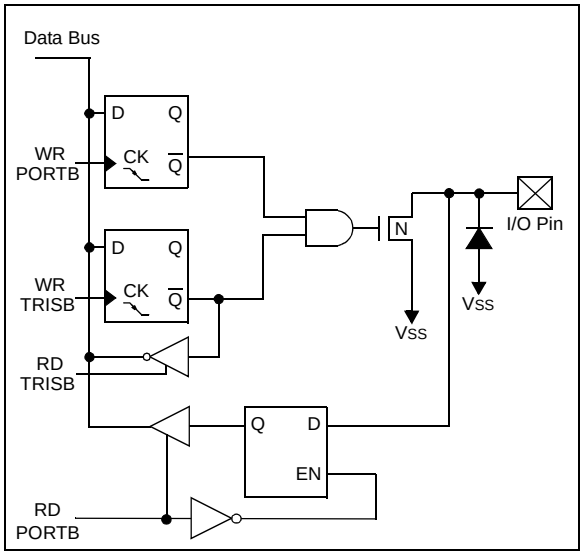


4.3.1.3 RB6

The RB6 pin is configurable to function as the following:

- Open drain general purpose I/O

FIGURE 4-8: BLOCK DIAGRAM OF RB6

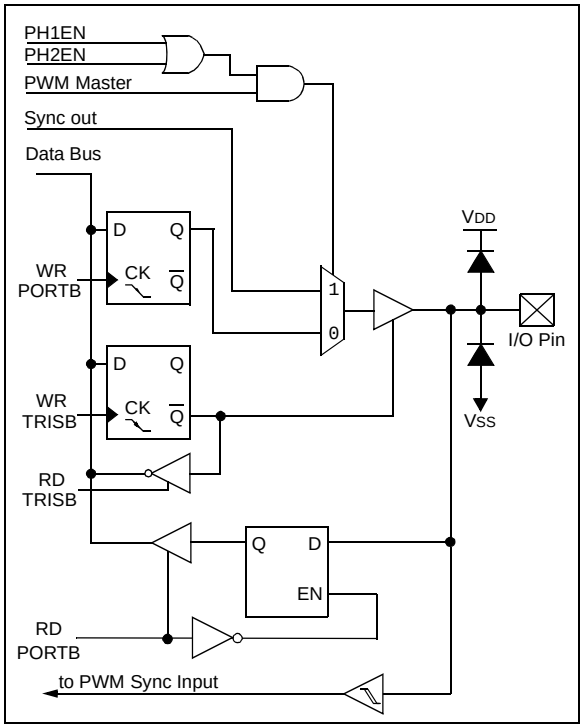


4.3.1.4 RB7/SYNC

The RB7/SYNC pin is configurable to function as one of the following:

- General purpose I/O
- PWM synchronization input and output

FIGURE 4-9: BLOCK DIAGRAM OF RB7



7.2 Timer2 Interrupt

The Timer2 module has an 8-bit period register, PR2. Timer2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle. PR2 is a readable and writable register. The PR2 register is initialized to FFh upon Reset.

FIGURE 7-1: TIMER2 BLOCK DIAGRAM

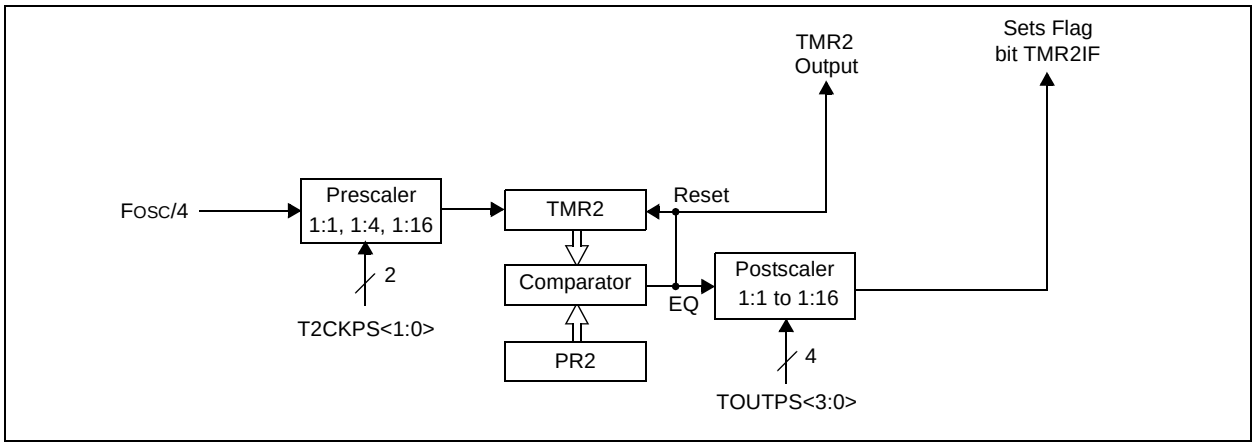


TABLE 7-1: REGISTERS ASSOCIATED WITH TIMER2

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
PIE1	EEIE	ADIE	CCP1IE	C2IE	C1IE	OSFIE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	EEIF	ADIF	CCP1IF	C2IF	C1IF	OSFIF	TMR2IF	TMR1IF	0000 0000	0000 0000
PR2	Timer2 Module Period register								1111 1111	1111 1111
T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
TMR2	Holding Register for the 8-bit TMR2 Register								0000 0000	0000 0000

Legend: – x = unknown, u = unchanged, – = unimplemented, read as '0'. Shaded cells are not used by the Timer2 module.

9.0 COMPARATOR MODULE

The Comparator module has two separate voltage comparators: Comparator 1 (C1) and Comparator 2 (C2).

Each comparator offers the following list of features:

- Control and Configuration register
- Comparator output available externally
- Programmable output polarity
- Interrupt-on-change flags
- Wake-up from Sleep
- Configurable as feedback input to the PWM
- Programmable four input multiplexer
- Programmable two input reference selections
- Programmable speed/power
- Output synchronization to Timer1 clock input (Comparator C2 only)

9.1 Control Registers

Both comparators have separate control and Configuration registers: CM1CON0 for C1 and CM2CON0 for C2. In addition, Comparator C2 has a second control register, CM2CON1, for synchronization control and simultaneous reading of both comparator outputs.

9.1.1 COMPARATOR C1 CONTROL REGISTER

The CM1CON0 register (shown in Register 9-1) contains the control and Status bits for the following:

- Comparator enable
- Comparator input selection
- Comparator reference selection
- Output mode
- Comparator speed

Setting C1ON (CM1CON0<7>) enables Comparator C1 for operation.

Bits C1CH<1:0> of the CM1CON0 Register select the comparator input from the four analog pins AN<7:5,1>.

Note:	To use AN<7:5,1> as analog inputs the appropriate bits must be programmed to '1' in the ANSEL0 register.

Setting C1R of the CM1CON0 Register selects the C1VREF output of the comparator voltage reference module as the reference voltage for the comparator. Clearing C1R selects the C1IN+ input on the RA0/AN0/C1IN+/ICSPDAT pin.

The output of the comparator is available internally via the C1OUT flag of the CM1CON0 Register. To make the output available for an external connection, the C1OE bit of the CM1CON0 Register must be set.

The polarity of the comparator output can be inverted by setting the C1POL bit of the CM1CON0 Register. Clearing C1POL results in a non-inverted output.

A complete table showing the output state versus input conditions and the polarity bit is shown in Table 9-1.

TABLE 9-1: C1 OUTPUT STATE VERSUS INPUT CONDITIONS

Input Condition	C1POL	C1OUT
C1VN > C1VP	0	0
C1VN < C1VP	0	1
C1VN > C1VP	1	1
C1VN < C1VP	1	0

Note 1:	The internal output of the comparator is latched at the end of each instruction cycle. External outputs are not latched.
2:	The C1 interrupt will operate correctly with C1OE set or cleared.
3:	To output C1 on RA2/AN2/T0CKI/INT/C1OUT:(C1OE = 1) and (C1ON = 1) and (TRISA<2> = 0).

C1SP of the CM1CON0 Register configures the speed of the comparator. When C1SP is set, the comparator operates at its normal speed. Clearing C1SP operates the comparator in a slower, low-power mode.

REGISTER 9-2: CM2CON0: COMPARATOR C2 CONTROL REGISTER 0

R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
C2ON	C2OUT	C2OE	C2POL	C2SP	C2R	C2CH1	C2CH0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **C2ON:** Comparator C2 Enable bit
1 = C2 Comparator is enabled
0 = C2 Comparator is disabled

bit 6 **C2OUT:** Comparator C2 Output bit
If C2POL = 1 (inverted polarity):
C2OUT = 1, C2VP < C2VN
C2OUT = 0, C2VP > C2VN
If C2POL = 0 (non-inverted polarity):
C2OUT = 1, C2VP > C2VN
C2OUT = 0, C2VP < C2VN

bit 5 **C2OE:** Comparator C2 Output Enable bit
1 = C2OUT is present on RC4/C2OUT/PH2**(1)**
0 = C2OUT is internal only

bit 4 **C2POL:** Comparator C2 Output Polarity Select bit
1 = C2OUT logic is inverted
0 = C2OUT logic is not inverted

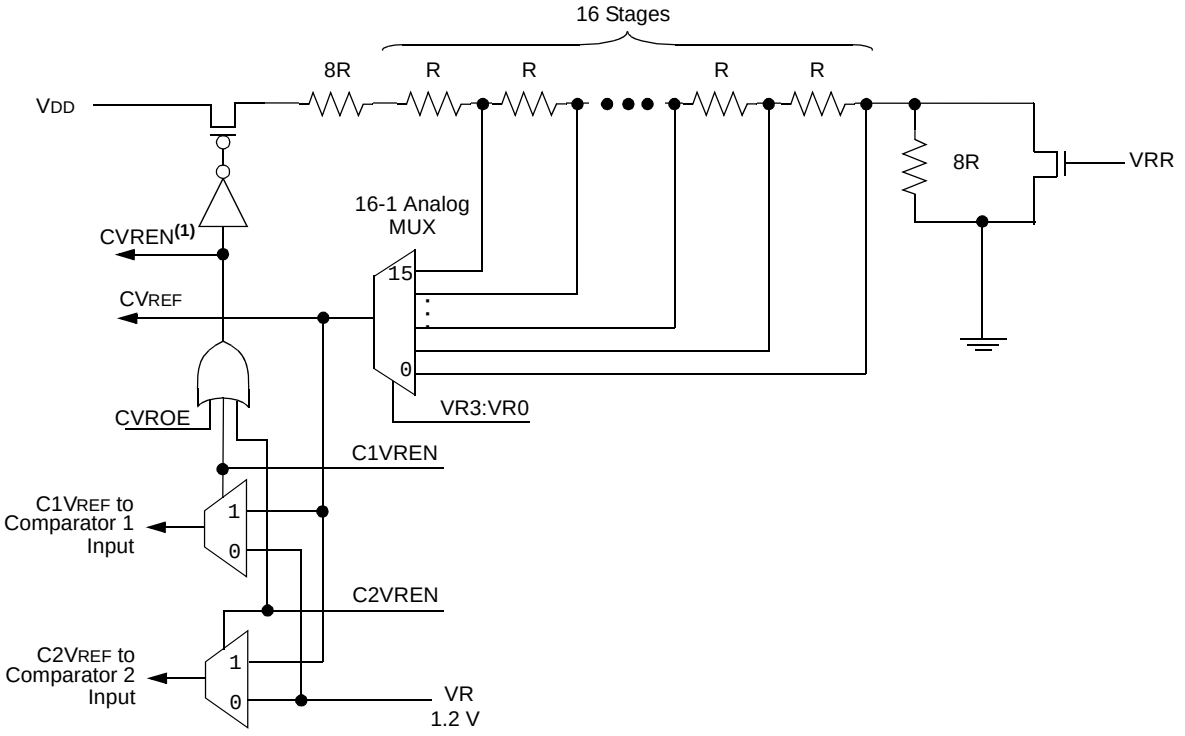
bit 3 **C2SP:** Comparator C2 Speed Select bit
1 = C2 operates in normal speed mode
0 = C2 operates in low power, slow speed mode.

bit 2 **C2R:** Comparator C2 Reference Select bits (non-inverting input)
1 = C2VP connects to $C2V_{REF}$
0 = C2VP connects to RC0/AN4/C2IN+

bit 1-0 **C2CH<1:0>:** Comparator C2 Channel Select bits
00 = C2VN of C2 connects to RA1/AN1/C12IN0-/V_{REF}/ICSPCLK
01 = C2VN of C2 connects to RC1/AN5/C12IN1-/PH1
10 = C2VN of C2 connects to RC2/AN6/C12IN2-/OP2
11 = C2VN of C2 connects to RC3/AN7/C12IN3-/OP1

Note 1: C2OUT will only drive RC4/C2OUT/PH2 if: (C2OE = 1) and (C2ON = 1) and (TRISC<4> = 0).

FIGURE 10-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM

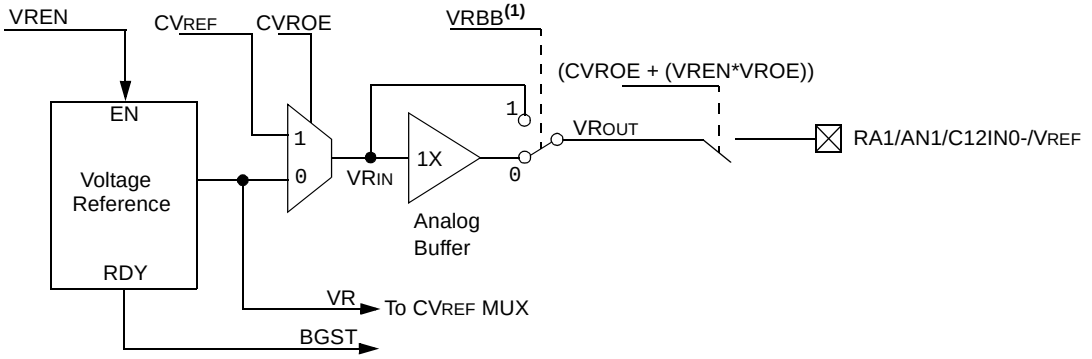


Note 1: See Register 10-1, bits 3-0.

10.2.1 VR STABILIZATION PERIOD

When the Voltage Reference module is enabled, it will require some time for the reference and its amplifier circuits to stabilize. The user program must include a small delay routine to allow the module to settle. See **Section 19.0 "Electrical Specifications"** for the minimum delay requirement.

FIGURE 10-2: VR REFERENCE BLOCK DIAGRAM



Note 1: Buffered output requires $V_{RIN} = (V_{DD} - 1.4)V$.
2: VREN is fixed high for PIC16HV785 device.

TABLE 10-1: REGISTERS ASSOCIATED WITH COMPARATOR AND VOLTAGE REFERENCE MODULES

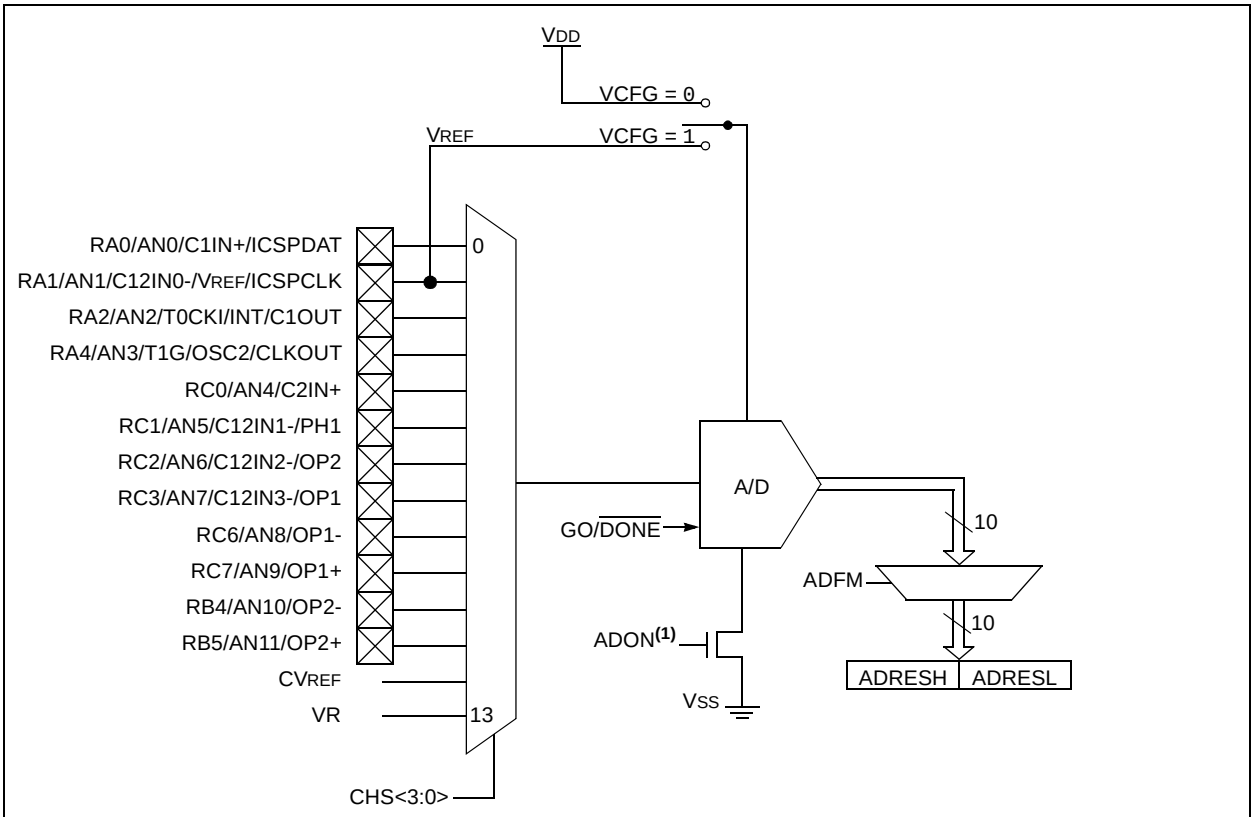
Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSEL0	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111
CM1CON0	C1ON	C1OUT	C1OE	C1POL	C1SP	C1R	C1CH1	C1CH0	0000 0000	0000 0000
CM2CON0	C2ON	C2OUT	C2OE	C2POL	C2SP	C2R	C2CH1	C2CH0	0000 0000	0000 0000
CM2CON1	MC1OUT	MC2OUT	—	—	—	—	T1GSS	C2SYNC	00-- --10	00-- --10
PIE1	EEIE	ADIE	CCP1IE	C2IE	C1IE	OSFIE	TMR2IE	TMR1IE	0000 ---0	0000 ---0
PIR1	EEIF	ADIF	CCP1IF	C2IF	C1IF	OSFIF	TMR2IF	TMR1IF	0000 ---0	0000 ---0
PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--xx xxxx	--uu uuuu
PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu
REFCON	—	—	BGST	VRBB	VREN	VROE	CVROE	—	--00 000-	--00 000-
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
VRCON	C1VREN	C2VREN	VRR	—	VR3	VR2	VR1	VR0	000- 0000	000- 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for comparator.

12.0 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The analog-to-digital converter (A/D) allows conversion of an analog input signal to a 10-bit binary representation of that signal. The PIC16F785/HV785 has twelve analog I/O inputs, plus two internal inputs, multiplexed into one sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a binary result via successive approximation and stores the result in a 10-bit register. The voltage reference used in the conversion is software selectable to either VDD or a voltage applied by the VREF pin. Figure 12-1 shows the block diagram of the A/D on the PIC16F785/HV785.

FIGURE 12-1: A/D BLOCK DIAGRAM



Note 1: When ADON = 0 all input channels are disconnected from ADC (no loading).

REGISTER 12-3: ADCON0: A/D CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	VCFG	CHS3	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ADFM:** A/D Result Formed Select bit
1 = Right justified
0 = Left justified

bit 6 **VCFG**: Voltage Reference bit
1 = V_{REF} pin
0 = V_{DD}

bit 5-2 **CHS<3:0>:** Analog Channel Select bits
0000 = Channel 00 (AN0)
0001 = Channel 01 (AN1)
0010 = Channel 02 (AN2)
0011 = Channel 03 (AN3)
0100 = Channel 04 (AN4)
0101 = Channel 05 (AN5)
0110 = Channel 06 (AN6)
0111 = Channel 07 (AN7)
1000 = Channel 08 (AN8)
1001 = Channel 09 (AN9)
1010 = Channel 10 (AN10)
1011 = Channel 11 (AN11)
1100 = CV_{REF}
1101 = VR
1110 = Reserved. Do not use.
1111 = Reserved. Do not use.

bit 1 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit
1 = A/D conversion cycle in progress. Setting this bit starts an A/D conversion cycle.
This bit is automatically cleared by hardware when the A/D conversion has completed.
0 = A/D conversion completed/not in progress

bit 0 **ADON:** A/D Enable bit
1 = A/D converter module is enabled
0 = A/D converter is shut-off and consumes no operating current

13.8 PWM Configuration

When configuring the Two-Phase PWM, care must be taken to avoid active output levels from the PH1 and PH2 pins before the PWM is fully configured. The following sequence is suggested before the TRISC register or any of the Two-Phase PWM control registers are first configured:

- Output inactive (OFF) levels to the PORTC RC1/AN5/C12IN1-/PH1 and RC4/C2OUT/PH2 pins.
- Clear TRISC bits 1 and 4 to configure the PH1 and PH2 pins as outputs.
- Configure the PWMCLK, PWMPH1, PWMPH2, and PWMCON1 registers.
- Configure the PWMCON0 register.

EXAMPLE 13-1: PWM SETUP EXAMPLE

```
;Example to configure PH1 as a free running PWM output using the SYNC output as the duty cycle
;termination feedback.
;This requires an external connection between the SYNC output and the comparator input.
;SYNC out = RB7 on pin 10
;C1 inverting input = RC2/AN6 on pin 14

;Configure PH1, PH2 and SYNC pins as outputs
;First, ensure output latches are low
    BCF     PORTC,1         ;PH1 low
    BCF     PORTC,4         ;PH2 low
    BCF     PORTB,7         ;SYNC low
;Configure the I/Os as outputs
    BANKSEL  TRISB
    BCF     TRISC,1         ;PH1 output
    BCF     TRISC,4         ;PH2 output
    BCF     TRISB,7         ;SYNC output
;PH1 shares its function with AN5
;Configure AN5 as digital I/O
    BCF     ANSEL0,5        ;AN5 is digital, all others default as analog
;Configure the PWM but don't enable PH1 or PH2 yet
    BANKSEL  PWMCLK
;PWM control setup
    MOVLW   B'00001100'     ;auto shutdown off, no blanking, SYNC on, PH1 and PH2 off
    MOVWF   PWMCON0         ;see data sheet page 93
;PWM clock setup
    MOVLW   B'00111101'     ;pwm_clk = Fosc, 30 clocks in PWM period
    MOVWF   PWMCLK          ;see data sheet page 94
;PH1 setup
    MOVLW   B'00101111'     ;non-inverted, terminate on C1, Start on clock 15
    MOVWF   PWMPH1          ;see data sheet page 95
;PH2 setup
    MOVLW   B'00110101'     ;non-inverted, terminate on C1, Start on clock 21
    MOVWF   PWMPH2          ;see data sheet page 96
;Configure Comparator 1
    MOVLW   B'10011110'     ;C1 on, internal, inverted, normal speed, +:C1VREF, -:AN6
    MOVWF   CM1CON0         ;see data sheet page 68
;Configure comparator voltage reference
    BANKSEL  VRCON
    MOVLW   B'10101100'     ;C1VREN on, low range, CVREF= VDD/2
    MOVWF   VRCON           ;see data sheet page 72
;Everything is setup at this point so now it is time to enable PH1
    BANKSEL  PWMCON0
    BSF     PWMCON0,PH1EN  ;enable PH1
;Module is running autonomously at this point
```

15.2.1 POWER-ON RESET

The on-chip POR circuit holds the chip in Reset until V_{DD} has reached a high enough level for proper operation. A minimum rise rate for V_{DD} is required. See **Section 19.0 "Electrical Specifications"** for details. If the BOR is enabled, the minimum rise rate specification does not apply. The BOR circuitry will keep the device in Reset until V_{DD} reaches V_{BOR} (see **Section 15.2.4 "Brown-Out Reset (BOR)"**)

The POR circuit, on this device, has a POR re-arm circuit. This circuit is designed to ensure a re-arm of the POR circuit if V_{DD} drops below a preset re-arming voltage (V_{PARM}) for at least the minimum required time. Once V_{DD} is below the re-arming point for the minimum required time, the POR Reset will reactivate and remain in Reset until V_{DD} returns to a value greater than V_{POR}. At this point, a 1 μs (typical) delay will be initiated to allow V_{DD} to continue to ramp to a voltage safely above V_{POR}.

When the device starts normal operation (exits the Reset condition), device operating parameters (i.e., voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

For additional information, refer to Application Note AN607, "*Power-up Trouble Shooting"* (DS00607).

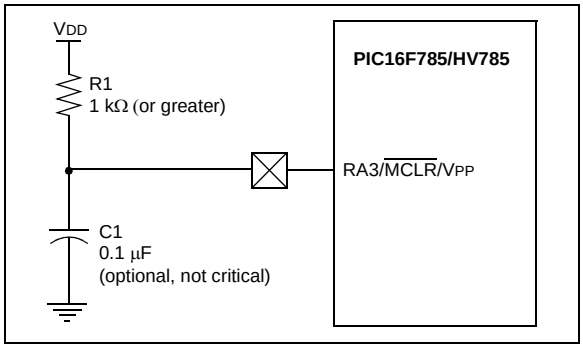
15.2.2 MASTER CLEAR ($\overline{MCLR}$)

PIC16F785/HV785 has a noise filter in the $\overline{MCLR}$ Reset path. The filter will detect and ignore small pulses.

It should be noted that a WDT Reset does not drive $\overline{MCLR}$ pin low.

The behavior of the ESD protection on the $\overline{MCLR}$ pin has been altered from earlier devices of this family. Voltages applied to the pin that exceed its specification can result in both $\overline{MCLR}$ Resets and excessive current beyond the device specification during the ESD event. For this reason, Microchip recommends that the $\overline{MCLR}$ pin no longer be tied directly to V_{DD}. The use of an RC network, as shown in Figure 15-1, is suggested.

FIGURE 15-2: RECOMMENDED $\overline{MCLR}$ CIRCUIT



An internal $\overline{MCLR}$ option is enabled by clearing the $\overline{MCLRE}$ bit in the Configuration Word. When cleared, $\overline{MCLR}$ is internally tied to V_{DD} and an internal Weak Pull-up is enabled for the $\overline{MCLR}$ pin. The V_{PP} function of the RA3/$\overline{MCLR}$/V_{PP} pin is not affected by selecting the internal $\overline{MCLR}$ option.

15.2.3 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 64 ms (nominal) time out on power-up only, from POR or Brown-out Reset. The Power-up Timer operates from the 31 kHz LFINTOSC oscillator. For more information, see **Section 3.4 "Internal Clock Modes"**. The chip is kept in Reset as long as PWRT is active. The PWRT delay allows the V_{DD} to rise to an acceptable level. A configuration bit, $\overline{PWRTE}$ can disable (if '1') or enable (if '0') the Power-up Timer. The Power-up Timer should be enabled when Brown-out Reset is enabled, although it is not required.

The Power-up Time Delay will vary from chip-to-chip and vary due to:

- V_{DD} variation
- Temperature variation
- Process variation

See DC parameters for details (**Section 19.0 "Electrical Specifications"**).

15.2.4 BROWN-OUT RESET (BOR)

The BOREN0 and BOREN1 bits in the Configuration Word select one of four BOR modes. Two modes have been added to allow software or hardware control of the BOR enable. When BOREN<1:0> = 01, the SBOREN bit of the PCON Register enables/disables the BOR allowing it to be controlled in software. By selecting BOREN<1:0>, the BOR is automatically disabled in Sleep to conserve power, and enabled on wake-up. In this mode, the SBOREN bit is disabled. See Register 15.2 for the Configuration Word definition.

If V_{DD} falls below V_{BOR} for greater than parameter (T_{BOR}), see **Section 19.0 "Electrical Specifications"**, the Brown-out situation will reset the device. This will occur regardless of the V_{DD} slew rate. A Reset is not assured if V_{DD} falls below V_{BOR} for less than parameter (T_{BOR}).

On any Reset (Power-on, Brown-out Reset, Watchdog, etc.), the chip will remain in Reset until V_{DD} rises above V_{BOR} (see Figure 15-3). The Power-up Timer will now be invoked, if enabled, and will keep the chip in Reset an additional 64 ms.

Note:	The Power-up Timer is enabled by the $\overline{PWRTE}$ bit in the Configuration Word.

If V_{DD} drops below V_{BOR} while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be re-initialized. Once V_{DD} rises above V_{BOR}, the Power-up Timer will execute a 64 ms Reset.

TABLE 15-5: INITIALIZATION CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	0001 1xxx	---1 --0x
$\overline{MCLR}$ Reset during normal operation	000h	000u uuuu	---u --uu
$\overline{MCLR}$ Reset during Sleep	000h	0001 0uuu	---u --uu
WDT Reset	000h	0000 uuuu	---u --uu
WDT Wake-up	PC + 1	uuu0 0uuu	---u --uu
Brown-out Reset	000h	0001 1uuu	---1 --u0
Interrupt Wake-up from Sleep	PC + 1(1)	uuu1 0uuu	---u --uu

Legend: u = unchanged, x = unknown, – = unimplemented bit, reads as '0'.

Note 1: When the wake-up is due to an interrupt and global enable bit GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

17.2 Instruction Descriptions

ADDLW	Add Literal and W
Syntax:	[*label*] ADDLW k
Operands:	$0 \le k \le 255$
Operation:	(W) + k → (W)
Status Affected:	C, DC, Z
Description:	The contents of the W register are added to the eight-bit literal 'k' and the result is placed in the W register.

ADDWF	Add W and f
Syntax:	[*label*] ADDWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) + (f) → (destination)
Status Affected:	C, DC, Z
Description:	Add the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

ANDLW	AND Literal with W
Syntax:	[*label*] ANDLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .AND. (k) → (W)
Status Affected:	Z
Description:	The contents of W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.

ANDWF	AND W with f
Syntax:	[*label*] ANDWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) .AND. (f) → (destination)
Status Affected:	Z
Description:	AND the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

BCF	Bit Clear f
Syntax:	[*label*] BCF f,b
Operands:	$0 \le f \le 127$ $0 \le b \le 7$
Operation:	0 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

BSF	Bit Set f
Syntax:	[*label*] BSF f,b
Operands:	$0 \le f \le 127$ $0 \le b \le 7$
Operation:	1 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is set.

COMF	Complement f
Syntax:	[*label*] COMF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	$(\bar{f}) \rightarrow$ (destination)
Status Affected:	Z
Description:	The contents of register 'f' are complemented. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f'.

DECF	Decrement f
Syntax:	[*label*] DECF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) - 1 $\rightarrow$ (destination)
Status Affected:	Z
Description:	Decrement register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

DECFSZ	Decrement f, Skip if 0
Syntax:	[*label*] DECFSZ f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) - 1 $\rightarrow$ (destination); skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are decremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', then a NOP is executed instead, making it a two-cycle instruction.

GOTO	Unconditional Branch
Syntax:	[*label*] GOTO k
Operands:	$0 \le k \le 2047$
Operation:	k $\rightarrow$ PC<10:0> PCLATH<4:3> $\rightarrow$ PC<12:11>
Status Affected:	None
Description:	GOTO is an unconditional branch. The eleven-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two-cycle instruction.

INCF	Increment f
Syntax:	[*label*] INCF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) + 1 $\rightarrow$ (destination)
Status Affected:	Z
Description:	The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

INCFSZ	Increment f, Skip if 0
Syntax:	[*label*] INCFSZ f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) + 1 $\rightarrow$ (destination), skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', a NOP is executed instead, making it a two-cycle instruction.

SUBLW **Subtract W from Literal**

Syntax: [*label*] SUBLW k

Operands: $0 \le k \le 255$

Operation: k - (W) → (W)

Status Affected: C, DC, Z

Encoding:

11	110x	kkkk	kkkk

Description: The W register is subtracted (2's complement method) from the eight-bit literal 'k'. The result is placed in the W register.

C = 1; result is positive or zero
C = 0; result is negative

SUBWF **Subtract W from f**

Syntax: [*label*] SUBWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) - (W) → (dest)

Status Affected: C, DC, Z

Encoding:

00	0010	dfff	ffff

Description: Subtract (2's complement method) W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

C = 1; result is positive or zero
C = 0; result is negative

SWAPF **Swap Nibbles in f**

Syntax: [*label* SWAPF f,d]

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f<3:0>) → (dest<7:4>),
(f<7:4>) → (dest<3:0>)

Status Affected: None

Encoding:

00	1110	dfff	ffff

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in W register. If 'd' is '1', the result is placed in register 'f'.

TRIS **Load TRIS Register**

Syntax: [*label*] TRIS f

Operands: $5 \le f \le 6$

Operation: (W) → TRIS register f;

Status Affected: None

Encoding:

00	0000	0110	0fff

Description: The instruction is supported for code compatibility with the PIC16C5X products. Since TRIS registers are readable and writable, the user can directly address them.

Words: 1

Cycles: 1

Example:

To maintain upward compatibility with future PIC® products, do not use this instruction.

XORLW **Exclusive OR Literal with W**

Syntax: [*label*] XORLW k

Operands: $0 \le k \le 255$

Operation: (W) .XOR. k → (W)

Status Affected: Z

Encoding:

11	1010	kkkk	kkkk

Description: The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.

FIGURE 19-3: EXTERNAL CLOCK TIMING

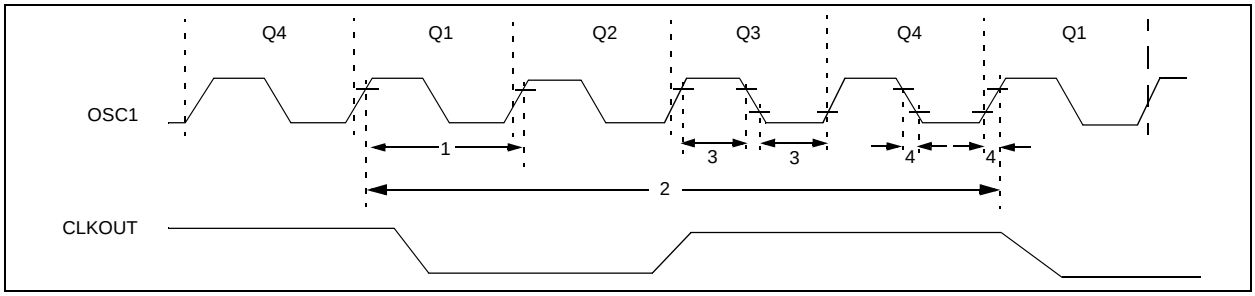


TABLE 19-1: EXTERNAL CLOCK TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	FOSC	External CLKIN Frequency(1)	—	32.768	—	kHz	LP mode (complementary input only)
			DC	—	4	MHz	XT mode
			DC	—	20	MHz	HS mode
			DC	—	20	MHz	EC mode
		Oscillator Frequency(1)	—	32.768	—	kHz	LP Osc mode
			—	4	—	MHz	INTOSC mode
			DC	—	4	MHz	RC Osc mode
			0.1	—	4	MHz	XT Osc mode
			1	—	20	MHz	HS Osc mode
1	TOSC	External CLKIN Period(1)	—	0.3052	—	µs	LP mode (complementary input only)
			50	—	∞	ns	HS Osc mode
			50	—	∞	ns	EC Osc mode
			250	—	∞	ns	XT Osc mode
		Oscillator Period(1)	—	0.3052	—	µs	LP Osc mode
			—	250	—	ns	INTOSC mode
			250	—	—	ns	RC Osc mode
			250	—	10,000	ns	XT Osc mode
			50	—	1,000	ns	HS Osc mode
2	TCY	Instruction Cycle Time(1)	200	TCY	DC	ns	TCY = 4/FOSC
3	TosL, TosH	External CLKIN (OSC1) High External CLKIN Low	2*	—	—	µs	LP oscillator, TOSC L/H duty cycle
			20*	—	—	ns	HS oscillator, TOSC L/H duty cycle
			100 *	—	—	ns	XT oscillator, TOSC L/H duty cycle
4	TosR, TosF	External CLKIN Rise External CLKIN Fall	—	—	50*	ns	LP oscillator
			—	—	25*	ns	XT oscillator
			—	—	15*	ns	HS oscillator

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at 'min' values with an external clock applied to OSC1 pin. When an external clock input is used, the 'max' cycle time limit is 'DC' (no clock) for all devices.

FIGURE 20-2: MAXIMUM IDD vs. FOSC OVER VDD (EC MODE)

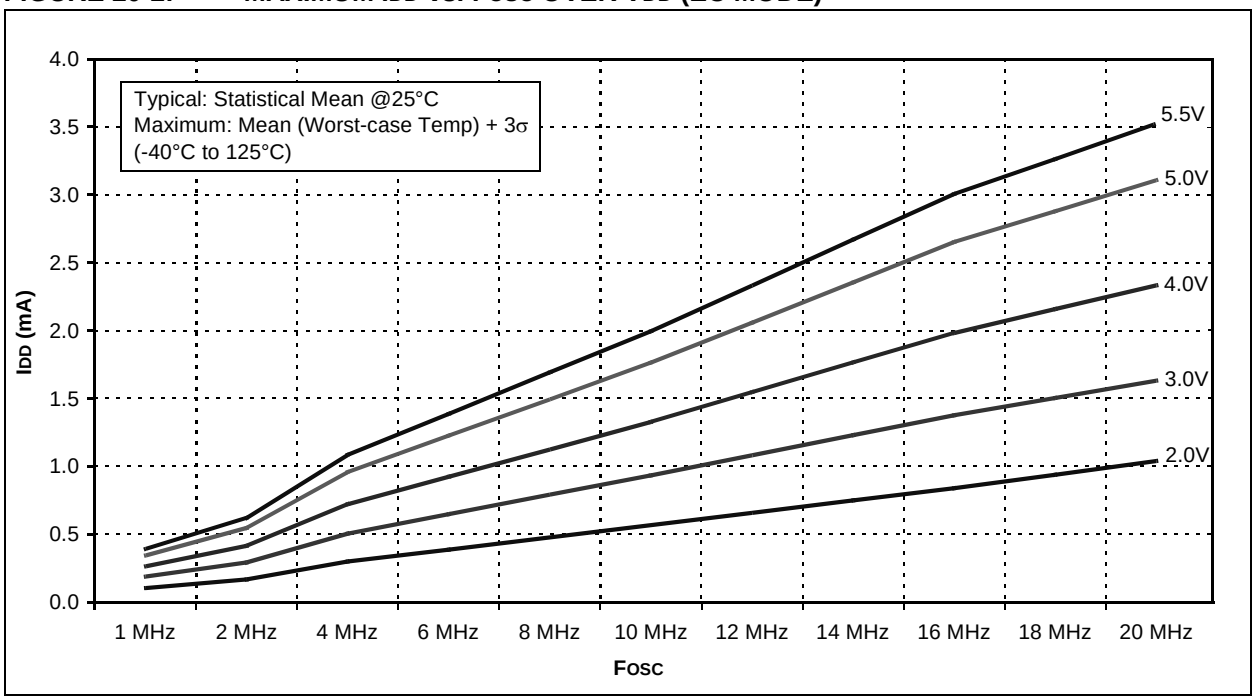


FIGURE 20-3: TYPICAL IDD vs. FOSC OVER VDD (HS MODE)

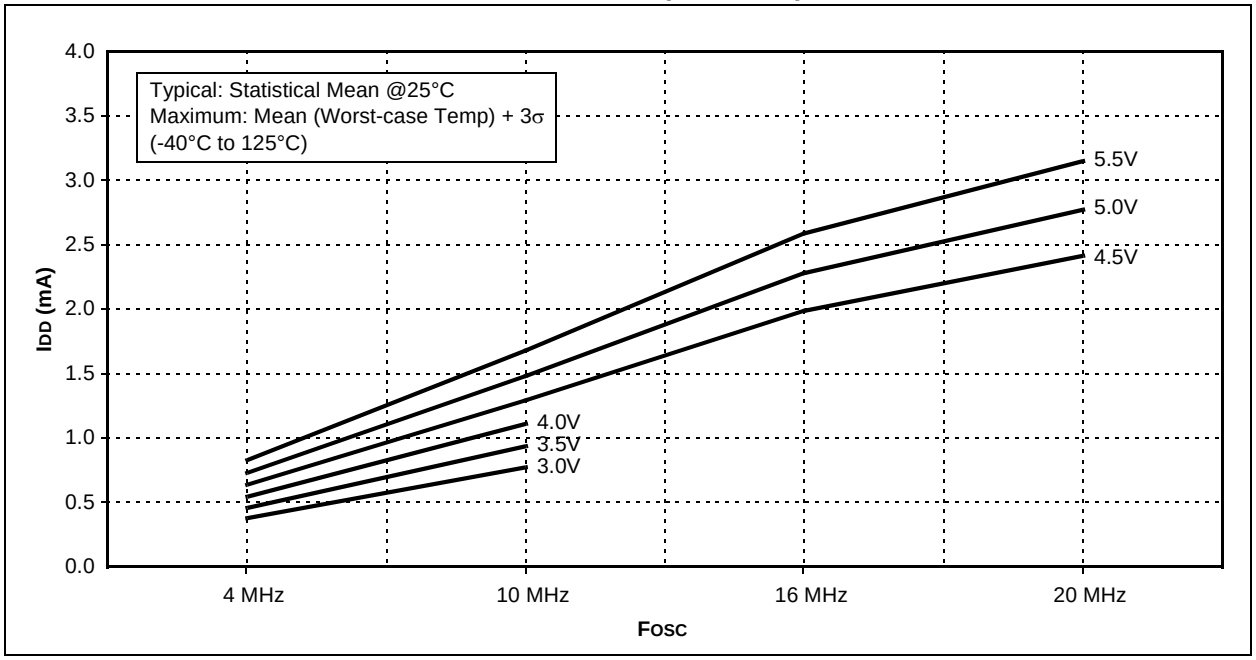


FIGURE 20-38: TYPICAL VP6 REFERENCE VOLTAGE OVER TEMPERATURE (3V)

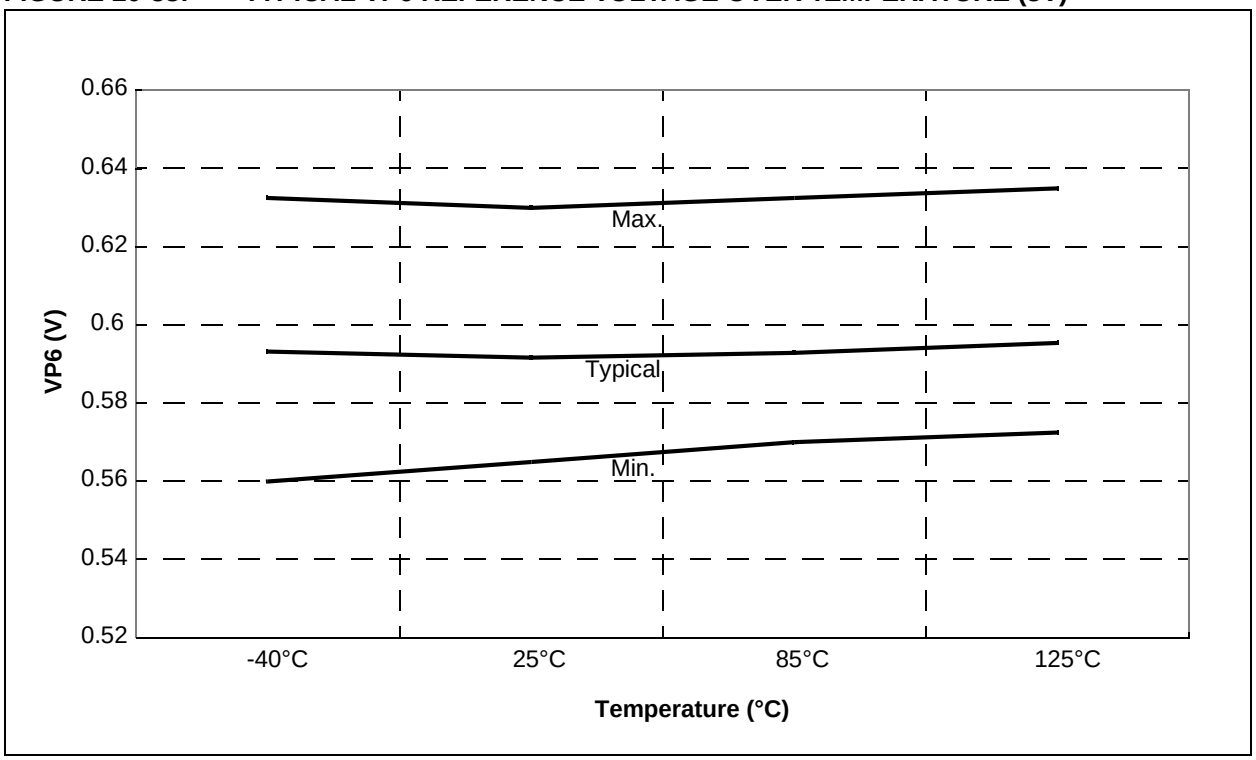
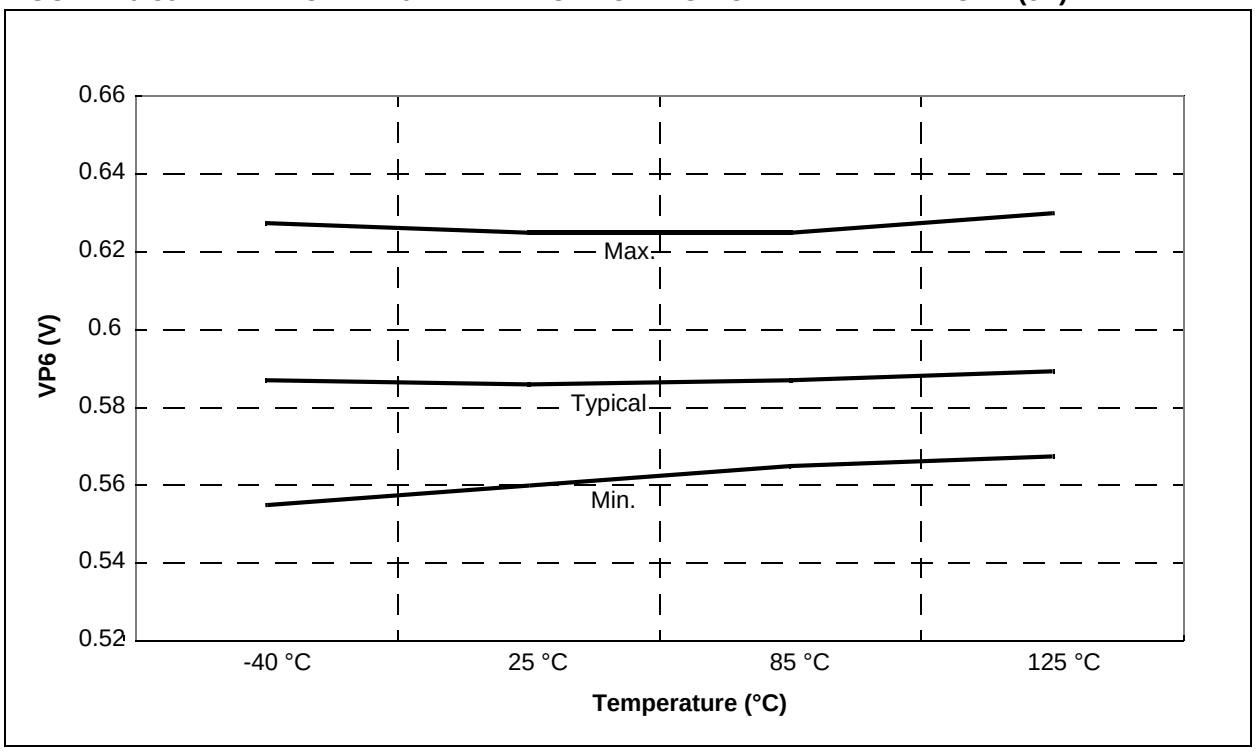
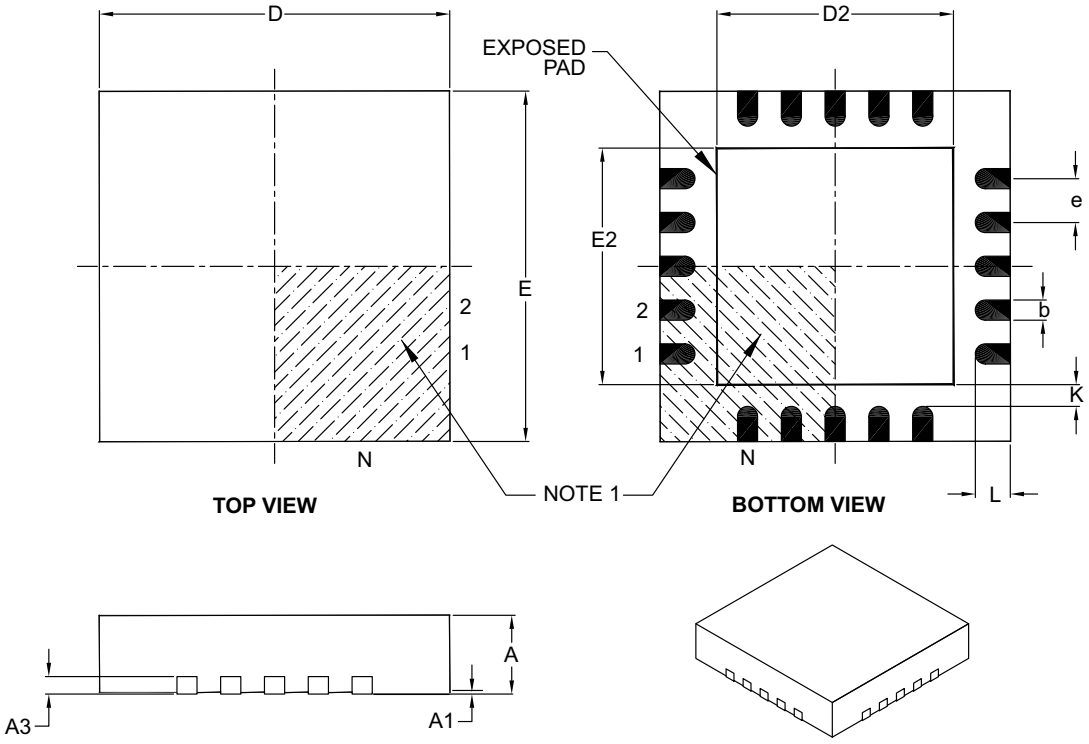


FIGURE 20-39: TYPICAL VP6 REFERENCE VOLTAGE OVER TEMPERATURE (5V)



20-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.60	2.70	2.80
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.60	2.70	2.80
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-126B