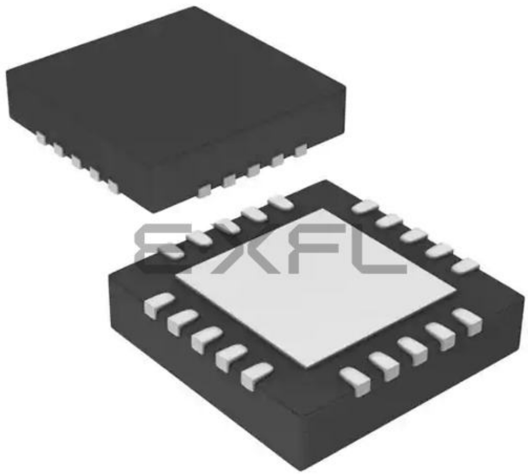

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Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 14x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	20-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16hv785-e-ml

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2.2.2.2 OPTION_REG Register

The Option register is a readable and writable register, which contains various control bits to configure the TMR0/WDT prescaler, the external RA2/INT interrupt, the TMR0 and the weak pull-ups on PORTA.

> **Note:** To achieve a 1:1 prescaler assignment for TMR0, assign the prescaler to the WDT by setting PSA bit to '1' in the OPTION Register. See **Section 5.4 "Prescaler"**.

REGISTER 2-2: OPTION_REG: OPTION REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RAPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **$\overline{\text{RAPU}}$:** PORTA Pull-up Enable bit
1 = PORTA pull-ups are disabled
0 = PORTA pull-ups are enabled by individual port latch values in WPUA register

bit 6 **INTEDG:** Interrupt Edge Select bit
1 = Interrupt on rising edge of RA2/AN2/T0CKI/INT/C1OUT pin
0 = Interrupt on falling edge of RA2/AN2/T0CKI/INT/C1OUT pin

bit 5 **T0CS:** TMR0 Clock Source Select bit
1 = Transition on RA2/AN2/T0CKI/INT/C1OUT pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4 **T0SE:** TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on RA2/AN2/T0CKI/INT/C1OUT pin
0 = Increment on low-to-high transition on RA2/AN2/T0CKI/INT/C1OUT pin

bit 3 **PSA:** Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate(1)
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

Note 1: A dedicated 16-bit WDT postscaler is available for the PIC16F785/HV785. See **Section 15.5 "Watchdog Timer (WDT)"** for more information.

REGISTER 4-2: TRISA: PORTA TRI-STATE REGISTER

U-0	U-0	R/W-1	R/W-1	R-1	R/W-1	R/W-1	R/W-1
—	—	TRISA5(2)	TRISA4(2)	TRISA3(1)	TRISA2	TRISA1	TRISA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **TRISA<5:0>:** PORTA Tri-State Control bit(1), (2)
1 = PORTA pin configured as an input (tri-stated)
0 = PORTA pin configured as an output

bit 0 **C:** Carry/$\overline{\text{Borrow}}$ bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)(1)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: TRISA<3> always reads ‘1’.
2: TRISA<5:4> always reads ‘1’ in XT, HS and LP OSC modes.

4.2 Additional Pin Functions

Every PORTA pin on the PIC16F785/HV785 has an interrupt-on-change option and a weak pull-up option. The next three sections describe these functions.

4.2.1 WEAK PULL-UPS

Each of the PORTA pins has an individually configurable internal weak pull-up. Control bits WPUAx enable or disable each pull-up. Refer to Register 4-3. Each weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset by the $\overline{\text{RAPU}}$ bit in the (OPTION Register. The weak pull-up on RA3 is automatically enabled when RA3 is configured as $\overline{\text{MCLR}}$.

REGISTER 4-3: WPUA: WEAK PULL-UP REGISTER

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	WPUA5(4)	WPUA4(4)	WPUA3(3)	WPUA2	WPUA1	WPUA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **WPUA<5:0>:** Weak Pull-up Register bits
1 = Pull-up enabled
0 = Pull-up disabled

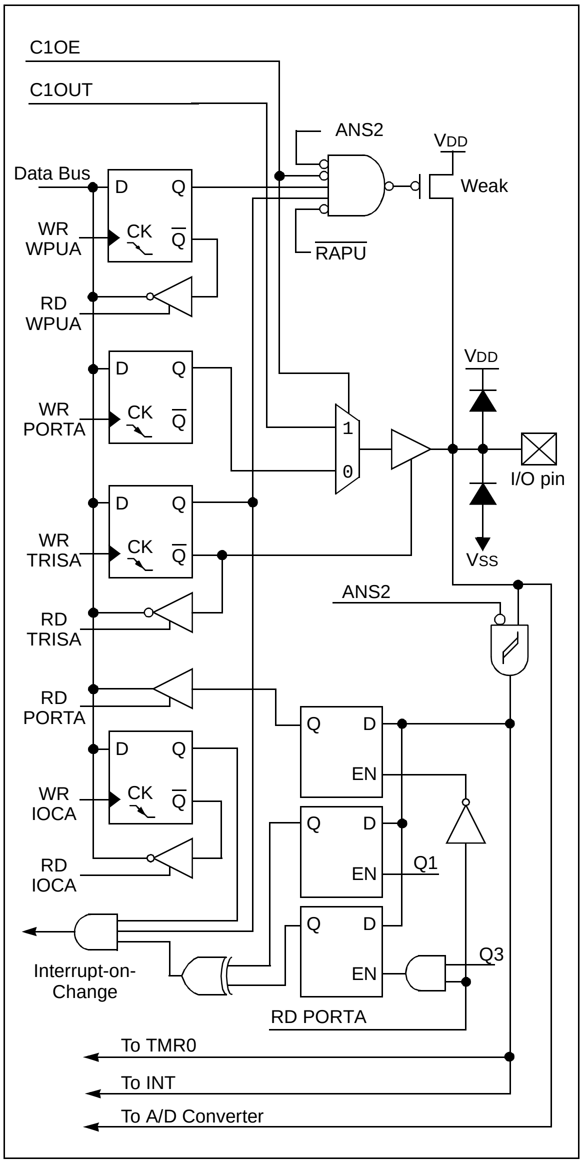
Note 1: Global $\overline{\text{RAPU}}$ must be enabled for individual pull-ups to be enabled.
2: The weak pull-up device is automatically disabled if the pin is in Output mode (TRISA = 0).
3: The RA3 pull-up is automatically enabled when configured as $\overline{\text{MCLR}}$ in the Configuration Word.
4: WPUA<5:4> always reads ‘1’ in XT, HS and LP OSC modes.

4.2.3.3 RA2/AN2/T0CKI/INT/C1OUT

Figure 4-3 shows the diagram for this pin. The RA2 pin is configurable to function as one of the following:

- General purpose I/O
- Analog input for the A/D
- Clock input for TMR0
- External edge triggered interrupt
- Digital output from Comparator 1

FIGURE 4-3: BLOCK DIAGRAM OF RA2

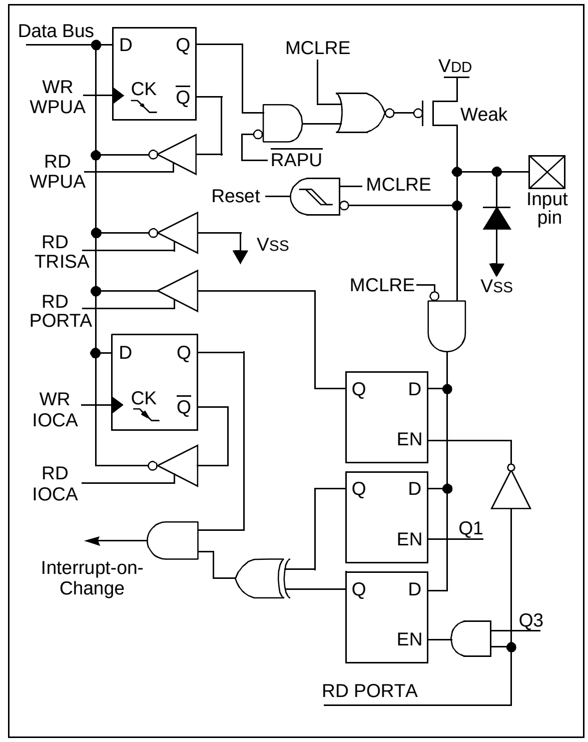


4.2.3.4 RA3/$\overline{\text{MCLR}}$/VPP

Figure 4-4 shows the diagram for this pin. The RA3 pin is configurable to function as one of the following:

- General purpose input
- Master Clear Reset with weak pull-up

FIGURE 4-4: BLOCK DIAGRAM OF RA3



5.3 Using Timer0 with an External Clock

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI, with the internal phase clocks, is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks. Therefore, it is necessary for T0CKI to be high for at least 2TOSC (and a small RC delay of 20 ns) and low for at least 2TOSC (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

5.4 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer. For simplicity, this counter will be referred to as "prescaler" throughout this Data Sheet. The prescaler assignment is controlled in software by the control bit PSA of the OPTION Register. Clearing the PSA bit will assign the prescaler to Timer0. Prescale values are selectable via the PS<2:0> bits of the OPTION Register.

The prescaler is not readable or writable. When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., `CLRF 1, MOVWF 1, BSF 1,x....etc.`) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the Watchdog Timer.

5.4.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed "on the fly" during program execution). To avoid an unintended device Reset, the following instruction sequence (Example 5-1 and Example 5-2) must be executed when changing the prescaler assignment between Timer0 and WDT.

EXAMPLE 5-1: CHANGING PRESCALER (TIMER0→WDT)

```
BCF     STATUS,RP0      ;Bank 0
BCF     STATUS,RP1      ;
CLRWDT                  ;Clear WDT
CLRF    TMR0            ;Clear TMR0 and
                        ; prescaler
BSF     STATUS,RP0      ;Bank 1

MOVLW   b'00101111'     ;Required if desired
MOVWF   OPTION_REG      ; PS2:PS0 is
CLRWDT                  ; 000 or 001
                        ;
MOVLW   b'00101xxx'     ;Set postscaler to
MOVWF   OPTION_REG      ; desired WDT rate
BCF     STATUS,RP0      ;Bank 0
```

To change prescaler from the WDT to the TMR0 module, use the sequence shown in Example 5-2. This precaution must be taken even if the WDT is disabled.

EXAMPLE 5-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT                  ;Clear WDT and
                        ; prescaler
BSF     STATUS,RP0      ;Bank 1
BCF     STATUS,RP1      ;

MOVLW   b'xxxx0xxx'     ;Select TMR0,
                        ; prescale, and
                        ; clock source
MOVWF   OPTION_REG      ;
BCF     STATUS,RP0      ;Bank 0
```

TABLE 5-1: REGISTERS ASSOCIATED WITH TIMER0

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSEL0	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
OPTION_REG	$\overline{\text{RAPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
TMR0	Timer0 Module Register								xxxx xxxx	uuuu uuuu
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111

Legend: – = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Timer0 module.

6.5 Timer1 Operation in Asynchronous Counter Mode

If control bit $\overline{\text{T1SYNC}}$ of the T1CON Register is set, the external clock input is not synchronized. The timer continues to increment asynchronous to the internal phase clocks. The timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (**Section 6.5.1 "Reading and Writing Timer1 in Asynchronous Counter Mode"**).

Note:	The ANSEL0 (91h) register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.

6.5.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the timer register.

6.6 Timer1 Oscillator

A crystal oscillator circuit is built-in between pins OSC1 (input) and OSC2 (amplifier output). It is enabled by setting control bit T1OSCEN of the T1CON Register. The oscillator is a low power oscillator rated for 32.768 kHz. It will continue to run during Sleep. It is primarily intended for a 32.768 kHz tuning fork crystal.

The Timer1 oscillator is shared with the system LP oscillator. Thus, Timer1 can use this mode only when the primary system clock is also the LP oscillator or is derived from the internal oscillator. As with the system LP oscillator, the user must provide a software time delay to ensure proper oscillator start-up.

Sleep mode will not disable the system clock when the system clock and Timer1 share the LP oscillator.

TRISA<5> and TRISA<4> bits are set when the Timer1 oscillator is enabled. RA5 and RA4 read as '0' and TRISA<5> and TRISA<4> bits read as '1'.

Note:	The oscillator requires a start-up and stabilization time before use. Thus, T1OSCEN should be set and a suitable delay observed prior to enabling Timer1.

6.7 Timer1 Operation During Sleep

Timer1 can only operate during Sleep when setup in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To setup the timer to wake the device:

- Timer1 of the T1CON Register must be on
- TMR1IE bit of the PIE1 Register must be set
- PEIE bit of the INTCON Register must be set

The device will wake-up on an overflow. If the GIE bit of the INTCON Register is set, the device will wake-up and jump to the Interrupt Service Routine (0004h) on an overflow. If the GIE bit is clear, execution will continue with the next instruction.

TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER1

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSEL0	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111
CM2CON1	MC1OUT	MC2OUT	—	—	—	—	T1GSS	C2SYNC	00-- --10	00-- --10
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
PIE1	EEIE	ADIE	CCP1IE	C2IE	C1IE	OSFIE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	EEIF	ADIF	CCP1IF	C2IF	C1IF	OSFIF	TMR2IF	TMR1IF	0000 0000	0000 0000
T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	0000 0000	uuuu uuuu
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu

Legend: – x = unknown, u = unchanged, – = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.

9.1.2.2 Control Register CM2CON1

Comparator C2 has one additional feature: its output can be synchronized to the Timer1 clock input. Setting C2SYNC of the CM2CON1 Register synchronizes the output of Comparator 2 to the falling edge of the Timer1 clock input (see Figure 9-2 and Register 9-3).

The CM2CON1 register also contains mirror copies of both comparator outputs, MC1OUT and MC2OUT of the CM2CON1 Register. The ability to read both outputs simultaneously from a single register eliminates the timing skew of reading separate registers.

Note:	Obtaining the status of C1OUT or C2OUT by reading CM2CON1 does not affect the comparator interrupt mismatch registers.

REGISTER 9-3: CM2CON1: COMPARATOR C2 CONTROL REGISTER 1

R-0	R-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0
MC1OUT	MC2OUT	—	—	—	—	T1GSS	C2SYNC
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7	**MC1OUT**: Mirror Copy of C1OUT bit (CM1CON0<6>)
bit 6	**MC2OUT**: Mirror Copy of C2OUT bit (CM2CON0<6>)
bit 5-2	**Unimplemented:** Read as ‘0’
bit 1	**T1GSS**: Timer1 Gate Source Select bit 1 = Timer1 gate source is RA4/AN3/T1G/OSC2/CLKOUT 0 = Timer1 gate source is SYNCC2OUT.
bit 0	**C2SYNC**: C2 Output Synchronous Mode bit 1 = C2 output is synchronous to falling edge of TMR1 clock 0 = C2 output is asynchronous

10.0 VOLTAGE REFERENCES

There are two voltage references available in the PIC16F785/HV785: The voltage referred to as the comparator reference (CVREF) is a variable voltage based on VDD; The voltage referred to as the VR reference (VR) is a fixed voltage derived from a stable band gap source. Each source may be individually routed internally to the comparators or output, buffered or unbuffered, on the RA1/AN1/C12IN0-/VREF/ICSPCLK pin.

10.1 Comparator Reference

The comparator module also allows the selection of an internally generated voltage reference for one of the comparator inputs. The VRCON register (Register 10-1) controls the voltage reference module shown in Figure 10-1.

10.1.1 CONFIGURING THE VOLTAGE REFERENCE

The voltage reference can output 32 distinct voltage levels, 16 in a high range and 16 in a low range.

The following equation determines the output voltages:

EQUATION 10-1: CVREF OUTPUT VOLTAGE

$V_{RR} = 1$ (low range):

$$CV_{REF} = VR<3:0> \times V_{DD}/24$$

$V_{RR} = 0$ (high range):

$$CV_{REF} = (V_{DD}/4) + (VR<3:0> \times V_{DD}/32)$$

10.1.2 VOLTAGE REFERENCE ACCURACY/ERROR

The full range of VSS to VDD cannot be realized due to the construction of the module. The transistors on the top and bottom of the resistor ladder network (Figure 10-1) keep CVREF from approaching VSS or VDD. The exception is when the module is disabled by clearing all CVROE, C1VREN and C2VREN bits. When disabled with VR<3:0> = 0000 and VRR = 1 the reference voltage will be VSS. This allows the comparators to detect a zero-crossing and not consume CVREF module current.

The voltage reference is VDD derived and therefore, the CVREF output changes with fluctuations in VDD. The tested absolute accuracy of the comparator voltage reference can be found in Table 19-8.

12.2 A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 12-4. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD), see Figure 12-4. **The maximum recommended impedance for analog sources is 10 k**Ω. As the impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (changed), this acquisition must be done before the conversion can be started.

To calculate the minimum acquisition time, Equation 12-1 may be used. This equation assumes that 1/2 LSb error is used (1024 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

EQUATION 12-1: ACQUISITION TIME EXAMPLE

Assumptions: $Temperature = 50°C \text{ and external impedance of } 10k\Omega\ 5.0V\ V_{DD}$

$$
\begin{aligned}
T_{ACQ} &= \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient} \\
&= T_{AMP} + T_C + T_{COFF} \\
&= 5\mu s + T_C + [(\text{Temperature} - 25°C)(0.05\mu s/°C)]
\end{aligned}
$$

The value for Tc can be approximated with the following equations:

$$V_{APPLIED}\left(1 - \frac{1}{2047}\right) = V_{CHOLD} \qquad \text{;[1] Vchold charged to within 1/2 lsb}$$

$$V_{APPLIED}\left(1 - e^{\frac{-T_C}{RC}}\right) = V_{CHOLD} \qquad \text{;[2] Vchold charge response to Vapplied}$$

$$V_{APPLIED}\left(1 - e^{\frac{-T_C}{RC}}\right) = V_{APPLIED}\left(1 - \frac{1}{2047}\right) \qquad \text{;Combining [1] and [2]}$$

Solving for Tc:

$$
\begin{aligned}
T_C &= -C_{HOLD}(R_{IC} + R_{SS} + R_S)\ \ln(1/2047) \\
&= -10pF(1k\Omega + 7k\Omega + 10k\Omega)\ \ln(0.0004885) \\
&= 1.37\mu s
\end{aligned}
$$

Therefore:

$$
\begin{aligned}
T_{ACQ} &= 5\mu s + 1.37\mu s + [(50°C - 25°C)(0.05\mu s/°C)] \\
&= 7.62\mu s
\end{aligned}
$$

Note 1: The reference voltage (VREF) has no effect on the equation, since it cancels itself out.
2: The charge holding capacitor (CHOLD) is not discharged after each conversion.
3: The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.

REGISTER 13-2: PWMCLK: PWM CLOCK CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWMASE	PWMP1	PWMP0	PER4	PER3	PER2	PER1	PER0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **PWMASE:** PWM Auto-Shutdown Event Status bit
0 = PWM outputs are operating
1 = A shutdown event has occured. PWM outputs are inactive.

bit 6-5 **PWMP<1:0>:** PWM Clock Prescaler bits
00 = pwm_clk = FOSC ÷ 1
01 = pwm_clk = FOSC ÷ 2
10 = pwm_clk = FOSC ÷ 4
11 = pwm_clk = FOSC ÷ 8

bit 4-0 **PER<4:0>:** PWM Period bits
00000 = Not used. (Period = 1/pwm_clk)
00001 = Period = 2/pwm_clk2
0•••• = •••
01111 = Period = 16/pwm_clk
10000 = Period = 17/pwm_clk
1•••• = •••
11110 = Period = 31/pwm_clk
11111 = Period = 32/pwm_clk

13.9 Complementary Output Mode

The Two-Phase PWM module may be configured to operate in a Complementary Output mode where PH1 and PH2 are always 180 degrees out-of-phase (see Figure 13-5). Three complementary modes are available and are selected by the COMOD<1:0> bits in the PWMCON1 register (see Register 13-5). The difference between the modes is the method by which the PH1 and PH2 outputs switch from the active to the inactive state during the PWM period.

In Complementary mode, there are three methods by which the duty cycle can be controlled. These modes are selected with the COMOD<1:0> bits (see Register 13-5). In each of these modes, the duty cycle is started when the pwm_count = PWMPH1<4:0> and terminates on one of the following:

- Feedback through C1 or C2
- When the pwm_count equals PWMPH1<4:0>
- Combined feedback and pwm_count match

When COMOD<1:0> = `01`, the duty cycle is controlled only by feedback through comparator C1 or C2. In this mode, the active drive cycle starts when pwm_count equals PWMPH1<4:0> and terminates when comparator C1's output goes high (if enabled by PWMPH1<5> = `1`) or when comparator C2 output goes high (if enabled by PWMPH1<6> = `1`).

When COMOD<1:0> = `10`, the duty cycle is controlled only by the PWM Phase counter. In this mode, the active drive cycle starts when the pwm_count equals PWMPH1<4:0> and terminates when the pwm_count equals PWMPH2<4:0>. For example, free running 50% duty cycle can be accomplished by setting COMOD<1:0> = `10` and choosing appropriate values for PWMPH1<4:0> and PWMPH2<4:0>.

When COMOD<1:0> = `11`, the duty cycle is controlled by the phase counter or feedback through comparator C1 or C2. For example, in this mode, the maximum duty cycle is determined by the values of PWMPH1<4:0> (duty cycle start) and PWMPH2<4:0> (duty cycle end). The duty cycle can be terminated earlier than the maximum by feedback through comparator C1 or C2.

13.9.1 DEAD BAND CONTROL

The Complementary Output mode facilitates driving series connected MOSFET drivers by providing dead band drive timing between each phase output (see Figure 13-6). Dead band times are selectable by the CMDLY<4:0> bits of the PWMCON1 register. Delays from 0 to 155 nanoseconds (typical) with a resolution of 5 nanoseconds (typical) are available.

13.9.2 OVERLAP CONTROL

Overlap timing can be accomplished by configuring the Complementary mode for the desired output polarity and overlap time (as dead time) then swapping the output connections and inverting the outputs. For example, to configure a complementary drive for 55 ns of overlap and an active-high drive output on PH1 and an active-low drive output on PH2, set the PWM control registers as follows:

- Connect PH1 driver to PH2 output
- Connect PH2 driver to PH1 output
- Initialize PORTC<1> to `1` (PH2 driver off)
- Initialize PORTC<4> to `0` (PH1 driver off)
- Set TRISC<1,4> to `0` for output
- Set PWMPH1<POL> to `1` (Inverted PH1)
- Set PWMPH2<POL> to `1` (Non-Inverted PH2)
- Set PWMCON1 for 55 ns delay and desired termination (comparator, count or both)
- Set PWMCON0 desired SYNC and auto-shutdown configuration and to enable PH1 and PH2

13.9.3 SHUTDOWN IN COMPLEMENTARY MODE

During shutdown the PH1 and PH2 complementary outputs are forced to their inactive states (see Figure 13-5). When shutdown ceases the PWM outputs revert to their start-up states for the first cycle which is PH1 inactive (output undriven) and PH2 active (output driven).

15.0 SPECIAL FEATURES OF THE CPU

The PIC16F785/HV785 has a host of features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving features and offer code protection.

These features are:

- Reset:
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Brown-out Reset (BOR)
- Interrupts
- Watchdog Timer (WDT)
- Oscillator selection
- Sleep
- Code protection
- ID Locations
- In-Circuit Serial Programming™ (ICSP™)

The PIC16F785/HV785 has two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 64 ms (nominal) on power-up only, designed to keep the part in Reset while the power supply stabilizes. There is also circuitry to reset the device if a brown-out occurs, which can use the Power-up Timer to provide at least a 64 ms Reset. With these three functions on-chip, most applications need no external Reset circuitry.

The Sleep mode is designed to offer a very low-current Power-down mode. The user can wake-up from Sleep through an external Reset, Watchdog Timer Wake-up or interrupt.

Several oscillator options are also made available to allow the part to fit the application. The INTOSC option saves system cost, while the LP crystal option saves power. A set of configuration bits are used to select various options (see Register 15.2).

15.1 Configuration Bits

The configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1') to select various device configurations as shown in Register 15.2. These bits are mapped in program memory location 2007h.

Note:	Address 2007h is beyond the user program memory space. It belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming. See "*PIC16F785/HV785 Memory Programming Specification*" (DS41237) for more information.

15.2 Reset

The PIC16F785/HV785 differentiates between various kinds of Reset:

- Power-on Reset (POR)
- WDT Reset during normal operation
- WDT Reset during Sleep
- $\overline{\text{MCLR}}$ Reset during normal operation
- $\overline{\text{MCLR}}$ Reset during Sleep
- Brown-out Reset (BOR)

Some registers are not affected in any Reset condition; their status is unknown on POR and unchanged in any other Reset. Most other registers are reset to a “Reset state” on:

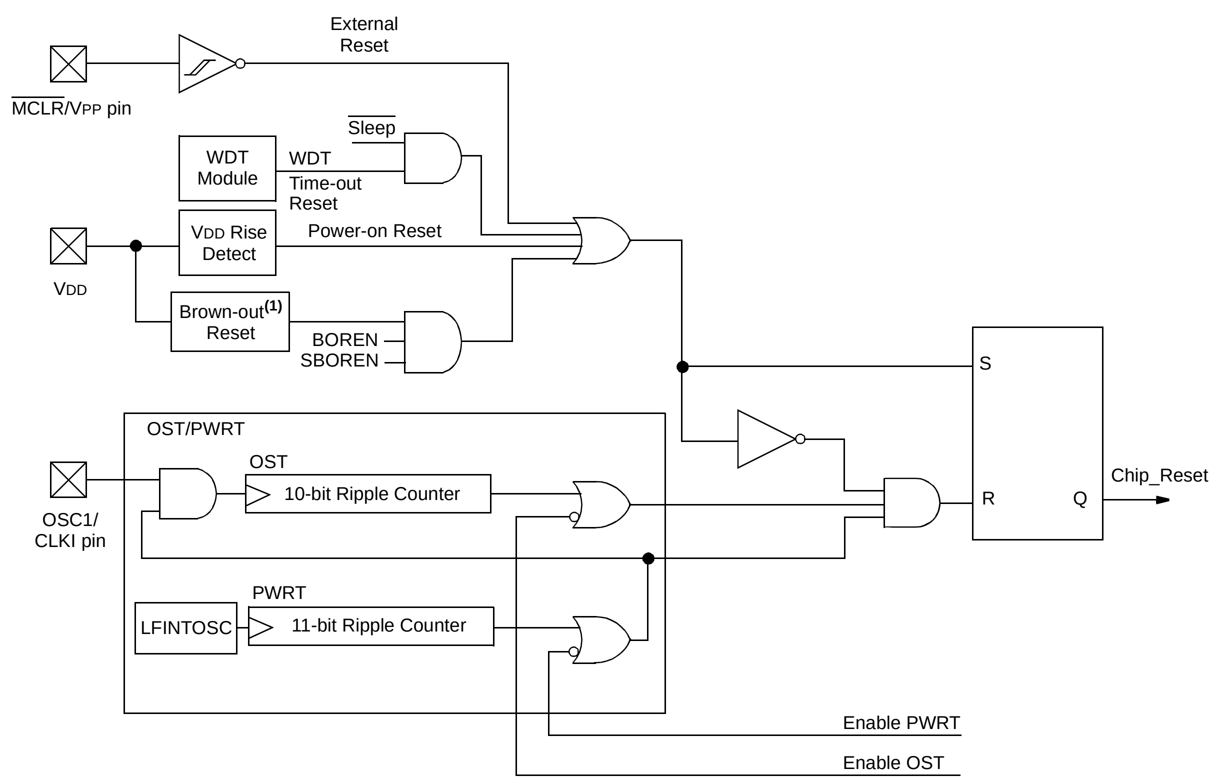
- Power-on Reset
- $\overline{\text{MCLR}}$ Reset
- $\overline{\text{MCLR}}$ Reset during Sleep
- WDT Reset
- Brown-out Reset (BOR)

They are not affected by a WDT wake-up since this is viewed as the resumption of normal operation. $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are set or cleared differently in different Reset situations, as indicated in Table 15-2. These bits are used in software to determine the nature of the Reset. See Table 15-4 for a full description of Reset states of all registers.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 15-1.

The $\overline{\text{MCLR}}$ Reset path has a noise filter to detect and ignore small pulses. See **Section 19.0 “Electrical Specifications”** for pulse width specifications.

FIGURE 15-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



Note 1: Refer to the Configuration Word register (Register 15.2).

TABLE 15-4: INITIALIZATION CONDITION FOR REGISTERS

Register	Address	Power-on Reset	MCLR Reset WDT Reset Brown-out Reset[1]	Wake-up from Sleep through interrupt Wake-up from Sleep through WDT Time-out
W	—	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h/80h	xxxx xxxx	xxxx xxxx	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h/82h	0000 0000	0000 0000	PC + 1[3]
STATUS	03h/83h	0001 1xxx	000q quuu[4]	uuuq quuu[4]
FSR	04h/84h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	05h	--x0 x000[6]	--u0 u000[7]	--uu uuuu
PORTB	06h	xx00 ----[6]	uu00 ----[7]	uuuu ----
PORTC	07h	00xx 0000[6]	00uu uuuu[7]	uuuu uuuu
PCLATH	0Ah/8Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh/8Bh	0000 0000	0000 0000	uuuu uuuu[2]
PIR1	0Ch	0000 0000	0000 0000	uuuu uuuu[2]
TMR1L	0Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	0Fh	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	10h	0000 0000	uuuu uuuu	uuuu uuuu
TMR2	11h	0000 0000	0000 0000	uuuu uuuu
T2CON	12h	-000 0000	-000 0000	-uuu uuuu
CCPR1L	13h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR1H	14h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CON	15h	--00 0000	--00 0000	--uu uuuu
WDTCON	18h	---0 1000	---0 1000	---u uuuu
ADRESH	1Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON0	1Fh	0000 0000	0000 0000	uuuu uuuu
OPTION_REG	81h	1111 1111	1111 1111	uuuu uuuu
TRISA	85h	--11 1111	--11 1111	--uu uuuu
TRISB	86h	1111 ----	1111 ----	uuuu ----
TRISC	87h	1111 1111	1111 1111	uuuu uuuu
PIE1	8Ch	0000 0000	0000 0000	uuuu uuuu
PCON	8Eh	---1 --0x	---u --uq[1,5]	---u --uu
OSCCON	8Fh	-110 q000	-110 q000	-uuu uuuu
OSCTUNE	90h	---0 0000	---u uuuu	---u uuuu
ANSEL0	91h	1111 1111	1111 1111	uuuu uuuu
PR2	92h	1111 1111	1111 1111	1111 1111
ANSEL1	93h	---- 1111	---- 1111	---- uuuu
WPUA	95h	--11 1111	--11 1111	--uu uuuu
IOCA	96h	--00 0000	--00 0000	--uu uuuu
REFCON	98h	--00 000-	--00 000-	--uu uuu-

Legend: u = unchanged, x = unknown, – = unimplemented bit, reads as ‘0’, q = value depends on condition.

Note 1: If V_{DD} goes too low, Power-on Reset will be activated and registers will be affected differently.
2: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).
3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).
4: See Table 15-5 for Reset value for specific condition.
5: If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.
6: Analog channels read 0 but data latches are unknown.
7: Analog channels read 0 but data latches are unchanged.

15.3 Interrupts

The PIC16F785/HV785 has 11 sources of interrupt:

- External Interrupt RA2/INT
- TMR0 Overflow Interrupt
- PORTA Change Interrupt
- 2 Comparator Interrupts
- A/D Interrupt
- Timer1 Overflow Interrupt
- Timer2 Match Interrupt
- EEPROM Data Write Interrupt
- Fail-Safe Clock Monitor Interrupt
- CCP Interrupt

The Interrupt Control register (INTCON) and Peripheral Interrupt register (PIR1) record individual interrupt requests in flag bits. The INTCON register also has individual and global interrupt enable bits.

A Global Interrupt Enable bit, GIE of the INTCON Register enables (if set) all unmasked interrupts, or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in INTCON register and PIE1 register. GIE is cleared on Reset.

The Return from Interrupt instruction, `RETFIE`, exits interrupt routine, as well as sets the GIE bit, which re-enables unmasked interrupts.

The following interrupt flags are contained in the INTCON register:

- INT Pin Interrupt
- PORTA Change Interrupt
- TMR0 Overflow Interrupt

The peripheral interrupt flags are contained in the special register PIR1. The corresponding interrupt enable bit is contained in special register PIE1.

The following interrupt flags are contained in the PIR1 register:

- EEPROM Data Write Interrupt
- A/D Interrupt
- 2 Comparator Interrupts
- Timer1 Overflow Interrupt
- Timer2 Match Interrupt
- Fail-Safe Clock Monitor Interrupt
- CCP Interrupt

When an interrupt is serviced:

- The GIE is cleared to disable any further interrupt
- The return address is PUSHed onto the stack
- The PC is loaded with 0004h

For external interrupt events, such as the INT pin or PORTA change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends upon when the interrupt event occurs (see Figure 15-8). The latency is the same for one or two-cycle instructions. Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid multiple interrupt requests.

Note 1:	Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.
2:	When an instruction that clears the GIE bit is executed, any interrupts that were pending for execution in the next cycle are ignored. The interrupts, which were ignored, are still pending to be serviced when the GIE bit is set again.

For additional information on Timer1, Timer2, comparators, A/D, Data EEPROM or CCP modules, refer to the respective peripheral section.

18.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
  - MPASM™ Assembler
  - MPLAB C18 and MPLAB C30 C Compilers
  - MPLINK™ Object Linker/
    MPLIB™ Object Librarian
  - MPLAB ASM30 Assembler/Linker/Library
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB ICE 2000 In-Circuit Emulator
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debugger
  - MPLAB ICD 2
- Device Programmers
  - PICSTART® Plus Development Programmer
  - MPLAB PM3 Device Programmer
  - PICkit™ 2 Development Programmer
- Low-Cost Demonstration and Development Boards and Evaluation Kits

18.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16-bit micro-controller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
  - Simulator
  - Programmer (sold separately)
  - Emulator (sold separately)
  - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Visual device initializer for easy register initialization
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as HI-TECH Software C Compilers and IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either assembly or C)
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
  - Source files (assembly or C)
  - Mixed assembly and C
  - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

FIGURE 19-7: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS

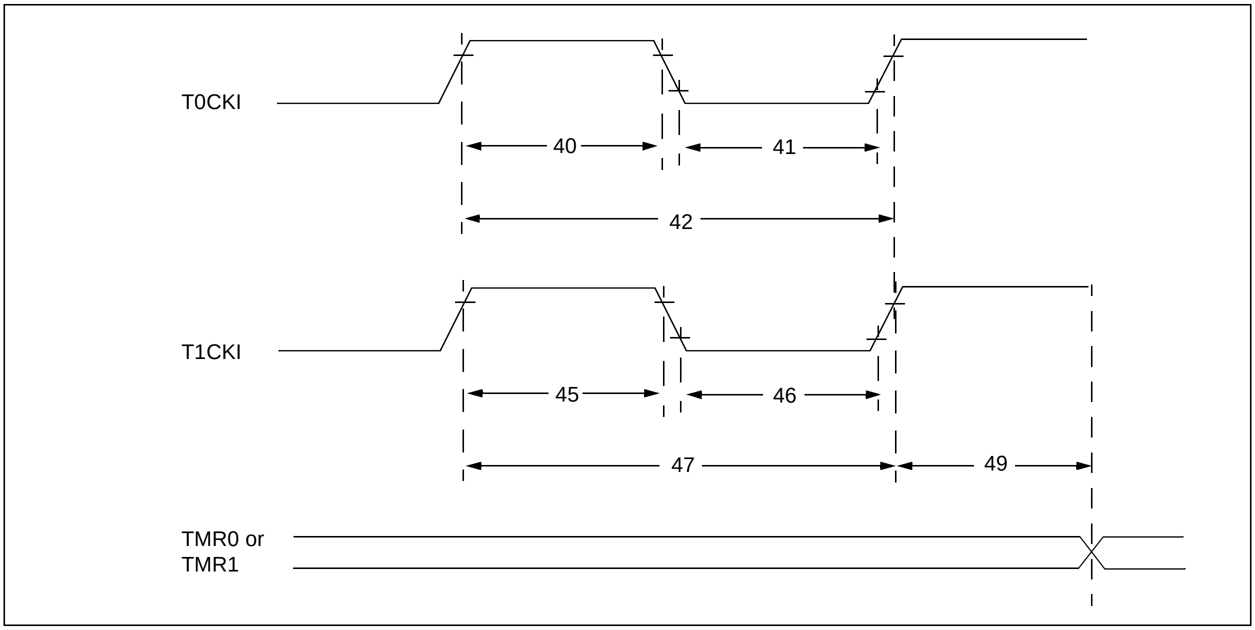


TABLE 19-5: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40*	TT0H	T0CKI High Pulse Width	No Prescaler	0.5 TCY + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
41*	TT0L	T0CKI Low Pulse Width	No Prescaler	0.5 TCY + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
42*	TT0P	T0CKI Period		Greater of: 20 or $\frac{T_{CY} + 40}{N}$	—	—	ns	N = prescale value (2, 4, ..., 256)
45*	TT1H	T1CKI High Time	Synchronous, No Prescaler	0.5 TCY + 20	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
46*	TT1L	T1CKI Low Time	Synchronous, No Prescaler	0.5 TCY + 20	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
47*	TT1P	T1CKI Input Period	Synchronous	Greater of: 30 or $\frac{T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous	60	—	—	ns	
48	FT1	Timer1 oscillator input frequency range (oscillator enabled by setting bit T1OSCEN)		DC	—	200*	kHz	
49	TCKEZTMR1	Delay from external clock edge to timer increment		2 TOSC*	—	7 TOSC*	—	

* These parameters are characterized but not tested.

† Data in ‘Typ’ column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 20-28: SCHMITT TRIGGER INPUT THRESHOLD VIN vs. VDD OVER TEMPERATURE

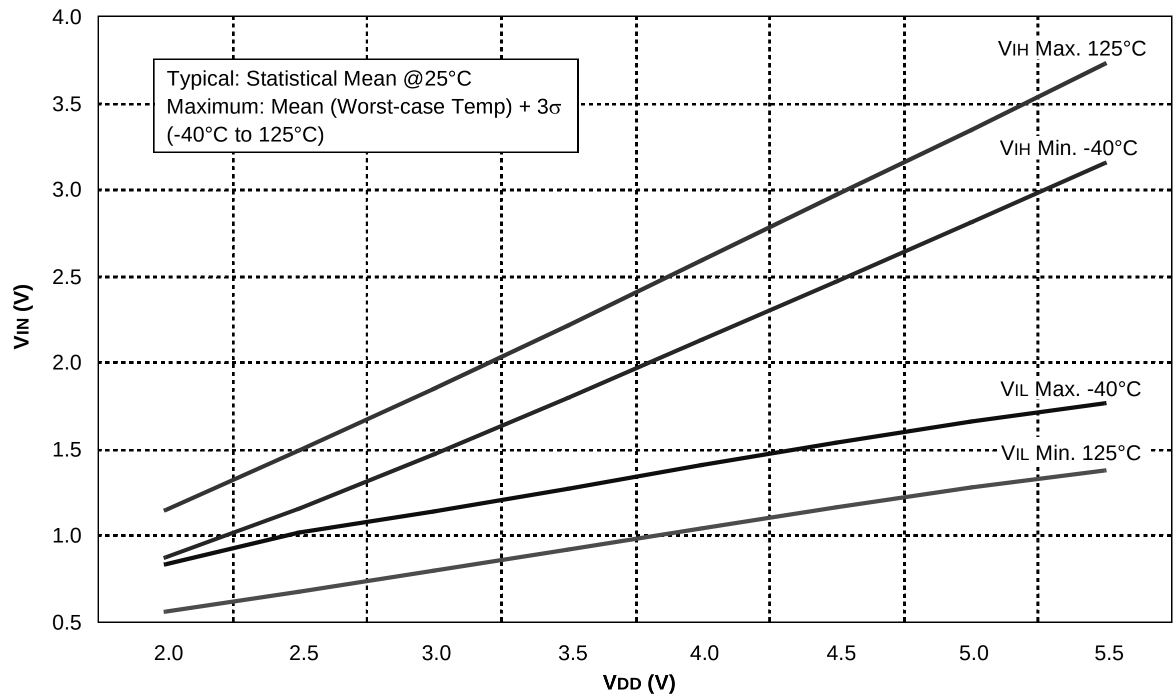
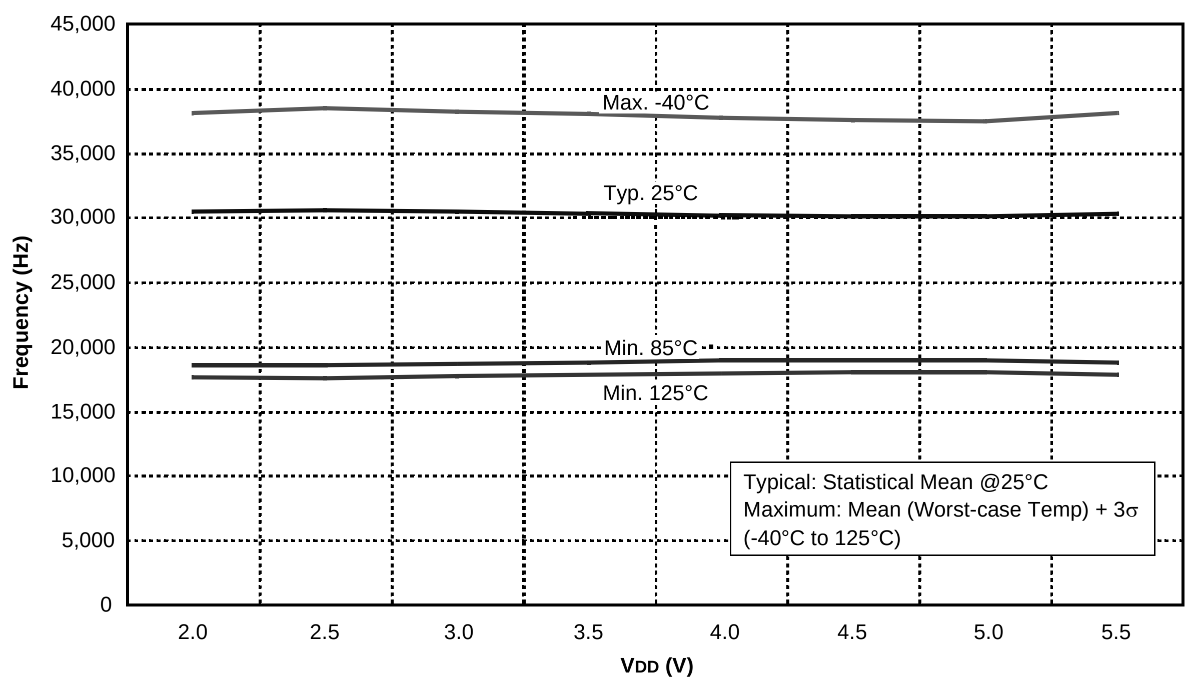
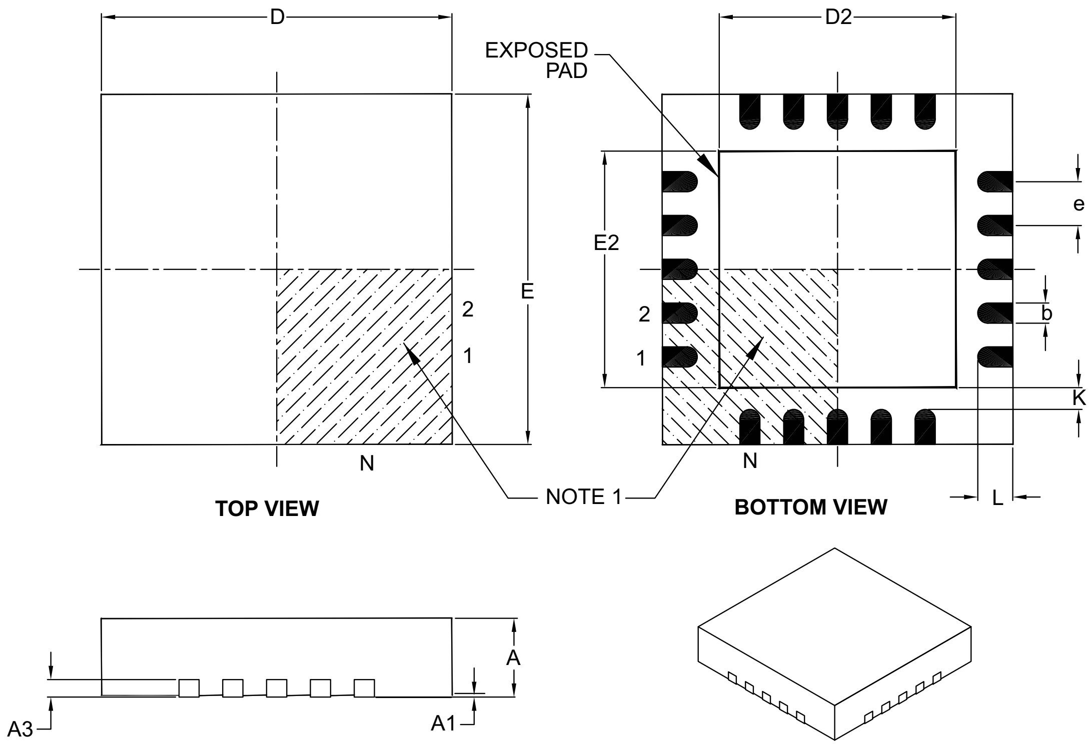


FIGURE 20-29: LFINTOSC FREQUENCY vs. VDD OVER TEMPERATURE (31 kHz)



20-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.60	2.70	2.80
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.60	2.70	2.80
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-126B