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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 14x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16hv785-e-p

NOTES:

2.2.2.4 PIE1 Register

The Peripheral Interrupt Enable Register 1 contains the interrupt enable bits, as shown in Register 2-4.

Note:	Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

REGISTER 2-4: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EEIE	ADIE	CCP1IE	C2IE	C1IE	OSFIE	TMR2IE	TMR1IE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EEIE:** EE Write Complete Interrupt Enable bit
1 = Enables the EE write complete interrupt
0 = Disables the EE write complete interrupt

bit 6 **ADIE:** A/D Converter Interrupt Enable bit
1 = Enables the A/D converter interrupt
0 = Disables the A/D converter interrupt

bit 5 **CCP1IE:** CCP1 Interrupt Enable bit
1 = Enables the CCP1 interrupt
0 = Disables the CCP1 interrupt

bit 4 **C2IE:** Comparator 2 Interrupt Enable bit
1 = Enables the Comparator 2 interrupt
0 = Disables the Comparator 2 interrupt

bit 3 **C1IE:** Comparator 1 Interrupt Enable bit
1 = Enables the Comparator 1 interrupt
0 = Disables the Comparator 1 interrupt

bit 2 **OSFIE:** Oscillator Fail Interrupt Enable bit
1 = Enables the Oscillator Fail interrupt
0 = Disables the Oscillator Fail interrupt

bit 1 **TMR2IE:** Timer2 to PR2 Match Interrupt Enable bit
1 = Enables the Timer2 to PR2 match interrupt
0 = Disables the Timer2 to PR2 match interrupt

bit 0 **TMR1IE:** Timer1 Overflow Interrupt Enable bit
1 = Enables the Timer1 overflow interrupt
0 = Disables the Timer1 overflow interrupt

2.3 PCL and PCLATH

The Program Counter (PC) specifies the address of the instruction to fetch for execution. The program counter is 13 bits wide. The low byte is called the PCL register. The PCL register is readable and writable. The high byte of the PC Register is called the PCH register. This register contains PC<12:8> bits which are not directly readable or writable. All updates to the PCH register goes through the PCLATH register.

On any Reset, the PC is cleared. Figure 2-3 shows the two situations for loading the PC. The upper example of Figure 2-3 shows how the PC is loaded on a write to PCL in the PCLATH Register→ PCH. The lower example of Figure 2-3 shows how the PC is loaded during a CALL or GOTO instruction in the PCLATH Register→ PCH).

2.3.1 MODIFYING PCL

Executing any instruction with the PCL register as the destination simultaneously causes the Program Counter PC<12:8> bits (PCH) to be replaced by the contents of the PCLATH register. This allows the entire contents of the program counter to be changed by writing the desired upper 5 bits to the PCLATH register. When the lower 8 bits are written to the PCL register, all 13 bits of the program counter will change to the values contained in the PCLATH register and those being written to the PCL register.

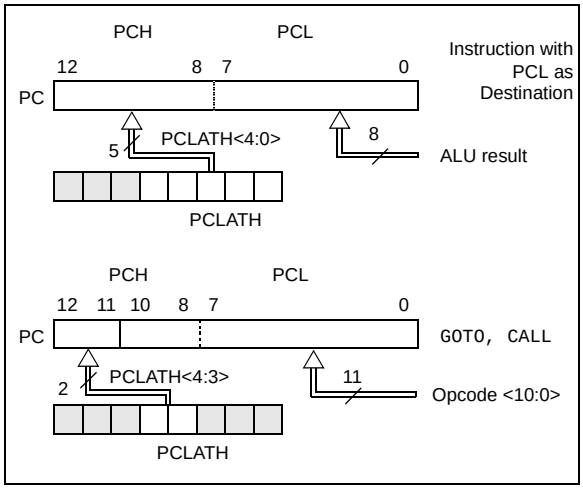
A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). Care should be exercised when jumping into a look-up table or program branch table (computed GOTO) by modifying the PCL register. Assuming that PCLATH is set to the table start address, if the table length is greater than 255 instructions or if the lower 8 bits of the memory address rolls over from 0xFF to 0x00 in the middle of the table, then PCLATH must be incremented for each address rollover that occurs between the table beginning and the target location within the table.

For more information refer to Application Note AN556, "*Implementing a Table Read*" (DS00556).

2.3.2 PROGRAM MEMORY PAGING

The CALL and GOTO instructions provide 11 bits of address to allow branching within any 2K program memory page. When using a CALL or GOTO instruction, the Most Significant bits of the address are provided by PCLATH<4:3> (page select bits). When using a CALL or GOTO instruction, the user must ensure that the page select bits are programmed so that the desired destination program memory page is addressed. When the CALL instruction (or interrupt) is executed, the entire 13-bit PC return address is PUSHed onto the stack. Therefore, manipulation of the PCLATH<4:3> bits are not required for the RETURN or RETFIE instructions (which POPs the address from the stack).

FIGURE 2-3: LOADING OF PC IN DIFFERENT SITUATIONS



2.3.3 STACK

The PIC16F785/HV785 family has an 8-level deep x 13-bit wide hardware stack (see Figure 2-1). The stack space is not part of either program or data space and the Stack Pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth PUSH overwrites the value that was stored from the first PUSH. The tenth PUSH overwrites the second PUSH (and so on).

Note 1:	There are no Status bits to indicate stack overflow or stack underflow conditions.
2:	There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW and RETFIE instructions or the vectoring to an interrupt address.

3.4.3 LFINTOSC

The Low-frequency Internal Oscillator (LFINTOSC) is an uncalibrated (approximate) 31 kHz internal clock source.

The output of the LFINTOSC connects to a postscaler and multiplexer (see Figure 3-1). 31 kHz can be selected via software using the IRCF bits (see **Section 3.4.4 "Frequency Select Bits (IRCF)"**). The LFINTOSC is also the frequency for the Power-up Timer (PWRT), Watchdog Timer (WDT) and Fail-Safe Clock Monitor (FSCM).

The LFINTOSC is enabled by selecting 31 kHz (IRCF = 000) as the system clock source (SCS = 1), or when any of the following are enabled:

- Two-Speed Start-up (IESO = 1 and IRCF = 000)
- Power-up Timer (PWRT)
- Watchdog Timer (WDT)
- Fail-Safe Clock Monitor (FSCM)

The LF Internal Oscillator (LTS) bit, in the OSCCON register, indicates whether the LFINTOSC is stable or not.

3.4.4 FREQUENCY SELECT BITS (IRCF)

The output of the 8 MHz HFINTOSC and 31 kHz LFINTOSC connect to a postscaler and multiplexer (see Figure 3-1). The Internal Oscillator Frequency select bits IRCF<2:0> in the OSCCON Register select the frequency output of the internal oscillators. One of eight frequencies can be selected via software:

- 8 MHz
- 4 MHz (Default after Reset)
- 2 MHz
- 1 MHz
- 500 kHz
- 250 kHz
- 125 kHz
- 31 kHz

Note:	Following any Reset, the IRCF bits are set to '110' and the frequency selection is forced to 4 MHz. The user can modify the IRCF bits to select a different frequency.

3.4.5 HF AND LF INTOSC CLOCK SWITCH TIMING

When switching between the LFINTOSC and the HFINTOSC, the new oscillator may already be shut down to save power. If this is the case, there is a 10 μs delay after the IRCF bits are modified before the frequency selection takes place. The LTS/HTS bits will reflect the current active status of the LFINTOSC and the HFINTOSC oscillators. The timing of a frequency selection is as follows:

1. IRCF bits are modified.
2. If the new clock is shut down, a 10 μs clock start-up delay is started.
3. Clock switch circuitry waits for a falling edge of the current clock.
4. CLKOUT is held low and the clock switch circuitry waits for a rising edge in the new clock.
5. CLKOUT is now connected with the new clock. HTS/LTS bits are updated as required.
6. Clock switch is complete.

If the internal oscillator speed selected is between 8 MHz and 125 kHz, there is no start-up delay before the new frequency is selected. This is because the old and the new frequencies are derived from the HFINTOSC via the postscaler and multiplexer.

Note:	Care must be taken to ensure an invalid voltage or frequency selection is not selected. An example of an invalid configuration is selecting 8 MHz when V_{DD} is 2.0V.

4.4.1.8 RC5/CCP1

The RC5 is configurable to function as one of the following:

- General purpose I/O
- Digital input for the capture/compare
- Digital output for the CCP

FIGURE 4-14: BLOCK DIAGRAM OF RC5

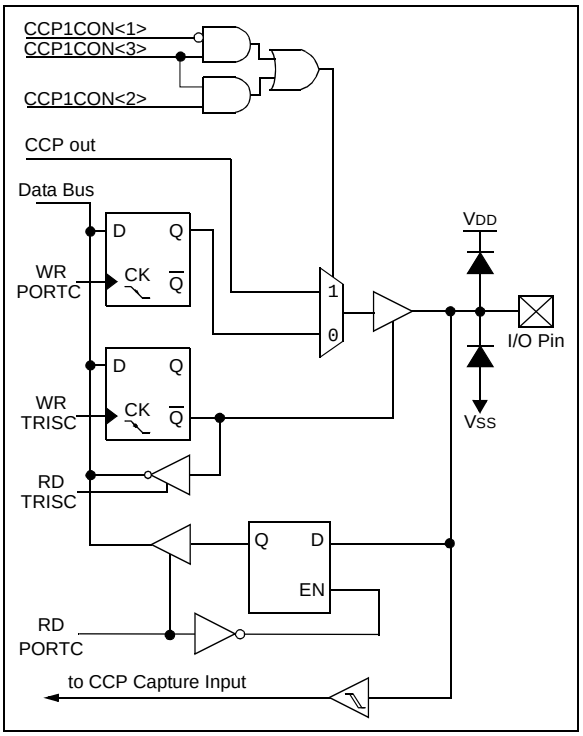


TABLE 4-3: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSEL1	—	—	—	—	ANS11	ANS10	ANS9	ANS8	---- 1111	---- 1111
CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	0000 0000	0000 0000
OPA1CON	OPAON	—	—	—	—	—	—	—	0--- ----	0--- ----
OPA2CON	OPAON	—	—	—	—	—	—	—	0--- ----	0--- ----
PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu
PWMCON0	PRSEN	PASEN	BLANK2	BLANK1	SYNC1	SYNC0	PH2EN	PH1EN	0000 0000	0000 0000
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by PORTC.

5.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

Figure 5-1 is a block diagram of the Timer0 module and the prescaler shared with the WDT.

5.1 Timer0 Operation

Timer mode is selected by clearing the T0CS bit of the OPTION Register. In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register.

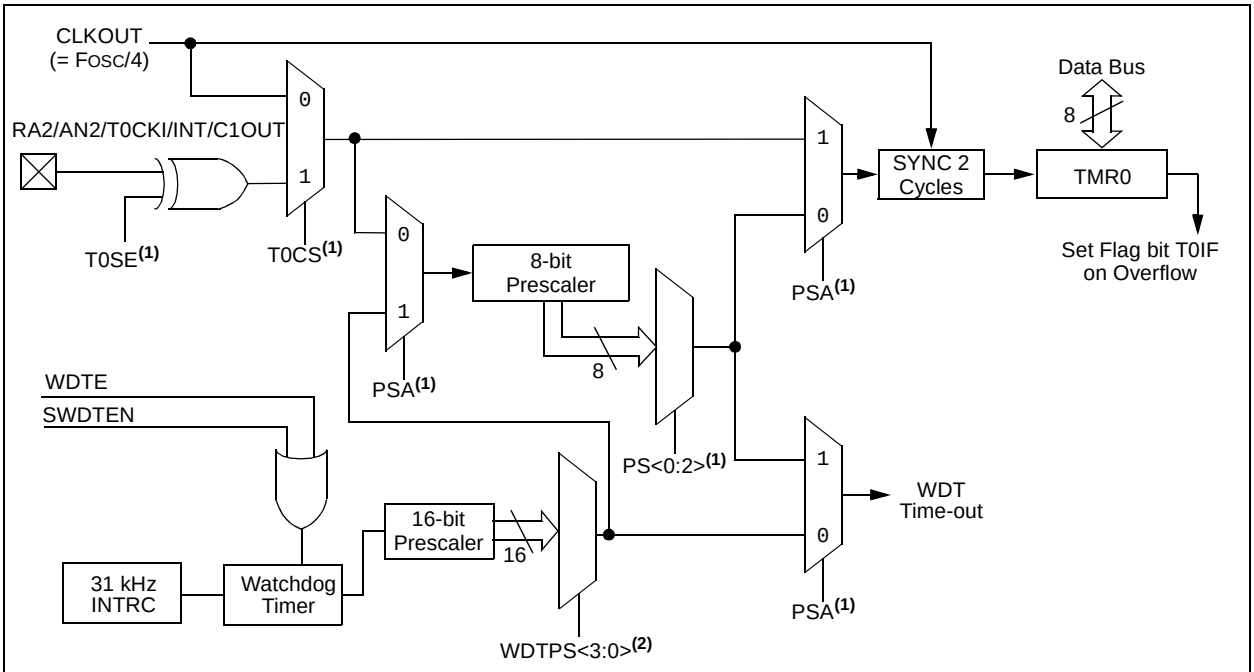
Counter mode is selected by setting the T0CS bit of the OPTION Register. In this mode, the Timer0 module will increment either on every rising or falling edge of pin RA2/AN2/T0CKI/INT/C1OUT. The incrementing edge is determined by the source edge (T0SE) control bit of the OPTION Register. Clearing the T0SE bit selects the rising edge.

Note 1:	Counter mode has specific external clock requirements.
2:	The ANSEL0 (91h) register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.

5.2 Timer0 Interrupt

A Timer0 interrupt is generated when the TMR0 register timer/counter overflows from FFh to 00h. This overflow sets the T0IF bit of the INTCON Register. The interrupt can be masked by clearing the T0IE bit of the INTCON Register. The T0IF bit must be cleared in software by the Timer0 module Interrupt Service Routine before re-enabling this interrupt. The Timer0 interrupt cannot wake the processor from Sleep since the timer is shut-off during Sleep.

FIGURE 5-1: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



Note 1: T0SE, T0CS, PSA, PS<2:0> are bits in the OPTION_REG (see Register 2.2.2.3).
2: WDTPS<3:0> are bits in the WDTCON register (see Register 15-2).

8.0 CAPTURE/COMPARE/PWM (CCP) MODULE

The Capture/Compare/PWM (CCP) module contains a 16-bit register which can operate as a:

- 16-bit Capture register
- 16-bit Compare register
- PWM Master/Slave Duty Cycle register

Capture/Compare/PWM Register 1 (CCPR1) is comprised of two 8-bit registers: CCPR1L (low byte) and CCPR1H (high byte). The CCP1CON register controls the operation of CCP. The special event trigger is generated by a compare match and will clear both TMR1H and TMR1L registers.

TABLE 8-1: CCP MODE – TIMER RESOURCES REQUIRED

CCP Mode	Timer Resource
Capture	Timer1
Compare	Timer1
PWM	Timer2

REGISTER 8-1: CCP1CON: CCP OPERATION REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as ‘0’.

bit 5-4 **DC1B<1:0>:** PWM Duty Cycle Least Significant bits

Capture mode:
Unused

Compare mode:
Unused

PWM mode:
These bits are the two LSbs of the PWM duty cycle. The eight MSbs are found in CCPR1L.

bit 3-0 **CCP1M<3:0>:** CCP Mode Select bits

0000 = Capture/Compare/PWM off (resets CCP module)
0001 = Unused (reserved)
0010 = Compare mode, toggle output on match (CCP1IF bit is set)
0011 = Unused (reserved)
0100 = Capture mode, every falling edge
0101 = Capture mode, every rising edge
0110 = Capture mode, every 4th rising edge
0111 = Capture mode, every 16th rising edge
1000 = Compare mode, set output on match (CCP1IF bit is set)
1001 = Compare mode, clear output on match (CCP1IF bit is set)
1010 = Compare mode, generate software interrupt on match (CCP1IF bit is set, CCP1 pin is unaffected)
1011 = Compare mode, trigger special event (CCP1IF bit is set; TMR1 is reset, and A/D conversion is started if the A/D module is enabled. CCP1 pin is unaffected.)
110x = PWM mode: CCP1 output is high true.
111x = PWM mode: CCP1 output is low true.

Note 1: For $\overline{\text{Borrow}}$, the polarity is reversed. A subtraction is executed by adding the two’s complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high-order or low-order bit of the source register.

13.0 TWO-PHASE PWM

The two-phase PWM (Pulse Width Modulator) is a stand-alone peripheral that supports:

- Single or dual-phase PWM
- Single complementary output PWM with overlap/ delay
- Sync input/output to cascade devices for additional phases

Setting either, or both, of the PH1EN or PH2EN bits of the PWMCON0 register will activate the PWM module (see Register 13-1). If PH1 is used then TRISC<1> must be cleared to configure the pin as an output. The same is true for TRISC<4> when using PH2. Both PH1EN and PH2EN must be set when using Complementary mode.

13.1 PWM Period

The PWM period is derived from the main clock (FOSC), the PWM prescaler and the period counter (see Figure 13-1). The prescale bits of the PWMP Register, (see Register 13-2) determine the value of the clock divider which divides the system clock (FOSC) to the pwm_clk. This pwm_clk is used to drive the PWM counter. In Master mode, the PWM counter is reset when the count reaches the period count of the PER Register, (see Register 13-2), which determines the frequency of the PWM. The relationship between the PWM frequency, prescale and period count is shown in Equation 13-1.

EQUATION 13-1: PWM FREQUENCY

$$PWM_{FREQ} = \frac{F_{OSC}}{(2^{PWMP} \bullet (PER + 1)}$$

The maximum PWM frequency is FOSC/2, since the period count must be greater than zero.

In Slave mode, the period counter is reset by the SYNC input, which is the master device period counter reset. For proper operation, the slave period count should be equal to or greater than that of the master.

13.2 PWM Phase

Each enabled phase output is driven active when the phase counter matches the corresponding PWM phase count in the PH Register (see Register 13-3 and Register 13-4). The phase output remains true until terminated by a feedback signal from either of the comparators or the auto-shutdown activates.

Phase granularity is a function of the period count value. For example, if PER<4:0> = 3, each output can be shifted in 90° steps (see Equation 13-2).

EQUATION 13-2: PHASE RESOLUTION

$$Phase_{DEG} = \frac{360}{(PER + 1)}$$

13.3 PWM Duty Cycle

Each PWM output is driven inactive, terminating the drive period, by asynchronous feedback through the internal comparators. The duty cycle resolution is in effect infinitely adjustable. Either or both comparators can be used to reset the PWM by setting the corresponding comparator enable bit (CxEN, see Register 13-3). Duty cycles of 100% can be obtained by suppressing the feedback which would otherwise terminate the pulse.

The comparator outputs can be “held off”, or blanked, by enabling the corresponding BLANK bit (BLANKx, see Register 13-1) for each phase. The blank bit disables the comparator outputs for 1/2 of a system clock (FOSC), thus ensuring at least TOSC/2 active time for the PWM output. Blanking avoids early termination of the PWM output which may result due to switching transients at the beginning of the cycle.

13.4 Master/Slave Operation

Multiple chips can operate together to achieve additional phases by operating one as the master and the others as slaves. When the PWM is configured as a master, the RB7/SYNC pin is an output and generates a high output for one pwm_clk period at the end of each PWM period (see Figure 13-4).

When the PWM is configured as a slave, the RB7/ SYNC pin is an input. The high input from a master in this configuration resets the PWM period counter which synchronizes the slave unit at the end of each PWM period. Proper operation of a slave device requires a common external FOSC clock source to drive the master and slave. The PWM prescale value of the slave device must also be identical to that of the master. As mentioned previously, the slave period count value must be greater than or equal to that of the master.

The PWM Counter will be reset and held at zero when both PH1EN and PH2EN of the PWMCON0 Register are false. If the PWM is configured as a slave, the PWM Counter will remain reset at zero until the first SYNC input is received.

REGISTER 13-2: PWMCLK: PWM CLOCK CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWMASE	PWMP1	PWMP0	PER4	PER3	PER2	PER1	PER0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **PWMASE:** PWM Auto-Shutdown Event Status bit
0 = PWM outputs are operating
1 = A shutdown event has occured. PWM outputs are inactive.

bit 6-5 **PWMP<1:0>:** PWM Clock Prescaler bits
00 = pwm_clk = FOSC ÷ 1
01 = pwm_clk = FOSC ÷ 2
10 = pwm_clk = FOSC ÷ 4
11 = pwm_clk = FOSC ÷ 8

bit 4-0 **PER<4:0>:** PWM Period bits
00000 = Not used. (Period = 1/pwm_clk)
00001 = Period = 2/pwm_clk2
0•••• = •••
01111 = Period = 16/pwm_clk
10000 = Period = 17/pwm_clk
1•••• = •••
11110 = Period = 31/pwm_clk
11111 = Period = 32/pwm_clk

13.8 PWM Configuration

When configuring the Two-Phase PWM, care must be taken to avoid active output levels from the PH1 and PH2 pins before the PWM is fully configured. The following sequence is suggested before the TRISC register or any of the Two-Phase PWM control registers are first configured:

- Output inactive (OFF) levels to the PORTC RC1/AN5/C12IN1-/PH1 and RC4/C2OUT/PH2 pins.
- Clear TRISC bits 1 and 4 to configure the PH1 and PH2 pins as outputs.
- Configure the PWMCLK, PWMPH1, PWMPH2, and PWMCON1 registers.
- Configure the PWMCON0 register.

EXAMPLE 13-1: PWM SETUP EXAMPLE

```
;Example to configure PH1 as a free running PWM output using the SYNC output as the duty cycle
;termination feedback.
;This requires an external connection between the SYNC output and the comparator input.
;SYNC out = RB7 on pin 10
;C1 inverting input = RC2/AN6 on pin 14

;Configure PH1, PH2 and SYNC pins as outputs
;First, ensure output latches are low
    BCF     PORTC,1         ;PH1 low
    BCF     PORTC,4         ;PH2 low
    BCF     PORTB,7         ;SYNC low
;Configure the I/Os as outputs
    BANKSEL  TRISB
    BCF     TRISC,1         ;PH1 output
    BCF     TRISC,4         ;PH2 output
    BCF     TRISB,7         ;SYNC output
;PH1 shares its function with AN5
;Configure AN5 as digital I/O
    BCF     ANSEL0,5        ;AN5 is digital, all others default as analog
;Configure the PWM but don't enable PH1 or PH2 yet
    BANKSEL  PWMCLK
;PWM control setup
    MOVLW   B'00001100'     ;auto shutdown off, no blanking, SYNC on, PH1 and PH2 off
    MOVWF   PWMCON0         ;see data sheet page 93
;PWM clock setup
    MOVLW   B'00111101'     ;pwm_clk = Fosc, 30 clocks in PWM period
    MOVWF   PWMCLK          ;see data sheet page 94
;PH1 setup
    MOVLW   B'00101111'     ;non-inverted, terminate on C1, Start on clock 15
    MOVWF   PWMPH1          ;see data sheet page 95
;PH2 setup
    MOVLW   B'00110101'     ;non-inverted, terminate on C1, Start on clock 21
    MOVWF   PWMPH2          ;see data sheet page 96
;Configure Comparator 1
    MOVLW   B'10011110'     ;C1 on, internal, inverted, normal speed, +:C1VREF, -:AN6
    MOVWF   CM1CON0         ;see data sheet page 68
;Configure comparator voltage reference
    BANKSEL  VRCON
    MOVLW   B'10101100'     ;C1VREN on, low range, CVREF= VDD/2
    MOVWF   VRCON           ;see data sheet page 72
;Everything is setup at this point so now it is time to enable PH1
    BANKSEL  PWMCON0
    BSF     PWMCON0,PH1EN  ;enable PH1
;Module is running autonomously at this point
```

14.0 DATA EEPROM MEMORY

The EEPROM data memory is readable and writable during normal operation (full V_{DD} range). This memory is not directly mapped in the register file space. Instead, it is indirectly addressed through the Special Function Registers. There are four SFRs used to read and write this memory:

- EECON1
- EECON2 (not a physically implemented register)
- EEDAT
- EEADR

EEDAT holds the 8-bit data for read/write, and EEADR holds the address of the EEPROM location being accessed. The PIC16F785/HV785 has 256 bytes of data EEPROM with an address range from 0h to FFh.

The EEPROM data memory allows byte read and write. A byte write automatically erases the location and writes the new data (erase before write). The EEPROM data memory is rated for high erase/write cycles. The write time is controlled by an on-chip timer. The write time will vary with voltage and temperature, as well as from chip-to-chip. Please refer to AC Specifications in **Section 19.0 "Electrical Specifications"** for exact limits.

When the data memory is code-protected, the CPU may continue to read and write the data EEPROM memory. The device programmer can no longer access the data EEPROM data and will read zeroes.

REGISTER 14-1: EEDAT: EEPROM DATA REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EEDATn**: Byte Value to Write to or Read From Data EEPROM bits

REGISTER 14-2: EEADR: EEPROM ADDRESS REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EEADR7	EEADR6	EEADR5	EEADR4	EEADR3	EEADR2	EEADR1	EEADR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EEADR**: Specifies one of 256 locations for EEPROM Read/Write Operation bits

17.0 INSTRUCTION SET SUMMARY

The PIC16F785/HV785 instruction set is highly orthogonal and is comprised of three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

Each PIC16 instruction is a 14-bit word divided into an **opcode,** which specifies the instruction type and one or more **operands,** which further specify the operation of the instruction. The format for each of the categories is presented in Figure 17-1, while the various opcode fields are summarized in Table 17-1.

Table 17-2 lists the instructions recognized by the MPASM™ assembler.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator, which selects the bit affected by the operation, while 'f' represents the address of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8-bit or 11-bit constant, or literal value.

One instruction cycle consists of four oscillator periods; for an oscillator frequency of 4 MHz, this gives a normal instruction execution time of 1 μs. All instructions are executed within a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of an instruction. When this occurs, the execution takes two instruction cycles, with the second cycle executed as a NOP.

Note:	To maintain upward compatibility with future products, do not use the OPTION and TRIS instructions.

All instruction examples use the format '0xhh' to represent a hexadecimal number, where 'h' signifies a hexadecimal digit.

17.1 Read-Modify-Write Operations

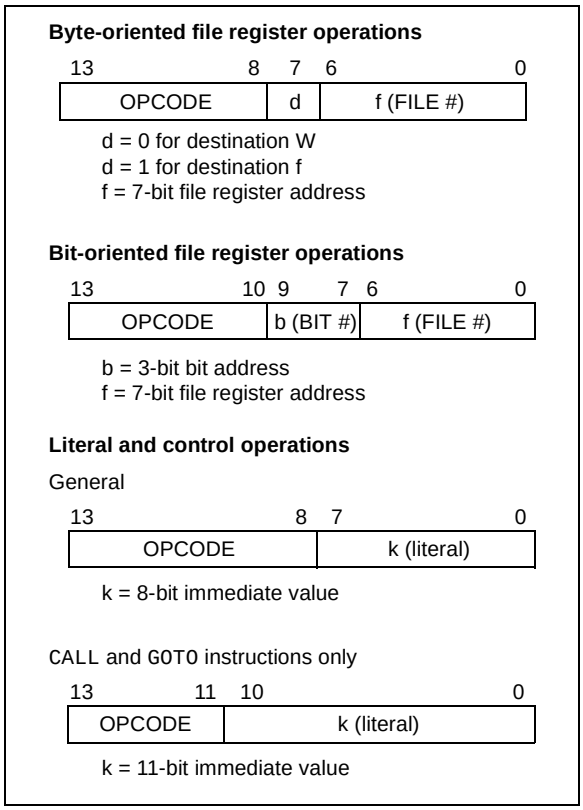
Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (RMW) operation. The register is read, the data is modified, and the result is stored according to either the instruction, or the destination designator 'd'. A read operation is always performed, even if the instruction is a Write command.

For example, a CLRF PORTA instruction will read PORTA, clear all the data bits, then write the result back to PORTA. This example would have the unintended result of clearing the condition that set the RAIF flag.

TABLE 17-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1). The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1.
PC	Program Counter
TO	Time-out bit
PD	Power-down bit

FIGURE 17-1: GENERAL FORMAT FOR INSTRUCTIONS



18.11 PICSTART Plus Development Programmer

The PICSTART Plus Development Programmer is an easy-to-use, low-cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. The PICSTART Plus Development Programmer supports most PIC devices in DIP packages up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus Development Programmer is CE compliant.

18.12 PICkit 2 Development Programmer

The PICkit™ 2 Development Programmer is a low-cost programmer and selected Flash device debugger with an easy-to-use interface for programming many of Microchip's baseline, mid-range and PIC18F families of Flash memory microcontrollers. The PICkit 2 Starter Kit includes a prototyping development board, twelve sequential lessons, software and HI-TECH's PICC™ Lite C compiler, and is designed to help get up to speed quickly using PIC® microcontrollers. The kit provides everything needed to program, evaluate and develop applications using Microchip's powerful, mid-range Flash memory family of microcontrollers.

18.13 Demonstration, Development and Evaluation Boards

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

19.1 DC Characteristics: PIC16F785/HV785-I (Industrial), PIC16F785/HV785-E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VDD	**Supply Voltage(2)**					FOSC ≤ 4 MHz:
D001			2.0	—	5.5	V	PIC16F785 with A/D off
D001A			2.2	—	5.5	V	PIC16F785 with A/D on, 0°C to +125°C
D001B			2.5	—	5.5	V	PIC16F785 with A/D on, -40°C to +125°C
D001C			3.0	—	5.5	V	4 MHz ≤ FOSC ≤ 10 MHz
D001D			4.5	—	5.5	V	10 MHz ≤ FOSC ≤ 20 MHz
D002	VDR	**RAM Data Retention Voltage(1)**	1.5*	—	—	V	Device in Sleep mode
D003	VPOR	VDD voltage above which the internal **POR releases**	—	1.8	—	V	See **Section 15.2.1 "Power-On Reset"** for details.
D003A	VPARM	VDD voltage below which the internal **POR rearms**	—	1.0	—	V	See **Section 15.2.1 "Power-On Reset"** for details.
D004	SVDD	VDD **Rise Rate** to ensure internal Power-on Reset signal	0.05*	—	—	V/ms	See **Section 15.2.1 "Power-On Reset"** for details.
D005	VBOR	**Brown-out Reset**	—	2.1	—	V	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

2: Maximum supply voltage is VSHUNT for PIC16HV785 device (see Table 19-14).

19.3 DC Characteristics: PIC16F785/HV785-E (Extended)(1), (2) (Continued)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for extended					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						VDD	
D020E	Power-down Base Current (IPD)(4)	—	0.15	9	µA	2.0	WDT, BOR, Comparators, VREF, T1OSC, Op Amps and VR disabled
		—	0.20	11	µA	3.0	
		—	0.35	15	µA	5.0	
D021E		—	1.7	17.5	µA	2.0	WDT Current(3)
		—	2	19	µA	3.0	
		—	3	22	µA	5.0	
D022E		—	42	65	µA	3.0	BOR Current(3)
		—	85	127	µA	5.0	
D023E		—	362	476	µA	2.0	Comparator Current(3) CxSP = 1
		—	418	554	µA	3.0	
		—	500	625	µA	5.0	
D023E		—	96	130	µA	2.0	Comparator Current(3) CxSP = 0
		—	112	147	µA	3.0	
		—	132	168	µA	5.0	
D024E		—	39	47	µA	2.0	CVREF Current(3) Low Range
		—	59	72	µA	3.0	
		—	98	124	µA	5.0	
D024E		—	30	36	µA	2.0	CVREF Current(3) High Range
		—	45	55	µA	3.0	
		—	75	95	µA	5.0	
D025E		—	2.5	21	µA	2.0	T1 OSC Current(3)
		—	3.2	28	µA	3.0	
		—	4.8	45	µA	5.0	
D026E		—	0.30	12	uA	3.0	A/D Current(3) (not converting)
		—	0.36	16	uA	5.0	
D027E		—	9	20	µA	3.0	VR Current(3)
		—	10	26	µA	3.0	
		—	11	30	µA	5.0	
D028E		—	202	417	µA	3.0	Op Amp Current(3)
		—	217	468	µA	5.0	

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in Active Operation mode are: OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD; $\overline{MCLR}$ = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature also have an impact on the current consumption.

3: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

4: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD. When A/D is off, it will not consume any current other than leakage current. The power-down current spec includes any such leakage from the A/D module.

FIGURE 19-7: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS

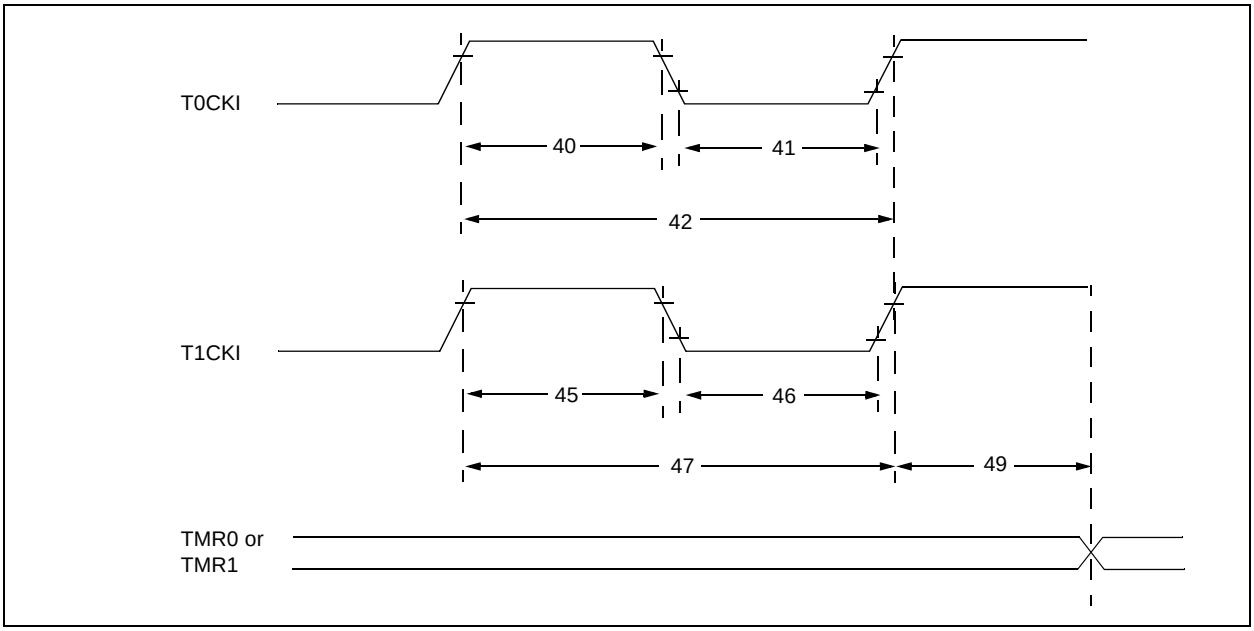


TABLE 19-5: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Param No.	Sym	Characteristic			Min	Typ†	Max	Units	Conditions
40*	TT0H	T0CKI High Pulse Width		No Prescaler	0.5 TCY + 20	—	—	ns	
				With Prescaler	10	—	—	ns	
41*	TT0L	T0CKI Low Pulse Width		No Prescaler	0.5 TCY + 20	—	—	ns	
				With Prescaler	10	—	—	ns	
42*	TT0P	T0CKI Period			Greater of: 20 or TCY + 40 / N	—	—	ns	N = prescale value (2, 4, ..., 256)
45*	TT1H	T1CKI High Time	Synchronous, No Prescaler		0.5 TCY + 20	—	—	ns	
			Synchronous, with Prescaler		15	—	—	ns	
			Asynchronous		30	—	—	ns	
46*	TT1L	T1CKI Low Time	Synchronous, No Prescaler		0.5 TCY + 20	—	—	ns	
			Synchronous, with Prescaler		15	—	—	ns	
			Asynchronous		30	—	—	ns	
47*	TT1P	T1CKI Input Period	Synchronous		Greater of: 30 or TCY + 40 / N	—	—	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous		60	—	—	ns	
48	FT1	Timer1 oscillator input frequency range (oscillator enabled by setting bit T1OSCEN)			DC	—	200*	kHz	
49	TCKEZTMR1	Delay from external clock edge to timer increment			2 TOSC*	—	7 TOSC*	—	

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 20-6: MAXIMUM IDD vs. VDD OVER FOSC (XT MODE)

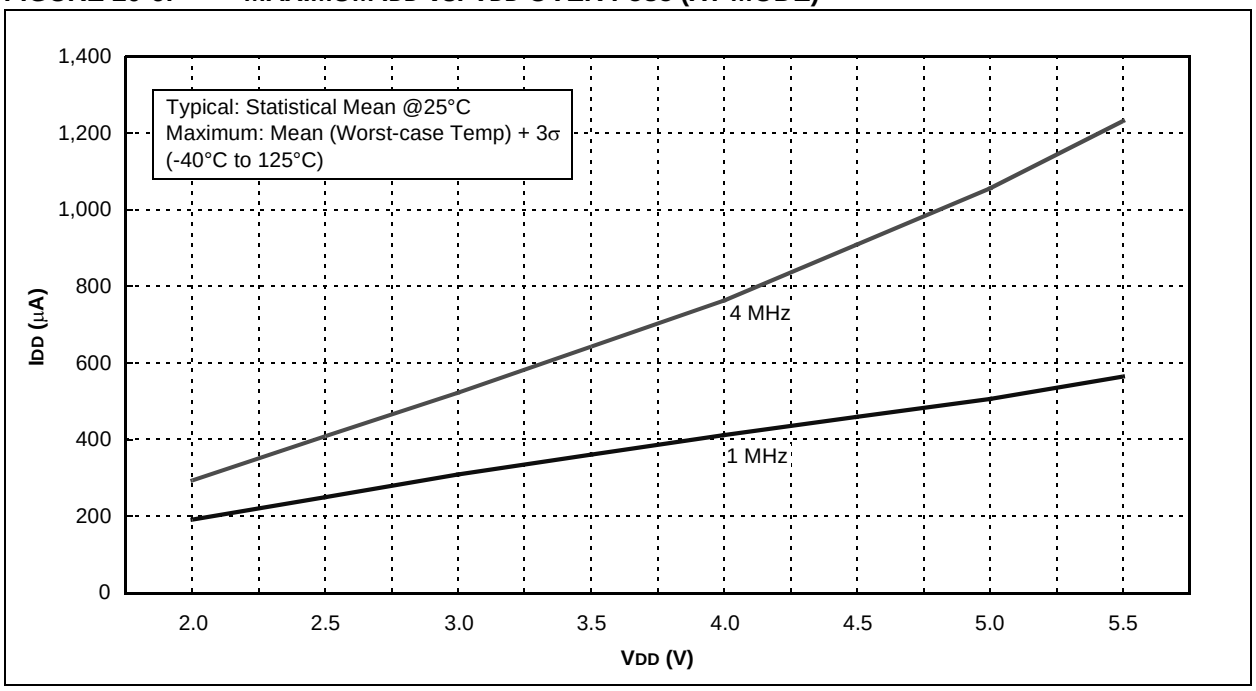


FIGURE 20-7: IDD vs. VDD (LP MODE)

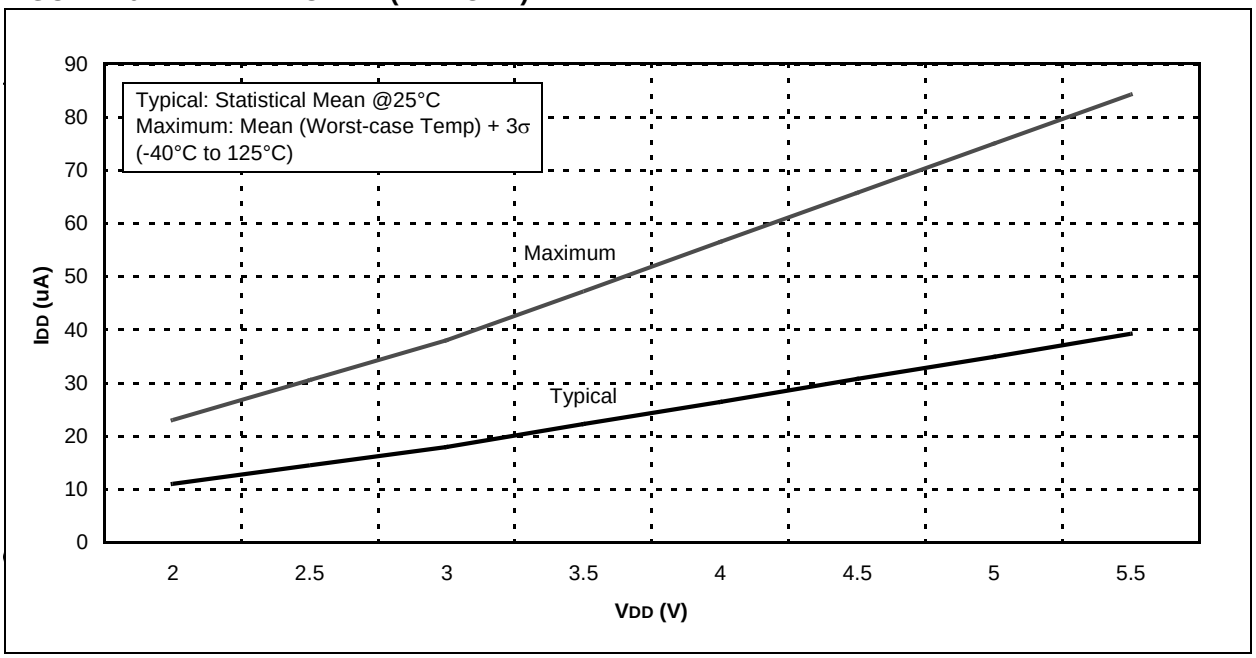


FIGURE 20-18: TYPICAL WDT IPD vs. VDD OVER TEMPERATURE

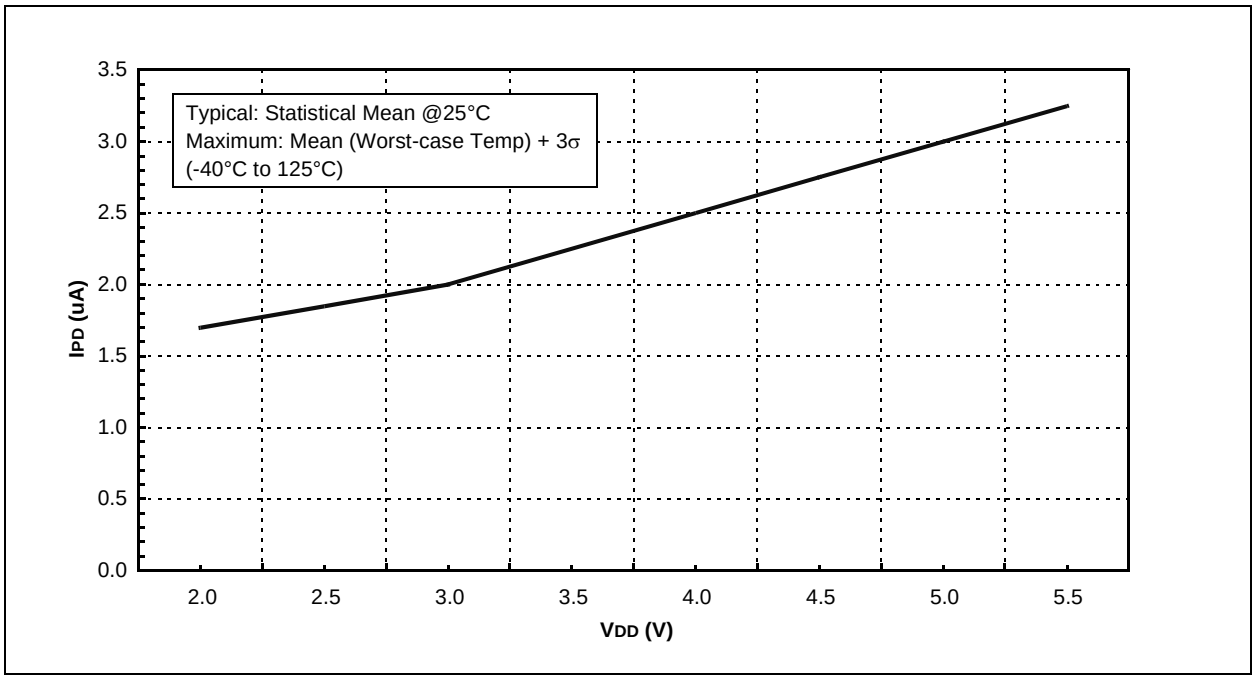
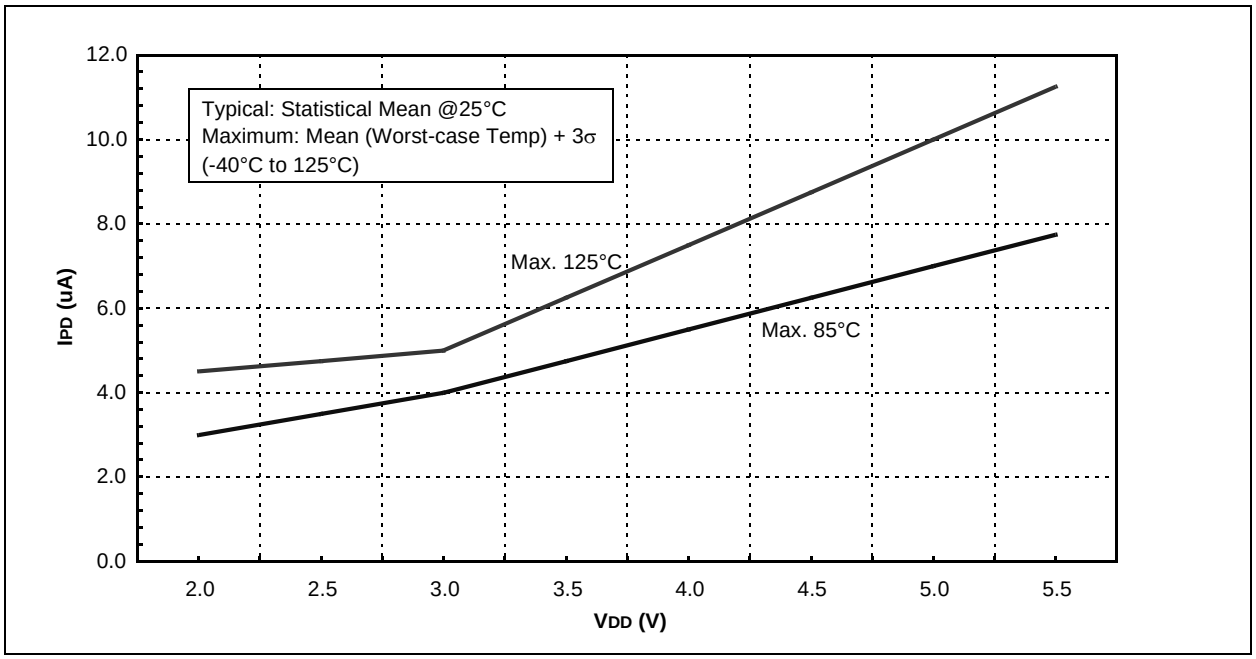
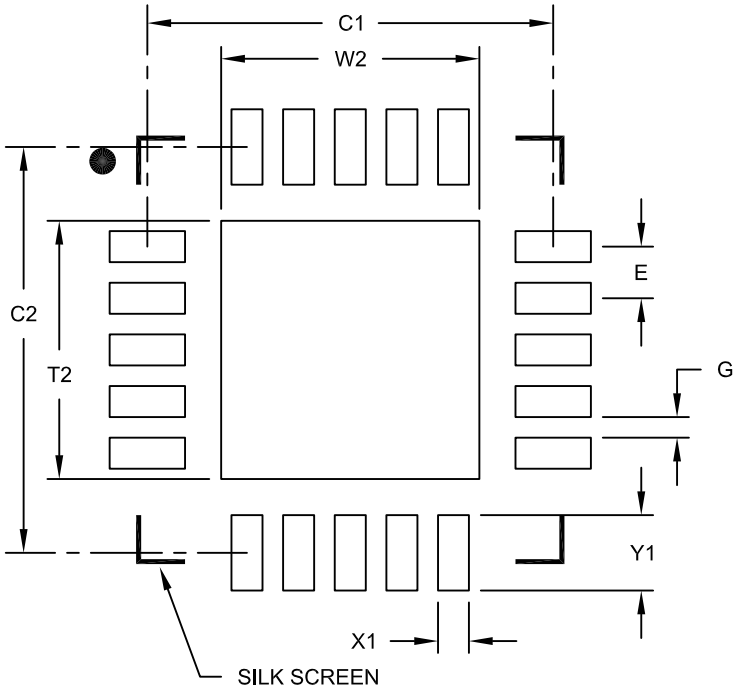


FIGURE 20-19: MAXIMUM WDT IPD vs. VDD OVER TEMPERATURE



20-Lead Plastic Quad Flat, No Lead Package (ML) - 4x4 mm Body [QFN]
With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			2.50
Optional Center Pad Length	T2			2.50
Contact Pad Spacing	C1		3.93	
Contact Pad Spacing	C2		3.93	
Contact Pad Width	X1			0.30
Contact Pad Length	Y1			0.73
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2126A

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