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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 14x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16hv785-i-p

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PIC16F785/HV785

20-Pin Flash-Based 8-Bit CMOS Microcontroller

High-Performance RISC CPU:

- Only 35 Instructions to Learn:
  - All single-cycle instructions except branches
- Operating Speed:
  - DC – 20 MHz oscillator/clock input
  - DC – 200 ns instruction cycle
- Interrupt Capability
- 8-Level Seep Hardware Stack
- Direct, Indirect and Relative Addressing modes

Special Microcontroller Features:

- Precision Internal Oscillator:
  - Factory calibrated to ±1%
  - Software selectable frequency range of 8 MHz to 32 kHz
  - Software tunable
  - Two-Speed Start-up mode
  - Crystal fail detect for critical applications
  - Clock mode switching during operation for power savings
- Power-Saving Sleep mode
- Wide Operating Voltage Range (2.0V-5.5V)
- Industrial and Extended Temperature Range
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Reset (BOR) with Software Control Option
- Enhanced Low-Current Watchdog Timer (WDT) with on-chip Oscillator (software selectable nominal 268 seconds with full prescaler) with Software Enable
- Multiplexed Master Clear with Pull-up/Input Pin
- Programmable Code Protection
- High-Endurance Flash/EEPROM cell:
  - 100,000 write Flash endurance
  - 1,000,000 write EEPROM endurance
  - Flash/Data EEPROM retention: > 40 years

Low-Power Features:

- Standby Current:
  - 30 nA @ 2.0V, typical
- Operating Current:
  - 8.5 μA @ 32 kHz, 2.0V, typical
  - 100 μA @ 1 MHz, 2.0V, typical
- Watchdog Timer Current:
  - 1 μA @ 2.0V, typical
- Timer1 Oscillator Current:
  - 2 μA @ 32 kHz, 2.0V, typical

Peripheral Features:

- High-Speed Comparator module with:
  - Two independent analog comparators
  - Programmable on-chip voltage reference (CV_{REF}) module (% of V_{DD})
  - 1.2V band gap voltage reference
  - Comparator inputs and outputs externally accessible
  - < 40 ns propagation delay
  - 2 mv offset, typical
- Operational Amplifier module with 2 independent Op Amps:
  - 3 MHz GBWP, typical
  - All I/O pins externally accessible
- Two-Phase Asynchronous Feedback PWM module:
  - Complementary output with programmable dead band delay
  - Infinite resolution analog duty cycle
  - Sync Output/Input for multi-phase PWM
  - F_{OSC}/2 maximum PWM frequency
- A/D Converter:
  - 10-bit resolution and 14 channels (2 internal)
- 17 I/O pins and 1 Input-only Pin:
  - High-current source/sink for direct LED drive
  - Interrupt-on-pin change
  - Individually programmable weak pull-ups
- Timer0: 8-Bit Timer/Counter with 8-Bit Programmable Prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Gate Input mode
  - Option to use OSC1 and OSC2 in LP mode as Timer1 oscillator, if INTOSC mode selected
- Timer2: 8-Bit Timer/Counter with 8-Bit Period Register, Prescaler and Postscaler
- Capture, Compare, PWM module:
  - 16-bit Capture, max resolution 12.5 ns
  - Compare, max resolution 200 ns
  - 10-bit PWM with 1 output channel, max frequency 20 kHz
- In-Circuit Serial Programming™ (ICSP™) via two pins
- Shunt Voltage Regulator (PIC16HV785 only):
  - 5 volt regulation
  - 4 mA to 50 mA shunt range

2.2.2.3 INTCON Register

The Interrupt Control register is a readable and writable register, which contains the various enable and flag bits for TMR0 register overflow, PORTA change and external RA2/INT pin interrupts.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE bit of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-3: INTCON: INTERRUPT CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	T0IE	INTE	RAIE(1)	T0IF(2)	INTF	RAIF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all unmasked interrupts
0 = Disables all interrupts

bit 6 **PEIE:** Peripheral Interrupt Enable bit
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts

bit 5 **T0IE:** TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

bit 4 **INTE:** RA2/AN2/T0CKI/INT/C1OUT External Interrupt Enable bit
1 = Enables the RA2/AN2/T0CKI/INT/C1OUT external interrupt
0 = Disables the RA2/AN2/T0CKI/INT/C1OUT external interrupt

bit 3 **RAIE:** PORTA Change Interrupt Enable bit(1)
1 = Enables the PORTA change interrupt
0 = Disables the PORTA change interrupt

bit 2 **T0IF:** TMR0 Overflow Interrupt Flag bit(2)
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1 **INTF:** RA2/AN2/T0CKI/INT/C1OUT External Interrupt Flag bit
1 = The RA2/AN2/T0CKI/INT/C1OUT external interrupt occurred (must be cleared in software)
0 = The RA2/AN2/T0CKI/INT/C1OUT external interrupt did not occur

bit 0 **RAIF:** PORTA Change Interrupt Flag bit
1 = When at least one of the PORTA <5:0> pins changed state (must be cleared in software)
0 = None of the PORTA <5:0> pins have changed state

Note 1: IOCA register must also be enabled.

2: T0IF bit is set when Timer0 rolls over. Timer0 is unchanged on Reset and should be initialized before clearing T0IF bit.

TABLE 3-4: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CONFIG	$\overline{CPD}$	$\overline{CP}$	MCLRE	$\overline{PWRTE}$	WDTE	FOSC2	FOSC1	FOSC0	—	—
OSCCON	—	IRCF2	IRCF1	IRCF0	OSTS	HTS	LTS	SCS	-110 q000	-110 q000
OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	---0 0000	---u uuuu
PIE1	EEIE	ADIE	CCP1IE	C2IE	C1IE	OSFIE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	EEIF	ADIF	CCP1IF	C2IF	C1IF	OSFIF	TMR2IF	TMR1IF	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0', q = value depends on condition. Shaded cells are not used by oscillators.

Note 1: See Register 15.2 for operation of all Configuration Word bits.

REGISTER 4-2: TRISA: PORTA TRI-STATE REGISTER

U-0	U-0	R/W-1	R/W-1	R-1	R/W-1	R/W-1	R/W-1
—	—	TRISA5(2)	TRISA4(2)	TRISA3(1)	TRISA2	TRISA1	TRISA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **TRISA<5:0>:** PORTA Tri-State Control bit(1), (2)
1 = PORTA pin configured as an input (tri-stated)
0 = PORTA pin configured as an output

bit 0 **C:** Carry/$\overline{\text{Borrow}}$ bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)(1)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: TRISA<3> always reads '1'.

2: TRISA<5:4> always reads '1' in XT, HS and LP OSC modes.

4.2 Additional Pin Functions

Every PORTA pin on the PIC16F785/HV785 has an interrupt-on-change option and a weak pull-up option. The next three sections describe these functions.

4.2.1 WEAK PULL-UPS

Each of the PORTA pins has an individually configurable internal weak pull-up. Control bits WPUAx enable or disable each pull-up. Refer to Register 4-3. Each weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset by the $\overline{\text{RAPU}}$ bit in the (OPTION Register. The weak pull-up on RA3 is automatically enabled when RA3 is configured as $\overline{\text{MCLR}}$.

REGISTER 4-3: WPUA: WEAK PULL-UP REGISTER

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	WPUA5(4)	WPUA4(4)	WPUA3(3)	WPUA2	WPUA1	WPUA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **WPUA<5:0>:** Weak Pull-up Register bits
1 = Pull-up enabled
0 = Pull-up disabled

Note 1: Global $\overline{\text{RAPU}}$ must be enabled for individual pull-ups to be enabled.

2: The weak pull-up device is automatically disabled if the pin is in Output mode (TRISA = 0).

3: The RA3 pull-up is automatically enabled when configured as $\overline{\text{MCLR}}$ in the Configuration Word.

4: WPUA<5:4> always reads '1' in XT, HS and LP OSC modes.

4.4 PORTC and TRISC Registers

PORTC is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISC (Register 4-8). Setting a TRISC bit (= 1) will make the corresponding PORTC pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISC bit (= 0) will make the corresponding PORTC pin an output (i.e., put the contents of the output latch on the selected pin). Example 4-3 shows how to initialize PORTC.

Reading the PORTC register (Register 4-7) reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the port data latch.

The TRISC register controls the direction of the PORTC pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISC register are maintained set when using them as analog inputs. I/O pins configured as analog input always read '0'.

When RC4 or RC5 is configured as an op amp output, the corresponding RC4 or RC5 digital output driver will automatically be disabled regardless of the TRISC<4> or TRISC<5> value.

Note:	The ANSEL0 (91h) and ANSEL1 (93h) registers must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.

EXAMPLE 4-3: INITIALIZING PORTC

```
BCF     STATUS,RP0      ;Bank 0
BCF     STATUS,RP1
CLRF    PORTC           ;Init PORTC
BSF     STATUS,RP0      ;Bank 1
CLRF    ANSEL0          ;digital I/O
CLRF    ANSEL1          ;digital I/O
MOVLW   0Ch             ;Set RC<3:2> as inputs
MOVWF   TRISC           ; and set RC<5:4,1:0>
                        ; as outputs
BCF     STATUS,RP0      ;Bank 0
```

REGISTER 4-7: PORTC: PORTC REGISTER

R/W-x(1)	R/W-x(1)	R/W-x	R/W-x	R/W-x(1)	R/W-x(1)	R/W-x(1)	R/W-x(1)
RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **RC<7:0>:** PORTC General Purpose I/O Pin bits
1 = Port pin is greater than VIH
0 = Port pin is less than VIL

Note 1: Data latches are unknown after a POR, but each port bit reads '0' when the corresponding analog select bit is '1' (see Registers 12-1 and 12-2 on page 82).

REGISTER 4-8: TRISC: PORTC TRI-STATE REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **TRISC<7:0>:** PORTC Tri-State Control bits
1 = PORTC pin configured as an input (tri-stated)
0 = PORTC pin configured as an output

REGISTER 6-1: T1CON: TIMER1 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T1GINV(1)	TMR1GE(2)	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **T1GINV:** Timer1 Gate Invert bit (1)
1 = Timer1 gate is high true (see bit 6)
0 = Timer1 gate is low true (see bit 6)

bit 6 **TMR1GE:** Timer1 Gate Enable bit (2)
If TMR1ON = 0:
This bit is ignored
If TMR1ON = 1:
1 = Timer1 is on if Timer1 gate is true (see bit 7)
0 = Timer1 is on independent of Timer1 gate

bit 5-4 **T1CKPS<1:0>:** Timer1 Input Clock Prescale Select bits
11 = 1:8 Prescale Value
10 = 1:4 Prescale Value
01 = 1:2 Prescale Value
00 = 1:1 Prescale Value

bit 3 **T1OSCEN:** LP Oscillator Enable Control bit
If System Clock is INTOSC without CLKOUT or LP mode:
1 = LP oscillator is enabled for Timer1 clock
0 = LP oscillator is off
Else:
This bit is ignored

bit 2 **$\overline{\text{T1SYNC}}$:** Timer1 External Clock Input Synchronization Control bit
TMR1CS = 1:
1 = Do not synchronize external clock input
0 = Synchronize external clock input
TMR1CS = 0:
This bit is ignored. Timer1 uses the internal clock.

bit 1 **TMR1CS:** Timer1 Clock Source Select bit
1 = External clock from T1CKI pin (on the rising edge)
0 = Internal clock (FOSC/4)

bit 0 **TMR1ON:** Timer1 On bit
1 = Enables Timer1
0 = Stops Timer1

Note 1: T1GINV bit inverts the Timer1 gate logic, regardless of source.

2: TMR1GE bit must be set to use either T1G pin or C2OUT, as selected by T1GSS bit (CM2CON1<1>), as a Timer1 gate source.

8.0 CAPTURE/COMPARE/PWM (CCP) MODULE

The Capture/Compare/PWM (CCP) module contains a 16-bit register which can operate as a:

- 16-bit Capture register
- 16-bit Compare register
- PWM Master/Slave Duty Cycle register

Capture/Compare/PWM Register 1 (CCPR1) is comprised of two 8-bit registers: CCPR1L (low byte) and CCPR1H (high byte). The CCP1CON register controls the operation of CCP. The special event trigger is generated by a compare match and will clear both TMR1H and TMR1L registers.

TABLE 8-1: CCP MODE – TIMER RESOURCES REQUIRED

CCP Mode	Timer Resource
Capture	Timer1
Compare	Timer1
PWM	Timer2

REGISTER 8-1: CCP1CON: CCP OPERATION REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as ‘0’.

bit 5-4 **DC1B<1:0>:** PWM Duty Cycle Least Significant bits

Capture mode:
Unused

Compare mode:
Unused

PWM mode:
These bits are the two LSbs of the PWM duty cycle. The eight MSbs are found in CCPR1L.

bit 3-0 **CCP1M<3:0>:** CCP Mode Select bits

0000 = Capture/Compare/PWM off (resets CCP module)
0001 = Unused (reserved)
0010 = Compare mode, toggle output on match (CCP1IF bit is set)
0011 = Unused (reserved)
0100 = Capture mode, every falling edge
0101 = Capture mode, every rising edge
0110 = Capture mode, every 4th rising edge
0111 = Capture mode, every 16th rising edge
1000 = Compare mode, set output on match (CCP1IF bit is set)
1001 = Compare mode, clear output on match (CCP1IF bit is set)
1010 = Compare mode, generate software interrupt on match (CCP1IF bit is set, CCP1 pin is unaffected)
1011 = Compare mode, trigger special event (CCP1IF bit is set; TMR1 is reset, and A/D conversion is started if the A/D module is enabled. CCP1 pin is unaffected.)
110x = PWM mode: CCP1 output is high true.
111x = PWM mode: CCP1 output is low true.

Note 1: For $\overline{\text{Borrow}}$, the polarity is reversed. A subtraction is executed by adding the two’s complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high-order or low-order bit of the source register.

8.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPR1L register and to the DC1B<1:0> bits of the CCP1CON register. Up to 10 bits of resolution is available. The CCPR1L contains the eight MSbs and the DC1B<1:0> contains the two LSbs. In PWM mode, CCPR1H is a read-only register.

Equation 8-2 is used to calculate the PWM duty cycle in time.

EQUATION 8-2: PWM DUTY CYCLE

$$PWM\ duty\ cycle = (CCPR1L{:}CCP1CON\langle 5{:}4\rangle) \bullet T_{OSC} \bullet (TMR2\ prescale\ value)$$

CCPR1L and DC1B<1:0> can be written to at any time, but the duty cycle value is not latched into CCPR1H until after a match between PR2 and TMR2 occurs (i.e. the period is complete). In PWM mode, CCPR1H is a read-only register.

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

Because of the buffering, the module waits until the timer resets, instead of starting immediately. This means that enhanced PWM waveforms do not exactly match the standard PWM waveforms, but are instead offset by one full instruction cycle (4 TOSC).

When the CCPR1H and 2-bit latch match TMR2, concatenated with an internal 2-bit Q clock or 2 bits of the TMR2 prescaler, the RC5/CCP1 pin is cleared.

The maximum PWM resolution is a function of PR2 as shown by Equation 8-3.

EQUATION 8-3: PWM RESOLUTION

$$Resolution = \frac{\log[4(PR2 + 1)]}{\log(2)}\ bits$$

Note:	If the PWM duty cycle value is longer than the PWM period, the assigned PWM pin(s) will remain unchanged.

TABLE 8-3: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 20 MHz)

PWM Frequency	1.22 kHz(1)	4.88 kHz(1)	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

Note 1: Changing duty cycle will cause a glitch.

9.2 Comparator Outputs

The comparator outputs are read through the CM1CON0, COM2CON0 or CM2CON1 registers. CM1CON0 and CM2CON0 each contain the individual comparator output of Comparator 1 and Comparator 2, respectively. CM2CON2 contains a mirror copy of both comparator outputs facilitating a simultaneous read of both comparators. These bits are read-only. The comparator outputs may also be directly output to the RA2/AN2/T0CKI/INT/C1OUT and RC4/C2OUT/PH2 I/O pins. When enabled, multiplexers in the output path of the RA2 and RC4 pins will switch and the output of each pin will be the unsynchronized output of the comparator. The uncertainty of each of the comparators is related to the input offset voltage and the response time given in the specifications. Figure 9-1 and Figure 9-2 show the output block diagrams for Comparators 1 and 2, respectively.

The TRIS bits will still function as an output enable/ disable for the RA2/AN2/T0CKI/INT/C1OUT and RC4/ C2OUT/PH2 pins while in this mode.

The polarity of the comparator outputs can be changed using the C1POL and C2POL bits of the CMxCON0 Register.

Timer1 gate source can be configured to use the T1G pin or Comparator 2 output as selected by the T1GSS bit of the CM2CON1 Register. The Timer1 gate feature can be used to time the duration or interval of analog events. The output of Comparator 2 can also be synchronized with Timer1 by setting the C2SYNC bit of the CM2CON1 Register. When enabled, the output of Comparator 2 is latched on the falling edge of the Timer1 clock source. If a prescaler is used with Timer1, Comparator 2 is latched after the prescaler. To prevent a race condition, the Comparator 2 output is latched on the falling edge of the Timer1 clock source and Timer1 increments on the rising edge of its clock source. See the Comparator 2 Block Diagram (Figure 9-2) and the Timer1 Block Diagram (Figure 6-1) for more information.

It is recommended to synchronize Comparator 2 with Timer1 by setting the C2SYNC bit when Comparator 2 is used as the Timer1 gate source. This ensures Timer1 does not miss an increment if Comparator 2 changes during an increment.

9.3 Comparator Interrupts

The comparator interrupt flags are set whenever there is a change in the output value of its respective comparator. Software will need to maintain information about the status of the output bits, as read from CM2CON0<7:6>, to determine the actual change that has occurred. The CxIF bits, PIR1<4:3>, are the Comparator Interrupt Flags. Each comparator interrupt bit must be reset in software by clearing it to '0'. Since it is also possible to write a '1' to this register, a simulated interrupt may be initiated.

The CxIE bits of the PIE1 Register and the PEIE bit of the INTCON Register must be set to enable the interrupts. In addition, the GIE bit must also be set. If any of these bits are cleared, the interrupt is not enabled, though the CxIF bits will still be set if an interrupt condition occurs.

The comparator interrupt of the PIC16F785/HV785 differs from previous designs in that the interrupt flag is set by the mismatch edge and not the mismatch level. This means that the interrupt flag can be reset without the additional step of reading or writing the CMxCON0 register to clear the mismatch registers. When the mismatch registers are not cleared, an interrupt will not occur when the comparator output returns to the previous state. When the mismatch registers are cleared, an interrupt will occur when the comparator returns to the previous state.

Note 1: If a change in the CMxCON0 register (CxOUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CxIF of the PIR1 Register interrupt flag may not get set.

2: When either comparator is first enabled, bias circuitry in the Comparator module may cause an invalid output from the comparator until the bias circuitry is stable. Allow about 1 μs for bias settling then clear the mismatch condition and interrupt flags before enabling comparator interrupts.

9.4 Effects of Reset

A Reset forces all registers to their Reset state. This disables both comparators.

13.8 PWM Configuration

When configuring the Two-Phase PWM, care must be taken to avoid active output levels from the PH1 and PH2 pins before the PWM is fully configured. The following sequence is suggested before the TRISC register or any of the Two-Phase PWM control registers are first configured:

- Output inactive (OFF) levels to the PORTC RC1/AN5/C12IN1-/PH1 and RC4/C2OUT/PH2 pins.
- Clear TRISC bits 1 and 4 to configure the PH1 and PH2 pins as outputs.
- Configure the PWMCLK, PWMPH1, PWMPH2, and PWMCON1 registers.
- Configure the PWMCON0 register.

EXAMPLE 13-1: PWM SETUP EXAMPLE

```
;Example to configure PH1 as a free running PWM output using the SYNC output as the duty cycle
;termination feedback.
;This requires an external connection between the SYNC output and the comparator input.
;SYNC out = RB7 on pin 10
;C1 inverting input = RC2/AN6 on pin 14

;Configure PH1, PH2 and SYNC pins as outputs
;First, ensure output latches are low
    BCF     PORTC,1         ;PH1 low
    BCF     PORTC,4         ;PH2 low
    BCF     PORTB,7         ;SYNC low
;Configure the I/Os as outputs
    BANKSEL  TRISB
    BCF     TRISC,1         ;PH1 output
    BCF     TRISC,4         ;PH2 output
    BCF     TRISB,7         ;SYNC output
;PH1 shares its function with AN5
;Configure AN5 as digital I/O
    BCF     ANSEL0,5        ;AN5 is digital, all others default as analog
;Configure the PWM but don't enable PH1 or PH2 yet
    BANKSEL  PWMCLK
;PWM control setup
    MOVLW   B'00001100'     ;auto shutdown off, no blanking, SYNC on, PH1 and PH2 off
    MOVWF   PWMCON0         ;see data sheet page 93
;PWM clock setup
    MOVLW   B'00111101'     ;pwm_clk = Fosc, 30 clocks in PWM period
    MOVWF   PWMCLK          ;see data sheet page 94
;PH1 setup
    MOVLW   B'00101111'     ;non-inverted, terminate on C1, Start on clock 15
    MOVWF   PWMPH1          ;see data sheet page 95
;PH2 setup
    MOVLW   B'00110101'     ;non-inverted, terminate on C1, Start on clock 21
    MOVWF   PWMPH2          ;see data sheet page 96
;Configure Comparator 1
    MOVLW   B'10011110'     ;C1 on, internal, inverted, normal speed, +:C1VREF, -:AN6
    MOVWF   CM1CON0         ;see data sheet page 68
;Configure comparator voltage reference
    BANKSEL  VRCON
    MOVLW   B'10101100'     ;C1VREN on, low range, CVREF= VDD/2
    MOVWF   VRCON           ;see data sheet page 72
;Everything is setup at this point so now it is time to enable PH1
    BANKSEL  PWMCON0
    BSF     PWMCON0,PH1EN  ;enable PH1
;Module is running autonomously at this point
```

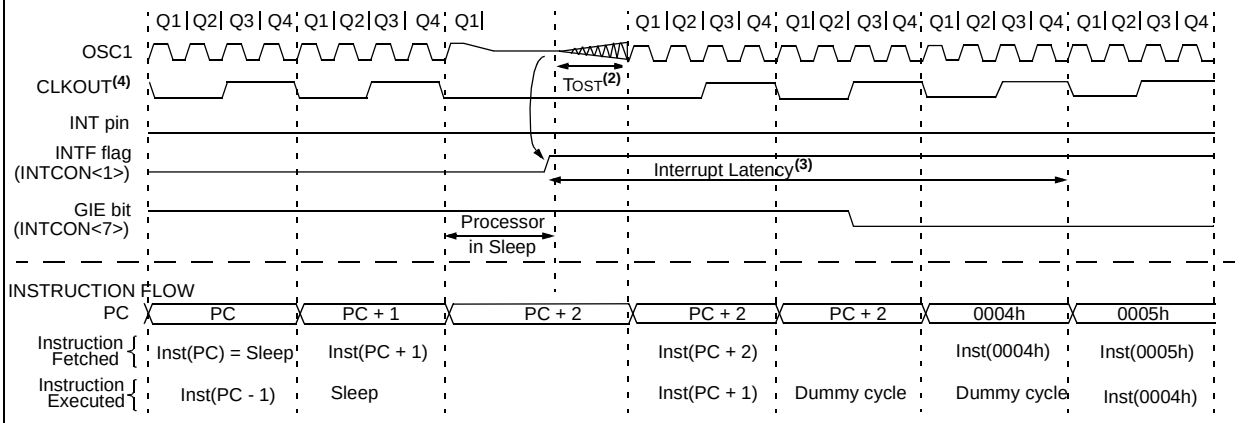
TABLE 15-5: INITIALIZATION CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	0001 1xxx	---1 --0x
$\overline{MCLR}$ Reset during normal operation	000h	000u uuuu	---u --uu
$\overline{MCLR}$ Reset during Sleep	000h	0001 0uuu	---u --uu
WDT Reset	000h	0000 uuuu	---u --uu
WDT Wake-up	PC + 1	uuu0 0uuu	---u --uu
Brown-out Reset	000h	0001 1uuu	---1 --u0
Interrupt Wake-up from Sleep	PC + 1(1)	uuu1 0uuu	---u --uu

Legend: u = unchanged, x = unknown, – = unimplemented bit, reads as '0'.

Note 1: When the wake-up is due to an interrupt and global enable bit GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

FIGURE 15-10: WAKE-UP FROM SLEEP THROUGH INTERRUPT(1)



Note 1: XT, HS or LP Oscillator mode assumed.

2: TOST = 1024TOSC (drawing not to scale). This delay does not apply to EC, RC and INTOSC Oscillator modes or Two-Speed Start-up (see **Section 3.6 "Two-Speed Clock Start-up Mode"**).

3: GIE = 1 assumed. In this case after wake-up, the processor jumps to 0004h. If GIE = 0, execution will continue in-line.

4: CLKOUT is not available in XT, HS, LP or EC Oscillator modes, but shown here for timing reference.

15.7 Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out using ICSP™ for verification purposes.

Note:	If the code protection is turned off, the entire data EEPROM and Flash program memory will be erased by performing a bulk erase command. See the "PIC16F785/HV785 *Memory Programming Specification*" (DS41237) for more information.

15.8 ID Locations

Four memory locations (2000h-2003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution, but are readable and writable during Program/Verify. Only the Least Significant 7 bits of the ID locations are used.

15.9 In-Circuit Serial Programming™ (ICSP™)

The PIC16F785/HV785 microcontrollers can be serially programmed while in the end application circuit. This is simply done with five lines:

- Clock
- Data
- Power
- Ground
- Programming voltage

This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware, or a custom firmware, to be programmed.

The device is placed into a Program/Verify mode by holding the RA0 and RA1 pins low, while raising the MCLR (VPP) pin from VIL to VIHH. See the "PIC16F785/HV785 *Memory Programming Specification*" (DS41237) for more information. RA0 becomes the programming data and RA1 becomes the programming clock. Both RA0 and RA1 are Schmitt Trigger inputs in this mode.

After Reset, to place the device into Program/Verify mode, the Program Counter (PC) is at location 00h. A 6-bit command is then supplied to the device. Depending on the command, 14 bits of program data are then supplied to or from the device, depending on whether the command was a load or a read. For complete details of serial programming, please refer to the "PIC16F785/HV785 *Memory Programming Specification*" (DS41237).

A typical In-Circuit Serial Programming connection is shown in Figure 15-11.

17.2 Instruction Descriptions

ADDLW	Add Literal and W
Syntax:	[*label*] ADDLW k
Operands:	$0 \le k \le 255$
Operation:	(W) + k → (W)
Status Affected:	C, DC, Z
Description:	The contents of the W register are added to the eight-bit literal 'k' and the result is placed in the W register.

ADDWF	Add W and f
Syntax:	[*label*] ADDWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) + (f) → (destination)
Status Affected:	C, DC, Z
Description:	Add the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

ANDLW	AND Literal with W
Syntax:	[*label*] ANDLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .AND. (k) → (W)
Status Affected:	Z
Description:	The contents of W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.

ANDWF	AND W with f
Syntax:	[*label*] ANDWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) .AND. (f) → (destination)
Status Affected:	Z
Description:	AND the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

BCF	Bit Clear f
Syntax:	[*label*] BCF f,b
Operands:	$0 \le f \le 127$ $0 \le b \le 7$
Operation:	0 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

BSF	Bit Set f
Syntax:	[*label*] BSF f,b
Operands:	$0 \le f \le 127$ $0 \le b \le 7$
Operation:	1 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is set.

19.1 DC Characteristics: PIC16F785/HV785-I (Industrial), PIC16F785/HV785-E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VDD	**Supply Voltage(2)**					FOSC ≤ 4 MHz:
D001			2.0	—	5.5	V	PIC16F785 with A/D off
D001A			2.2	—	5.5	V	PIC16F785 with A/D on, 0°C to +125°C
D001B			2.5	—	5.5	V	PIC16F785 with A/D on, -40°C to +125°C
D001C			3.0	—	5.5	V	4 MHz ≤ FOSC ≤ 10 MHz
D001D			4.5	—	5.5	V	10 MHz ≤ FOSC ≤ 20 MHz
D002	VDR	**RAM Data Retention Voltage(1)**	1.5*	—	—	V	Device in Sleep mode
D003	VPOR	VDD voltage above which the internal **POR releases**	—	1.8	—	V	See **Section 15.2.1 "Power-On Reset"** for details.
D003A	VPARM	VDD voltage below which the internal **POR rearms**	—	1.0	—	V	See **Section 15.2.1 "Power-On Reset"** for details.
D004	SVDD	VDD **Rise Rate** to ensure internal Power-on Reset signal	0.05*	—	—	V/ms	See **Section 15.2.1 "Power-On Reset"** for details.
D005	VBOR	**Brown-out Reset**	—	2.1	—	V	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

2: Maximum supply voltage is VSHUNT for PIC16HV785 device (see Table 19-14).

19.4 DC Characteristics: PIC16F785/HV785-I (Industrial), PIC16F785/HV785-E (Extended) (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Capacitive Loading Specs on Output Pins					
D100	COSC2	OSC2 pin	—	—	15*	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101	CIO	All I/O pins	—	—	50*	pF	
		Data EEPROM Memory					
D120	ED	Byte Endurance	100K	1M	—	E/W	-40°C ≤ TA ≤ +85°C
D120A	ED	Byte Endurance	10K	100K	—	E/W	+85°C ≤ TA ≤ +125°C
D121	VDRW	VDD for Read/Write	VMIN	—	5.5	V	Using EECON1 to read/write VMIN = Minimum operating voltage
D122	TDEW	Erase/Write cycle time	—	5	6	ms	
D123	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated
D124	TREF	Number of Total Erase/Write Cycles before Refresh(4)	1M	10M	—	E/W	-40°C ≤ TA ≤ +85°C
		Program Flash Memory					
D130	EP	Cell Endurance	10K	100K	—	E/W	-40°C ≤ TA ≤ +85°C
D130A	EP	Cell Endurance	1K	10K	—	E/W	+85°C ≤ TA ≤ +125°C
D131	VPR	VDD for Read	VMIN	—	5.5	V	VMIN = Minimum operating voltage
D132	VPEW	VDD for Erase/Write	4.5	—	5.5	V	
D133	TPEW	Erase/Write cycle time	—	2	2.5	ms	
D134	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

2: Negative current is defined as current sourced by the pin.

3: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

4: See **Section 14.4.1 "Using the Data EEPROM"** on page 105.

19.5 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	$\overline{RD}$
cs	$\overline{CS}$	rw	$\overline{RD}$ or $\overline{WR}$
di	SDI	sc	SCK
do	SDO	ss	$\overline{SS}$
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	$\overline{MCLR}$	wr	$\overline{WR}$

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (High-impedance)	V	Valid
L	Low	Z	High-impedance

FIGURE 19-2: LOAD CONDITIONS

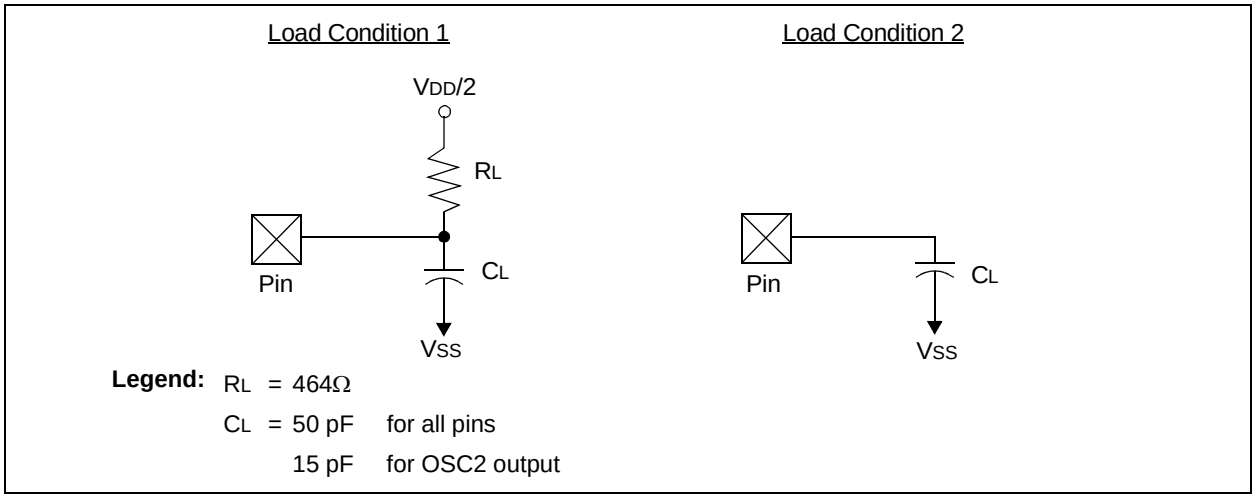


FIGURE 20-8: TYPICAL IDD vs. VDD OVER FOSC (EXTRC MODE)

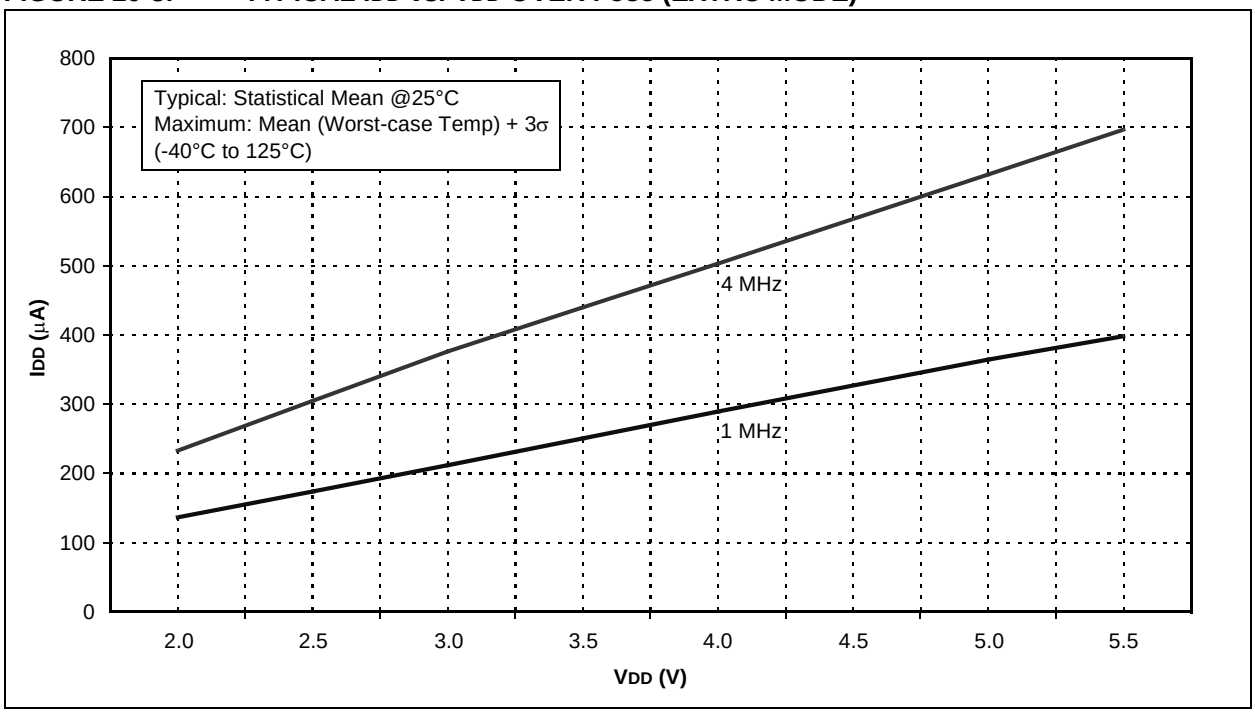


FIGURE 20-9: MAXIMUM IDD vs. VDD OVER FOSC (EXTRC MODE)

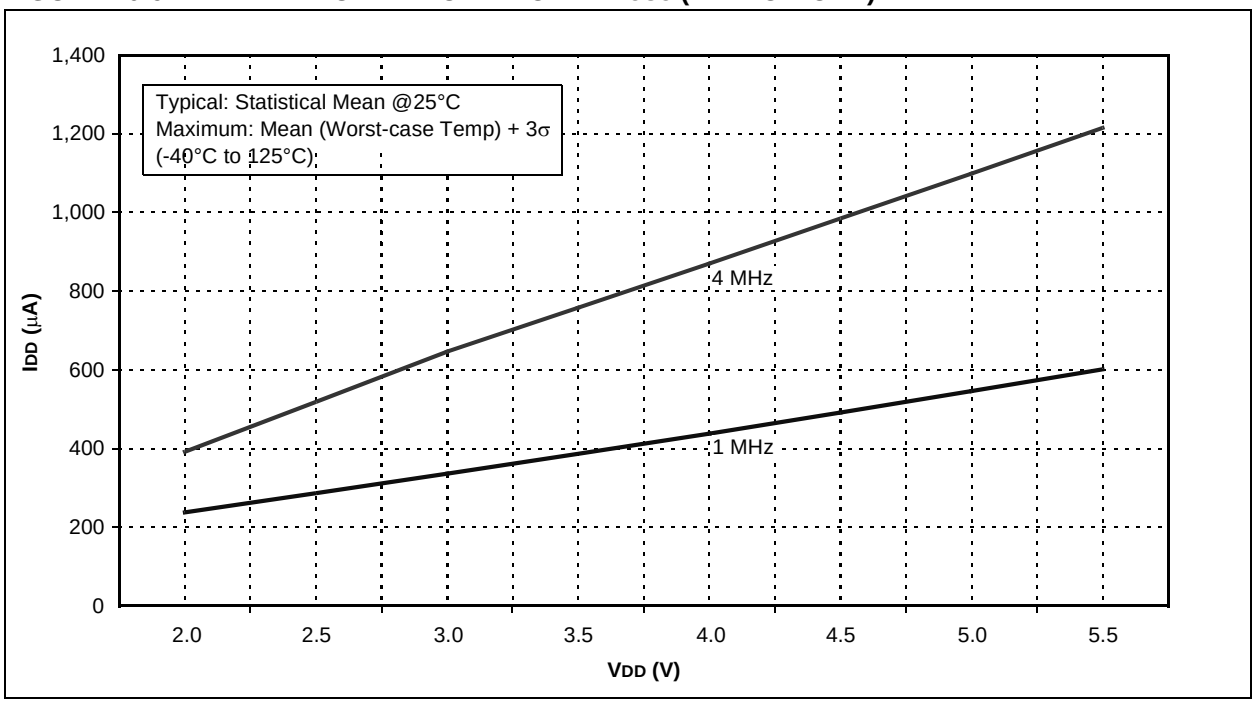


FIGURE 20-34: TYPICAL HFINTOSC FREQUENCY CHANGE vs. VDD (25°C)

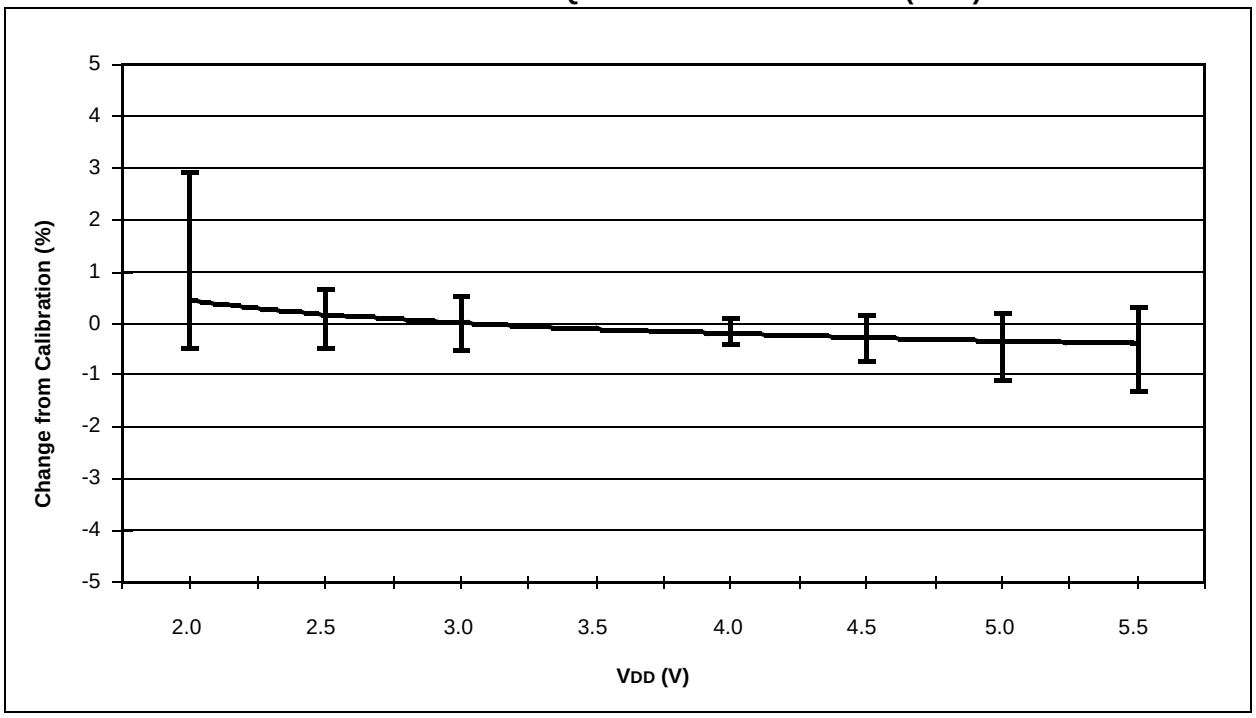
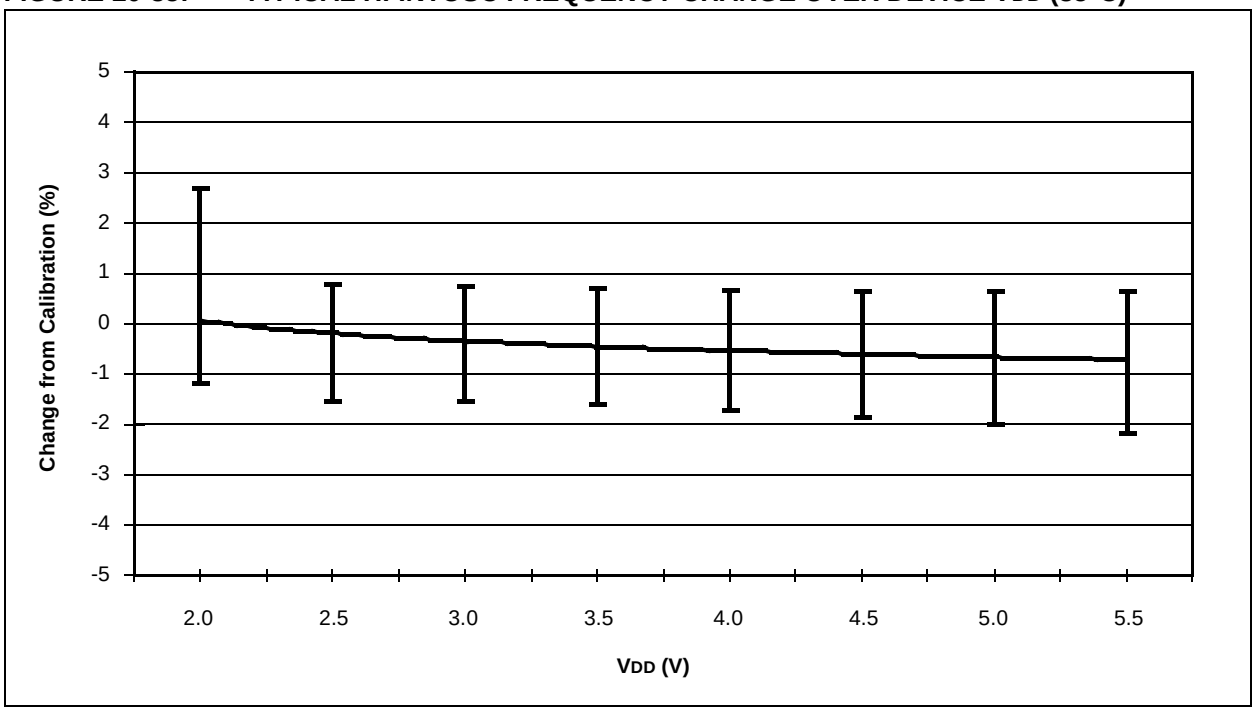


FIGURE 20-35: TYPICAL HFINTOSC FREQUENCY CHANGE OVER DEVICE VDD (85°C)



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