Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 14x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16hv785t-i-ss

2.4 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

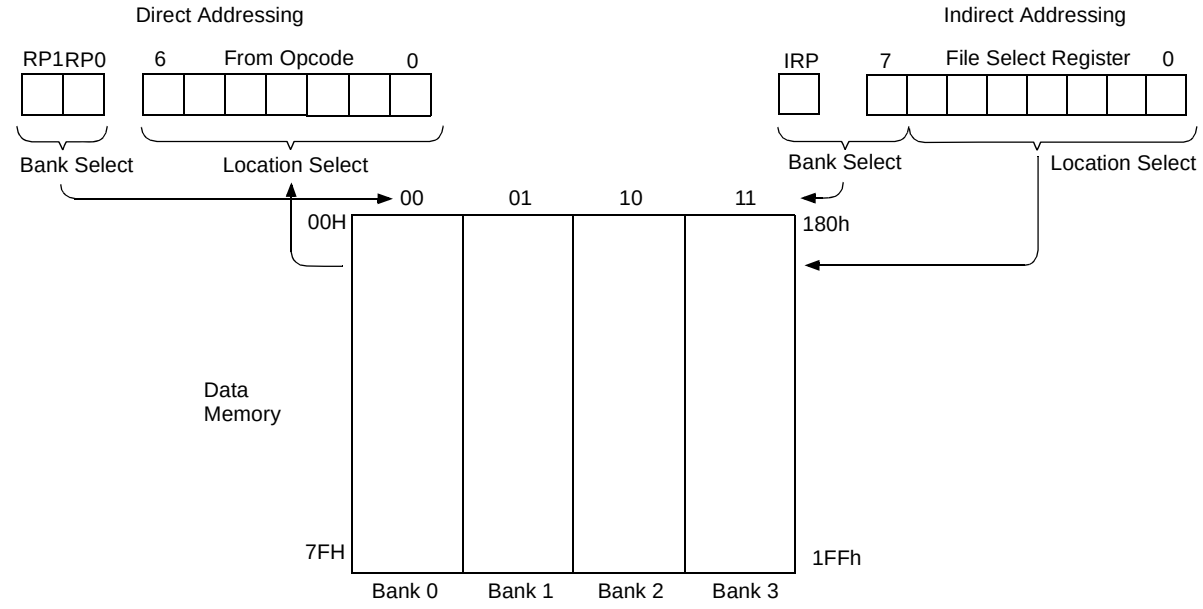
Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the File Select Register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no operation (although Status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR and the IRP bit in the STATUS Register, as shown in Figure 2-4.

A simple program to clear RAM location 20h-2Fh using indirect addressing is shown in Example 2-1.

EXAMPLE 2-1: INDIRECT ADDRESSING

```
     MOVLW  0x20   ;initialize pointer
     MOVWF  FSR    ;to RAM
NEXT CLRF   INDF   ;clear INDF register
     INCF   FSR    ;increment pointer
     BTFSS  FSR,4  ;all done?
     GOTO   NEXT   ;no clear next
CONTINUE           ;yes continue
```

FIGURE 2-4: DIRECT/INDIRECT ADDRESSING PIC16F785/HV785



Note: For memory map detail see Figure 2-2.

3.5 Clock Switching

The system clock source can be switched between external and internal clock sources via software using the System Clock Select (SCS) bit.

3.5.1 SYSTEM CLOCK SELECT (SCS) BIT

The System Clock Select (SCS) bit, in the OSCCON Register, selects the system clock source that is used for the CPU and peripherals.

- When SCS = 0, the system clock source is determined by configuration of the FOSC<2:0> bits in Configuration Word (CONFIG).
- When SCS = 1, the system clock source is chosen by the internal oscillator frequency selected by the IRCF bits. After a Reset, SCS is always cleared.

Note:	Any automatic clock switch, which may occur from Two-Speed Start-up or Fail-Safe Clock Monitor, does not update the SCS bit. The user can monitor the OSTS (OSCCON<3>) to determine the current system clock source.

3.5.2 OSCILLATOR START-UP TIME-OUT STATUS BIT

The Oscillator Start-up Time-out Status (OSTS) bit, (OSCCON<3>), indicates whether the system clock is running from the external clock source as defined by the FOSC bits, or from internal clock source. In particular, OSTS indicates that the Oscillator Start-up Timer (OST) has timed out for LP, XT or HS modes.

3.6 Two-Speed Clock Start-up Mode

Two-Speed Start-up mode provides additional power savings by minimizing the latency between external oscillator start-up and code execution. In applications that make heavy use of the Sleep mode, Two-Speed Start-up will remove the external oscillator start-up time from the time spent awake and can reduce the overall power consumption of the device.

This mode allows the application to wake-up from Sleep, perform a few instructions using the INTOSC as the clock source and go back to Sleep without waiting for the primary oscillator to become stable.

Note:	Executing a SLEEP instruction will abort the Oscillator Start-up Time and will cause the OSTS bit in the OSCCON Register to remain clear.

When the PIC16F785/HV785 is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) is enabled (see **Section 3.3.1 "Oscillator Start-up Timer (OST)"**). The OST timer will suspend program execution until 1024 oscillations are counted. Two-Speed Start-up mode minimizes the delay in code execution by operating from the internal oscillator as the OST is counting. When the OST count reaches 1024 and the OSTS bit in the OSCCON Register is set, program execution switches to the external oscillator.

3.6.1 TWO-SPEED START-UP MODE CONFIGURATION

Two-Speed Start-up mode is configured by the following settings:

- IESO = 1 (CONFIG<10>) Internal/External Switch Over bit.
- SCS = 0.
- FOSC configured for LP, XT or HS mode.

Two-Speed Start-up mode is entered after:

- Power-on Reset (POR) and, if enabled, after PWRT has expired, or
- Wake-up from Sleep.

If the external clock oscillator is configured to be anything other than LP, XT or HS mode, then Two-Speed Start-up is disabled. This is because the external clock oscillator does not require any stabilization time after POR or an exit from Sleep.

3.6.2 TWO-SPEED START-UP SEQUENCE

1. Wake-up from Power-on Reset or Sleep.
2. Instructions begin execution by the internal oscillator at the frequency set in the IRCF bits (in the OSCCON Register.
3. OST enabled to count 1024 clock cycles.
4. OST timed out, wait for falling edge of the internal oscillator.
5. OSTS is set.
6. System clock held low until the next falling edge of new clock (LP, XT or HS mode).
7. System clock is switched to external clock source.

3.6.3 CHECKING EXTERNAL/INTERNAL CLOCK STATUS

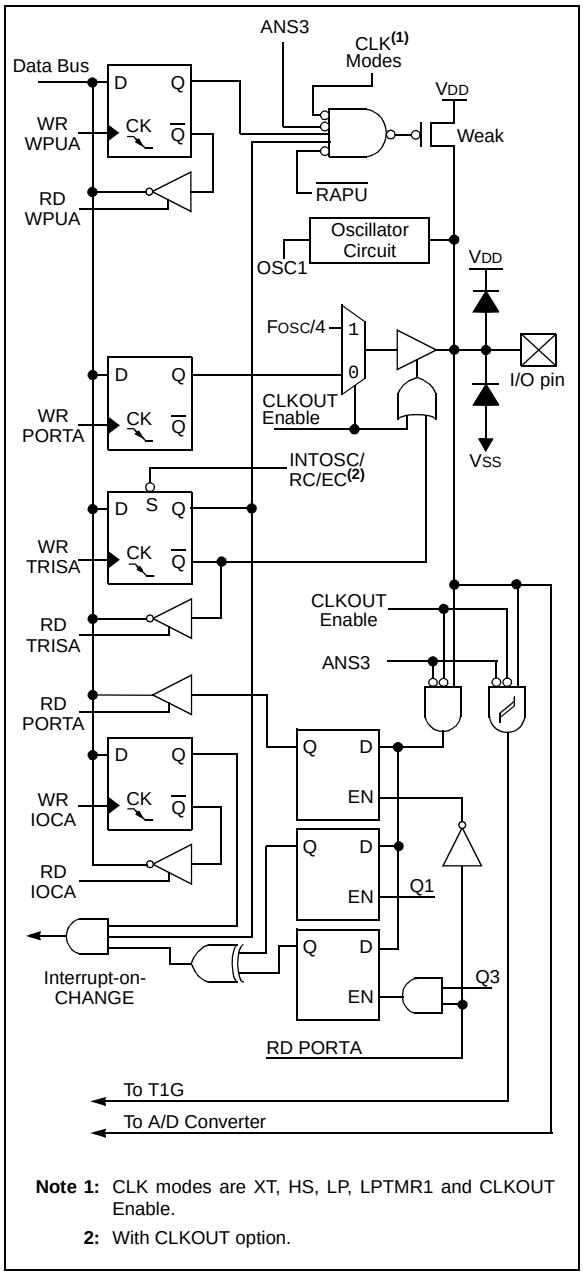
Checking the state of the OSTS bit in the OSCCON Register) will confirm if the PIC16F785/HV785 is running from the external clock source as defined by the FOSC bits in the Configuration Word (CONFIG) or the internal oscillator.

4.2.3.5 RA4/AN3/T1G/OSC2/CLKOUT

Figure 4-5 shows the diagram for this pin. The RA4 pin is configurable to function as one of the following:

- General purpose I/O
- Analog input for the A/D
- TMR1 gate input
- Crystal/resonator connection
- Clock output

FIGURE 4-5: BLOCK DIAGRAM OF RA4



Note 1: CLK modes are XT, HS, LP, LPTMR1 and CLKOUT Enable.

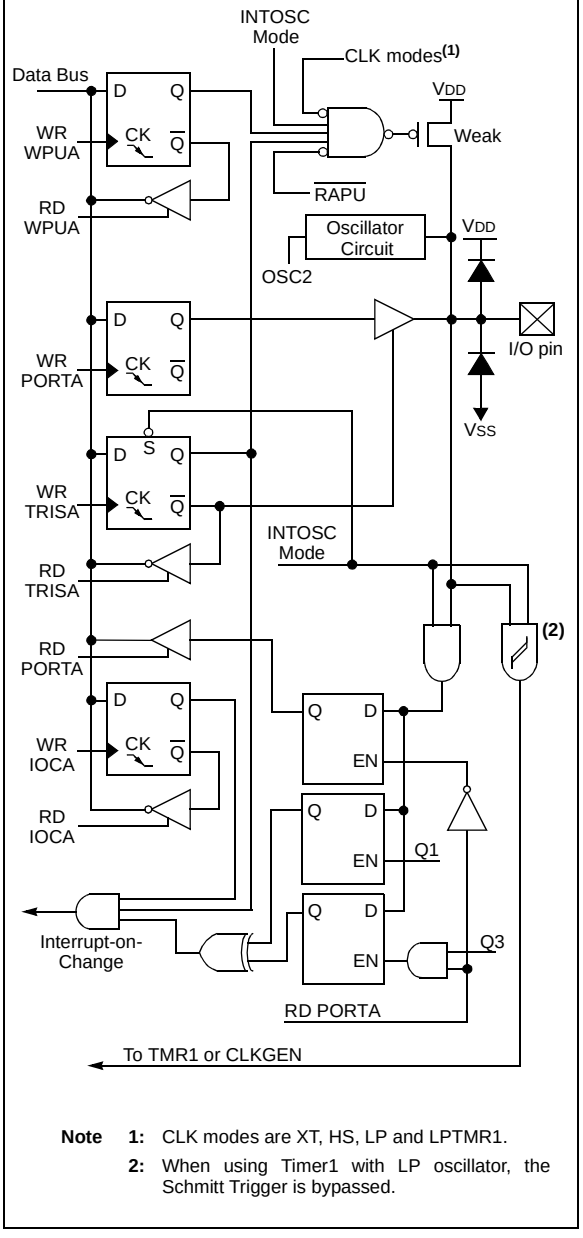
2: With CLKOUT option.

4.2.3.6 RA5/T1CKI/OSC1/CLKIN

Figure 4-6 shows the diagram for this pin. The RA5 pin is configurable to function as one of the following:

- General purpose I/O
- TMR1 clock input
- Crystal/resonator connection
- Clock input

FIGURE 4-6: BLOCK DIAGRAM OF RA5



Note 1: CLK modes are XT, HS, LP and LPTMR1.

2: When using Timer1 with LP oscillator, the Schmitt Trigger is bypassed.

4.3.1 PORTB PIN DESCRIPTIONS AND DIAGRAMS

Each PORTB pin is multiplexed with other functions. The pins and their combined functions are briefly described here. For specific information about individual functions such as the PWM, operational amplifier, or the A/D, refer to the appropriate section in this Data Sheet.

4.3.1.1 RB4/AN10/OP2-

The RB4/AN10/OP2- pin is configurable to function as one of the following:

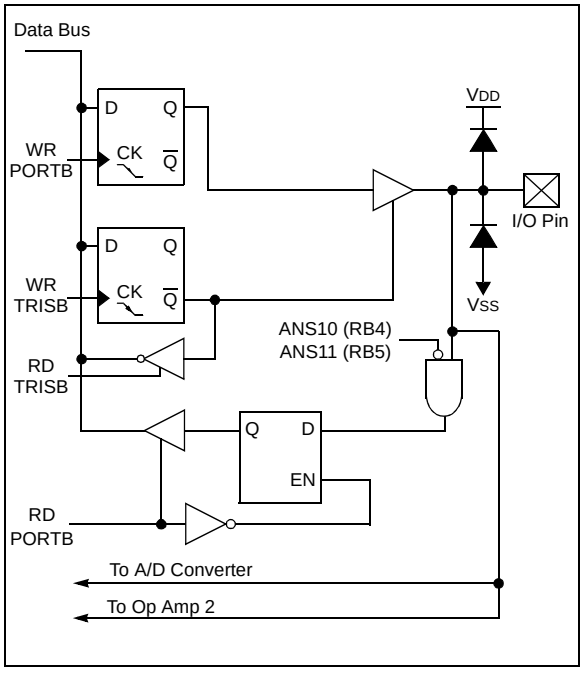
- General purpose I/O
- Analog input to the A/D
- Analog input to Op Amp 2

4.3.1.2 RB5/AN11/OP2+

The RB5/AN11/OP2+ pin is configurable to function as one of the following:

- General purpose I/O
- Analog input to the A/D
- Analog input to Op Amp 2

FIGURE 4-7: BLOCK DIAGRAM OF RB4 AND RB5

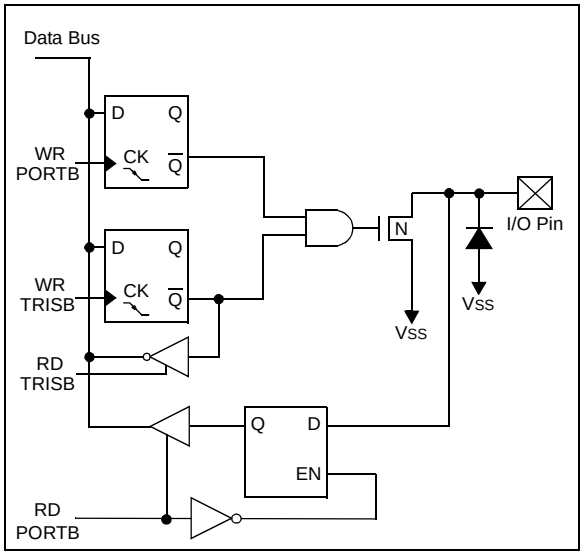


4.3.1.3 RB6

The RB6 pin is configurable to function as the following:

- Open drain general purpose I/O

FIGURE 4-8: BLOCK DIAGRAM OF RB6

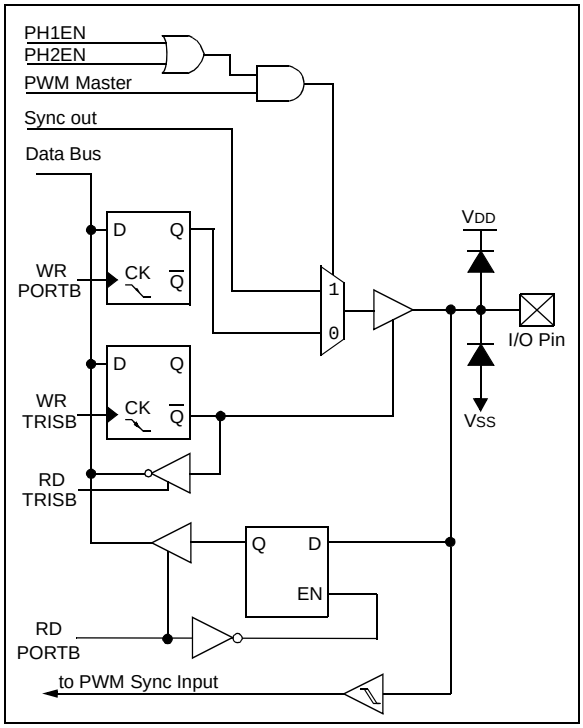


4.3.1.4 RB7/SYNC

The RB7/SYNC pin is configurable to function as one of the following:

- General purpose I/O
- PWM synchronization input and output

FIGURE 4-9: BLOCK DIAGRAM OF RB7



8.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPR1L register and to the DC1B<1:0> bits of the CCP1CON register. Up to 10 bits of resolution is available. The CCPR1L contains the eight MSbs and the DC1B<1:0> contains the two LSbs. In PWM mode, CCPR1H is a read-only register.

Equation 8-2 is used to calculate the PWM duty cycle in time.

EQUATION 8-2: PWM DUTY CYCLE

$$PWM\ duty\ cycle = (CCPR1L{:}CCP1CON\langle 5{:}4\rangle) \bullet T_{OSC} \bullet (TMR2\ prescale\ value)$$

CCPR1L and DC1B<1:0> can be written to at any time, but the duty cycle value is not latched into CCPR1H until after a match between PR2 and TMR2 occurs (i.e. the period is complete). In PWM mode, CCPR1H is a read-only register.

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

Because of the buffering, the module waits until the timer resets, instead of starting immediately. This means that enhanced PWM waveforms do not exactly match the standard PWM waveforms, but are instead offset by one full instruction cycle (4 TOSC).

When the CCPR1H and 2-bit latch match TMR2, concatenated with an internal 2-bit Q clock or 2 bits of the TMR2 prescaler, the RC5/CCP1 pin is cleared.

The maximum PWM resolution is a function of PR2 as shown by Equation 8-3.

EQUATION 8-3: PWM RESOLUTION

$$Resolution = \frac{\log[4(PR2 + 1)]}{\log(2)}\ bits$$

Note:	If the PWM duty cycle value is longer than the PWM period, the assigned PWM pin(s) will remain unchanged.

TABLE 8-3: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 20 MHz)

PWM Frequency	1.22 kHz(1)	4.88 kHz(1)	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

Note 1: Changing duty cycle will cause a glitch.

12.1 A/D Configuration and Operation

There are four registers available to control the functionality of the A/D module:

1. ANSEL0 (Register 12-1)
2. ANSEL1 (Register 12-2)
3. ADCON0 (Register 12-3)
4. ADCON1 (Register 12-4)

12.1.1 ANALOG PORT PINS

The ANS<11:0> bits, of the ANSEL1 and ANSEL0 Registers, and the TRISA<4,2:0>, TRISB<5:4> and TRISC<7:6,3:0>> bits control the operation of the A/D port pins. Set the corresponding TRISx bits to '1' to set the pin output driver to its high-impedance state. Likewise, set the corresponding ANSx bit to disable the digital input buffer.

Note:	Analog voltages on any pin that is defined as a digital input may cause the input buffer to conduct excess current.

12.1.2 CHANNEL SELECTION

There are fourteen analog channels on the PIC16F785/HV785. The CHS<3:0> bits of the ADCON0 Register control which channel is connected to the sample and hold circuit.

12.1.3 VOLTAGE REFERENCE

There are two options for the voltage reference to the A/D converter: either V_{DD} is used or an analog voltage applied to V_{REF} is used. The VCFG bit of the ADCON0 Register controls the voltage reference selection. If VCFG is set, then the voltage on the V_{REF} pin is the reference; otherwise, V_{DD} is the reference.

12.1.4 CONVERSION CLOCK

The A/D conversion cycle requires 11 T_{AD}. The source of the conversion clock is software selectable via the ADCS bits of the ADCON1 Register. There are seven possible clock options:

- F_{OSC}/2
- F_{OSC}/4
- F_{OSC}/8
- F_{OSC}/16
- F_{OSC}/32
- F_{OSC}/64
- F_{RC} (dedicated internal oscillator)

For correct conversion, the A/D conversion clock (1/T_{AD}) must be selected to ensure a minimum T_{AD} of 1.6 μs. Table 12-1 shows a few T_{AD} calculations for selected frequencies.

TABLE 12-1: T_{AD} VS. DEVICE OPERATING FREQUENCIES

A/D Clock Source (T_{AD})		Device Frequency			
Operation	**ADCS2:ADCS0**	**20 MHz**	**5 MHz**	**4 MHz**	**1.25 MHz**
2 T_{OSC}	000	100 ns(2)	400 ns(2)	500 ns(2)	1.6 μs
4 T_{OSC}	100	200 ns(2)	800 ns(2)	1.0 μs(2)	3.2 μs
8 T_{OSC}	001	400 ns(2)	1.6 μs	2.0 μs	6.4 μs
16 T_{OSC}	101	800 ns(2)	3.2 μs	4.0 μs	12.8 μs(3)
32 T_{OSC}	010	1.6 μs	6.4 μs	8.0 μs(3)	25.6 μs(3)
64 T_{OSC}	110	3.2 μs	12.8 μs(3)	16.0 μs(3)	51.2 μs(3)
A/D RC	x11	2-6 μs(1), (4)	2-6 μs(1), (4)	2-6 μs(1), (4)	2-6 μs(1), (4)

Legend: Shaded cells are outside of recommended range.

Note 1: The A/D RC source has a typical T_{AD} time of 4 μs for V_{DD} > 3.0V.

2: These values violate the minimum required T_{AD} time.

3: For faster conversion times, the selection of another clock source is recommended.

4: When the device frequency is greater than 1 MHz, the A/D RC clock source is only recommended if the conversion will be performed during Sleep.

NOTES:

13.0 TWO-PHASE PWM

The two-phase PWM (Pulse Width Modulator) is a stand-alone peripheral that supports:

- Single or dual-phase PWM
- Single complementary output PWM with overlap/ delay
- Sync input/output to cascade devices for additional phases

Setting either, or both, of the PH1EN or PH2EN bits of the PWMCON0 register will activate the PWM module (see Register 13-1). If PH1 is used then TRISC<1> must be cleared to configure the pin as an output. The same is true for TRISC<4> when using PH2. Both PH1EN and PH2EN must be set when using Complementary mode.

13.1 PWM Period

The PWM period is derived from the main clock (FOSC), the PWM prescaler and the period counter (see Figure 13-1). The prescale bits of the PWMP Register, (see Register 13-2) determine the value of the clock divider which divides the system clock (FOSC) to the pwm_clk. This pwm_clk is used to drive the PWM counter. In Master mode, the PWM counter is reset when the count reaches the period count of the PER Register, (see Register 13-2), which determines the frequency of the PWM. The relationship between the PWM frequency, prescale and period count is shown in Equation 13-1.

EQUATION 13-1: PWM FREQUENCY

$$PWM_{FREQ} = \frac{F_{OSC}}{(2^{PWMP} \bullet (PER + 1)}$$

The maximum PWM frequency is FOSC/2, since the period count must be greater than zero.

In Slave mode, the period counter is reset by the SYNC input, which is the master device period counter reset. For proper operation, the slave period count should be equal to or greater than that of the master.

13.2 PWM Phase

Each enabled phase output is driven active when the phase counter matches the corresponding PWM phase count in the PH Register (see Register 13-3 and Register 13-4). The phase output remains true until terminated by a feedback signal from either of the comparators or the auto-shutdown activates.

Phase granularity is a function of the period count value. For example, if PER<4:0> = 3, each output can be shifted in 90° steps (see Equation 13-2).

EQUATION 13-2: PHASE RESOLUTION

$$Phase_{DEG} = \frac{360}{(PER + 1)}$$

13.3 PWM Duty Cycle

Each PWM output is driven inactive, terminating the drive period, by asynchronous feedback through the internal comparators. The duty cycle resolution is in effect infinitely adjustable. Either or both comparators can be used to reset the PWM by setting the corresponding comparator enable bit (CxEN, see Register 13-3). Duty cycles of 100% can be obtained by suppressing the feedback which would otherwise terminate the pulse.

The comparator outputs can be “held off”, or blanked, by enabling the corresponding BLANK bit (BLANKx, see Register 13-1) for each phase. The blank bit disables the comparator outputs for 1/2 of a system clock (FOSC), thus ensuring at least TOSC/2 active time for the PWM output. Blanking avoids early termination of the PWM output which may result due to switching transients at the beginning of the cycle.

13.4 Master/Slave Operation

Multiple chips can operate together to achieve additional phases by operating one as the master and the others as slaves. When the PWM is configured as a master, the RB7/SYNC pin is an output and generates a high output for one pwm_clk period at the end of each PWM period (see Figure 13-4).

When the PWM is configured as a slave, the RB7/ SYNC pin is an input. The high input from a master in this configuration resets the PWM period counter which synchronizes the slave unit at the end of each PWM period. Proper operation of a slave device requires a common external FOSC clock source to drive the master and slave. The PWM prescale value of the slave device must also be identical to that of the master. As mentioned previously, the slave period count value must be greater than or equal to that of the master.

The PWM Counter will be reset and held at zero when both PH1EN and PH2EN of the PWMCON0 Register are false. If the PWM is configured as a slave, the PWM Counter will remain reset at zero until the first SYNC input is received.

REGISTER 13-3: PWMPH1: PWM PHASE 1 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POL	C2EN	C1EN	PH4	PH3	PH2	PH1	PH0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **POL:** PH1 Output Polarity bit
1 = PH1 Pin is active-low
0 = PH1 Pin is active-high

bit 6 **C2EN:** Comparator 2 Enable bit
When COMOD<1:0> = 00(1)
1 = PH1 is reset when C2OUT goes high
0 = PH1 ignores Comparator 2
When COMOD<1:0> = X1(1)
1 = Complementary drive terminates when C2OUT goes high
0 = Comparator 2 is ignored
When COMOD<1:0> = 10(1)
C2EN has no effect

bit 5 **C1EN:** Comparator 1 Enable bit
When COMOD<1:0> = 00(1)
1 = PH1 is reset when C1OUT goes high
0 = PH1 ignores Comparator 1
When COMOD<1:0> = X1(1)
1 = Complementary drive terminates when C1OUT goes high
0 = Comparator 1 is ignored
When COMOD<1:0> = 10(1)
C1EN has no effect

bit 4-0 **PH<4:0>:** PWM Phase bits
When COMOD<1:0> = 00(1)
00000 = PH1 starts 1 pwm_clk period after falling edge of SYNC pulse. All other PH1 delays are expressed relative to this time.
00001 = PH1 is delayed by 1 pwm_clk pulse
••••• = •••
11111 = PH1 is delayed by 31 pwm_clk pulses
When COMOD<1:0> = X1 or 1X(1)
00000 = Complementary drive starts 1 pwm_clk period after falling edge of SYNC pulse. All other delays are expressed relative to this time.
00001 = Complementary drive start is delayed by 1 pwm_clk pulse
••••• = •••
11111 = Complementary drive start is delayed by 31 pwm_clk pulses

Note 1: See PWMCON1 register (Register 13-5).

15.0 SPECIAL FEATURES OF THE CPU

The PIC16F785/HV785 has a host of features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving features and offer code protection.

These features are:

- Reset:
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Brown-out Reset (BOR)
- Interrupts
- Watchdog Timer (WDT)
- Oscillator selection
- Sleep
- Code protection
- ID Locations
- In-Circuit Serial Programming™ (ICSP™)

The PIC16F785/HV785 has two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 64 ms (nominal) on power-up only, designed to keep the part in Reset while the power supply stabilizes. There is also circuitry to reset the device if a brown-out occurs, which can use the Power-up Timer to provide at least a 64 ms Reset. With these three functions on-chip, most applications need no external Reset circuitry.

The Sleep mode is designed to offer a very low-current Power-down mode. The user can wake-up from Sleep through an external Reset, Watchdog Timer Wake-up or interrupt.

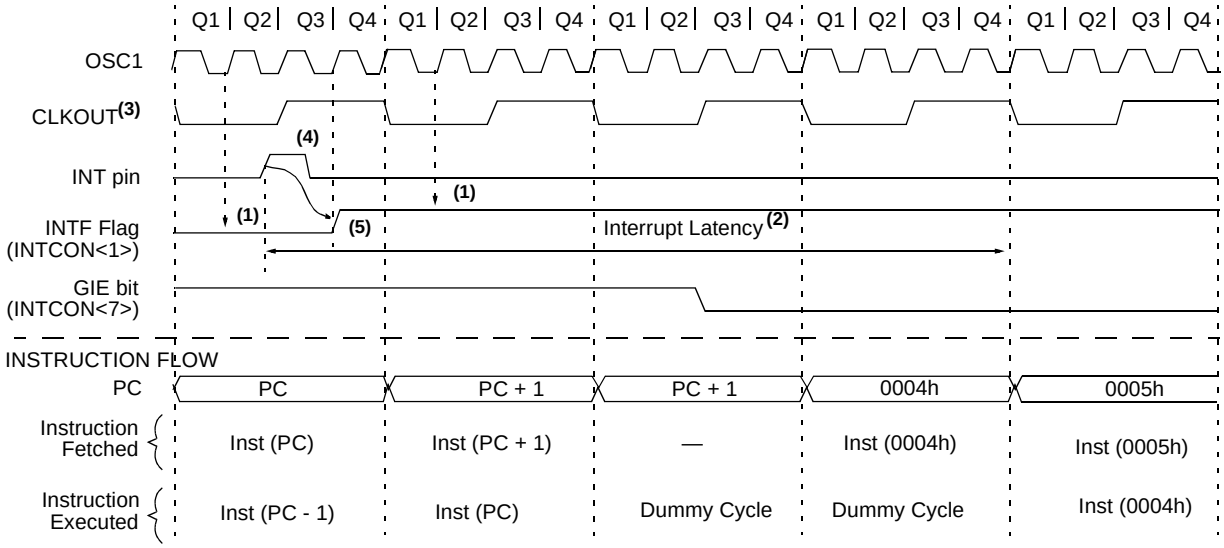
Several oscillator options are also made available to allow the part to fit the application. The INTOSC option saves system cost, while the LP crystal option saves power. A set of configuration bits are used to select various options (see Register 15.2).

15.1 Configuration Bits

The configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1') to select various device configurations as shown in Register 15.2. These bits are mapped in program memory location 2007h.

Note:	Address 2007h is beyond the user program memory space. It belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming. See "*PIC16F785/HV785 Memory Programming Specification*" (DS41237) for more information.

FIGURE 15-8: INT PIN INTERRUPT TIMING



Note 1: INTF flag is sampled here (every Q1).

2: Asynchronous interrupt latency = 3-4 TCY. Synchronous latency = 3 TCY, where TCY = instruction cycle time. Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.

3: CLKOUT is available only in INTOSC and RC Oscillator modes.

4: For minimum width of INT pulse, refer to AC specifications in **Section 19.0 "Electrical Specifications"**.

5: INTF is enabled to be set any time during the Q4-Q1 cycles.

TABLE 15-6: SUMMARY OF INTERRUPT REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
PIE1	EEIE	ADIE	CCP1IE	C2IE	C1IE	OSFIE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	EEIF	ADIF	CCP1IF	C2IF	C1IF	OSFIF	TMR2IF	TMR1IF	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, – = unimplemented read as '0', q = value depends upon condition. Shaded cells are not used by the Interrupt module.

REGISTER 15-2: WDTCON: WATCHDOG TIMER CONTROL REGISTER

U-0	U-0	U-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0
—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4-1 **WDTPS<3:0>:** Watchdog Timer Period Select bits

Bit Value = Prescale Rate

0000 = 1:32
0001 = 1:64
0010 = 1:128
0011 = 1:256
0100 = 1:512 (Reset value)
0101 = 1:1024
0110 = 1:2048
0111 = 1:4096
1000 = 1:8192
1001 = 1:16384
1010 = 1:32768
1011 = 1:65536
1100 = reserved
1101 = reserved
1110 = reserved
1111 = reserved

bit 0 **SWDTEN:** Software Enable or Disable the Watchdog Timer bit(1)

1 = WDT is turned on
0 = WDT is turned off (Reset value)

Note 1: If WDTE configuration bit = 1, then WDT is always enabled, irrespective of this control bit. If WDTE configuration bit = 0, then it is possible to turn WDT on/off with this control bit.

TABLE 15-8: SUMMARY OF WATCHDOG TIMER REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
OPTION_REG	$\overline{RAPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
STATUS	IRP	RP1	RPO	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
WDTCON	—	—	—	WDTPS3	WDTPS2	WSTPS1	WDTPS0	SWDTEN	---0 1000	---0 1000

Legend: Shaded cells are not used by the Watchdog Timer.
Note 1: See Register 15.2 for operation of all Configuration Word bits.

19.1 DC Characteristics: PIC16F785/HV785-I (Industrial), PIC16F785/HV785-E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VDD	**Supply Voltage(2)**					FOSC ≤ 4 MHz:
D001			2.0	—	5.5	V	PIC16F785 with A/D off
D001A			2.2	—	5.5	V	PIC16F785 with A/D on, 0°C to +125°C
D001B			2.5	—	5.5	V	PIC16F785 with A/D on, -40°C to +125°C
D001C			3.0	—	5.5	V	4 MHz ≤ FOSC ≤ 10 MHz
D001D			4.5	—	5.5	V	10 MHz ≤ FOSC ≤ 20 MHz
D002	VDR	**RAM Data Retention Voltage(1)**	1.5*	—	—	V	Device in Sleep mode
D003	VPOR	VDD voltage above which the internal **POR releases**	—	1.8	—	V	See **Section 15.2.1 "Power-On Reset"** for details.
D003A	VPARM	VDD voltage below which the internal **POR rearms**	—	1.0	—	V	See **Section 15.2.1 "Power-On Reset"** for details.
D004	SVDD	VDD **Rise Rate** to ensure internal Power-on Reset signal	0.05*	—	—	V/ms	See **Section 15.2.1 "Power-On Reset"** for details.
D005	VBOR	**Brown-out Reset**	—	2.1	—	V	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

2: Maximum supply voltage is VSHUNT for PIC16HV785 device (see Table 19-14).

FIGURE 20-24: VOL VS. IOL OVER TEMPERATURE (VDD = 5.0V)

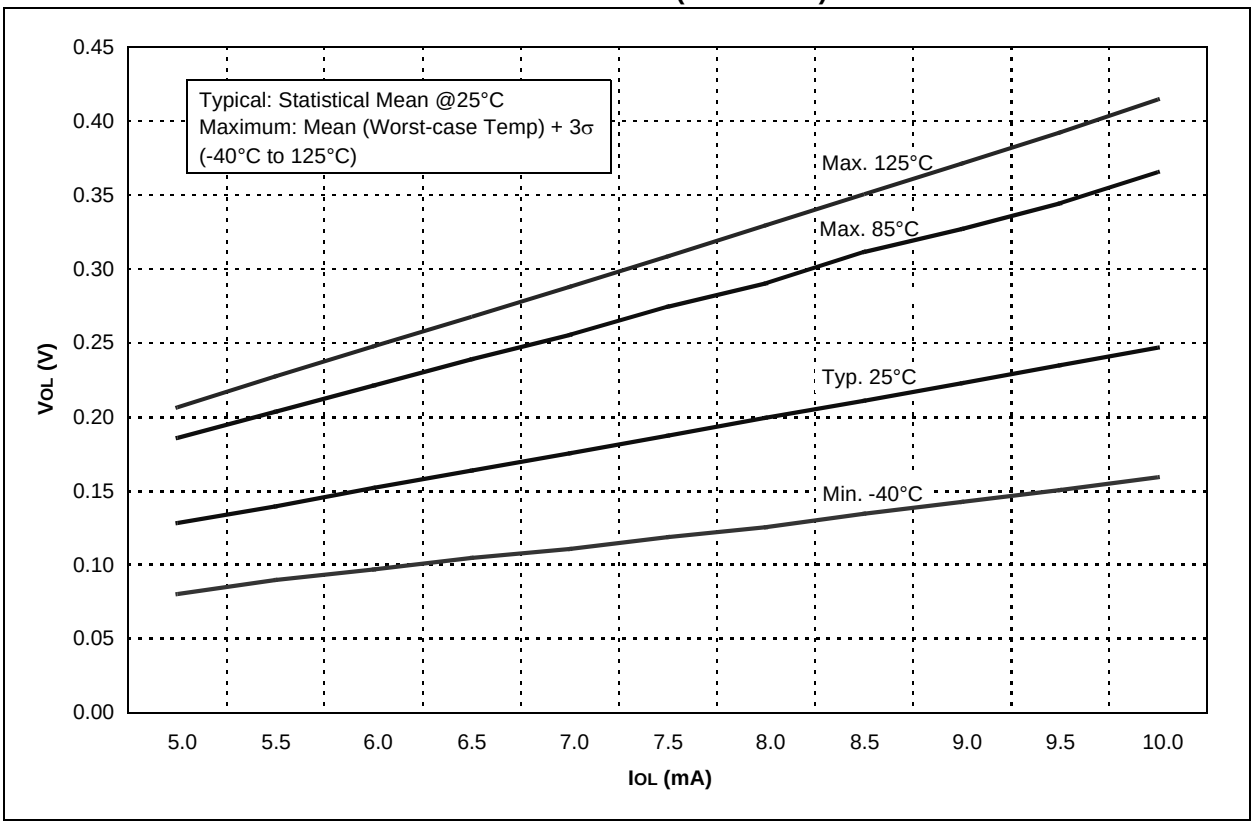


FIGURE 20-25: VOH VS. IOH OVER TEMPERATURE (VDD = 3.0V)

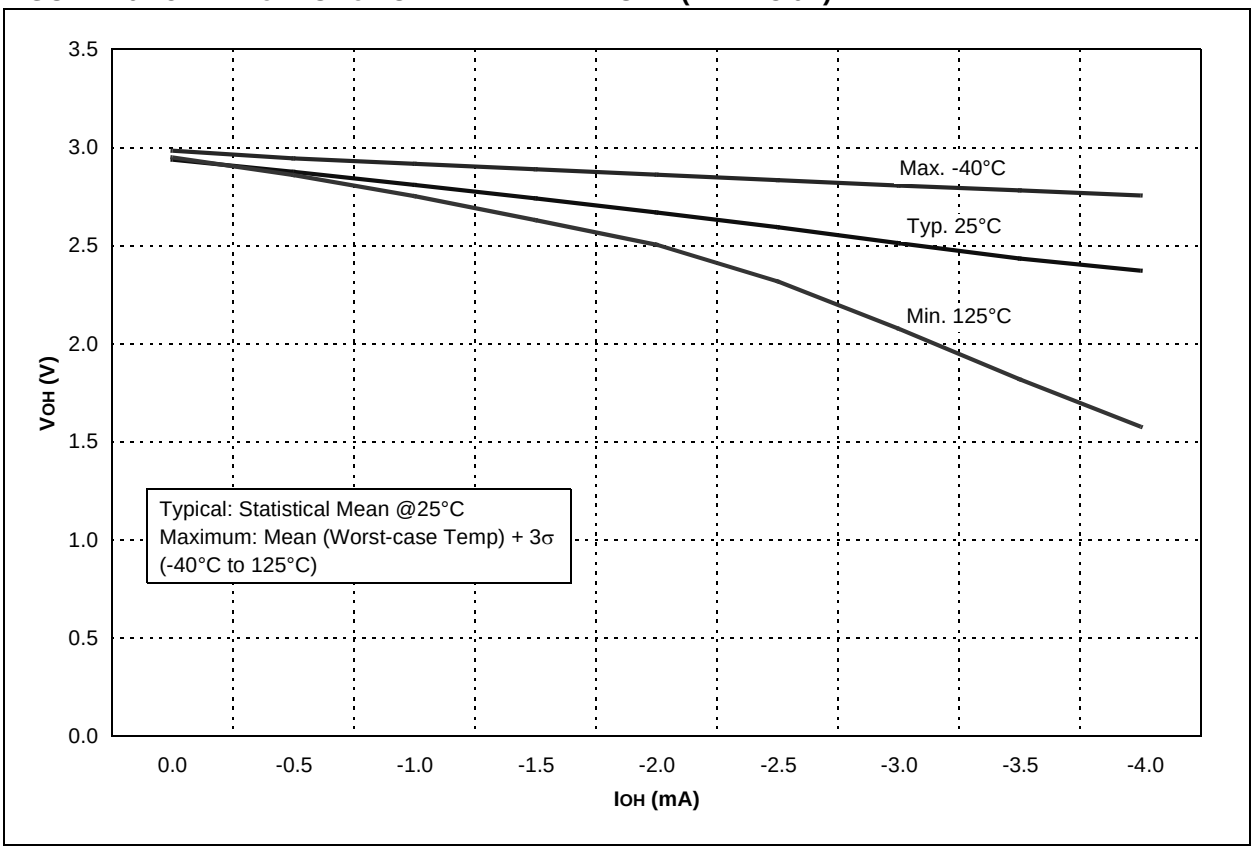


FIGURE 20-26: V_{OH} vs. I_{OH} OVER TEMPERATURE (V_{DD} = 5.0V)

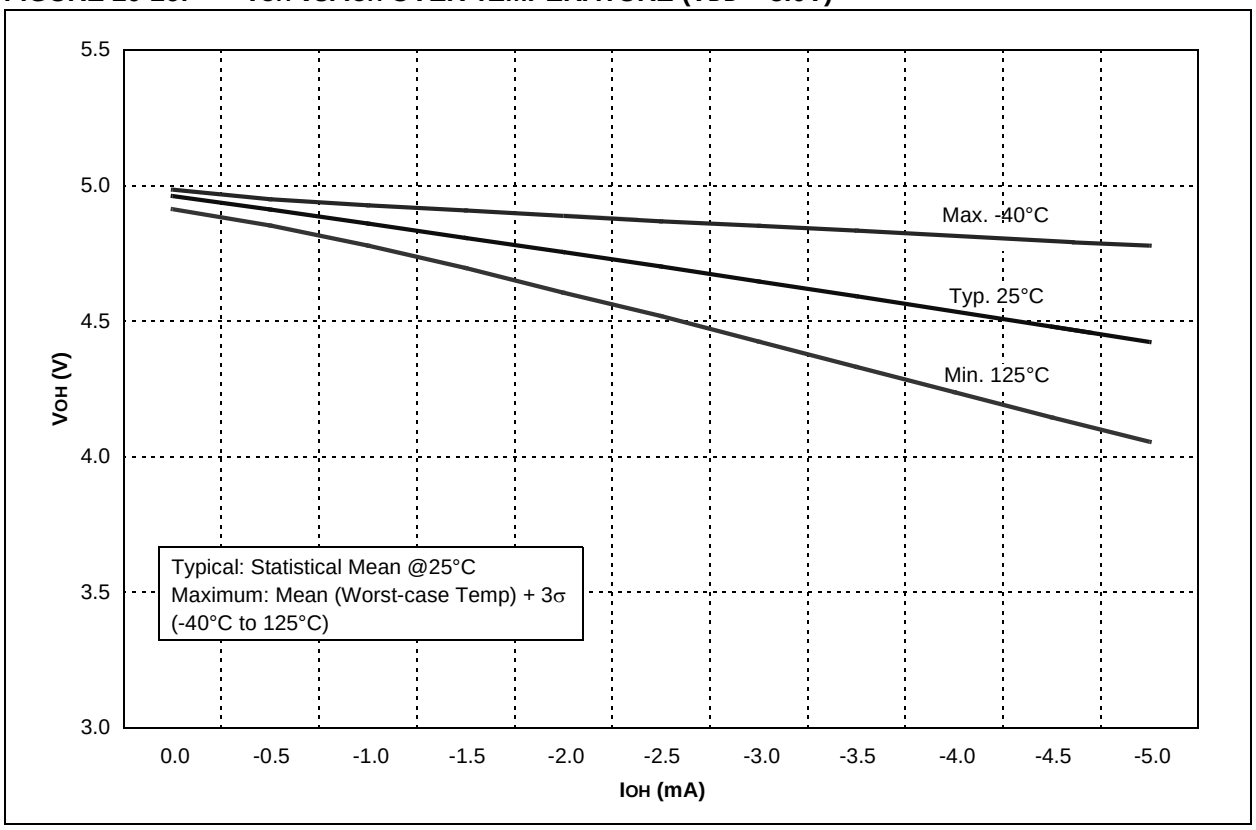


FIGURE 20-27: TTL INPUT THRESHOLD V_{IN} vs. V_{DD} OVER TEMPERATURE

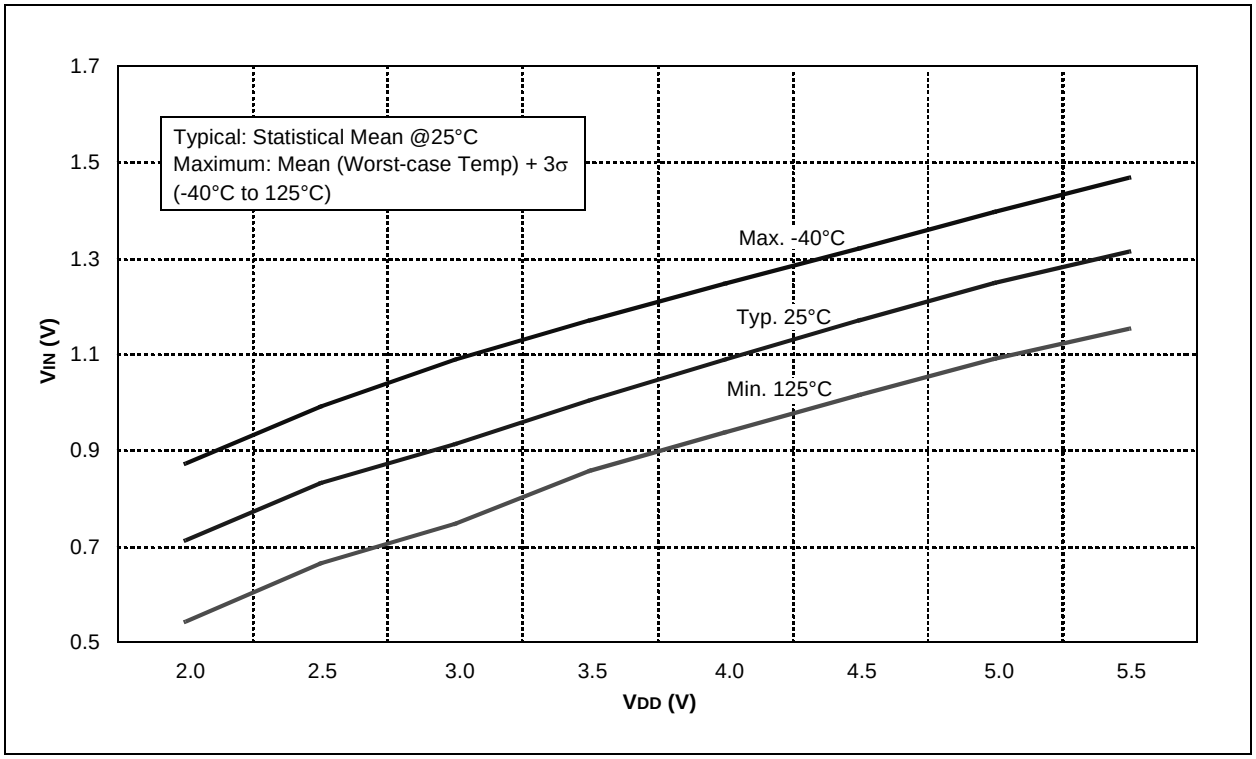


FIGURE 20-28: SCHMITT TRIGGER INPUT THRESHOLD VIN vs. VDD OVER TEMPERATURE

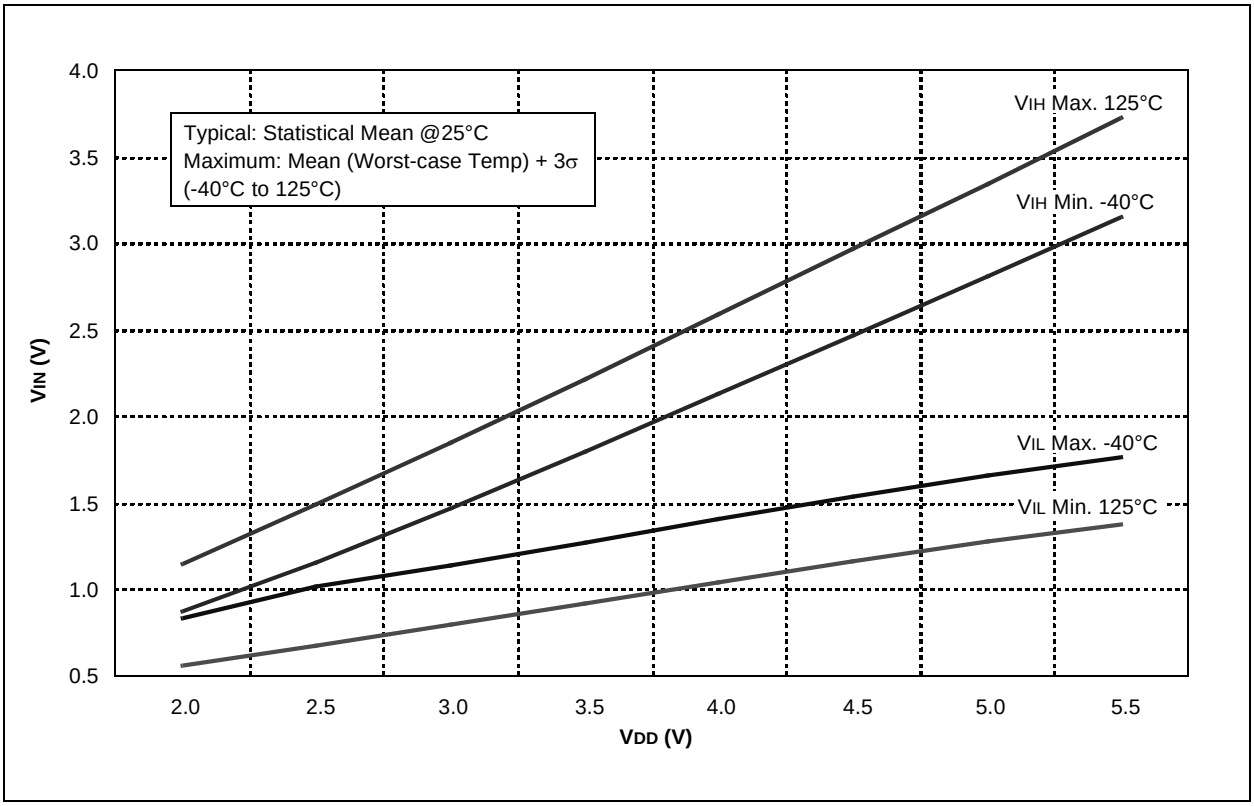
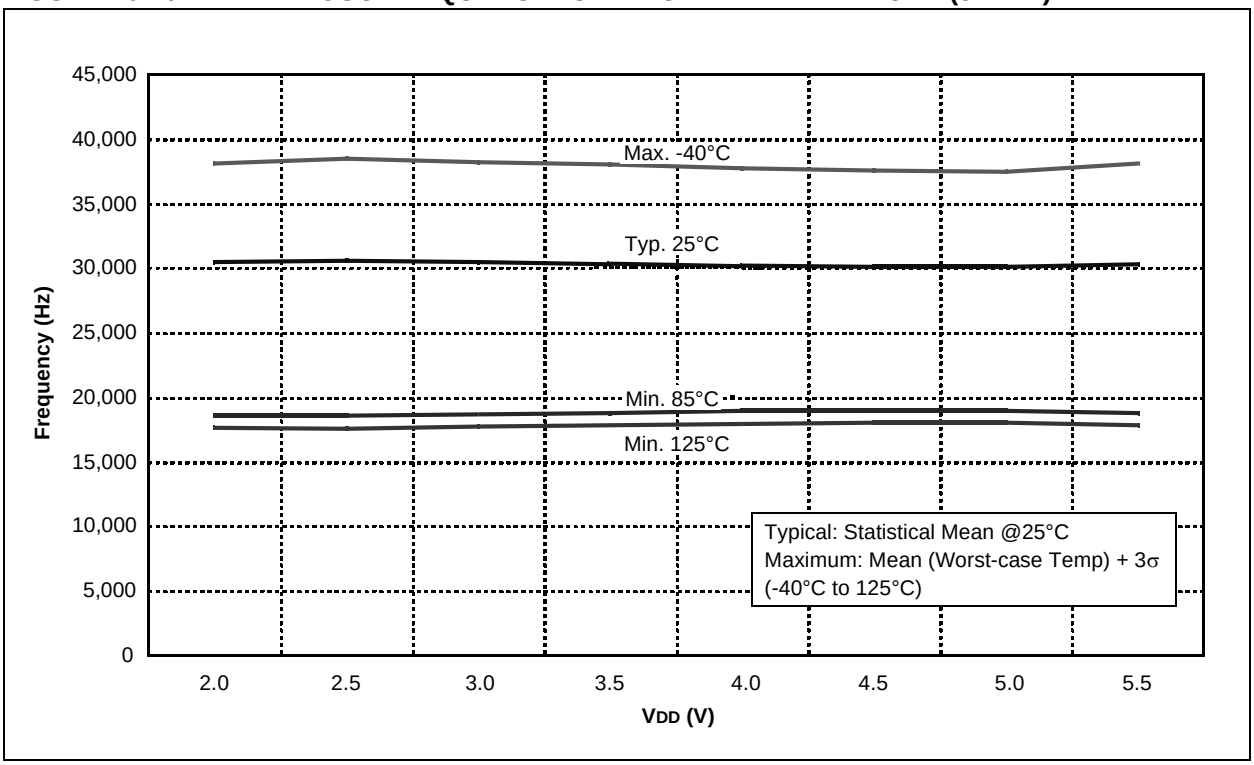


FIGURE 20-29: LFINTOSC FREQUENCY vs. VDD OVER TEMPERATURE (31 kHz)



APPENDIX A: DATA SHEET REVISION HISTORY

Revision A

This is a new data sheet.

Revision B

Updates throughout document.

Revision C

Revised part number to include “HV785”; Added PWM Setup Example; Added Voltage Regulator secton.

Revision D

Revised VROUT min./max. limits in Table 19-9.

Revision E

Adding Characterization Data and small updates and reformatting.

APPENDIX B: MIGRATING FROM OTHER PIC® DEVICES

This discusses some of the issues in migrating from the PIC16F684 PIC® device to the PIC16F785/HV785.

B.1 PIC16F684 to PIC16F785/HV785

TABLE B-1: FEATURE COMPARISON

Feature	PIC16F684	PIC16F785
Max Operating Speed	20 MHz	20 MHz
Max Program Memory (Words)	2048	2048
SRAM (bytes)	128	128
A/D Resolution	10-bit	10-bit
Data EEPROM (bytes)	256	256
Timers (8/16-bit)	2/1	2/1
Oscillator modes	8	8
Brown-out Reset	Y	Y
Internal Pull-ups	RA0/1/2/4/5 $\overline{\text{MCLR}}$	RA0/1/2/3/4/5 $\overline{\text{MCLR}}$
Interrupt-on-change	RA0/1/2/3/4/5	RA0/1/2/3/4/5
Comparator		2
CCP	ECCP	Y
Op Amps	N	2
PWM	N	Two-Phase
Ultra Low-Power Wake-up	Y	N
Extended WDT	Y	Y
Software Control Option of WDT/BOR	Y	Y
INTOSC Frequencies	32 kHz - 8 MHz	32 kHz - 8 MHz
Clock Switching	Y	Y

NOTES:

READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this document.

To: Technical Publications Manager Total Pages Sent _____

RE: Reader Response

From: Name _____

Company _____

Address _____

City / State / ZIP / Country _____

Telephone: (_____) _____ - _____ FAX: (_____) _____ - _____

Application (optional):

Would you like a reply? ___Y ___N

Device: PIC16F785/HV785 Literature Number: DS41249E

Questions:

1. What are the best features of this document?

2. How does this document meet your hardware and software development needs?

3. Do you find the organization of this document easy to follow? If not, why?

4. What additions to the document do you think would enhance the structure and subject?

5. What deletions from the document could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?