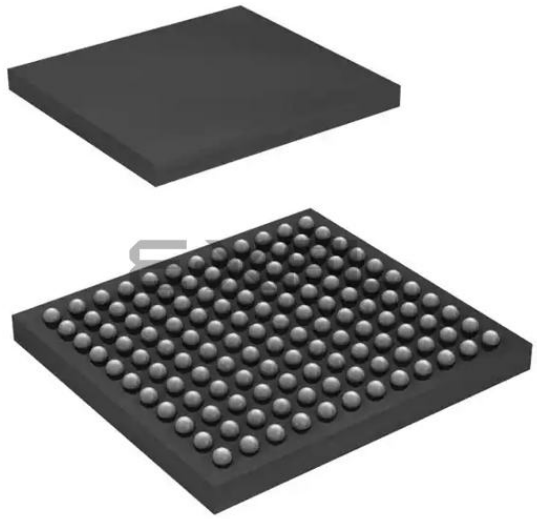
Lattice Semiconductor Corporation - ICE65L01F-LCB132C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

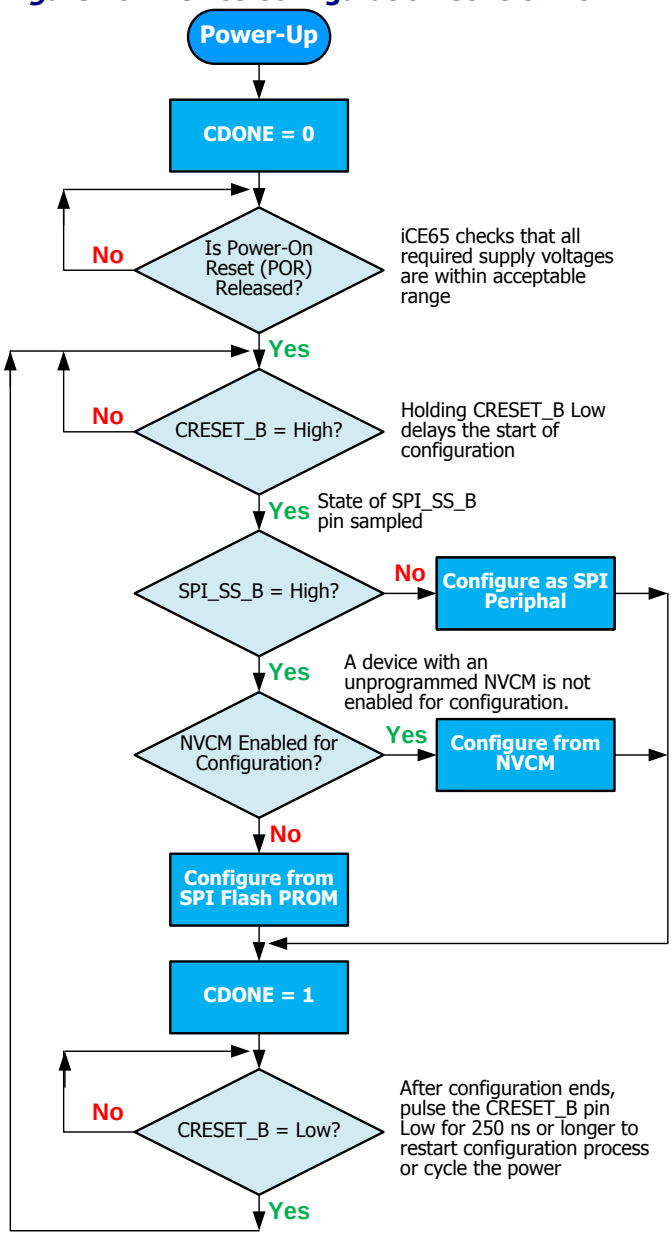
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	160
Number of Logic Elements/Cells	1280
Total RAM Bits	65536
Number of I/O	93
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	132-VFBGA, CSPBGA
Supplier Device Package	132-CSBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice65l01f-lcb132c

Figure 20: **Device Configuration Control Flow**



Configuration Image Size

Table 23 shows the number of memory bits required to configure an iCE65 device. Two values are provided for each device. The "Logic Only" value indicates the minimum configuration size, the number of bits required to configure only the logic fabric, leaving the RAM4K blocks uninitialized. The "Logic + RAM4K" column indicates the maximum configuration size, the number of bits to configure the logic fabric and to pre-initialize all the RAM4K blocks.

Table 21: **iCE65 Configuration Image Size (Kbits)**

Device	MINIMUM Logic Only (RAM4K not initialized)	MAXIUM Logic + RAM4K (RAM4K pre-initialized)
iCE65L01	181 Kbits	245 Kbits*
iCE65L04	453 Kbits	533 Kbits
iCE65L08	929 Kbits	1,057 Kbits

* Note: only 14 of the 16 RAM4K Memory Blocks may be pre-initialized in the iCE65L01.

Nonvolatile Configuration Memory (NVCM)

All standard iCE65 devices have an internal, nonvolatile configuration memory (NVCM). The NVCM is large enough to program a complete iCE65 device, including initializing all RAM4K block locations (MAXIMUM column in Table 23. The NVCM memory also has very high programming yield due to extensive error checking and correction (ECC) circuitry.

The NVCM is ideal for cost-sensitive, high-volume production applications, saving the cost and board space associated with an external configuration PROM. Furthermore, the NVCM provides exceptional design security, protecting critical intellectual property (IP). The NVCM contents are entirely contained within the iCE65 device and are not readable once protected by the one-time programmable Security bits. Furthermore, there is no observable difference between a programmed or un-programmed memory cell using optical or electron microscopy.

The NVCM memory has a programming interface similar to a 25-series SPI serial Flash PROM. Consequently, it can be programmed using standard device programmers before or after circuit board assembly or programmed in-system from a microprocessor or other intelligent controller. NVCM programming requires VCCIO_1, Bank 1 voltage to be applied on power-up, at the same time as other voltage supplies.

Configuration Control Signals

The iCE65 configuration process is self-timed and controlled by a few internal signals and device I/O pins, as described in Table 22.

Table 22: **iCE65 Configuration Control Signals**

Signal Name	Direction	Description
POR	Internal control	Internal Power-On Reset (POR) circuit.
OSC	Internal control	Internal configuration oscillator.
CRESET_B	Input	Configuration Reset input. Active-Low. No internal pull-up resistor.
CDONE	Open-drain Output	Configuration Done output. Permanent, weak pull-up resistor to VCCIO_2.

The Power-On Reset circuit, POR, automatically resets the iCE65 component to a known state during power-up (cold boot). The POR circuit monitors the relevant voltage supply inputs, as shown in Figure 22. Once all supplies exceed their minimum thresholds, the configuration controller can start the configuration process.

The configuration controller begins configuring the iCE65 device, clocked by the Internal Oscillator, OSC. The OSC oscillator continues controlling configuration unless the iCE65 device is configured using the SPI Peripheral Configuration Interface.

Figure 21: iCE65 Configuration Control Pins

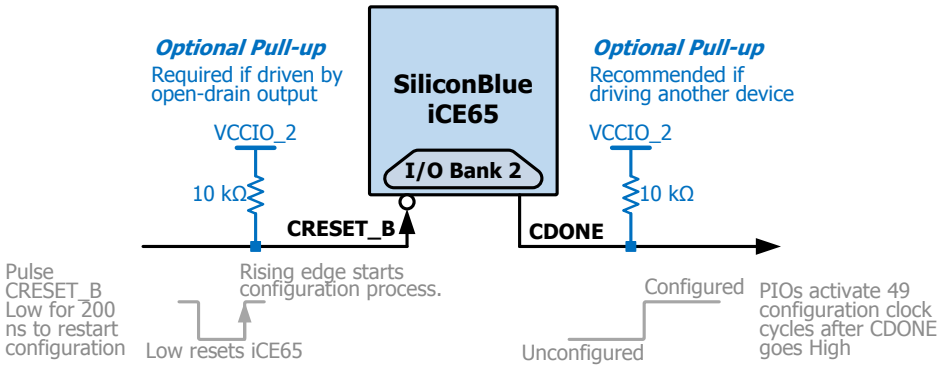


Figure 21 shows the two iCE65 configuration control pins, CRESET_B and CDONE. Table 23 lists the ball/pin numbers for the configuration control pins by package. When driven Low for at least 200 ns, the dedicated Configuration Reset input, CRESET_B, resets the iCE65 device. When CRESET_B returns High, the iCE65 FPGA restarts the configuration process from its power-on conditions (Cold Boot). The CRESET_B pin is a pure input with no internal pull-up resistor. If driven by open-drain driver or un-driven, then connect the CRESET_B pin to a 10 kΩ pull-up resistor connected to the VCCIO_2 supply.

***Table 23:* Configuration Control Ball/Pin Numbers by Package**

Configuration Control Pins	CB81	QN84	VQ100	CB132	CB196	CB284
CRESET_B	J6	A21	44	L10	L10	R14
CDONE	H6	B16	43	M10	M10	T14

The iCE65 device signals the end of the configuration process by actively turning off the internal pull-down transistor on the Configuration Done output pin, CDONE. The pin has a permanent, weak internal pull-up resistor to the VCCIO_2 rail. If the iCE65 device drives other devices, then optionally connect the CDONE pin to a 10 kΩ pull-up resistor connected to the VCCIO_2 supply.

The PIO pins activate according to their configured function after 49 configuration clock cycles. The internal oscillator is the configuration clock source for the SPI Master Configuration Interface and when configuring from

* Note: only 14 of the 16 RAM4K Memory Blocks may be pre-initialized in the iCE65L01.

Nonvolatile Configuration Memory (NVCM). When using the SPI Peripheral Configuration Interface, the configuration clock source is the SPI_SCK clock input pin.

Internal Oscillator

During SPI Master or NVCM configuration mode, the controlling clock signal is generated from an internal oscillator. The oscillator starts operating at the Default frequency. During the configuration process, however, bit settings within the configuration bitstream can specify a higher-frequency mode in order to maximize SPI bandwidth and reduce overall configuration time. See Table 57: Internal Oscillator Frequency on page 105 for the specified oscillator frequency range.

Using the SPI Master Configuration Interface, internal oscillator controls all the interface timing and clocks the SPI serial Flash PROM via the SPI_SCK clock output pin.

The oscillator output, which also supplies the SPI SCK clock output during the SPI Flash configuration process, has a 50% duty cycle.

Internal Device Reset

Figure 22 presents the various signals that internally reset the iCE65 internal logic.

- Power-On Reset (POR)
- CRESET_B Pin
- JTAG Interface

CB81 Chip-Scale Ball-Grid Array

The CB81 package is a full ball grid array with 0.5 mm ball pitch. The iCE65L01 device is available in this package.

Footprint Diagram

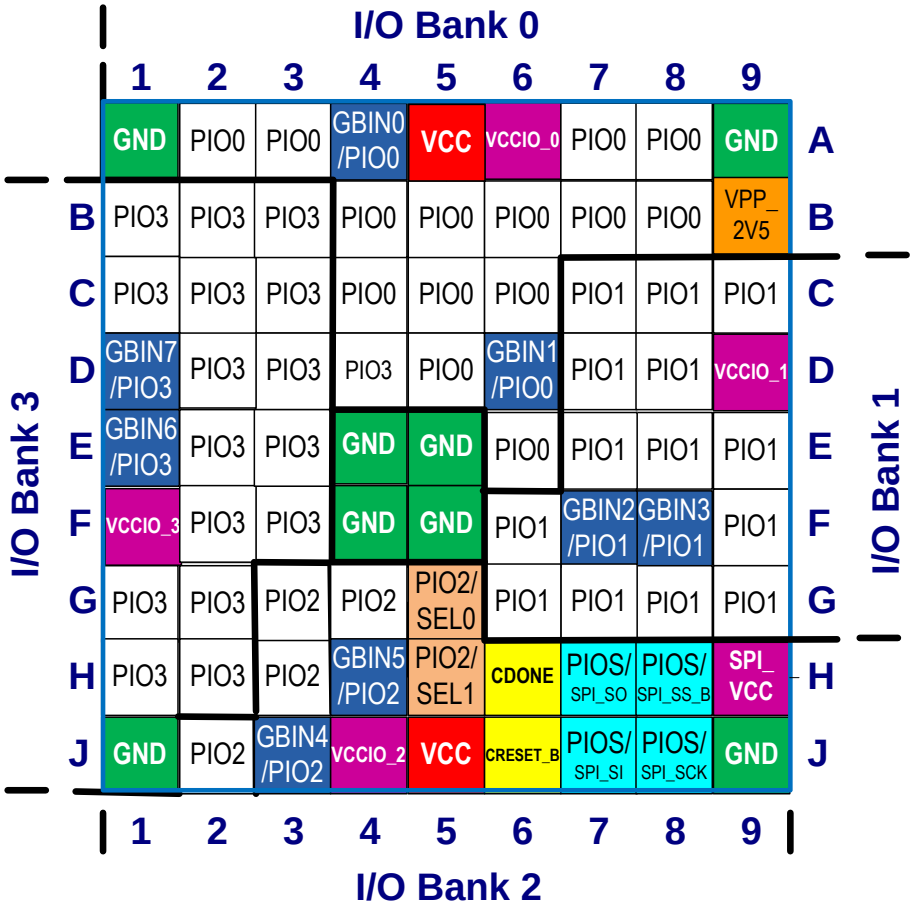
Figure 32 shows the iCE65 footprint diagram for the CB81 package.

Figure 31 shows the conventions used in the diagram.

Also see Table 37 for a complete, detailed pinout for the 81-ball BGA package.

The signal pins are also grouped into the four I/O Banks and the SPI interface.

***Figure 32*: iCE65L01 CB81 Chip-Scale BGA Footprint (Top View)**



Pinout Table

Table 37 provides a detailed pinout table for the CB81 package. Pins are generally arranged by I/O bank, then by ball function.

Table 37: iCE65 CB81 Chip-scale BGA Pinout Table

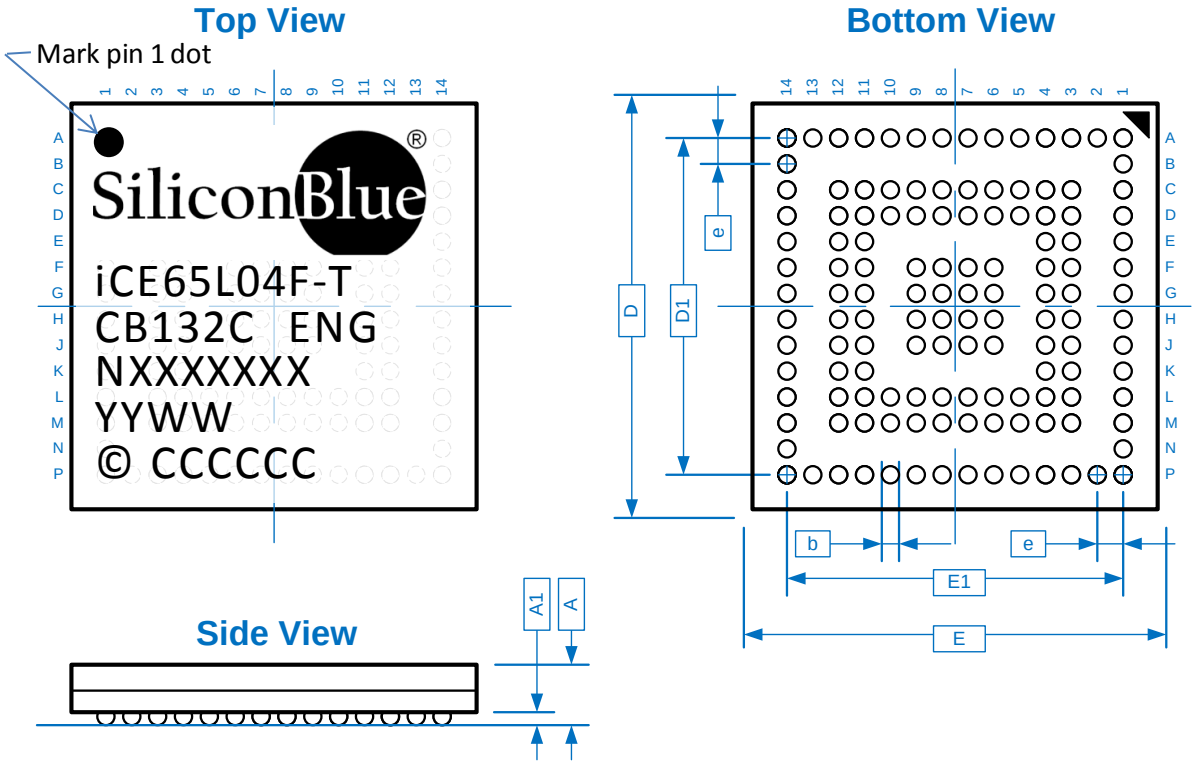
Ball Function	Ball Number	Pin Type	Bank
PIO0	A2	PIO	0
PIO0	A3	PIO	0
GBIN0/PIO0	A4	GBIN	0
PIO0	A7	PIO	0
PIO0	A8	PIO	0
PIO0	B4	PIO	0
PIO0	B5	PIO	0
PIO0	B6	PIO	0
PIO0	B7	PIO	0
PIO0	B8	PIO	0
PIO0	C4	PIO	0
PIO0	C5	PIO	0
PIO0	C6	PIO	0
PIO0	D4	PIO	0
PIO0	D5	PIO	0
GBIN1/PIO0	D6	GBIN	0
PIO0	E6	PIO	0
VCCIO_0	A6	VCCIO	0
PIO1	C7	PIO	1
PIO1	C8	PIO	1
PIO1	C9	PIO	1
PIO1	D7	PIO	1
PIO1	D8	PIO	1
PIO1	E7	PIO	1
PIO1	E8	PIO	1
PIO1	E9	PIO	1
PIO1	F6	PIO	1
GBIN2/PIO1	F7	GBIN	1
GBIN3/PIO1	F8	GBIN	1
PIO1	F9	PIO	1
PIO1	G6	PIO	1
PIO1	G7	PIO	1
PIO1	G8	PIO	1
PIO1	G9	PIO	1
VCCIO_1	D9	VCCIO	1
CDONE	H6	CONFIG	2
CRESET_B	J6	CONFIG	2
PIO2	G3	PIO	2
PIO2	G4	PIO	2
PIO2/CBSEL0	G5	PIO	2
PIO2	H3	PIO	2
GBIN5/PIO2	H4	PIO	2
PIO2/CBSEL1	H5	PIO	2
PIO2	J2	PIO	2
GBIN4/PIO2	J3	PIO	2
VCCIO_2	J4	PIO	2

Ball Function	Ball Number	Pin Type	Bank
GND	K2	GND	GND
GND	K10	GND	GND
VCC	B6	VCC	VCC
VCC	F1	VCC	VCC
VCC	F11	VCC	VCC
VCC	K6	VCC	VCC
VPP_2V5	C10	VPP	VPP
VPP_FAST	A9	VPP	VPP

Package Mechanical Drawing

Figure 44: **CB132 Package Mechanical Drawing**

CB132: 8 x 8 mm, 132-ball, 0.5 mm ball-pitch, chip-scale ball grid array



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			14		Columns
Number of Ball Rows	Y			14		Rows
Number of Signal Balls		n		132		Balls
Body Size	X	E	7.90	8.00	8.10	mm
	Y	D	7.90	8.00	8.10	
Ball Pitch		e	—	0.50	—	
Ball Diameter		b	0.27	—	0.37	
Edge Ball Center to Center	X	E1	—	6.50	—	
	Y	D1	—	6.50	—	
Package Height		A	—	—	1.00	
Stand Off		A1	0.16	—	0.26	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65L04F	Part number
	-T	Power/Speed
3	CB132C	Package type
	ENG	Engineering
4	NXXXXXXX	Lot Number
5	YYWW	Date Code
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
42	34

Ball Function	Ball Number	Pin Type	Bank
PIO1	F14	PIO	1
PIO1	G10	PIO	1
PIO1	G11	PIO	1
PIO1	G13	PIO	1
PIO1	G14	PIO	1
PIO1	H10	PIO	1
PIO1	H11	PIO	1
PIO1	H12	PIO	1
PIO1	H13	PIO	1
PIO1	J10	PIO	1
PIO1	J11	PIO	1
PIO1	J12	PIO	1
PIO1	J13	PIO	1
PIO1	K11	PIO	1
PIO1	K12	PIO	1
PIO1	K14	PIO	1
PIO1	L13	PIO	1
PIO1	L14	PIO	1
PIO1	M13	PIO	1
TCK	L12	JTAG	1
TDI	M12	JTAG	1
TDO	N14	JTAG	1
TMS	P14	JTAG	1
TRST_B	M14	JTAG	1
VCCIO_1	F9	VCCIO	1
VCCIO_1	H14	VCCIO	1
CDONE	M10	CONFIG	2
CRESET_B	L10	CONFIG	2
GBIN4/PIO2 (◆)	***iCE65L04:*** L7 ***iCE65L08:*** N8	GBIN	2
GBIN5/PIO2 (◆)	***iCE65L04:*** P5 ***iCE65L08:*** M7	GBIN	2
PIO2	K5	PIO	2
PIO2	K6	PIO	2
PIO2	K7	PIO	2
PIO2	K8	PIO	2
PIO2	K9	PIO	2
PIO2	L4	PIO	2
PIO2	L5	PIO	2
PIO2	L6	PIO	2
PIO2	L8	PIO	2
PIO2	M3	PIO	2
PIO2	M4	PIO	2
PIO2	M6	PIO	2
PIO2 (◆)	***iCE65L04:*** M7 ***iCE65L08:*** P5	PIO	2
PIO2	M8	PIO	2
PIO2	M9	PIO	2
PIO2	N3	PIO	2
PIO2	N4	PIO	2
PIO2	N5	PIO	2
PIO2	N6	PIO	2

Ball Function	Ball Number iCE65L04 iCE65L08	Pin Type by Device iCE65L04	Pin Type by Device iCE65L08	Bank	CB132 Ball Equivalent
PIO0	E15	PIO	PIO	0	A11
PIO0	E16	PIO	PIO	0	A12
PIO0	G8	PIO	PIO	0	C4
PIO0	G9	PIO	PIO	0	C5
PIO0	G10	PIO	PIO	0	C6
PIO0	G11	PIO	PIO	0	C7
PIO0	G12	PIO	PIO	0	C8
PIO0	G13	PIO	PIO	0	C9
PIO0	G14	PIO	PIO	0	C10
PIO0	G15	PIO	PIO	0	C11
PIO0	G16	PIO	PIO	0	C12
PIO0	H9	PIO	PIO	0	D5
PIO0	H10	PIO	PIO	0	D6
PIO0	H11	PIO	PIO	0	D7
PIO0	H12	PIO	PIO	0	D8
PIO0	H13	PIO	PIO	0	D9
PIO0	H14	PIO	PIO	0	D10
PIO0	H15	PIO	PIO	0	D11
VCCIO_0	A8	VCCIO	VCCIO	0	—
VCCIO_0	A21	VCCIO	VCCIO	0	—
VCCIO_0	E12	VCCIO	VCCIO	0	A8
VCCIO_0	K10	VCCIO	VCCIO	0	F6
GBIN2/PIO1	L18	GBIN	GBIN	1	G14
GBIN3/PIO1	K18	GBIN	GBIN	1	F14
PIO1 (●)	A22	N.C.	PIO	1	—
PIO1 (●)	AA22	N.C.	PIO	1	—
PIO1 (●)	B22	N.C.	PIO	1	—
PIO1	C20	PIO	PIO	1	—
PIO1 (●)	C22	N.C.	PIO	1	—
PIO1	D20	PIO	PIO	1	—
PIO1 (●)	D22	N.C.	PIO	1	—
PIO1	E20	PIO	PIO	1	—
PIO1 (●)	E22	N.C.	PIO	1	—
PIO1	F18	PIO	PIO	1	B14
PIO1	F20	PIO	PIO	1	—
PIO1 (●)	F22	N.C.	PIO	1	—
PIO1	G18	PIO	PIO	1	C14
PIO1	G20	PIO	PIO	1	—
PIO1	G22	PIO	PIO	1	—
PIO1	H16	PIO	PIO	1	D12
PIO1	H18	PIO	PIO	1	D14
PIO1	H20	PIO	PIO	1	—
PIO1	J15	PIO	PIO	1	E11
PIO1	J16	PIO	PIO	1	E12
PIO1	J18	PIO	PIO	1	E14
PIO1 (●)	J22	N.C.	PIO	1	—
PIO1	K15	PIO	PIO	1	F11
PIO1	K16	PIO	PIO	1	F12
PIO1	K20	PIO	PIO	1	—
PIO1 (●)	K22	N.C.	PIO	1	—

Ball Function	Ball Number iCE65L04 iCE65L08	Pin Type by Device iCE65L04	Pin Type by Device iCE65L08	Bank	CB132 Ball Equivalent
PIO2	T13	PIO	PIO	2	M9
PIO2	V6	PIO	PIO	2	P2
PIO2	V7	PIO	PIO	2	P3
PIO2	V8	PIO	PIO	2	P4
PIO2	V9	PIO	PIO	2	P5
PIO2	V13	PIO	PIO	2	P9
PIO2	Y4	PIO	PIO	2	—
PIO2	Y5	PIO	PIO	2	—
PIO2	Y6	PIO	PIO	2	—
PIO2	Y7	PIO	PIO	2	—
PIO2	Y9	PIO	PIO	2	—
PIO2	Y10	PIO	PIO	2	—
PIO2	Y13	PIO	PIO	2	—
PIO2	Y14	PIO	PIO	2	—
PIO2	Y15	PIO	PIO	2	—
PIO2	Y17	PIO	PIO	2	—
PIO2	Y18	PIO	PIO	2	—
PIO2	Y19	PIO	PIO	2	—
PIO2	Y20	PIO	PIO	2	—
PIO2	AB2	PIO	PIO	2	—
PIO2 (●)	AB3	N.C.	PIO	2	—
PIO2 (●)	AB4	N.C.	PIO	2	—
PIO2	AB6	PIO	PIO	2	—
PIO2	AB7	PIO	PIO	2	—
PIO2	AB8	PIO	PIO	2	—
PIO2	AB9	PIO	PIO	2	—
PIO2	AB10	PIO	PIO	2	—
PIO2	AB11	PIO	PIO	2	—
PIO2	AB12	PIO	PIO	2	—
PIO2	AB13	PIO	PIO	2	—
PIO2	AB14	PIO	PIO	2	—
PIO2	AB15	PIO	PIO	2	—
PIO2 (●)	AB16	N.C.	PIO	2	—
PIO2 (●)	AB17	N.C.	PIO	2	—
PIO2 (●)	AB18	N.C.	PIO	2	—
PIO2 (●)	AB19	N.C.	PIO	2	—
PIO2 (●)	AB20	N.C.	PIO	2	—
PIO2 (●)	AB21	N.C.	PIO	2	—
PIO2 (●)	AB22	N.C.	PIO	2	—
PIO2/CBSEL0	R13	PIO	PIO	2	L9
PIO2/CBSEL1	V14	PIO	PIO	2	P10
VCCIO_2	N13	VCCIO	VCCIO	2	J9
VCCIO_2	T9	VCCIO	VCCIO	2	M5
VCCIO_2	Y11	VCCIO	VCCIO	2	—
PIO3/DP00A	F5	DPIO	DPIO	3	B1
PIO3/DP00B	G5	DPIO	DPIO	3	C1
PIO3/DP01A	G7	DPIO	DPIO	3	C3
PIO3/DP01B	H7	DPIO	DPIO	3	D3
PIO3/DP02A	H8	DPIO	DPIO	3	D4
PIO3/DP02B	J8	DPIO	DPIO	3	E4

Die Cross Reference

The tables in this section list all the pads on a specific die type and provide a cross reference on how a specific pad connects to a ball or pin in each of the available package offerings. Similarly, the tables provide the pad coordinates for the die-based version of the product (DiePlus). These tables also provide a way to prototype with one package option and then later move to a different package or die.

As described in "Input and Output Register Control per PIO Pair" on page 16, PIO pairs share register control inputs. Similarly, as described in "Differential Inputs and Outputs" on page 12, a PIO pair can form a differential input or output. PIO pairs in I/O Bank 3 are optionally differential inputs or differential outputs. PIO pairs in all other I/O Banks are optionally differential outputs. In the tables, differential pairs are surrounded by a heavy blue box.

iCE65L04

Table 45 lists all the pads on the iCE65L04 die and how these pads connect to the balls or pins in the supported package styles. Most VCC, VCCIO, and GND pads are double-bonded inside the package although the table shows only a single connection.

For additional information on the iCE65L04 DiePlus product, please refer to the following data sheet.

DiePlus Advantage FPGA Known Good Die

Table 45: iCE65L04 Die Cross Reference

iCE65L04	DiePlus						
Pad Name	VQ100	CB132	CB196	CB284	Pad	X (µm)	Y (µm)
PIO3_00/DP00A	1	B1	C1	F5	1	129.40	2,687.75
PIO3_01/DP00B	2	C1	B1	G5	2	231.40	2,642.74
PIO3_02/DP01A	3	C3	D3	G7	3	129.40	2,597.75
PIO3_03/DP01B	4	D3	C3	H7	4	231.40	2,552.74
GND	5	F1	F1	K5	5	129.40	2,507.75
GND	—	—	—	—	6	231.40	2,462.74
VCCIO_3	6	E3	E3	J7	7	129.40	2,417.75
VCCIO_3	—	—	—	—	8	231.40	2,372.74
PIO3_04/DP02A	7	D4	D1	H8	9	129.40	2,327.75
PIO3_05/DP02B	8	E4	D2	J8	10	231.40	2,292.74
PIO3_06/DP03A	—	D1	E1	H5	11	129.40	2,257.75
PIO3_07/DP03B	—	E1	E2	J5	12	231.40	2,222.74
VCC	—	—	H9	D3	13	129.40	2,187.75
PIO3_08/DP04A	9	F4	D4	K8	14	231.40	2,152.74
PIO3_09/DP04B	10	F3	E4	K7	15	129.40	2,117.75
PIO3_10/DP05A	—	—	F3	E3	16	231.40	2,082.74
PIO3_11/DP05B	—	—	F4	F3	17	129.40	2,047.75
GND	—	H6	A9	M10	18	231.40	2,012.74
PIO3_12/DP06A	—	—	F5	G3	19	129.40	1,977.75
PIO3_13/DP06B	—	—	E5	H3	20	231.40	1,942.74
GND	—	—	A9	J3	21	129.40	1,907.75
GND	—	—	—	—	22	231.40	1,872.74
PIO3_14/DP07A	—	—	—	H1	23	129.40	1,837.75
PIO3_15/DP07B	—	—	—	J1	24	231.40	1,802.74
VCCIO_3	—	—	K1	K3	25	129.40	1,767.75
VCC	11	G6	G6	L10	26	231.40	1,732.74
PIO3_16/DP08A	—	—	—	K1	27	129.40	1,697.75
PIO3_17/DP08B	—	—	—	L1	28	231.40	1,662.74

iCE65L04 Pad Name	DiePlus VQ100	CB132	CB196	CB284	Pad	X (µm)	Y (µm)
PIO3_18/DP09A	12	—	G2	L3	29	129.40	1,627.75
GBIN7/PIO3_19/DP09B	13	G1	G1	L5	30	231.40	1,592.74
VCCIO_3	14	J6	J6	N10	31	129.40	1,557.75
VREF	N/A	N/A	N/A	M1	32	231.40	1,522.74
GND	—	—	A9	N1	33	129.40	1,487.75
GBIN6/PIO3_20/DP10A	15	H1	H1	M5	34	231.40	1,452.74
PIO3_21/DP10B	16	—	H2	M3	35	129.40	1,417.75
GND	17	H7	A9	M11	36	231.40	1,382.74
PIO3_22/DP11A	—	—	G3	N3	37	129.40	1,347.75
PIO3_23/DP11B	—	—	G4	P3	38	231.40	1,312.74
VCCIO_3	—	—	K1	R3	39	129.40	1,277.75
VCCIO_3	—	—	—	—	40	231.40	1,242.74
GND	—	—	A9	T3	41	129.40	1,207.75
GND	—	—	—	—	42	231.40	1,172.74
PIO3_24/DP12A	—	—	J1	U3	43	129.40	1,137.75
PIO3_25/DP12B	—	—	J2	V3	44	231.40	1,102.74
GND	—	—	A9	V1	45	129.40	1,067.75
PIO3_26/DP13A	—	—	H4	W3	46	231.40	1,032.74
PIO3_27/DP13B	—	—	H3	Y3	47	129.40	997.75
PIO3_28/DP14A	18	G3	K2	L7	48	231.40	962.74
PIO3_29/DP14B	19	G4	J3	L8	49	129.40	927.75
PIO3_30/DP15A	—	H3	H5	M7	50	231.40	892.74
PIO3_31/DP15B	—	H4	G5	M8	51	129.40	857.75
VCC	—	J4	F2	N8	52	231.40	822.74
PIO3_32/DP16A	20	J3	L1	N7	53	129.40	787.75
PIO3_33/DP16B	21	J1	L2	N5	54	231.40	752.74
VCCIO_3	22	K1	K1	P5	55	129.40	717.75
VCCIO_3	—	—	—	—	56	231.40	682.74
GND	23	L3	L3	R7	57	129.40	637.75
GND	—	—	—	—	58	231.40	592.74
PIO3_34/DP17A	—	K3	M1	P7	59	129.40	547.75
PIO3_35/DP17B	—	K4	M2	P8	60	231.40	502.74
PIO3_36/DP18A	24	L1	K3	R5	61	129.40	457.75
PIO3_37/DP18B	25	M1	K4	T5	62	231.40	412.74
PIO3_38/DP19A	—	N1	N1	U5	63	129.40	367.75
PIO3_39/DP19B	—	P1	N2	V5	64	231.40	322.74
PIO2_00	—	—	—	AB2	65	545.00	139.20
PIO2_01	—	P2	L4	V6	66	595.00	37.20
PIO2_02	—	M3	M3	T7	67	645.00	139.20
GND	—	—	C2	AB5	68	695.00	37.20
PIO2_03	26	L4	P1	R8	69	745.00	139.20
PIO2_04	27	P3	N3	V7	70	795.00	37.20
PIO2_05	28	M4	P2	T8	71	845.00	139.20
PIO2_06	29	L5	L5	R9	72	895.00	37.20
PIO2_07	30	P4	M4	V8	73	930.00	139.20

iCE65L04 Pad Name	DiePlus VQ100	CB132	CB196	CB284	Pad	X (µm)	Y (µm)
PIO2_08	—	L6	P3	R10	74	965.00	37.20
VCCIO_2	31	M5	M5	T9	75	1,000.00	139.20
PIO2_09	—	P5	K5	V9	76	1,035.00	37.20
PIO2_10	—	M6	N4	T10	77	1,070.00	139.20
GND	32	P6	H7	V10	78	1,105.00	37.20
PIO2_11	—	—	P4	Y4	79	1,140.00	139.20
PIO2_12	—	—	L6	Y5	80	1,175.00	37.20
PIO2_13	—	—	—	AB6	81	1,210.00	139.20
PIO2_14	—	—	—	AB7	82	1,245.00	37.20
PIO2_15	—	—	—	AB8	83	1,280.00	139.20
PIO2_16	—	—	—	AB9	84	1,315.00	37.20
PIO2_17	—	—	—	AB10	85	1,350.00	139.20
PIO2_18	—	—	—	AB11	86	1,385.00	37.20
GND	—	J8	H8	N12	87	1,420.00	139.20
PIO2_19	—	—	K6	Y6	88	1,455.00	37.20
PIO2_20	—	—	N5	Y7	89	1,490.00	139.20
VCC	—	—	J4	Y8	90	1,525.00	37.20
PIO2_21	—	—	M6	Y9	91	1,560.00	139.20
PIO2_22	—	—	N6	Y10	92	1,595.00	37.20
GBIN5/PIO2_23	33	P7	P5	V11	93	1,630.00	139.20
GBIN4/PIO2_24	34	P8	L7	V12	94	1,665.00	37.20
PIO2_25	—	—	—	AB12	95	1,700.00	139.20
VCCIO_2	—	—	J9	Y11	96	1,735.00	37.20
PIO2_26	—	—	—	AB13	97	1,770.00	139.20
PIO2_27	—	—	K7	AB14	98	1,805.00	37.20
GND	—	—	J5	Y12	99	1,840.00	139.20
PIO2_28	—	—	K9	AB15	100	1,875.00	37.20
PIO2_29	—	—	M7	Y13	101	1,910.00	139.20
PIO2_30	—	—	K8	Y14	102	1,945.00	37.20
PIO2_31	—	—	P7	Y15	103	1,980.00	139.20
PIO2_32	—	—	L8	Y17	104	2,015.00	37.20
PIO2_33	—	—	P8	Y18	105	2,050.00	139.20
PIO2_34	—	—	N8	Y19	106	2,085.00	37.20
PIO2_35	—	—	M8	Y20	107	2,120.00	139.20
VCC	35	J7	J7	N11	108	2,155.00	37.20
VCC	—	—	—	—	109	2,190.00	139.20
PIO2_36	36	P9	P9	V13	110	2,225.00	37.20
PIO2_37	37	M7	N9	T11	111	2,260.00	139.20
VCCIO_2	38	J9	N10	N13	112	2,295.00	37.20
PIO2_38	—	L7	M9	R11	113	2,330.00	139.20
GND	39	H8	J8	M12	114	2,365.00	37.20
PIO2_39	—	M8	N12	T12	115	2,400.00	139.20
PIO2_40	—	L8	N11	R12	116	2,435.00	37.20
PIO2_41	40	M9	N13	T13	117	2,470.00	139.20
PIO2_42/CBSEL0	41	L9	L9	R13	118	2,505.00	37.20
PIO2_43/CBSEL1	42	P10	P10	V14	119	2,540.00	139.20
CDONE	43	M10	M10	T14	120	2,575.00	37.20

iCE65L04 Pad Name	DiePlus VQ100	CB132	CB196	CB284	Pad	X (µm)	Y (µm)
CRESET_B	44	L10	L10	R14	121	2,625.00	139.20
PIOS_00/SPI_SO	45	M11	M11	T15	122	2,690.00	37.20
PIOS_01/SPI_SI	46	P11	P11	V15	123	2,740.00	139.20
GND	47	—	P6	Y16	124	2,790.00	37.20
PIOS_02/SPI_SCK	48	P12	P12	V16	125	2,840.00	139.20
PIOS_03/SPI_SS_B	49	P13	P13	V17	126	2,890.00	37.20
SPI_VCC	50	L11	L11	R15	127	2,990.00	37.20
TDI	N/A	M12	M12	T16	128	3,610.80	342.00
TMS	N/A	P14	P14	V18	129	3,712.80	392.00
TCK	N/A	L12	L12	R16	130	3,610.80	442.00
TDO	N/A	N14	N14	U18	131	3,712.80	492.00
TRST_B	N/A	M14	M14	T18	132	3,610.80	542.00
PIO1_00	51	L14	K11	R18	133	3,712.80	592.00
PIO1_01	52	K12	L13	P16	134	3,610.80	642.00
PIO1_02	53	K11	K12	P15	135	3,712.80	692.00
PIO1_03	54	K14	M13	P18	136	3,610.80	727.00
GND	55	J14	J14	N18	137	3,712.80	762.00
GND	55	J14	J14	N18	138	3,610.80	797.00
PIO1_04	56	J12	J10	N16	139	3,712.80	832.00
PIO1_05	57	J11	L14	N15	140	3,610.80	867.00
VCCIO_1	58	H14	H14	M18	141	3,712.80	902.00
VCCIO_1	—	—	—	—	142	3,610.80	937.00
PIO1_06	59	H12	J11	M16	143	3,712.80	972.00
PIO1_07	60	H11	K14	M15	144	3,610.80	1,007.00
PIO1_08	—	—	H10	W20	145	3,712.80	1,042.00
PIO1_09	—	—	J13	V20	146	3,610.80	1,077.00
PIO1_10	—	—	J12	U20	147	3,712.80	1,112.00
VCC	61	H9	N7	M13	148	3,610.80	1,147.00
VCC	—	—	—	—	149	3,712.80	1,182.00
PIO1_11	—	—	H13	T22	150	3,610.80	1,217.00
PIO1_12	—	—	H12	R22	151	3,712.80	1,252.00
PIO1_13	—	—	—	P22	152	3,610.80	1,287.00
PIO1_14	—	—	—	N22	153	3,712.80	1,322.00
PIO1_15		—	G13	T20	154	3,610.80	1,357.00
PIO1_16	—	—	H11	R20	155	3,712.80	1,392.00
PIO1_17	—	—	G14	P20	156	3,610.80	1,427.00
GND	—	—	K10	N20	157	3,712.80	1,462.00
GND	—	—	—	—	158	3,610.80	1,497.00
PIO1_18	—	—	G10	M20	159	3,712.80	1,532.00
GBIN3/PIO1_19	62	F14	G12	K18	160	3,610.80	1,567.00
GBIN2/PIO1_20	63	G14	F10	L18	161	3,712.80	1,602.00
PIO1_21	—	—	F14	K20	162	3,610.80	1,637.00
VCCIO_1	—	—	H14	J20	163	3,712.80	1,672.00
VCCIO_1	—	—	—	—	164	3,610.80	1,707.00
PIO1_22	—	—	F13	H20	165	3,712.80	1,742.00
PIO1_23	—	—	D13	G20	166	3,610.80	1,777.00

iCE65L08

Table 46 lists all the pads on the iCE65L08 die and how these pads connect to the balls or pins in the supported package styles. Most VCC, VCCIO, and GND pads are double-bonded inside the package although the table shows only a single connection.

For additional information on the iCE65L08 DiePlus product, please refer to the following data sheet.

- DiePlusAdvantage FPGA Known Good Die

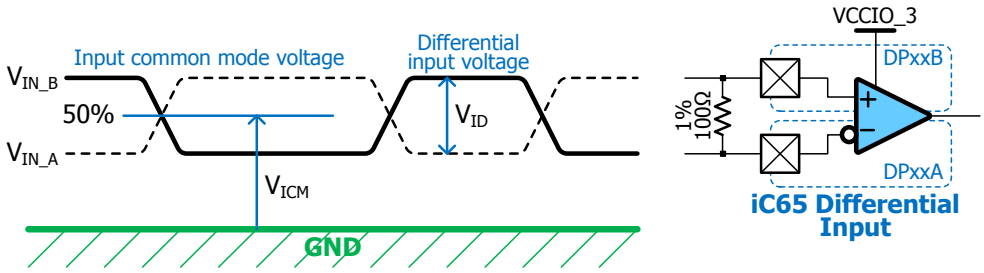
Table 46: iCE65L08 Die Cross Reference

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO3_00/DP00A	—	B1	1	129.735	3,882.665
PIO3_01/DP00B	—	C1	2	231.735	3,837.665
PIO3_02/DP01A	C1	F5	3	129.735	3,792.665
PIO3_03/DP01B	B1	G5	4	231.735	3,747.665
GND	C2	K5	5	129.735	3,702.665
GND	—	—	6	231.735	3,657.665
VCCIO_3	E3	J7	7	129.735	3,612.665
VCCIO_3	—	—	8	231.735	3,567.665
PIO3_04/DP02A	D3	E3	9	129.735	3,512.665
PIO3_05/DP02B	C3	F3	10	231.735	3,477.665
PIO3_06/DP03A	D1	G3	11	129.735	3,442.665
PIO3_07/DP03B	D2	H3	12	231.735	3,407.665
VCC	F2	D3	13	129.735	3,372.665
VCC	—	—	14	231.735	3,337.665
PIO3_08/DP04A	D4	D1	15	129.735	3,302.665
PIO3_09/DP04B	E4	E1	16	231.735	3,267.665
PIO3_10/DP05A	—	H1	17	129.735	3,232.665
PIO3_11/DP05B	—	J1	18	231.735	3,197.665
GND	F1	M10	19	129.735	3,162.665
GND	—	—	20	231.735	3,127.665
PIO3_12/DP06A	E2	H5	21	129.735	3,092.665
PIO3_13/DP06B	E1	J5	22	231.735	3,057.665
GND	L3	J3	23	129.735	3,022.665
GND	—	—	24	231.735	2,987.665
PIO3_14/DP07A	F5	K1	25	129.735	2,952.665
PIO3_15/DP07B	E5	L1	26	231.735	2,917.665
VCCIO_3	E3	K3	27	129.735	2,882.665
VCCIO_3	—	—	28	231.735	2,847.665
VCC	G6	L10	29	129.735	2,812.665
VCC	—	—	30	231.735	2,777.665
PIO3_16/DP08A	F4	G7	31	129.735	2,742.665
PIO3_17/DP08B	F3	H7	32	231.735	2,707.665
VCCIO_3	K1	F1	33	129.735	2,672.665
VCCIO_3	—	—	34	231.735	2,637.665
GND	—	G1	35	129.735	2,602.665
GND	—	—	36	231.735	2,567.665
PIO3_18/DP09A	G3	K8	37	129.735	2,532.665
PIO3_19/DP09B	G4	K7	38	231.735	2,497.665

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO0_42	C5	A5	316	1,559.48	4,054.5
PIO0_43	B5	G9	317	1,524.48	4,156.5
PIO0_44	A4	A3	318	1,489.48	4,054.5
PIO0_45	—	A4	319	1,454.48	4,156.5
PIO0_46	—	A2	320	1,419.48	4,054.5
PIO0_47	—	C7	321	1,384.48	4,156.5
PIO0_48	—	C6	322	1,331.98	4,054.5
VCCIO_0	A8	K10	323	1,281.98	4,156.5
VCCIO_0	—	—	324	1,231.98	4,054.5
PIO0_49	—	E8	325	1,181.98	4,156.5
PIO0_50	B4	A1	326	1,131.98	4,054.5
PIO0_51	C4	E7	327	1,081.98	4,156.5
PIO0_52	A3	C5	328	1,031.98	4,054.5
PIO0_53	B3	E6	329	981.98	4,156.5
PIO0_54	D5	C3	330	931.98	4,054.5
GND	A9	L11	331	881.98	4,156.5
GND	—	—	332	831.98	4,054.5
PIO0_55	B2	G8	333	781.98	4,156.5
PIO0_56	A2	C4	334	731.98	4,054.5
PIO0_57	A1	H10	335	681.98	4,156.5
PIO0_58	—	E5	336	631.98	4,054.5
PIO0_59	—	H9	337	581.98	4,156.5

Differential Inputs

Figure 50: Differential Input Specifications



Input common mode voltage: $$V_{ICM} = \frac{VCCIO\_3}{2} \pm \Delta V_{ICM}$$

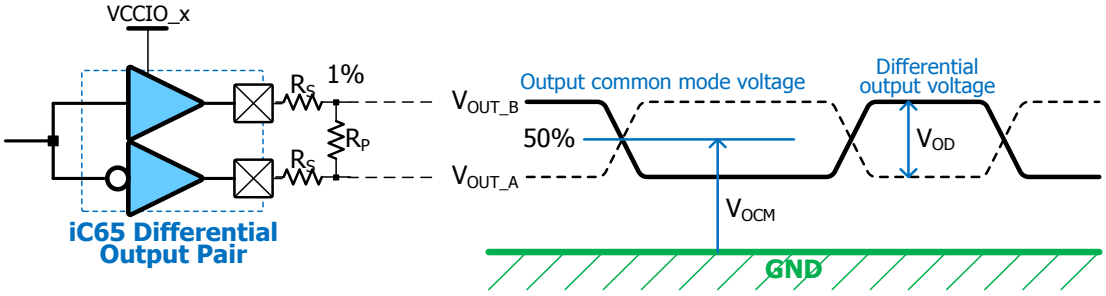
Differential input voltage: $$V_{ID} = |V_{IN\_B} - V_{IN\_A}|$$

Table 52: **Recommended Operating Conditions for Differential Inputs**

I/O Standard	VCCIO_3 (V)			V_{ID} (mV)			V_{ICM} (V)		
	Min	**Nom**	**Max**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
LVDS	2.38	2.50	2.63	250	350	450	$\frac{VCCIO\_3}{2} - 0.30$	$\frac{VCCIO\_3}{2}$	$\frac{VCCIO\_3}{2} + 0.30$
SubLVDS	1.71	1.80	1.89	100	150	200	$\frac{VCCIO\_3}{2} - 0.25$	$\frac{VCCIO\_3}{2}$	$\frac{VCCIO\_3}{2} + 0.25$

Differential Outputs

Figure 51: Differential Output Specifications



Output common mode voltage: $$V_{OCM} = \frac{VCCIO\_x}{2} \pm \Delta V_{OCM}$$

Differential output voltage: $$V_{OD} = |V_{OUT\_B} - V_{OUT\_A}|$$

Table 53: **Recommended Operating Conditions for Differential Outputs**

I/O Standard	VCCIO_x (V)			Ω		V_{OD} (mV)			V_{OCM} (V)		
	Min	**Nom**	**Max**	**R_S**	**R_P**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
LVDS	2.38	2.50	2.63	150	140	300	350	400	$\frac{VCCIO}{2} - 0.15$	$\frac{VCCIO}{2}$	$\frac{VCCIO}{2} + 0.15$
SubLVDS	1.71	1.80	1.89	270	120	100	150	200	$\frac{VCCIO}{2} - 0.10$	$\frac{VCCIO}{2}$	$\frac{VCCIO}{2} + 0.10$

Programmable Input/Output (PIO) Block

Table 55 provides timing information for the logic in a Programmable Logic Block (PLB), which includes the paths shown in Figure 57 and Figure 58. The timing shown is for the LVCMOS25 I/O standard in all I/O banks. The iCEcube development software reports timing adjustments for other I/O standards.

Figure 57: **Programmable I/O (PIO) Pad-to-Pad Timing Circuit**

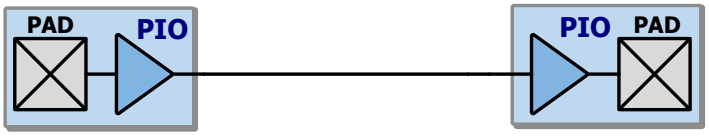


Figure 58: **Programmable I/O (PIO) Sequential Timing Circuit**

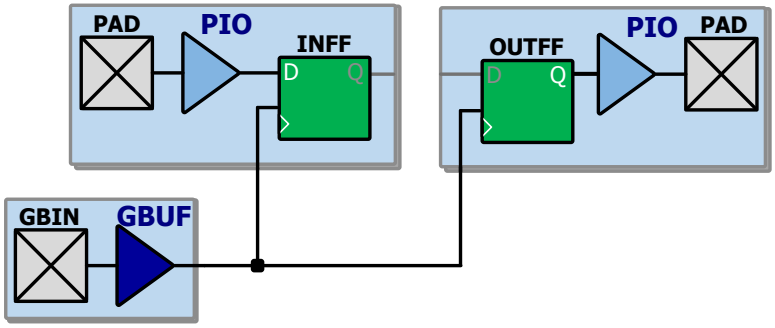


Table 55: **Typical Programmable Input/Output (PIO) Timing (LVCMOS25)**

Symbol	From	To	Device: iCE65	L01	L04, L08			Units
			Power/Speed Grad	–T	–L		–T	
			Nominal VCC	1.2 V	1.0 V	1.2 V	1.2 V	
			Description	Typ.	Typ.	Typ.	Typ.	
		Synchronous Output Paths						
t_{OCKO}	OUTFF clock input	PIO output	Delay from clock input on OUTFF output flip-flop to PIO output pad.	4.7	13.8	7.3	5.6	ns
t_{GBCKIO}	GBIN input	OUTFF clock input	Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to clock input on the PIO OUTFF output flip-flop.	2.1	7.3	3.8	2.6	ns
		Synchronous Input Paths						
t_{SUPDIN}	PIO input	GBIN input	Setup time on PIO input pin to INFF input flip-flop before active clock edge on GBIN input, including interconnect delay.	0	0	0	0	ns
t_{HDPDIN}	GBIN input	PIO input	Hold time on PIO input to INFF input flip-flop after active clock edge on the GBIN input, including interconnect delay.	2.7	7.1	3.6	2.8	ns
		Pad to Pad						
t_{PADIN}	PIO input	Inter-connect	Asynchronous delay from PIO input pad to adjacent interconnect.	2.5	9.5	5.0	3.2	ns
t_{PADO}	Inter-connect	PIO output	Asynchronous delay from adjacent interconnect to PIO output pad including interconnect delay.	4.5	14.6	7.7	6.2	ns

Internal Configuration Oscillator Frequency

Table 57 shows the operating frequency for the iCE65's internal configuration oscillator.

Table 57: Internal Oscillator Frequency

Symbol	Oscillator Mode	Frequency (MHz)		Description
		Min.	Max.	
f_{OSCD}	**Default**	4.0	6.8	Default oscillator frequency. Slow enough to safely operate with any SPI serial PROM.
f_{OSCL}	**Low Frequency**	14	21	Supported by most SPI serial Flash PROMs
f_{OSCH}	**High Frequency**	21	31	Supported by some high-speed SPI serial Flash PROMs
	Off	0	0	Oscillator turned off by default after configuration to save power.

Configuration Timing

Table 58 shows the maximum time to configure an iCE65 device, by oscillator mode. The calculations use the slowest frequency for a given oscillator mode from Table 57 and the maximum configuration bitstream size from Table 1 which includes full RAM4K block initialization. The configuration bitstream selects the desired oscillator mode based on the performance of the configuration data source.

***Table 58:* Maximum SPI Master or NVCM Configuration Timing by Oscillator Mode**

Symbol	Description	Device	Default	Low Freq.	High Freq.	Units
$t_{CONFIGL}$	Time from when minimum Power-on Reset (POR) threshold is reached until user application starts.	**iCE65L01**	53	25	11	ms
		iCE65L04	115	55	25	ms
		iCE65L08	230	110	50	ms

Table 59 provides timing for the CRESET_B and CDONE pins.

Table 59: General Configuration Timing

Symbol	From	To	Description		All Grades		Units
					Min.	Max.	
t_{CRESET_B}	CREST_B	CREST_B	Minimum CRESET_B Low pulse width required to restart configuration, from falling edge to rising edge		200	—	ns
t_{DONE_IO}	CDONE High	PIO pins active	Number of configuration clock cycles after CDONE goes High before the PIO pins are activated.		—	49	Clock cycles
			SPI Peripheral Mode (Clock = SPI_SCK, cycles measured rising-edge to rising-edge)		Depends on SPI_SCK frequency		
			NVCM or SPI Master Mode by internal oscillator frequency setting (Clock = internal oscillator)	Default	7.20	12.25	µs
				Low	2.34	3.50	µs
				High	1.59	2.33	µs

Revision History

Version	Date	Description
2.42	30-MAR-2012	Changed company name. Updated Table 1
2.41	1-AUG-2011	Added VQ100 marking for NVCM programming.
2.4	13-MAY-2011	Added L01 CB121 package Figure 39. Added note "else VCCIO_1 draws current" to JTAG inputs TCK, TDI and TMS do not have the input pull-up resistor and must be tied off to GND when unused, Table 32. Input pin leakage current Table 49 split by bank. QN84 package drawing, Figure 35, added note "underside metal is at ground potential", increased thermal resistance. Added Marking Format and Thermal resistance to CB81 Packag Mechanical Drawing Figure 33. Added coplanarity specification to VQ100 Package Mechanical Drawing Figure 37
2.3	18-OCT-2010	Added L01 CB81 and L08 CB132 packages.
2.2.3	12-OCT-2010	Changed Figure 29: Application Processor Waveforms for SPI Peripheral Mode Configuration Process and Table 60 from 300 µs CRESET_B to 800 µs for iCE65L01/04 and 1200 µs for iCE65L08.
2.2.2	8-OCT-2010	Added iCE65L04 marking specification to Figure 47 CB196 Package Mechanical Drawing.
2.2.1	5-OCT-2010	Changed FSPI_SCK from 0.125 MHz to 1 MHz in SPI Peripheral Configuration Interface and in Table 60.
2.2	6-AUG-2010	Programmable Interconnect section removed.
2.1.1	26-MAY-2010	Switched labels on Figure 53 LVCMOS Output High, VCCIO = 1.8V with VCCIO = 2.5V.
2.1	15-MAR-2010	Added JTAG unused input tie off guideline. Added marking specification and thermal characteristics to package drawings. Added production datasheet for iCE65L01 with timing update, including QN84, VQ100 and CB132. Added NVCM shut-off on SPI configuration. Added non-standard VCCIO operating conditions. Increased the minimum voltage supply specification for LVCMOS33 to 3.14V in Table 48.
2.0.1	12-NOV-2009	Recommended Operation Conditions, Table 47, replaced junction with ambient.
2.0	14-SEPT-2009	Finalized production data sheet for iCE65L04 and iCE65L08. Improved SubLVDS input specification V_{ICM} in Table 52. CS63 and CC72 packages removed and placed in iCE DiCE KGD, Known Good Die datasheet. Added "IBIS Models for I/O Banks 0, 1, 2 and the SPI Bank". Added "Printed Circuit Board Layout Information".
1.5.1	13-JUL-2009	Updated the text in "SPI PROM Requirements" section. Minor label change in Figure 48.
1.5	20-JUN-2009	Updated timing information and added –T high-speed device option (affected Figure 2, Table 48, Table 54, Table 55, Table 56, and Table 61). Added support for 3.3V LVCMOS I/Os in I/O Bank 3 (affected Figure 7, Table 5, Table 7, Table 8, Table 47, Table 48, and Table 51). Added a section about the SPI Peripheral Configuration Interface and timing in Table 60. Added a warning that a Warm Boot operation can only jump to another configuration image that has Warm Boot disabled. Updated configuration image size and configuration time for the iCE65L02 in Table 27 and Table 58. Reduced the minimum voltage supply specification for LVCMOS33 to 2.7V in Table 48. Added information about which power rails can be disconnected without effecting the Power-On Reset (POR) circuit and clarified description of VPP_2V5 pin in Table 36. Added I/O characterization curves (Figure 52, Figure 53, and Figure 54). Minor changes to Figure 20 and Figure 21. Changed timing per Figures 54-58 and Tables 55-57.
1.4.4	25-MAR-2009	Clarified the voltage requirements for the VPP_2V5 pin in Table 36 and notes under Table 48.
1.4.3	9-MAR-2009	Removed volatile-only (-V) product offering from Figure 2. Corrected NC on ball V22, removed it for ball T22 on CB284 package (Figure 48).
1.4.2	27-FEB-2009	Updated Table 14, Table 23, Table 26, Table 30, Table 33, Table 35, and Table 46. Updated I/O Bank 3 information in Table 7 and Table 48.
1.4.1	24-FEB-2009	Based on characterization data, reduced 32KHz operating current by 40% in Table 1, Table 61, and Figure 1. Corrected that SSTL18 standards require VREF pin in Table 7. Correct ball numbers for GBIN4/GBIN5 for CS110 package.
1.4	9-FEB-2009	Added footprint and pinout information for the VQ100 Very-thin Quad Flat Package. Added footprint for iCE65L08 in CB196 (Figure 46) and added Table 43 showing the differences between the 'L04 and 'L08 in the CB196 package. Unified the package footprint nomenclature in the Package and Pinout Information section. Added note to Global Buffer Inputs that the differential clock direct input is not available on the CB132 package. Added tables showing the ball/pin number for various control functions, by package (Table 14, Table 23, Table 26, Table 30, and Table 33). Corrected the GBIN/GBUF designations. GBIN4 and GBIN5 were swapped as were GBIN6 and GBIN7. This change affected all pinout tables and footprint diagrams. Updated and corrected "Differential Global Buffer Input." Tested and corrected the clock-enable and reset connections between global buffers and various resources (Table 11, Table 12, and Table 13). Added "Automatic Global Buffer Insertion, Manual Insertion." Added "Die Cross Reference" section. Improved industrial temperature range by lowering