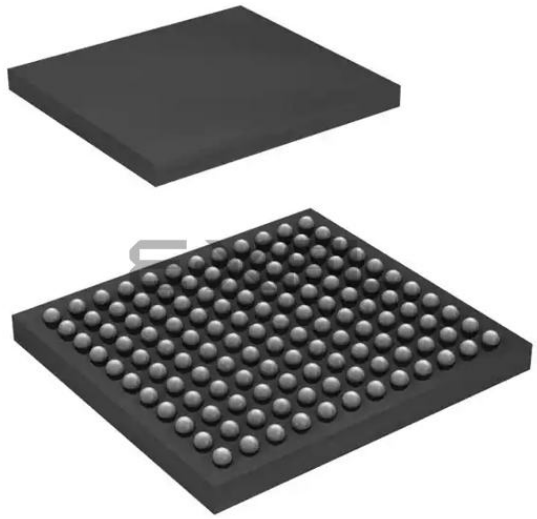
Lattice Semiconductor Corporation - ICE65L01F-LCB132I Datasheet



Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	160
Number of Logic Elements/Cells	1280
Total RAM Bits	65536
Number of I/O	93
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	132-VFBGA, CSPBGA
Supplier Device Package	132-CSBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice65l01f-lcb132i

Packaging Options

iCE65 components are available in a variety of package options to support specific application requirements. The available options, including the number of available user-programmable I/O pins (PIOs), are listed in Table 2. Fully-tested Known-Good Die (KGD) DiePlus™ are available for die stacking and highly space-conscious applications. All iCE65 devices are provided exclusively in Pb-free, RoHS-compliant packages.

Table 2: **iCE65 Family Packaging Options, Maximum I/O per Package**

Package	Package Body (mm)	Package Code	Ball/Lead Pitch (mm)	65L01	65L04	65L08
81-ball chip-scale BGA	5 x 5	CB81	0.5	63 *(0)*	—	—
84-pin quad flat no-lead package	7 x 7	QN84	0.5	67 *(0)*	—	—
100-pin very thin quad flat package	14 x 14	VQ100	0.5	72 *(0)* ⟺	72 *(9)*	—
121-ball chip-scale BGA	6 x 6	CB121	0.5	92 *(0)*	—	—
132-ball chip-scale BGA	8 x 8	CB132		93 *(0)* ⇔	95 *(11)* ⇔	95 *(12)*
196-ball chip-scale BGA	8 x 8	CB196		—	150 *(18)* ⇔	150 *(18)*
284-ball chip-scale BGA	12 x 12	CB284		—	176 *(20)* ⟺	222 *(25)*
Known Good Die	See DiePlus data sheet	DI	—	95 *(0)*	176 *(20)*	222 *(25)*

⟺ = Common footprint allows each density migration on the same printed circuit board. *(Differential input count)*.

The iCE65L04 and the iCE65L08 are both available in the CB196 package and have similar footprints but are not completely pin compatible. See "Pinout Differences between iCE65L04 and iCE65L08 in CB196 Package" on page 73 for more information.

When iCE65 components are supplied in the same package style, devices of different gate densities share a common footprint. The common footprint improves manufacturing flexibility. Different models of the same product can share a common circuit board. Feature-rich versions of the end application mount a larger iCE65 device on the circuit board. Low-end versions mount a smaller iCE65 device.

Table 8 lists the I/O standards that can co-exist in I/O Bank 3, depending on the VCCIO_3 voltage.

***Table 8:* Compatible I/O Standards in I/O Bank 3 of iCE65L04 and iCE65L08**

VCCIO_3 Voltage	3.3V	2.5V	1.8V	1.5V
Compatible I/O Standards	SB_LVCMOS33_8	Any SB_LVCMOS25 SB_SSTL2_Class_2 SB_SSTL2_Class_1 SB_LVDS_INPUT	Any SB_LVCMOS18 SB_SSTL18_FULL SB_SSTL18_HALF SB_MDDR10 SB_MDDR8 SB_MDDR4 SB_MDDR2 SB_LVDS_INPUT	Any SB_LVCMOS15

Programmable Output Drive Strength

Each PIO in I/O Bank 3 offers programmable output drive strength, as listed in Table 8. For the LVCMOS and MDDR I/O standards, the output driver has settings for static drive currents ranging from 2 mA to 16 mA output drive current, depending on the I/O standard and supply voltage.

The SSTL18 and SSTL2 I/O standards offer full- and half-strength drive current options

Differential Inputs and Outputs

All PIO pins support "single-ended" I/O standards, such as LVCMOS. However, iCE65 FPGAs also support differential I/O standards where a single data value is represented by two complementary signals transmitted or received using a pair of PIO pins. The PIO pins in I/O Bank 3 of iCE65L04 and iCE65L08L08 support Low-Voltage Differential Swing (LVDS) and SubLVDS inputs as shown in Figure 8. Differential outputs are available in all four I/O banks.

Differential Inputs Only on I/O Bank 3 of iCE65L04 and iCE65L08

Differential receivers are required for popular applications such as LVDS and LVPECL clock inputs, camera interfaces, and for various telecommunications standards.

Specific pairs of PIO pins in I/O Bank 3 form a differential input. Each pair consists of a DPxxA and DPxxB pin, where "xx" represents the pair number. The DPxxB receives the true version of the signal while the DPxxA receives the complement of the signal. Typically, the resulting signal pair is routed on the printed circuit board (PCB) with matched 50Ω signal impedance. The differential signaling, the low voltage swing, and the matched signal routing are ideal for communicating very-high frequency signals. Differential signals are generally also more tolerant of system noise and generate little EMI themselves.

The LVDS input circuitry requires 2.5V on the VCCIO_3 voltage supply. Similarly, the SubLVDS input circuitry requires 1.8V on the VCCIO_3 voltage supply. For electrical specifications, see "Differential Inputs" on page 100.

Each differential input pair requires an external 100 Ω termination resistor, as shown in Figure 8.

The PIO pins that make up a differential input pair are indicated with a blue bounding box in the footprint diagrams and in the pinout tables.

Input Signal Path

As shown in Figure 7, a signal from a package pin optionally feeds directly into the device, or is held in an input register. The input signal connects to the programmable interconnect resources through the IN signal. Table 9 describes the input behavior, assuming that the output path is not used or if a bidirectional I/O, that the output driver is in its high-impedance state (Hi-Z). Table 9 also indicates the effect of the Power-Saving I/O Bank iCEgate Latch and the Input Pull-Up Resistors on I/O Banks 0, 1, and 2.

See Input and Output Register Control per PIO Pair for information about the registered input path.

Power-Saving I/O Bank iCEgate Latch

To save power, the optional iCEgate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Registered inputs are effectively frozen by their associated clock or clock-enable control. As shown in Figure 10, the iCEgate HOLD control signal captures the external value from the associated asynchronous input. The HOLD signal prevents switching activity on the PIO pad from affecting internal logic or programmable interconnect. Minimum power consumption occurs when there is no switching. However, individual pins within the I/O bank can bypass the iCEgate latch and directly feed into the programmable interconnect, remaining active during low-power operation. This behavior is described in Table 9. The decision on which asynchronous inputs use the iCEgate feature and which inputs bypass it is determined during system design. In other words, the iCEgate function is part of the source design used to create the iCE65 configuration image.

Figure 10: Power-Saving iCEgate Latch

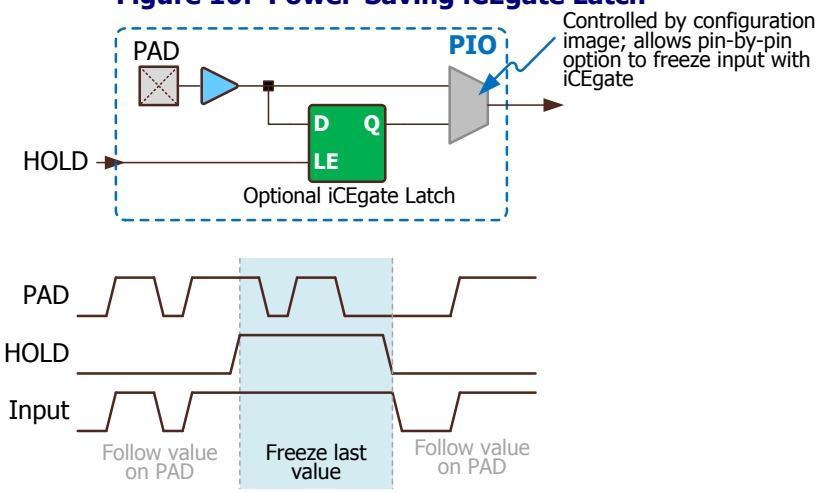


***Table 9:* PIO Non-Registered Input Operations**

Operation	HOLD	Bitstream Setting		PAD	IN
	iCEgate Latch	Controlled by iCEgate?	Input Pull-Up Enabled?	Pin Value	Input Value to Interconnect
Data Input	0	X	X	PAD	PAD Value
Pad Floating, No Pull-up	0	X	No	Z	(Undefined)
Pad Floating, Pull-up	0	X	Yes	Z	1
Data Input, Latch Bypassed	X	No	X	PAD	PAD Value
Pad Floating, No Pull-up, Latch Bypassed	X	No	No	Z	(Undefined)
Pad Floating, Pull-up, Latch Bypassed	X	No	Yes	Z	1
Low Power Mode, Hold Last Value	1	Yes	X	X	Last Captured PAD Value

There are four iCEgate HOLD controls, one per each I/O bank. The iCEgate HOLD control input originates within the interconnect fabric, near the middle of the I/O edge. Consequently, the HOLD signal is optionally controlled externally through a PIO pin or from other logic within the iCE65 device.

Figure 19: RAM4K Read Logic

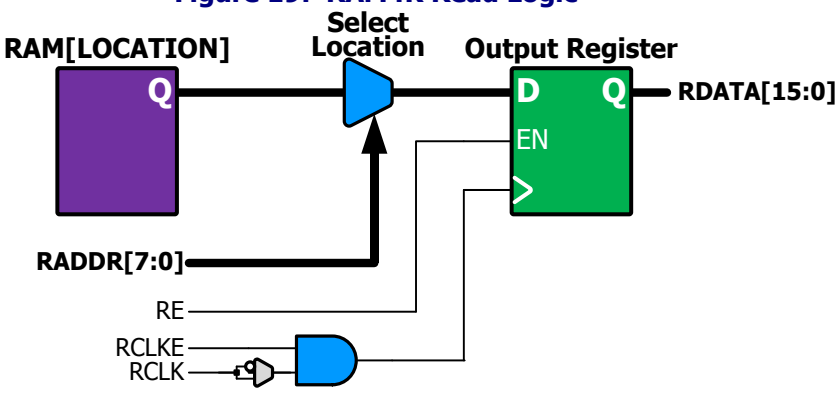


Table 19: RAM4K Read Operations

Operation	RADDR[7:0] Address	RE Read Enable	RCLKE Clock Enabe	RCLK Clock	RDATA[15:0]
After configuration, before first valid Read Data operation	X	X	X	X	Undefined
Disabled	X	X	X	0	No Change
Disabled		X	0	X	No Change
Disabled	X	0	X	X	No change
Read Data	RADDR	1	1	↑	RAM[RADDR]

To read data from the RAM4K block, perform the following operations.

- Supply a valid address on the RADDR[7:0] address input port
- Enable the RAM4K read port (RE = 1)
- Enable the RAM4K read clock (RCLKE = 1)
- Apply a rising clock edge on RCLK
- After the clock edge, the RAM contents located at the specified address (RADDR) appear on the RDATA output port

Read Data Register Undefined Immediately after Configuration

Unlike the flip-flops in the Programmable Logic Blocks and Programmable I/O pins, the RDATA[15:0] read data output register is not automatically reset after configuration. Consequently, immediately following configuration and before the first valid Read Data operation, the initial RDATA[15:0] read value is undefined.

Pre-loading RAM Data

The data contents for a RAM4K block can be optionally pre-loaded during iCE65 configuration. If not pre-loaded during configuration, then the RAM contents must be initialized by the iCE65 application before the RAM contents are valid.

Pre-loading the RAM data in the configuration bitstream increases the size of the configuration image accordingly.

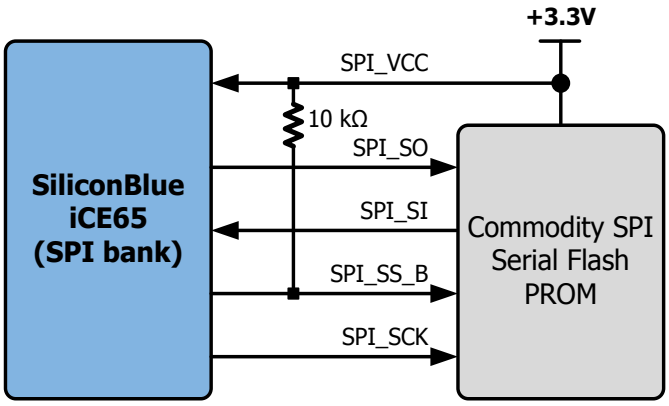
RAM Contents Preserved during Configuration

RAM contents are preserved (write protected) during configuration, assuming that voltage supplies are maintained throughout. Consequently, data can be passed between multiple iCE65 configurations by leaving it in a RAM4K block and then skipping pre-loading during the subsequent reconfiguration. See "Cold Boot Configuration Option" and "Warm Boot Configuration Option" for more information.

Low-Power Setting

To place a RAM4K block in its lowest power mode, keep WCLKE = 0 and RCLKE = 0. In other words, when not actively using a RAM4K block, disable the clock inputs.

Figure 23: **iCE65 SPI Master Configuration Interface**



The SPI configuration interface is used primarily during development before mass production, where the configuration is then permanently programmed in the NVCM configuration memory. However, the SPI interface can also be the primary configuration interface allowing easy in-system upgrades and support for multiple configuration images.

The SPI control signals are defined in Table 25. Table 26 lists the SPI interface ball or pins numbers by package.

Table 25: **SPI Master Configuration Interface Pins (SPI_SS_B High before Configuration)**

Signal Name	Direction	Description
SPI_VCC	Supply	SPI Flash PROM voltage supply input.
SPI_SO	Output	SPI Serial Output from the iCE65 device.
SPI_SI	Input	SPI Serial Input to the iCE65 device, driven by the select SPI serial Flash PROM.
SPI_SS_B	Output	SPI Slave Select output from the iCE65 device. Active Low.
SPI_SCK	Output	SPI Slave Clock output from the iCE65 device.

After configuration, the SPI port pins are available to the user-application as additional PIO pins, supplied by the SPI_VCC input voltage, essentially providing a fifth "mini" I/O bank.

Table 26: **SPI Interface Ball/Pin Numbers by Package**

SPI Interface	VQ100	CB132	CB196	CB284
SPI_VCC	50	L11	L11	R15
PIOS/SPI_SO	45	M11	M11	T15
PIOS/SPI_SI	46	P11	P11	V15
PIOS/SPI_SS_B	49	P13	P13	V17
PIOS/SPI_SCK	48	P12	P12	V16

SPI PROM Requirements

The iCE65 mobileFPGA SPI Flash configuration interface supports a variety of SPI Flash memory vendors and product families. However, Lattice Semiconductor does not specifically test, qualify, or otherwise endorse any specific SPI Flash vendor or product family. The iCE65 SPI interface supports SPI PROMs that they meet the following requirements.

- The PROM must operate at 3.3V or 2.5V in order to trigger the iCE65 FPGA's power-on reset circuit.
- The PROM must support the `0x0B` Fast Read command, using a 24-bit start address and has 8 dummy bits before the PROM provides first data (see Figure 25: SPI Fast Read Command).
- The PROM must have enough bits to program the iCE65 device (see Table 27: Smallest SPI PROM Size (bits), by Device, by Number of Images).
- The PROM must support data operations at the upper frequency range for the selected iCE65 internal oscillator frequency (see Table 57). The oscillator frequency is selectable when creating the FPGA bitstream image.

Figure 24: **SPI Release from Deep Power-down Command**

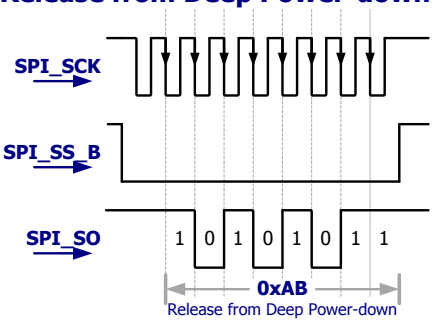
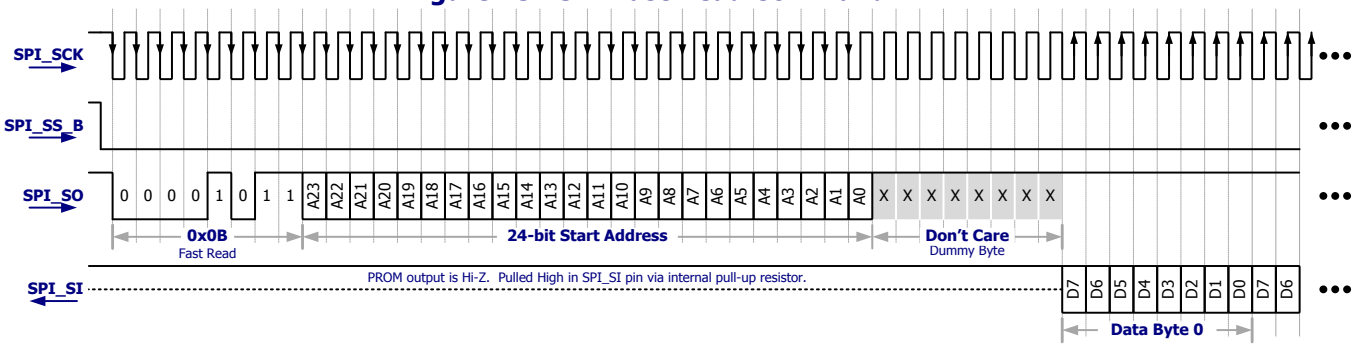


Figure 25 illustrates the next command issued by the iCE65 device. The iCE65 SPI interface again drives SPI_SS_B Low, followed by a Fast Read command, hexadecimal command code 0x0B, followed by a 24-bit start address, transmitted on the SPI_SO output. The iCE65 device provides data on the falling edge of SPI_SS_B. Upon initial power-up, the start address is always 0x00_0000. After waiting eight additional clock cycles, the iCE65 device begins reading serial data from the SPI PROM. Before presenting data, the SPI PROM's serial data output is high-impedance. The SPI_SI input pin has an internal pull-up resistor and sees high-impedance as logic '1'.

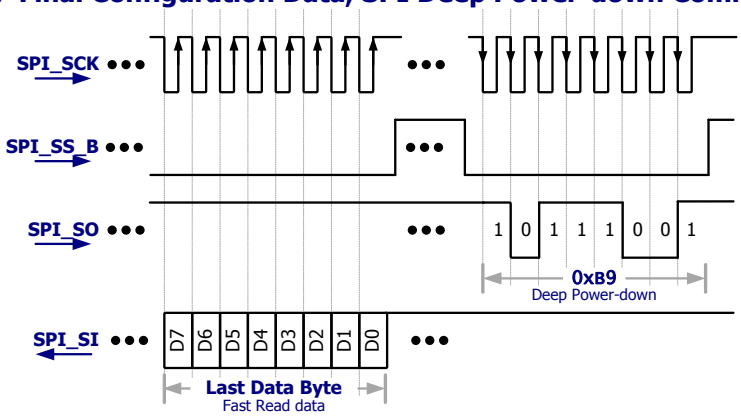
Figure 25: SPI Fast Read Command



The external SPI PROM supplies data on the falling edge of the iCE65 device's SPI_SCK clock output. The iCE65 device captures each PROM data value on the SPI_SI input, using the rising edge of the SPI_SCK clock signal. The SPI PROM data starts at the 24-bit address presented by the iCE65 device. PROM data is serially output, byte by byte, with most-significant bit, D7, presented first. The PROM automatically increments an internal byte counter as long as the PROM is selected and clocked.

After transferring the required number configuration data bits, the iCE65 device ends the Fast Read command by de-asserting its SPI_SS_B PROM select output, as shown in Figure 26. To conserve power, the iCE65 device then optionally issues a final Deep Power-down command, hexadecimal command code 0xB9. After de-asserting the SPI_SS_B output, the SPI PROM enters its Deep Power-down mode. The final power-down step is optional; the application may use the SPI PROM and can skip this step, controlled by a configuration option.

Figure 26: **Final Configuration Data, SPI Deep Power-down Command**



After driving CRESET_B High or allowing it to float High, the AP must wait a minimum of t_{CR_SCK} µs, (see Table 60) allowing the iCE65 FPGA to clear its internal configuration memory.

After waiting for the configuration memory to clear, the AP sends the configuration image generated by the iCEcube development system. An SPI peripheral mode configuration image must not use the ColdBoot or WarmBoot options. Send the entire configuration image, without interruption, serially to the iCE65's SPI_SI input on the falling edge of the SPI_SCK clock input. Once the AP sends the 0x7EAA997E synchronization pattern, the generated SPI_SCK clock frequency must be within the specified 1 MHz to 25 MHz range (40 ns to 1 µs clock period) while sending the configuration image. Send each byte of the configuration image with most-significant bit (msb) first. The AP sends data to the iCE65 FPGA on the falling edge of the SPI_SCK clock. The iCE65 FPGA internally captures each incoming SPI_SI data bit on the rising edge of the SPI_SCK clock. The iCE65's SPI_SO output pin is not used during SPI peripheral mode but must connect to the AP if the AP also programs the iCE65's Nonvolatile Configuration Memory (NVCM).

Prior to sending the iCE65 configuration image , an SPI NVCM shut-off sequence must be sent. See AN014 for details.
The iCE65 configuration image must be sent as one contiguous stream without interruption.
The SPI_SCK clock period must be between 40 ns to 1 µs (1 MHz to 25 MHz).

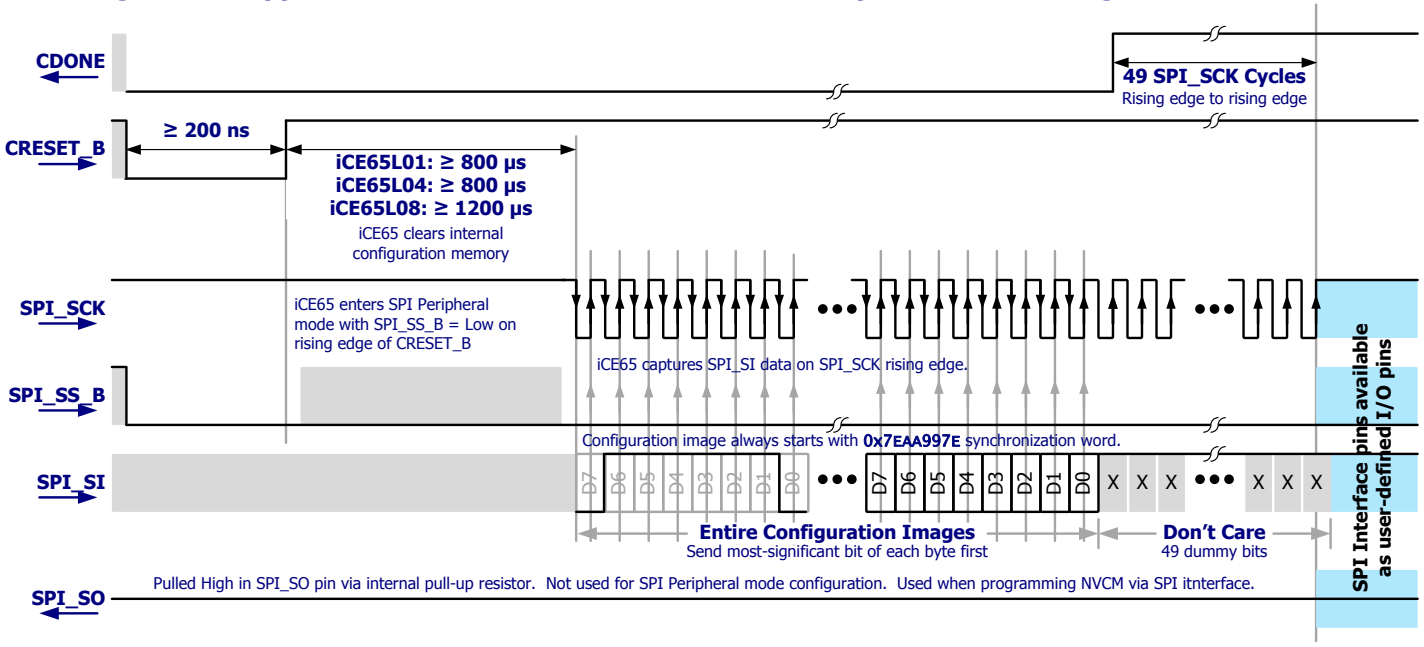
After sending the entire image, the iCE65 FPGA releases the CDONE output allowing it to float High via the 10 kΩ pull-up resistor to AP_VCC. If the CDONE pin remains Low, then an error occurred during configuration and the AP should handle the error accordingly for the application.

After the CDONE output pin goes High, send at least 49 additional dummy bits, effectively 49 additional SPI_SCK clock cycles measured from rising-edge to rising-edge.

After the additional SPI_CLK cycles, the SPI interface pins then become available to the user application loaded in FPGA.

To reconfigure the iCE65 FPGA or to load a different configuration image, merely restart the configuration process by pulsing CRESET_B Low or power-cycling the FPGA.

Figure 29: **Application Processor Waveforms for SPI Peripheral Mode Configuration Process**



The iCE65 configuration image must be sent as one contiguous stream without interruption.

The SPI_SCK clock period must be between 40 ns to 1 µs (1 MHz to 25 MHz).

QN84 Quad Flat Pack No-Lead

The QN84 is a Quad Flat Pack No-Lead package with a 0.5 mm pad pitch.

Footprint Diagram

Figure 34 shows the iCE65 footprint diagram for the QN84 package.

Also see Table 38 for a complete, detailed pinout for the QN84 package.

The signal pins are also grouped into the four I/O Banks and the SPI interface.

Figure 34: **iCE65 QN84 Quad Flat Pack No-Lead Footprint (Top View)**

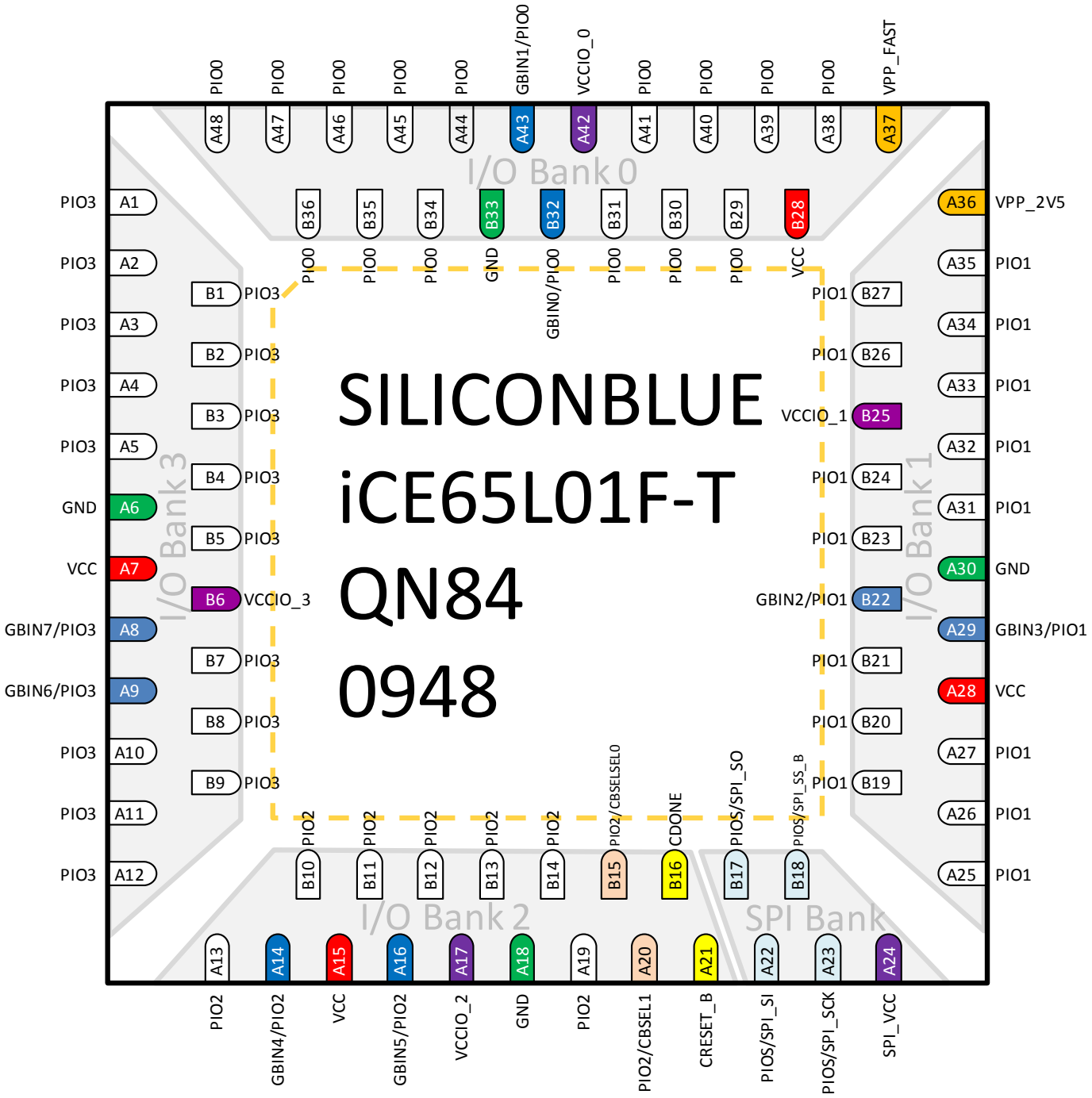
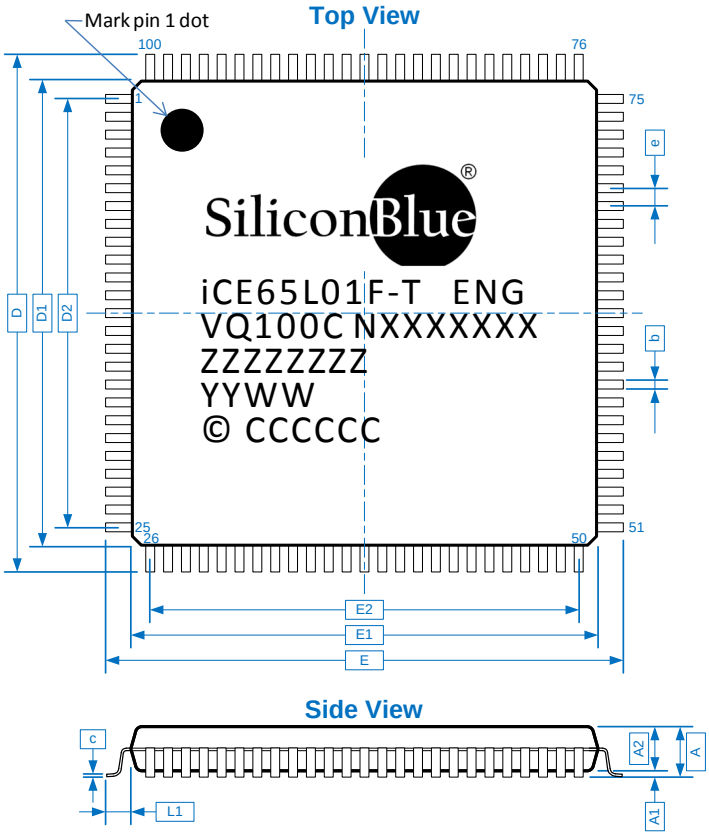


Figure 38: VQ100 Package Mechanical Drawing: NVCM Programmed Device Marking



Description		Symbol	Min.	Nominal	Max.	Units
Leads per Edge	X			25		Leads
	Y			25		
Number of Signal Leads		n		100		
Maximum Size (lead tip to lead tip)	X	E	—	16.0	—	mm
	Y	D	—	16.0	—	
Body Size	X	E1	—	14.0	—	
	Y	D1	—	14.0	—	
Edge Pin Center to Center	X	E2	—	12.0	—	
	Y	D2	—	12.0	—	
Lead Pitch		e	—	0.50	—	
Lead Width		b	0.17	0.20	0.27	
Total Package Height		A	—	1.20	—	
Stand Off		A1	0.05	—	0.15	
Body Thickness		A2	0.95	1.00	1.05	
Lead Length		L1	—	1.00	—	
Lead Thickness		c	0.09	—	0.20	
Coplanarity			—	0.08	—	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65L01F	Part number
	-T	Power/Speed
	ENG	Engineering
3	VQ100C NXXXXXXX	Package type and Lot number
4	ZZZZZZZZ	NVCM Program. code
5	YYWW	Date Code
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
38	32

Ball Function	Ball Number	Pin Type	Bank
PIO0	A5	PIO	0
PIO0	A6	PIO	0
PIO0	A8	PIO	0
PIO0	A10	PIO	0
PIO0	B3	PIO	0
PIO0	B4	PIO	0
PIO0	B5	PIO	0
PIO0	B8	PIO	0
PIO0	B9	PIO	0
PIO0	C5	PIO	0
PIO0	C7	PIO	0
PIO0	C8	PIO	0
PIO0	C9	PIO	0
PIO0	D5	PIO	0
PIO0	D7	PIO	0
PIO0	E5	PIO	0
PIO0	E6	PIO	0
PIO0	E7	PIO	0
PIO0	F7	PIO	0
VCCIO_0	B7	VCCIO	0
GBIN2/PIO1	F9	GBIN	1
GBIN3/PIO1	F8	GBIN	1
PIO1	A11	PIO	1
PIO1	B11	PIO	1
PIO1	C11	PIO	1
PIO1	D8	PIO	1
PIO1	D9	PIO	1
PIO1	D10	PIO	1
PIO1	D11	PIO	1
PIO1	E8	PIO	1
PIO1	E9	PIO	1
PIO1	E11	PIO	1
PIO1	F10	PIO	1
PIO1	G7	PIO	1
PIO1	G8	PIO	1
PIO1	G9	PIO	1
PIO1	G10	PIO	1
PIO1	H7	PIO	1
PIO1	H8	PIO	1
PIO1	H9	PIO	1
PIO1	H10	PIO	1
VCCIO_1	E10	VCCIO	1
CDONE	J7	CONFIG	2
CRESET_B	K7	CONFIG	2
GBIN4/PIO2	L8	GBIN	2
GBIN5/PIO2	L9	GBIN	2
PIO2	H4	PIO	2
PIO2	H5	PIO	2
PIO2	H11	PIO	2
PIO2	J4	PIO	2
PIO2	J5	PIO	2

Ball Function	Ball Number	Pin Type	Bank
PIO2	J11	PIO	2
PIO2	K3	PIO	2
PIO2	K4	PIO	2
PIO2	K11	PIO	2
PIO2	L2	PIO	2
PIO2	L3	PIO	2
PIO2	L4	PIO	2
PIO2	L5	PIO	2
PIO2	L10	PIO	2
PIO2	L11	PIO	2
PIO2/CBSEL0	H6	PIO	2
PIO2/CBSEL1	J6	PIO	2
VCCIO_2	K5	VCCIO	2
PIO3	C1	PIO	3
PIO3	B1	PIO	3
PIO3	D1	PIO	3
PIO3	E2	PIO	3
PIO3	C2	PIO	3
PIO3	D2	PIO	3
PIO3	C3	PIO	3
PIO3	C4	PIO	3
PIO3	E4	PIO	3
PIO3	D4	PIO	3
PIO3	F3	PIO	3
PIO3	G3	PIO	3
PIO3	G4	PIO	3
GBIN6/PIO3	F4	GBIN	3
GBIN7/PIO3	D3	GBIN	3
PIO3	E3	PIO	3
PIO3	F2	PIO	3
PIO3	G1	PIO	3
PIO3	H1	PIO	3
PIO3	J1	PIO	3
PIO3	H2	PIO	3
PIO3	H3	PIO	3
PIO3	J3	PIO	3
PIO3	J2	PIO	3
VCCIO_3	A1	VCCIO	3
VCCIO_3	G2	VCCIO	3
PIOS/SPI_SO	J8	SPI	SPI
PIOS/SPI_SI	K8	SPI	SPI
PIOS/SPI_SCK	K9	SPI	SPI
PIOS/SPI_SS_B	J9	SPI	SPI
SPI_VCC	J10	SPI	SPI
GND	B2	GND	GND
GND	B10	GND	GND
GND	E1	GND	GND
GND	F5	GND	GND
GND	F6	GND	GND
GND	G5	GND	GND
GND	G6	GND	GND
GND	G11	GND	GND

CB132 Chip-Scale Ball-Grid Array

The CB132 package is a partially-populated ball grid array with 0.5 mm ball pitch. The empty ball rings simplify PCB layout. The iCE65L01, iCE65L04 and iCE65L08 devices are available in this package.

Footprint Diagram

Figure 41, Figure 42 and

Figure 43 show the iCE65 footprint diagrams for the CB132 package in iCE65L01, iCE65L04 and iCE65L08 devices. See Figure 48 for the "universal" chip-scale BGA footprint for the CB132 and CB284 packages. The 8 x 8 mm CB132 package fits within the same ball pattern as the 12 x 12 mm CB284 package.

Figure 31 shows the conventions used in the diagram.

Also see Table 41 for a complete, detailed pinout for the 132-ball BGA package.

The signal pins are also grouped into the four I/O Banks and the SPI interface.

***Figure 41*: iCE65L01 CB132 Chip-Scale BGA Footprint (Top View)**

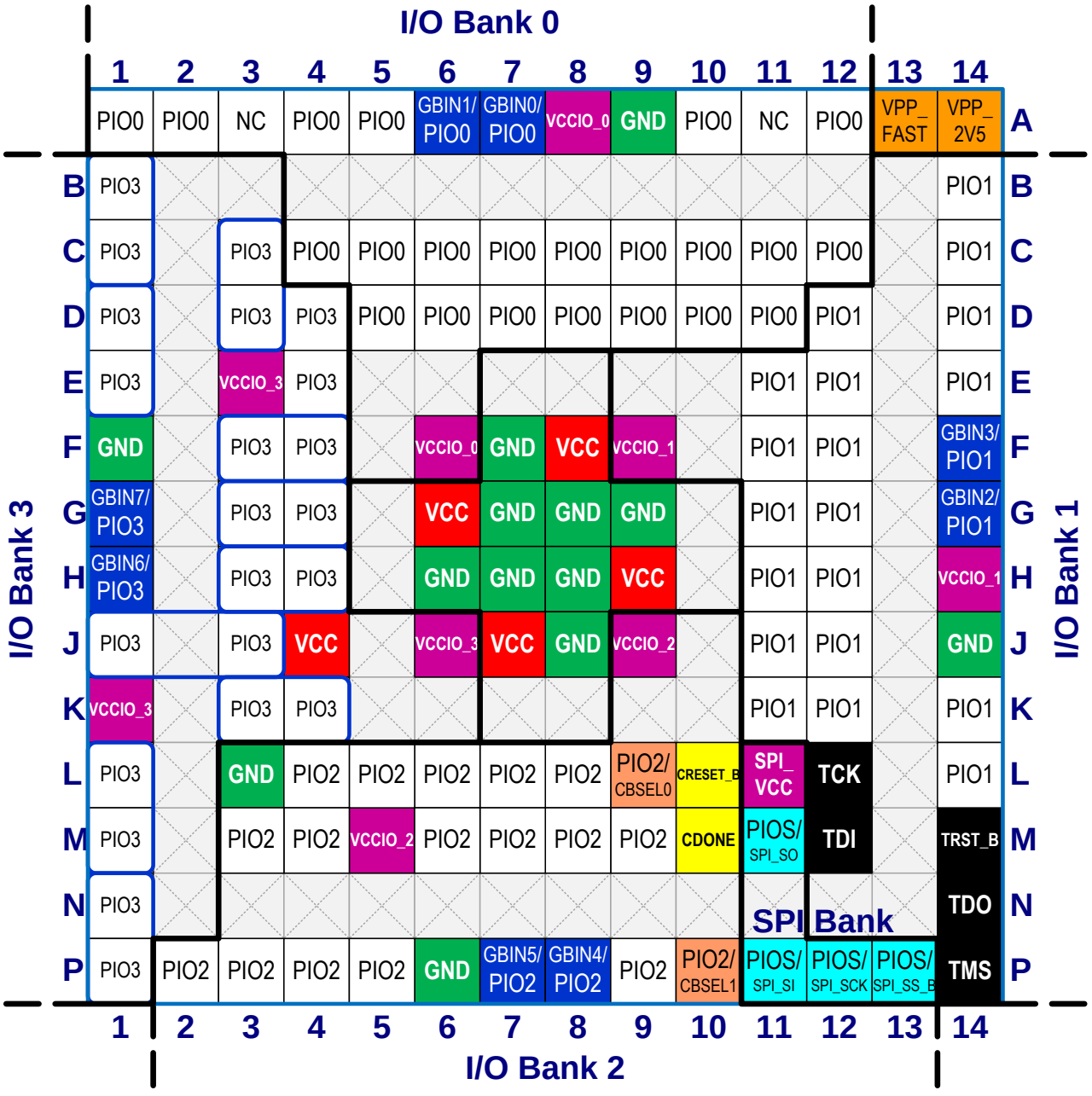
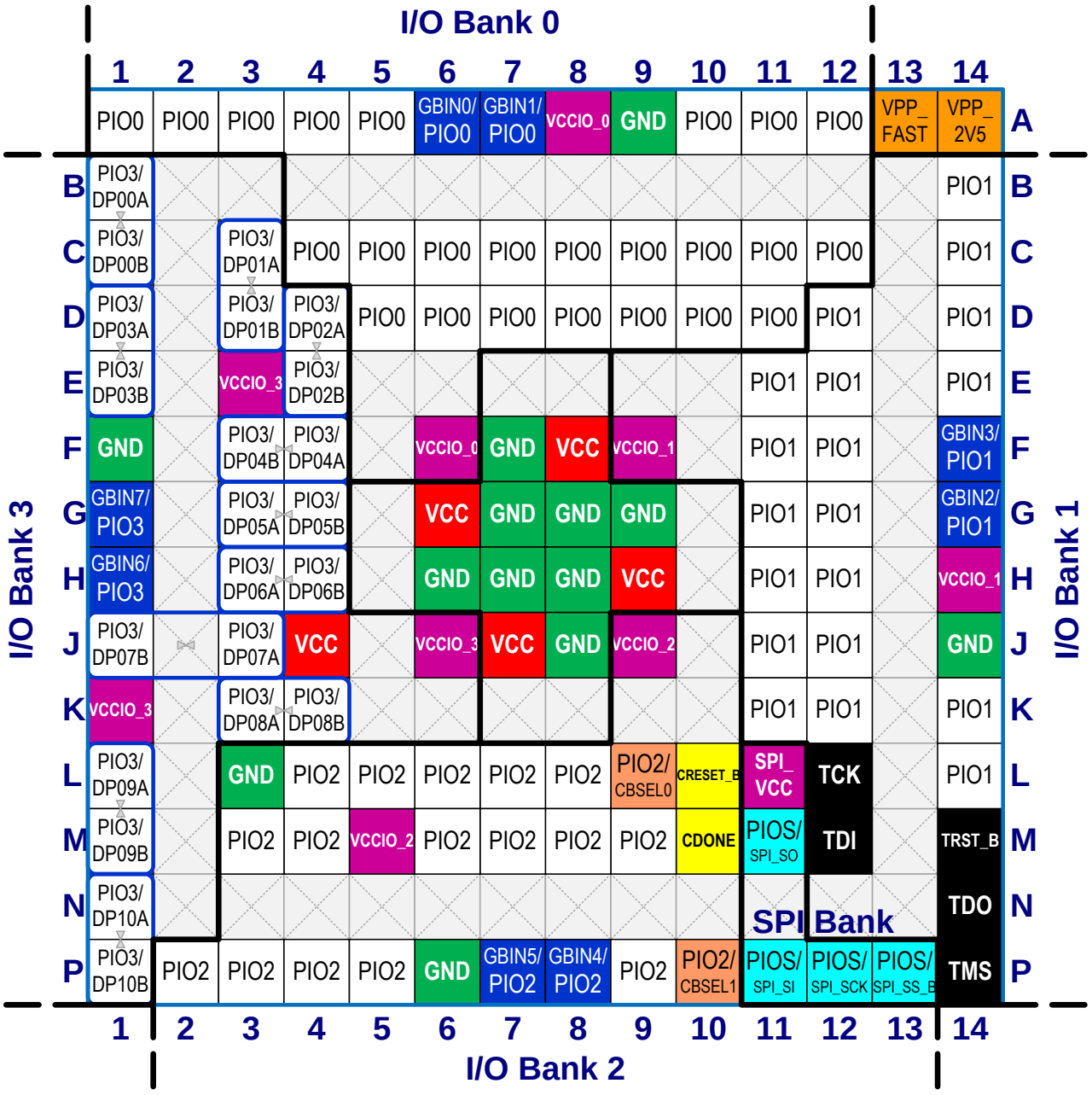


Figure 42: **iCE65L04 CB132 Chip-Scale BGA Footprint (Top View)**



Ball Function	Ball Number	Pin Type	Bank
PIO2 (◆)	***iCE65L04:*** N8 ***iCE65L08:*** L7	PIO	2
PIO2	N9	PIO	2
PIO2	N11	PIO	2
PIO2	N12	PIO	2
PIO2	N13	PIO	2
PIO2	P1	PIO	2
PIO2	P2	PIO	2
PIO2	P3	PIO	2
PIO2	P4	PIO	2
PIO2	P7	PIO	2
PIO2	P8	PIO	2
PIO2	P9	PIO	2
PIO2/CBSEL0	L9	PIO	2
PIO2/CBSEL1	P10	PIO	2
VCCIO_2	J9	VCCIO	2
VCCIO_2	M5	VCCIO	2
VCCIO_2	N10	VCCIO	2
PIO3/DP00A	C1	DPIO	3
PIO3/DP00B	B1	DPIO	3
PIO3/DP01A	D3	DPIO	3
PIO3/DP01B	C3	DPIO	3
PIO3/DP02A	D1	DPIO	3
PIO3/DP02B	D2	DPIO	3
PIO3/DP03A (◆)	***iCE65L04:*** E1 ***iCE65L08:*** E2	DPIO	3
PIO3/DP03B (◆)	***iCE65L04:*** E2 ***iCE65L04:*** E1	DPIO	3
PIO3/DP04A	D4	DPIO	3
PIO3/DP04B	E4	DPIO	3
PIO3/DP05A (◆)	***iCE65L04:*** F3 ***iCE65L08:*** F4	DPIO	3
PIO3/DP05B (◆)	***iCE65L04:*** F4 ***iCE65L08:*** F3	DPIO	3
PIO3/DP06A	F5	DPIO	3
PIO3/DP06B	E5	DPIO	3
PIO3/DP07A (◆)	***iCE65L04:*** G2 ***iCE65L08:*** H4	DPIO	3
GBIN7/PIO3/DP07B (◆)	***iCE65L04:*** G1 ***iCE65L08:*** H3	GBIN	3
GBIN6/PIO3/DP08A	H1	GBIN	3
PIO3/DP08B	H2	DPIO	3
PIO3/DP09A	G3	DPIO	3
PIO3/DP09B	G4	DPIO	3
PIO3/DP10A	J1	DPIO	3
PIO3/DP10B	J2	DPIO	3
PIO3/DP11A (◆)	***iCE65L04:*** H4 ***iCE65L08:*** G1	DPIO	3
PIO3/DP11B (◆)	***iCE65L04:*** H3 ***iCE65L08:*** G2	DPIO	3
PIO3/DP12A	K2	DPIO	3
PIO3/DP12B	J3	DPIO	3

CB284 Chip-Scale Ball-Grid Array

The CB284 package, partially-populated 0.5 mm pitch, ball grid array simplifies PCB layout with empty ball rings.

Footprint Diagram

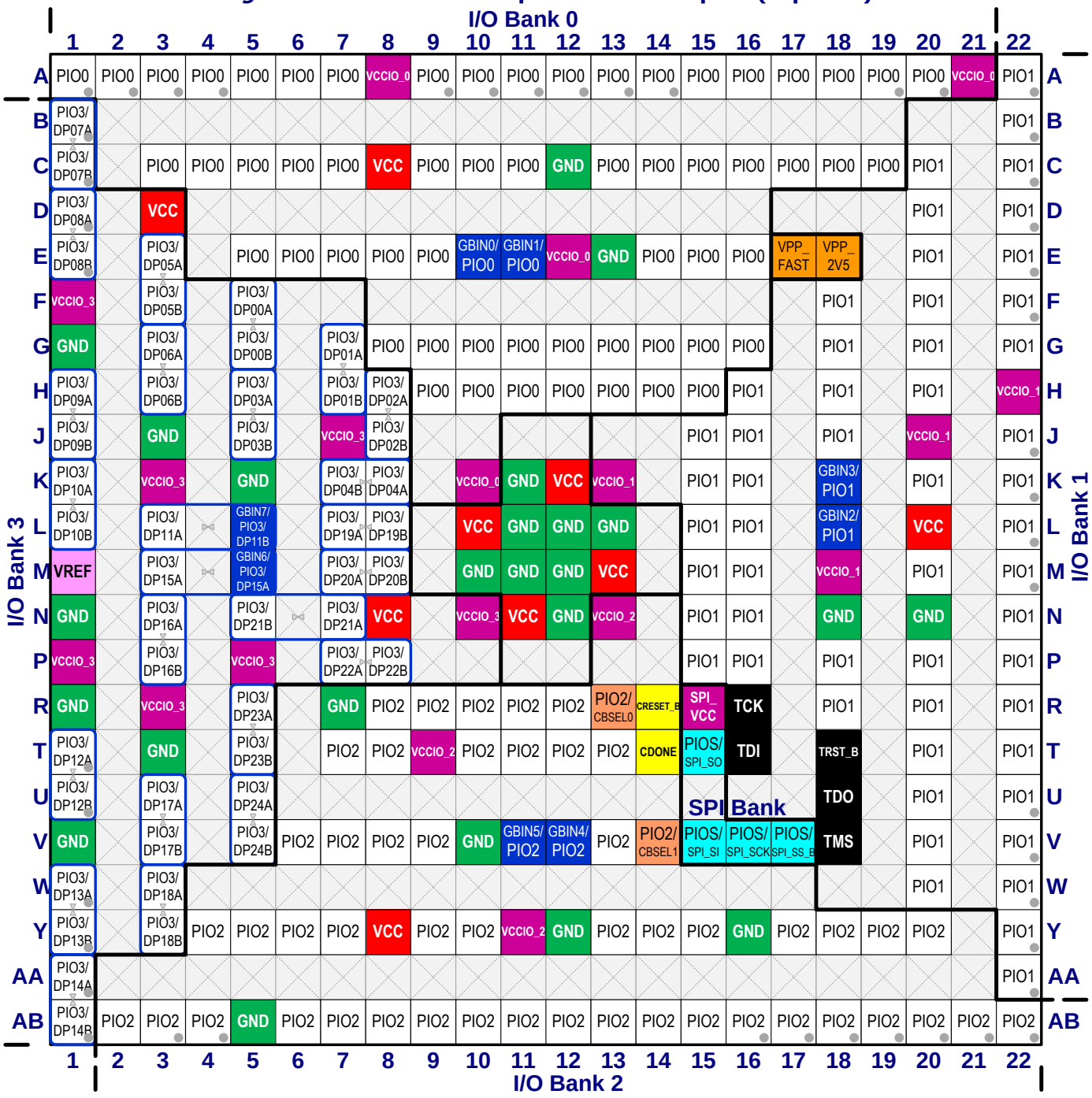
Figure 48 shows the CB284 chip-scale BGA footprint. The 8 x 8 mm CB132 package fits within the same ball pattern as the 12 x 12 mm CB284 package. In other words, the central 8 x 8 section of the CB284 footprint matches the CB132 footprint.

Figure 31 shows the conventions used in the diagram.

Also see Table 44 for a complete, detailed pinout for the 132-ball and 284-ball chip-scale BGA packages.

The signal pins are also grouped into the four I/O Banks and the SPI interface.

Figure 48: **iCE65 CB284 Chip-Scale BGA Footprint (Top View)**



Ball Function	Ball Number iCE65L04 iCE65L08	Pin Type by Device iCE65L04	Pin Type by Device iCE65L08	Bank	CB132 Ball Equivalent
PIO0	E15	PIO	PIO	0	A11
PIO0	E16	PIO	PIO	0	A12
PIO0	G8	PIO	PIO	0	C4
PIO0	G9	PIO	PIO	0	C5
PIO0	G10	PIO	PIO	0	C6
PIO0	G11	PIO	PIO	0	C7
PIO0	G12	PIO	PIO	0	C8
PIO0	G13	PIO	PIO	0	C9
PIO0	G14	PIO	PIO	0	C10
PIO0	G15	PIO	PIO	0	C11
PIO0	G16	PIO	PIO	0	C12
PIO0	H9	PIO	PIO	0	D5
PIO0	H10	PIO	PIO	0	D6
PIO0	H11	PIO	PIO	0	D7
PIO0	H12	PIO	PIO	0	D8
PIO0	H13	PIO	PIO	0	D9
PIO0	H14	PIO	PIO	0	D10
PIO0	H15	PIO	PIO	0	D11
VCCIO_0	A8	VCCIO	VCCIO	0	—
VCCIO_0	A21	VCCIO	VCCIO	0	—
VCCIO_0	E12	VCCIO	VCCIO	0	A8
VCCIO_0	K10	VCCIO	VCCIO	0	F6
GBIN2/PIO1	L18	GBIN	GBIN	1	G14
GBIN3/PIO1	K18	GBIN	GBIN	1	F14
PIO1 (●)	A22	N.C.	PIO	1	—
PIO1 (●)	AA22	N.C.	PIO	1	—
PIO1 (●)	B22	N.C.	PIO	1	—
PIO1	C20	PIO	PIO	1	—
PIO1 (●)	C22	N.C.	PIO	1	—
PIO1	D20	PIO	PIO	1	—
PIO1 (●)	D22	N.C.	PIO	1	—
PIO1	E20	PIO	PIO	1	—
PIO1 (●)	E22	N.C.	PIO	1	—
PIO1	F18	PIO	PIO	1	B14
PIO1	F20	PIO	PIO	1	—
PIO1 (●)	F22	N.C.	PIO	1	—
PIO1	G18	PIO	PIO	1	C14
PIO1	G20	PIO	PIO	1	—
PIO1	G22	PIO	PIO	1	—
PIO1	H16	PIO	PIO	1	D12
PIO1	H18	PIO	PIO	1	D14
PIO1	H20	PIO	PIO	1	—
PIO1	J15	PIO	PIO	1	E11
PIO1	J16	PIO	PIO	1	E12
PIO1	J18	PIO	PIO	1	E14
PIO1 (●)	J22	N.C.	PIO	1	—
PIO1	K15	PIO	PIO	1	F11
PIO1	K16	PIO	PIO	1	F12
PIO1	K20	PIO	PIO	1	—
PIO1 (●)	K22	N.C.	PIO	1	—

Ball Function	Ball Number iCE65L04 iCE65L08	Pin Type by Device iCE65L04	Pin Type by Device iCE65L08	Bank	CB132 Ball Equivalent
PIO2	T13	PIO	PIO	2	M9
PIO2	V6	PIO	PIO	2	P2
PIO2	V7	PIO	PIO	2	P3
PIO2	V8	PIO	PIO	2	P4
PIO2	V9	PIO	PIO	2	P5
PIO2	V13	PIO	PIO	2	P9
PIO2	Y4	PIO	PIO	2	—
PIO2	Y5	PIO	PIO	2	—
PIO2	Y6	PIO	PIO	2	—
PIO2	Y7	PIO	PIO	2	—
PIO2	Y9	PIO	PIO	2	—
PIO2	Y10	PIO	PIO	2	—
PIO2	Y13	PIO	PIO	2	—
PIO2	Y14	PIO	PIO	2	—
PIO2	Y15	PIO	PIO	2	—
PIO2	Y17	PIO	PIO	2	—
PIO2	Y18	PIO	PIO	2	—
PIO2	Y19	PIO	PIO	2	—
PIO2	Y20	PIO	PIO	2	—
PIO2	AB2	PIO	PIO	2	—
PIO2 (●)	AB3	N.C.	PIO	2	—
PIO2 (●)	AB4	N.C.	PIO	2	—
PIO2	AB6	PIO	PIO	2	—
PIO2	AB7	PIO	PIO	2	—
PIO2	AB8	PIO	PIO	2	—
PIO2	AB9	PIO	PIO	2	—
PIO2	AB10	PIO	PIO	2	—
PIO2	AB11	PIO	PIO	2	—
PIO2	AB12	PIO	PIO	2	—
PIO2	AB13	PIO	PIO	2	—
PIO2	AB14	PIO	PIO	2	—
PIO2	AB15	PIO	PIO	2	—
PIO2 (●)	AB16	N.C.	PIO	2	—
PIO2 (●)	AB17	N.C.	PIO	2	—
PIO2 (●)	AB18	N.C.	PIO	2	—
PIO2 (●)	AB19	N.C.	PIO	2	—
PIO2 (●)	AB20	N.C.	PIO	2	—
PIO2 (●)	AB21	N.C.	PIO	2	—
PIO2 (●)	AB22	N.C.	PIO	2	—
PIO2/CBSEL0	R13	PIO	PIO	2	L9
PIO2/CBSEL1	V14	PIO	PIO	2	P10
VCCIO_2	N13	VCCIO	VCCIO	2	J9
VCCIO_2	T9	VCCIO	VCCIO	2	M5
VCCIO_2	Y11	VCCIO	VCCIO	2	—
PIO3/DP00A	F5	DPIO	DPIO	3	B1
PIO3/DP00B	G5	DPIO	DPIO	3	C1
PIO3/DP01A	G7	DPIO	DPIO	3	C3
PIO3/DP01B	H7	DPIO	DPIO	3	D3
PIO3/DP02A	H8	DPIO	DPIO	3	D4
PIO3/DP02B	J8	DPIO	DPIO	3	E4

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO3_20/DP10A	—	H8	39	129.735	2,462.665
PIO3_21/DP10B	—	J8	40	231.735	2,427.665
PIO3_22/DP11A	G1	T1	41	129.735	2,392.665
PIO3_23/DP11B	G2	U1	42	231.735	2,357.665
VCCIO_3	K1	N10	43	129.735	2,322.665
VCCIO_3	—	—	44	231.735	2,287.665
VREF	N/A	M1	45	129.735	2,252.665
VREF	N/A	—	46	231.735	2,217.665
GND	J5	N1	47	129.735	2,182.665
GND	—	—	48	231.735	2,147.665
VCCIO_3	J6	P1	49	129.735	2,112.665
VCCIO_3	—	—	50	231.735	2,077.665
GND	H6	R1	51	129.735	2,042.665
GND	—	—	52	231.735	2,007.665
PIO3_24/DP12A	H4	L3	53	129.735	1,972.665
GBIN7/PIO3_25/DP12B	H3	L5	54	231.735	1,937.665
GND	H7	V1	55	129.735	1,902.665
GBIN6/PIO3_26/DP13A	H1	M5	56	231.735	1,867.665
PIO3_27/DP13B	H2	M3	57	129.735	1,832.665
PIO3_28/DP14A	—	N7	58	231.735	1,798.665
PIO3_29/DP14B	—	N5	59	129.735	1,762.665
PIO3_30/DP15A	J1	N3	60	231.735	1,727.665
PIO3_31/DP15B	J2	P3	61	129.735	1,692.665
GND	J5	M11	62	231.735	1,657.665
GND	—	—	63	129.735	1,622.665
PIO3_32/DP16A	H5	W1	64	231.735	1,587.665
PIO3_33/DP16B	G5	Y1	65	129.735	1,552.665
VCCIO_3	J6	R3	66	231.735	1,517.665
VCCIO_3	—	—	67	129.735	1,482.665
GND	J5	T3	68	231.735	1,447.665
GND	—	—	69	129.735	1,412.665
PIO3_34/DP17A	K2	AA1	70	231.735	1,377.665
PIO3_35/DP17B	J3	AB1	71	129.735	1,342.665
PIO3_36/DP18A	—	L7	72	231.735	1,307.665
PIO3_37/DP18B	—	L8	73	129.735	1,272.665
PIO3_38/DP19A	—	M7	74	231.735	1,237.665
PIO3_39/DP19B	—	M8	75	129.735	1,202.665
PIO3_40/DP20A	L1	P7	76	231.735	1,167.665
PIO3_41/DP20B	L2	P8	77	129.735	1,132.665
VCC	J4	N8	78	231.735	1,097.665
VCC	—	—	79	129.735	1,062.665
PIO3_42/DP21A	K4	R5	80	231.735	1,027.665
PIO3_43/DP21B	K3	T5	81	129.735	992.665
VCCIO_3	K1	P5	82	231.735	957.665
VCCIO_3	—	—	83	129.735	912.665
GND	L3	R7	84	231.735	867.665
GND	—	—	85	129.735	822.67

I/O Banks 0, 1, 2 and SPI Bank Characteristic Curves

Figure 52: **Typical LVCMOS Output Low Characteristics (I/O Banks 0, 1, 2, and SPI)**

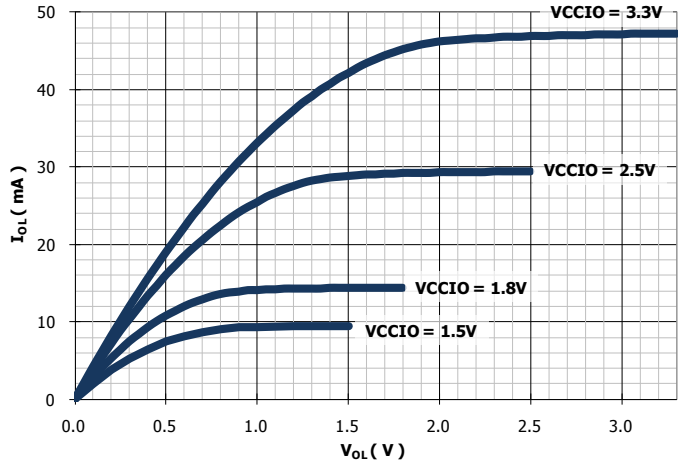


Figure 53: **Typical LVCMOS Output High Characteristics (I/O Banks 0, 1, 2, and SPI)**

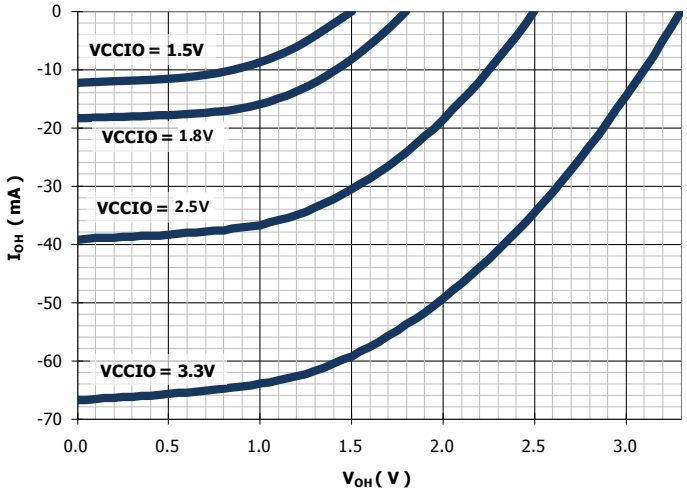


Figure 54: **Input with Internal Pull-Up Resistor Enabled (I/O Banks 0, 1, 2, and SPI)**

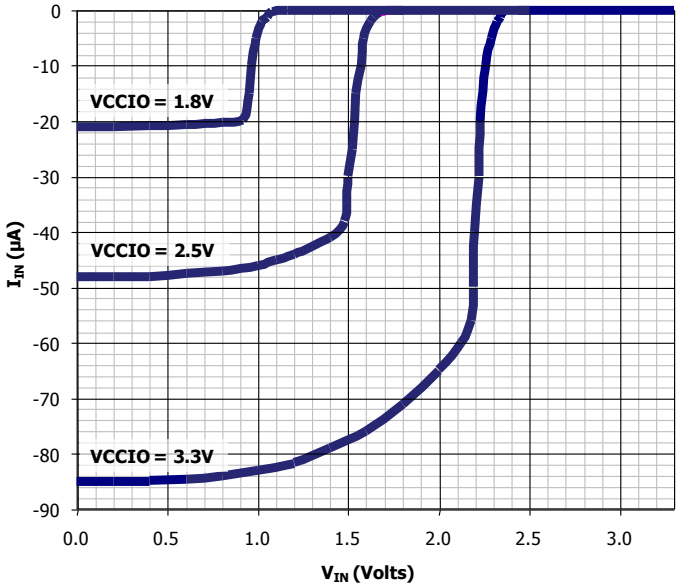


Table 60 provides various timing specifications for the SPI peripheral mode interface.

Table 60: SPI Peripheral Mode Timing

Symbol	From	To	Description		All Grades Min.	All Grades Max.	Units
t_{CR_SCK}	CRESET_B	SPI_SCK	Minimum time from a rising edge on CRESET_B until the first SPI write operation, first SPI_SCK. During this time, the iCE65 FPGA is clearing its internal configuration memory	iC65L01	800	—	µs
				iC65L04	800		
				iC65L08	1200		
$t_{SUSPISI}$	SPI_SI	SPI_SCK	Setup time on SPI_SI before the rising SPI_SCK clock edge		12	—	ns
$t_{HDSPISI}$	SPI_SCK	SPI_SI	Hold time on SPI_SI after the rising SPI_SCK clock edge		12	—	ns
$t_{SPISCKH}$	SPI_SCK	SPI_SCK	SPI_SCK clock High time		20	—	ns
$t_{SPISCKL}$	SPI_SCK	SPI_SCK	SPI_SCK clock Low time		20	—	ns
$t_{SPISCKCYC}$	SPI_SCK	SPI_SCK	SPI_SCK clock period*		40	1,000	ns
F_{SPI_SCK}	SPI_SCK	SPI_SCK	Sustained SPI_SCK clock frequency*		1	25	MHz

* = Applies after sending the synchronization pattern.

Power Consumption Characteristics

Core Power

Table 61 shows the power consumed on the internal VCC supply rail when the device is filled with 16-bit binary counters, measured with a 32.768 kHz and at 32.0 MHz. Low power (-L) at 1.0 V operation and high-performance (-T) version at 1.2V operation is provided.

***Table 61:* VCC Power Consumption for Device Filled with 16-Bit Binary Counters**

Symbol	Description	Grade	VCC	iCE65L01 Typical	iCE65L01 Max.	iCE65L04 Typical	iCE65L04 Max.	iCE65L08 Typical	iCE65L08 Max.	Units
I_{CC0K}	f =0,	-L	1.0V	12		26		54		µA
		-T	1.2V	19		43		90		
I_{CC32K}	f ≤ 32.768 kHz	-L	1.0V	15		31		62		µA
		-T	1.2V	23		50		100		
I_{CC32M}	f = 32.0 MHz	-L	1.0V	3		7		14		mA
		-T	1.2V	4		8		17		

I/O Power

Table 62 provides the static current by I/O bank. The typical current for I/O Banks 0, 1, 2 and the SPI bank is not measurable within the accuracy of the test environment. The PIOs in I/O Bank 3 use different circuitry and dissipate a small amount of static current.

Table 62: I/O Bank Static Current (f = 0 MHz)

Symbol	Description		Typical	Max	Units
I_{CCO_0}	I/O Bank 0	Static current consumption per I/O bank. f = 0 MHz. No PIO pull-up resistors enabled. All inputs grounded. All outputs driving Low.	« 1		µA
I_{CCO_1}	I/O Bank 1		« 1		µA
I_{CCO_2}	I/O Bank 2		« 1		µA
I_{CCO_3}	I/O Bank 3		iCE65L01: « 1 iCE65L04/08: 1.2		µA
I_{CCO_SPI}	SPI Bank		« 1		µA

NOTE: The typical static current for I/O Banks 0, 1, 2, and the SPI bank is less than the accuracy of the device tester.

Power Estimator

To estimate the power consumption for a specific application, please download and use the iCE65 Power Estimator Spreadsheet our use the power estimator built into the iCEcube software.

- iCE65 Power Estimator Spreadsheet