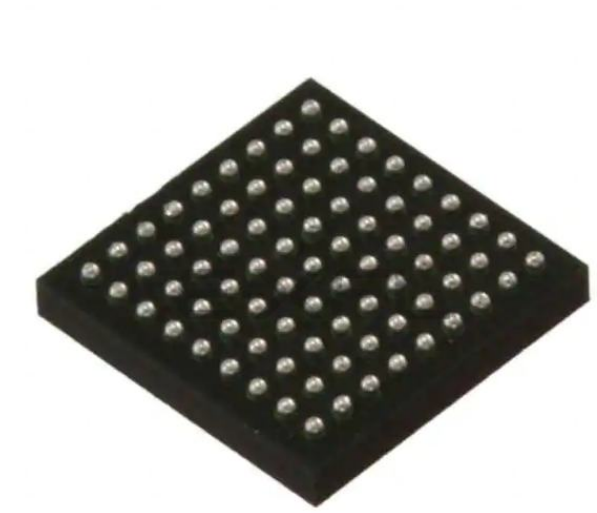

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

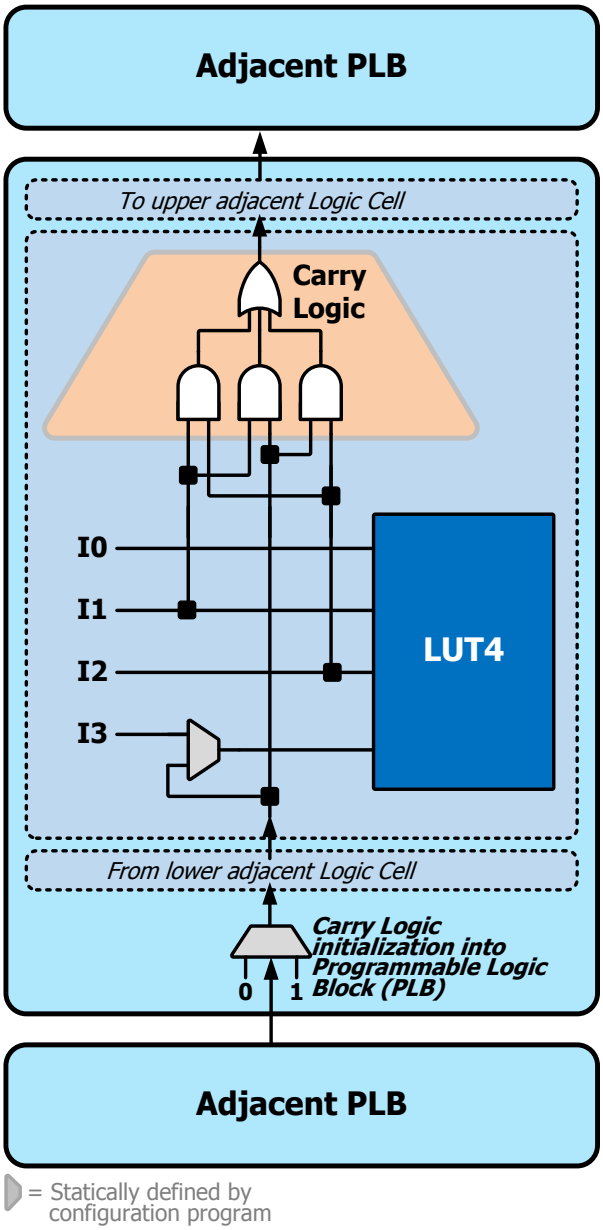
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	160
Number of Logic Elements/Cells	1280
Total RAM Bits	65536
Number of I/O	63
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	81-VFBGA, CSPBGA
Supplier Device Package	81-CSBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice65l01f-lcb81c

The Carry Logic generates the carry value to feed the next bit in the adder. The calculated carry value replaces the I3 input to the next LUT4 in the upper Logic Cell.

If required by the application, the carry output from the final stage of the adder is available by passing it through the final LUT4.

Figure 5: **Carry Logic Structure within a Logic Cell and between PLBs**



If not connected to an external SPI PROM, the four pins associated with the SPI Master Configuration Interface can be used as PIO pins, supplied by the SPI_VCC input, essentially forming a fifth "mini" I/O bank. If using an SPI Flash PROM, then connect SPI_VCC to 3.3V.

I/O Banks 0, 1, 2, SPI and Bank 3 of iCE65L01

Table 6 highlights the available I/O standards when using an iCE65 device, indicating the drive current options, and in which bank(s) the standard is supported. I/O Banks 0, 1, 2 and SPI interface support the same standards. I/O Bank 3 has additional capabilities in iCE65L04 and iCE65L08, including support for MDDR memory standards and LVDS differential I/O.

***Table 6:* I/O Standards for I/O Banks 0, 1, 2, SPI Interface Bank, and Bank 3 of iCE65L01**

I/O Standard	Supply Voltage	Drive Current (mA)	Attribute Name
5V Input Tolerance	3.3V	N/A	N/A
LVCMOS33	3.3V	±11	SB_LVCMOS
LVCMOS25	2.5V	±8	
LVCMOS18	1.8V	±5	
LVCMOS15 outputs	1.5V	±4	

IBIS Models for I/O Banks 0, 1, 2 and the SPI Bank

The IBIS (I/O Buffer Information Specification) file that describes the output buffers used in I/O Banks 0, 1, 2, SPI Bank and Bank 3 of iCE65L01 is available from the following link.

- IBIS Models for I/O Banks 0, 1, 2, SPI Bank and Bank 3 of iCE65L01

I/O Bank 3 of iCE65L04 and iCE65L08

I/O Bank 3, located along the left edge of the die, has additional special I/O capabilities to support memory components and differential I/O signaling (LVDS). Table 7 lists the various I/O standards supported by I/O Bank 3. The SSTL2 and SSTL18 I/O standards require the VREF voltage reference input pin which is only available on the CB284 package. Also see Table 51 for electrical characteristics.

***Table 7:* I/O Standards for I/O Bank 3 Only of iCE65L04 and iCE65L08**

I/O Standard	Supply Voltage	VREF Pin (CB284 or DiePlus) Required?	Target Drive Current (mA)	Attribute Name
LVCMOS33	3.3V	No	±8	SB_LVCMOS33_8
LVCMOS25	2.5V	No	±16	SB_LVCMOS25_16
			±12	SB_LVCMOS25_12
			±8	SB_LVCMOS25_8
			±4	SB_LVCMOS25_4
LVCMOS18	1.8V	No	±10	SB_LVCMOS18_10
			±8	SB_LVCMOS18_8
			±4	SB_LVCMOS18_4
			±2	SB_LVCMOS18_2
LVCMOS15	1.5V	No	±4	SB_LVCMOS15_4
			±2	SB_LVCMOS15_2
SSTL2_II	2.5V	Yes	±16.2	SB_SSTL2_CLASS_2
SSTL2_I			±8.1	SB_SSTL2_CLASS_1
SSTL18_II	1.8V	Yes	±13.4	SB_SSTL18_FULL
SSTL18_I			±6.7	SB_SSTL18_HALF
MDDR	1.8V	No	±10	SB_MDDR10
			±8	SB_MDDR8
			±4	SB_MDDR4
			±2	SB_MDDR2
LVDS	2.5V	No	N/A	SB_LVDS_INPUT

Input Signal Path

As shown in Figure 7, a signal from a package pin optionally feeds directly into the device, or is held in an input register. The input signal connects to the programmable interconnect resources through the IN signal. Table 9 describes the input behavior, assuming that the output path is not used or if a bidirectional I/O, that the output driver is in its high-impedance state (Hi-Z). Table 9 also indicates the effect of the Power-Saving I/O Bank iCEgate Latch and the Input Pull-Up Resistors on I/O Banks 0, 1, and 2.

See Input and Output Register Control per PIO Pair for information about the registered input path.

Power-Saving I/O Bank iCEgate Latch

To save power, the optional iCEgate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Registered inputs are effectively frozen by their associated clock or clock-enable control. As shown in Figure 10, the iCEgate HOLD control signal captures the external value from the associated asynchronous input. The HOLD signal prevents switching activity on the PIO pad from affecting internal logic or programmable interconnect. Minimum power consumption occurs when there is no switching. However, individual pins within the I/O bank can bypass the iCEgate latch and directly feed into the programmable interconnect, remaining active during low-power operation. This behavior is described in Table 9. The decision on which asynchronous inputs use the iCEgate feature and which inputs bypass it is determined during system design. In other words, the iCEgate function is part of the source design used to create the iCE65 configuration image.

Figure 10: Power-Saving iCEgate Latch

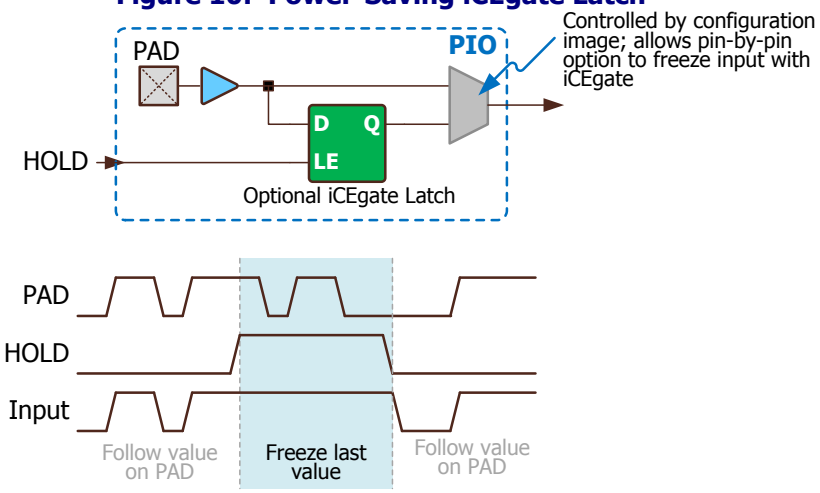


***Table 9:* PIO Non-Registered Input Operations**

Operation	HOLD	Bitstream Setting		PAD	IN
	iCEgate Latch	Controlled by iCEgate?	Input Pull-Up Enabled?	Pin Value	Input Value to Interconnect
Data Input	0	X	X	PAD	PAD Value
Pad Floating, No Pull-up	0	X	No	Z	(Undefined)
Pad Floating, Pull-up	0	X	Yes	Z	1
Data Input, Latch Bypassed	X	No	X	PAD	PAD Value
Pad Floating, No Pull-up, Latch Bypassed	X	No	No	Z	(Undefined)
Pad Floating, Pull-up, Latch Bypassed	X	No	Yes	Z	1
Low Power Mode, Hold Last Value	1	Yes	X	X	Last Captured PAD Value

There are four iCEgate HOLD controls, one per each I/O bank. The iCEgate HOLD control input originates within the interconnect fabric, near the middle of the I/O edge. Consequently, the HOLD signal is optionally controlled externally through a PIO pin or from other logic within the iCE65 device.

For best possible performance, the global buffer inputs (GBIN[7:0]) connect directly to the their associated global buffers (GBUF[7:0]), bypassing the PIO logic and iCEgate circuitry as shown in Figure 7. Consequently, the direct GBIN-to-GBUF connection cannot be blocked by the iCEgate circuitry. However, it is possible to use iCEgate to block PIO-to-GBUF clock connections.

For additional information on using the iCEgate feature, please refer to the following application note.

AN002: Using iCEgate Blocking for Ultra-Low Power

Input Pull-Up Resistors on I/O Banks 0, 1, and 2

The PIO pins in I/O Banks 0, 1, and 2 have an optional input pull-up resistor. Pull-up resistors are not provided in iCE65L04 and iCE65L08 I/O Bank 3. During the iCE65 configuration process, the input pull-up resistor is unconditionally enabled and pulls the input to within a diode drop of the associated I/O bank supply voltage (VCCIO_#). This prevents any signals from floating on the circuit board during configuration.

After iCE65 configuration is complete, the input pull-up resistor is optional, defined by a configuration bit. The pull-up resistor is also useful to tie off unused PIO pins. The Lattice iCEcube development software defines all unused PIO pins in I/O Banks 0, 1 and 2 as inputs with the pull-up resistor turned on. The pull-up resistor value depends on the VCCIO voltage applied to the bank, as shown in Table 49.

Note: JTAG inputs TCK, TDI and TMS do not have the input pull-up resistor and must be tied off to GND when unused, else VCCIO_1 draws current.

No Input Pull-up Resistors on I/O Bank 3 of iCE65L04 and iCE65L08

The PIO pins in I/O Bank 3 do not have an internal pull-up resistor. To minimize power consumption, tie unused PIO pins in Bank 3 to a known logic level or drive them as a disabled high-impedance output.

Input Hysteresis

Inputs typically have about 50 mV of hysteresis, as indicated in Table 49.

Output and Output Enable Signal Path

As shown in Figure 7, a signal from programmable interconnect feeds the OUT signal on a Programmable I/O pad. This output connects either directly to the associated package pin or is held in an optional output flip-flop. Because all flip-flops are automatically reset after configuration, the output from the output flip-flop can be optionally inverted so that an active-Low output signal is held in the disabled (High) state immediately after configuration.

Similarly, each Programmable I/O pin has an output enable or three-state control called OE. When OE = High, the OUT output signal drives the associated pad, as described in Table 10. When OE = Low, the output driver is in the high-impedance (Hi-Z) state. The OE output enable control signal itself connects either directly to the output buffer or is held in an optional register. The output buffer is optionally permanently enabled or permanently disabled, either to unconditionally drive output signals, or to allow input-only signals.

Table 10: **PIO Output Operations (non-registered operation, no inversions)**

Operation	OUT Data Output	OE Enable	PAD
Three-State	X	0	Hi-Z
Drive Output Data	OUT	1*	OUT

X = don't care, 1* = High or unused, Hi-Z = high-impedance, three-stated, floating.

See Input and Output Register Control per PIO Pair for information about the registered input path.

Input and Output Register Control per PIO Pair

PIO pins are grouped into pairs for synchronous control. Registers within pairs of PIO pins share common input clock, output clock, and I/O clock enable control signals, as illustrated in Figure 11. The combinational logic paths are removed from the drawing for clarity.

The INCLK clock signal only controls the input flip-flops within the PIO pair.

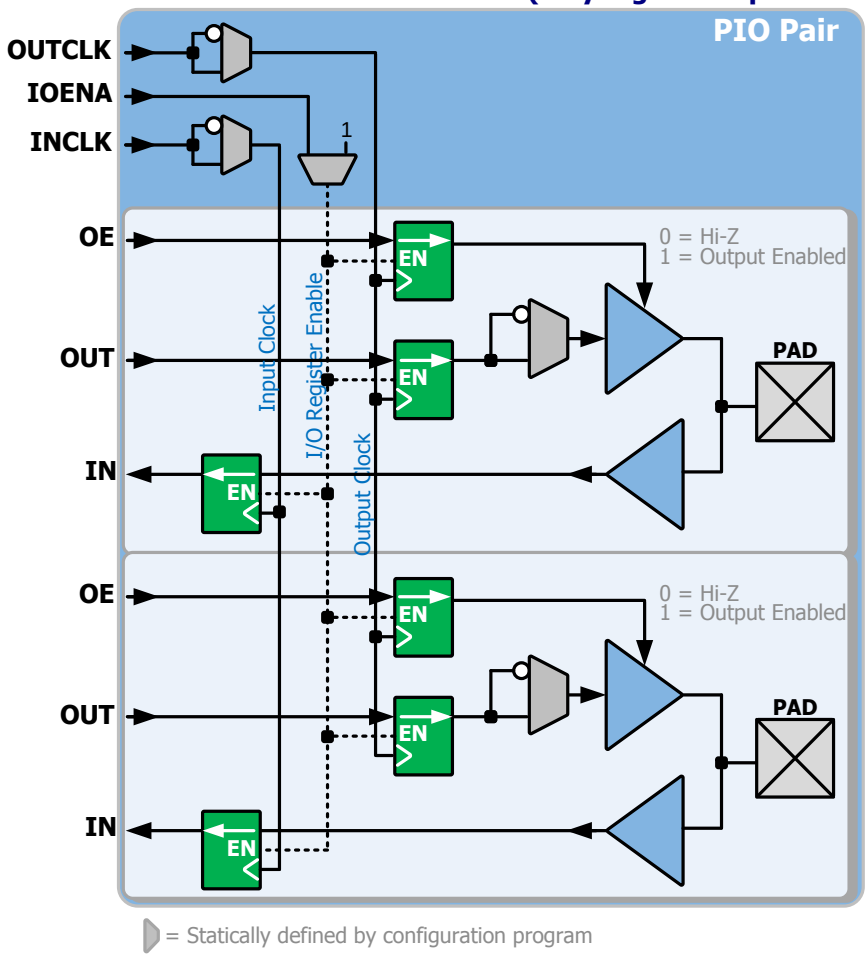
The OUTCLK clock signal controls the output flip-flops and the output-enable flip-flops within the PIO pair.

If desired in the iCE65 application, the INCLK and OUTCLK signals can be connected together.

The IOENA clock-enable input, if used, enables all registers in the PIO pair, as shown in Figure 11. By default, the registers are always enabled.

Before laying out your printed-circuit board, run the design through the iCEcube development software to verify that your selected pinout complies with these I/O register pairing requirements. See tables in "Die Cross Reference" starting on page 84.

Figure 11: **PIO Pairs Share Clock and Clock Enable Controls (only registered paths shown for clarity)**

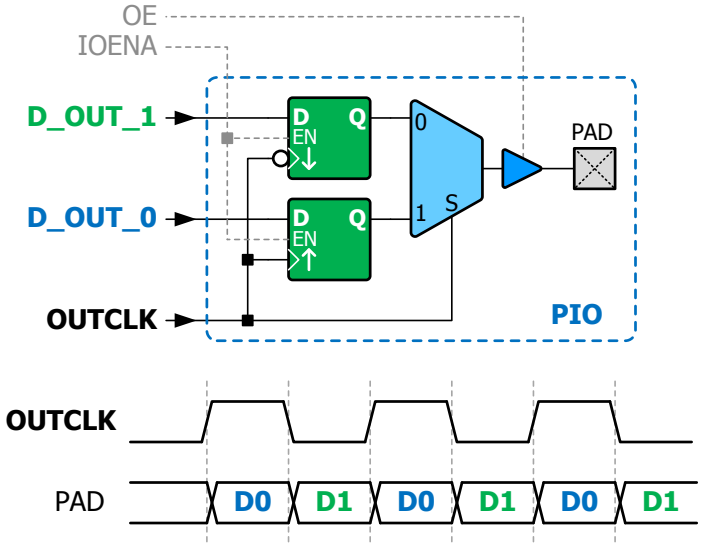


The pairing of PIO pairs is most evident in the tables in "Die Cross Reference" starting on page 84.

Double Data Rate (DDR) Flip-Flops

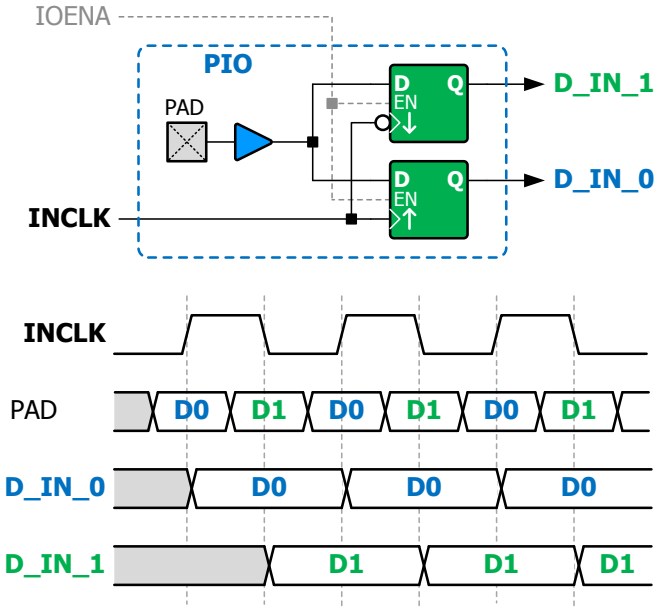
Each individual PIO pin optionally has two sets of double data rate (DDR) flip-flops; one input pair and one output pair. Figure 12 demonstrates the functionality of the output DDR flip-flop. Two signals from within the iCE65 device drive the DDR output flip-flop. The D_OUT_0 signal is clocked by the rising edge of the OUTCLK signal while the D_OUT_1 signal is clocked by the falling edge of the OUTCLK signal, assuming no optional clock polarity inversion. Internally, the two individual flip-flops are multiplexed together before the data appears at the pad, effectively doubling the output data rate.

Figure 12: DDR Output Flip-Flop



Similarly, Figure 13 demonstrates the DDR input flip-flop functionality. A double data rate (DDR) signal arrives at the pad. Internally, one value is clocked by the rising edge of the INCLK signal and another value is clocked by the falling edge of the INCLK signal. The DDR data stream is effectively de-multiplexed within the PIO pin and presented to the programmable interconnect on D_IN_0 and D_IN_1.

Figure 13: DDR Input Flip-Flop



The DDR flip-flops provide several design advantages. Internally within the iCE65 device, the clock frequency is half the effective external data rate. The lower clock frequency eases internal timing, doubling the clock period, and slashes the clock-related power in half.

Global Routing Resources

Global Buffers

Each iCE65 component has eight global buffer routing connections, illustrated in Figure 14. There are eight high-drive buffers, connected to the eight low-skew, global lines. These lines are designed primarily for clock distribution but are also useful for other high-fanout signals such as set/reset and enable signals. The global buffers originate either from the Global Buffer Inputs (GBINx) or from programmable interconnect. The associated GBINx pin represents the best pin to drive a global buffer from an external source. However, the application with an iCE65 FPGA can also drive a global buffer via any other PIO pin or from internal logic using the programmable interconnect.

If not used in an application, individual global buffers are turned off to save power.

Figure 14: **High-drive, Low-skew, High-fanout Global Buffer Routing Resources**

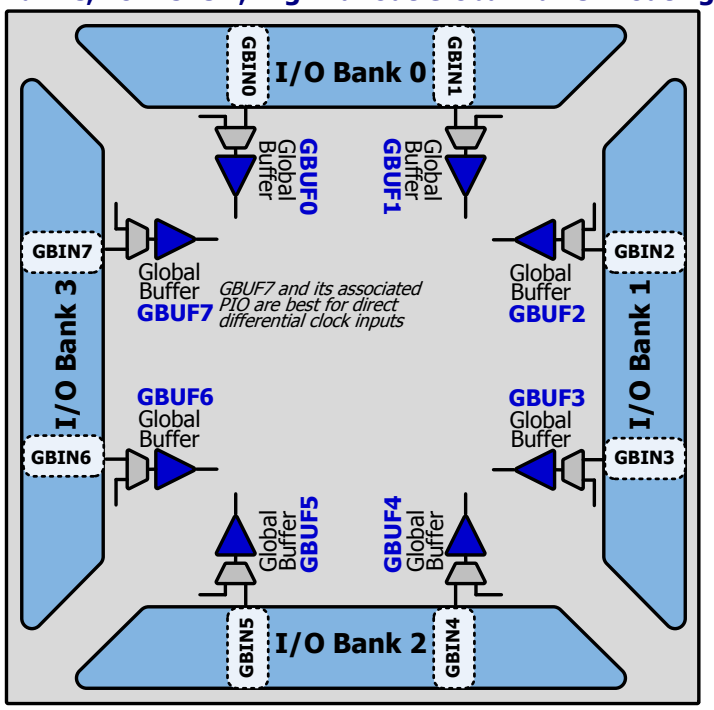


Table 11 lists the connections between a specific global buffer and the inputs on a Programmable Logic Block (PLB). All global buffers optionally connect to all clock inputs. Any four of the eight global buffers can drive logic inputs to a PLB. Even-numbered global buffers optionally drive the Reset input to a PLB. Similarly, odd-numbered buffers optionally drive the PLB clock-enable input.

Table 11: **Global Buffer (GBUF) Connections to Programmable Logic Block (PLB)**

Global Buffer	LUT Inputs	Clock	Clock Enable	Reset
GBUF0	Yes, any 4 of 8 GBUF buffers	Yes	Yes	No
GBUF1		Yes	No	Yes
GBUF2		Yes	Yes	No
GBUF3		Yes	No	Yes
GBUF4		Yes	Yes	No
GBUF5		Yes	No	Yes
GBUF6		Yes	Yes	No
GBUF7		Yes	No	Yes

- Register file and scratchpad RAM
- First-In, First-Out (FIFO) memory for data buffering applications
- Circuit buffer
- A 256-deep by 16-wide ROM with registered outputs, contents loaded during configuration
  - Sixteen different 8-input look-up tables
  - Function or waveform tables such as sine, cosine, etc.
  - Correlators or pattern matching operations
- Counters, sequencers

As pictured in Figure 17, a RAM4K block has separate write and read ports, each with independent control signals. Table 17 lists the signals for both ports. Additionally, the write port has an active-Low bit-line write-enable control; optionally mask write operations on individual bits. By default, input and output data is 16 bits wide, although the data width is configurable using programmable logic and, if needed, multiple RAM4K blocks.

The WCLK and RCLK inputs optionally connect to one of the following clock sources.

- The output from any one of the eight Global Buffers, or
- A connection from the general-purpose interconnect fabric

The data contents of the RAM4K block are optionally pre-loaded during iCE65 device configuration. If the RAM4K blocks are not pre-loaded during configuration, then the resulting configuration bitstream image is smaller. However, if an uninitialized RAM4K block is used in the application, then the application must initialize the RAM contents to guarantee the data value.

See Table 56 for detailed timing information.

Signals

Table 17 lists the signal names, direction, and function of each connection to the RAM4K block. See also Figure 17.

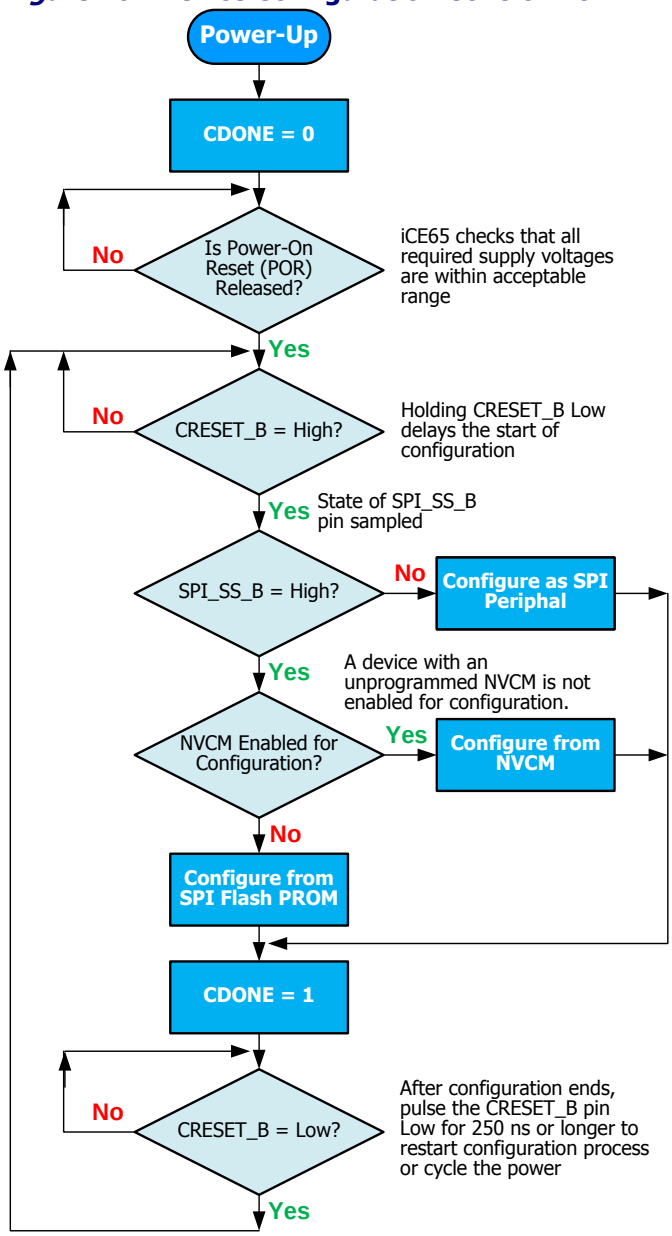
Table 17: RAM4K Block RAM Signals

Signal Name	Direction	Description
WDATA[15:0]	Input	Write Data input.
MASK[15:0]	Input	Masks write operations for individual data bit-lines. 0 = Write bit; 1 = Don't write bit
WADDR[7:0]	Input	Write Address input. Selects one of 256 possible RAM locations.
WE	Input	Write Enable input.
WCLKE	Input	Write Clock Enable input.
WCLK	Input	Write Clock input. Default rising-edge, but with falling-edge option.
RDATA[15:0]	Output	Read Data output.
RADDR[7:0]	Input	Read Address input. Selects one of 256 possible RAM locations.
RE	Input	Read Enable input.
RCLKE	Input	Read Clock Enable input.
RCLK	Input	Read Clock input. Default rising-edge, but with falling-edge option.

Write Operations

Figure 18 shows the logic involved in writing a data bit to a RAM location. Table 18 describes various write operations for a RAM4K block. By default, all RAM4K write operations are synchronized to the rising edge of WCLK although the clock is invertible as shown in Figure 18.

Figure 20: **Device Configuration Control Flow**



Configuration Image Size

Table 23 shows the number of memory bits required to configure an iCE65 device. Two values are provided for each device. The "Logic Only" value indicates the minimum configuration size, the number of bits required to configure only the logic fabric, leaving the RAM4K blocks uninitialized. The "Logic + RAM4K" column indicates the maximum configuration size, the number of bits to configure the logic fabric and to pre-initialize all the RAM4K blocks.

- For lowest possible power consumption after configuration, the PROM should also support the 0xB9 Deep Power Down command and the 0xAB Release from Deep Power-down Command (see Figure 24 and Figure 26). The low-power mode is optional.
- The PROM must be ready to accept commands 10 µs after meeting its power-on conditions. In the PROM data sheet, this may be specified as t_{VSL} or t_{VCSL}. It is possible to use slower PROMs by holding the CRESET_B input Low until the PROM is ready, then releasing CRESET_B, either under program control or using an external power-on reset circuit.

The Lattice iCEman65 development board and associated programming software uses an ST Micro/Numonyx M25Pxx SPI serial Flash PROM.

SPI PROM Size Requirements

Table 27 lists the minimum SPI PROM size required to configure an iCE65 device. Larger PROM sizes are allowed, but not required unless the end application uses the additional space. SPI serial PROM sizes are specified in bits. For each device size, the table shows the required minimum PROM size for "Logic Only" (no BRAM initialization) and "Logic + RAM4K" (RAM4K blocks pre-initialized). Furthermore, the table shows the PROM size for varying numbers of configuration images. Most applications will use a single image. Applications that use the Cold Boot or Warm Boot features may use more than one image.

Table 27: Smallest SPI PROM Size (bits), by Device, by Number of Images

Device	1 Image		2 Images		3 Images		4 Images	
	Logic Only	**Logic + RAM4K**	**Logic Only**	**Logic + RAM4K**	**Logic Only**	**Logic + RAM4K**	**Logic Only**	**Logic + RAM4K**
iCE65L01	256K	256K	512K	512K	1M	1M	1M	1M
iCE65L04	512K	1M	1M	2M	2M	2M	2M	4M
iCE65L08	1M	2M	2M	4M	4M	4M	4M	8M

Enabling SPI Configuration Interface

To enable the SPI configuration mode, the SPI_SS_B pin must be allowed to float High. The SPI_SS_B pin has an internal pull-up resistor. If SPI_SS_B is Low, then the iCE65 component defaults to the SPI Slave configuration mode.

SPI Master Configuration Process

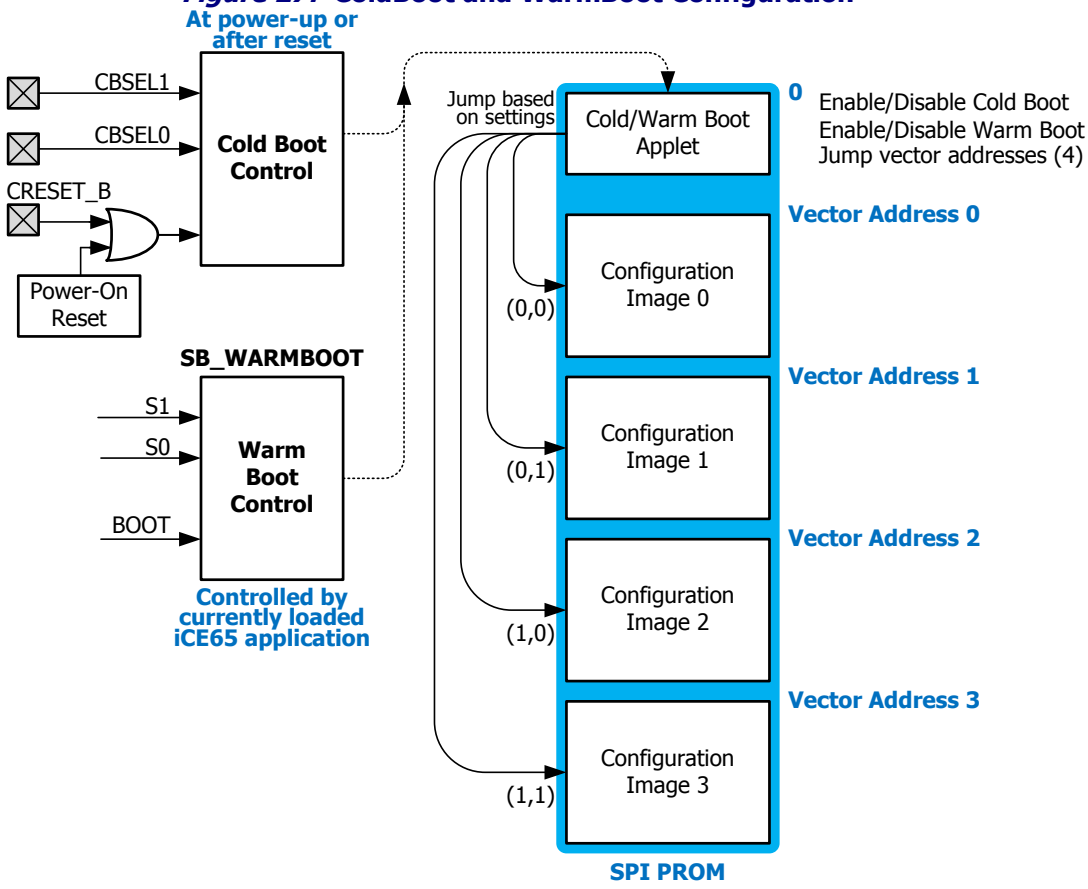
The iCE65 SPI Master Configuration Interface supports a variety of modern, high-density, low-cost SPI serial Flash PROMs. Most modern SPI PROMs include a power-saving Deep Power-down mode. The iCE65 component exploits this mode for additional system power savings.

The iCE65 SPI interface starts by driving SPI_SS_B Low, and then sends a Release from Power-down command to the SPI PROM, hexadecimal command code 0xAB. Figure 24 provides an example waveform. This initial command wakes up the SPI PROM if it is already in Deep Power-down mode. If the PROM is not in Deep Power-down mode, the extra command has no adverse affect other than that it requires a few additional microseconds during the configuration process. The iCE65 device transmits data on the SPI_SO output, on the falling edge of the SPI_SCK output. The SPI PROM does not provide any data to the iCE65 device's SPI_SI input. After sending the last command bit, the iCE65 device de-asserts SPI_SS_B High, completing the command. The iCE65 device then waits a minimum of 10 µS before sending the next SPI PROM command.

Cold Boot Configuration Option

By default, the iCE65 FPGA is programmed with a single configuration image, either from internal NVCM memory, from an external SPI Flash PROM, or externally from a processor or microcontroller.

Figure 27: **ColdBoot and WarmBoot Configuration**



When self loading from NVCM or from an SPI Flash PROM, there is an additional configuration option called Cold Boot mode. When this option is enabled in the configuration bitstream, the iCE65 FPGA boots normally from power-on or a master reset (CRESET_B = Low pulse), but monitors the value on two PIO pins that are borrowed during configuration, as shown in Figure 27. These pins, labeled PIO2/CBSEL0 and PIO2/CBSEL1, tell the FPGA which of the four possible SPI configurations to load into the device. Table 30 provides the pin or ball locations for these pins.

- Load from initial location, either from NVCM or from address 0 in SPI Flash PROM. For Cold Boot or Warm Boot applications, the initial configuration image contains the cold boot/warm boot applet.
- Check if Cold Boot configuration feature is enabled in the bitstream.
  - If not enabled, FPGA configures normally.
  - If Cold Boot is enabled, then the FPGA reads the logic values on pins CBSEL[1:0]. The FPGA uses the value as a vector and then reads from the indicated vector address.
  - At the selected CBSEL[1:0] vector address, there is a starting address for the selected configuration image.
    - For SPI Flash PROMs, the new address is a 24-bit start address in Flash.
    - If the selected bitstream is in NVCM, then the address points to the internal NVCM.
- Using the new start address, the FPGA restarts reading configuration memory from the new location.

Table 39: iCE65 VQ100 Pinout Table

Pin Function	Pin Number	Type	Bank
GBIN0/PIO0	90	GBIN	0
GBIN1/PIO0	89	GBIN	0
PIO0	78	PIO	0
PIO0	79	PIO	0
PIO0	80	PIO	0
PIO0	81	PIO	0
PIO0	82	PIO	0
PIO0	83	PIO	0
PIO0	85	PIO	0
PIO0	86	PIO	0
PIO0	87	PIO	0
PIO0	91	PIO	0
PIO0	93	PIO	0
PIO0	94	PIO	0
PIO0	95	PIO	0
PIO0	96	PIO	0
PIO0	97	PIO	0
PIO0	99	PIO	0
PIO0	100	PIO	0
VCCIO_0	88	VCCIO	0
VCCIO_0	92	VCCIO	0
GBIN2/PIO1	63	GBIN	1
GBIN3/PIO1	62	GBIN	1
PIO1	51	PIO	1
PIO1	52	PIO	1
PIO1	53	PIO	1
PIO1	54	PIO	1
PIO1	56	PIO	1
PIO1	57	PIO	1
PIO1	59	PIO	1
PIO1	60	PIO	1
PIO1	64	PIO	1
PIO1	65	PIO	1
PIO1	66	PIO	1
PIO1	68	PIO	1
PIO1	69	PIO	1
PIO1	71	PIO	1
PIO1	72	PIO	1
PIO1	73	PIO	1
PIO1	74	PIO	1
VCCIO_1	58	VCCIO	1
VCCIO_1	67	VCCIO	1
CDONE	43	CONFIG	2
CRESET_B	44	CONFIG	2
GBIN4/PIO2	iCE65L01: 33 iCE65L04: 34	GBIN	2
GBIN5/PIO2	iCE65L01: 36 iCE65L04: 33	GBIN	2
PIO2	26	PIO	2
PIO2	27	PIO	2

Ball Function	Ball Number	Pin Type	Bank
PIO2	J11	PIO	2
PIO2	K3	PIO	2
PIO2	K4	PIO	2
PIO2	K11	PIO	2
PIO2	L2	PIO	2
PIO2	L3	PIO	2
PIO2	L4	PIO	2
PIO2	L5	PIO	2
PIO2	L10	PIO	2
PIO2	L11	PIO	2
PIO2/CBSEL0	H6	PIO	2
PIO2/CBSEL1	J6	PIO	2
VCCIO_2	K5	VCCIO	2
PIO3	C1	PIO	3
PIO3	B1	PIO	3
PIO3	D1	PIO	3
PIO3	E2	PIO	3
PIO3	C2	PIO	3
PIO3	D2	PIO	3
PIO3	C3	PIO	3
PIO3	C4	PIO	3
PIO3	E4	PIO	3
PIO3	D4	PIO	3
PIO3	F3	PIO	3
PIO3	G3	PIO	3
PIO3	G4	PIO	3
GBIN6/PIO3	F4	GBIN	3
GBIN7/PIO3	D3	GBIN	3
PIO3	E3	PIO	3
PIO3	F2	PIO	3
PIO3	G1	PIO	3
PIO3	H1	PIO	3
PIO3	J1	PIO	3
PIO3	H2	PIO	3
PIO3	H3	PIO	3
PIO3	J3	PIO	3
PIO3	J2	PIO	3
VCCIO_3	A1	VCCIO	3
VCCIO_3	G2	VCCIO	3
PIOS/SPI_SO	J8	SPI	SPI
PIOS/SPI_SI	K8	SPI	SPI
PIOS/SPI_SCK	K9	SPI	SPI
PIOS/SPI_SS_B	J9	SPI	SPI
SPI_VCC	J10	SPI	SPI
GND	B2	GND	GND
GND	B10	GND	GND
GND	E1	GND	GND
GND	F5	GND	GND
GND	F6	GND	GND
GND	G5	GND	GND
GND	G6	GND	GND
GND	G11	GND	GND

Ball Function	Ball Number	Pin Type	Bank
PIO1	F14	PIO	1
PIO1	G10	PIO	1
PIO1	G11	PIO	1
PIO1	G13	PIO	1
PIO1	G14	PIO	1
PIO1	H10	PIO	1
PIO1	H11	PIO	1
PIO1	H12	PIO	1
PIO1	H13	PIO	1
PIO1	J10	PIO	1
PIO1	J11	PIO	1
PIO1	J12	PIO	1
PIO1	J13	PIO	1
PIO1	K11	PIO	1
PIO1	K12	PIO	1
PIO1	K14	PIO	1
PIO1	L13	PIO	1
PIO1	L14	PIO	1
PIO1	M13	PIO	1
TCK	L12	JTAG	1
TDI	M12	JTAG	1
TDO	N14	JTAG	1
TMS	P14	JTAG	1
TRST_B	M14	JTAG	1
VCCIO_1	F9	VCCIO	1
VCCIO_1	H14	VCCIO	1
CDONE	M10	CONFIG	2
CRESET_B	L10	CONFIG	2
GBIN4/PIO2 (◆)	***iCE65L04:*** L7 ***iCE65L08:*** N8	GBIN	2
GBIN5/PIO2 (◆)	***iCE65L04:*** P5 ***iCE65L08:*** M7	GBIN	2
PIO2	K5	PIO	2
PIO2	K6	PIO	2
PIO2	K7	PIO	2
PIO2	K8	PIO	2
PIO2	K9	PIO	2
PIO2	L4	PIO	2
PIO2	L5	PIO	2
PIO2	L6	PIO	2
PIO2	L8	PIO	2
PIO2	M3	PIO	2
PIO2	M4	PIO	2
PIO2	M6	PIO	2
PIO2 (◆)	***iCE65L04:*** M7 ***iCE65L08:*** P5	PIO	2
PIO2	M8	PIO	2
PIO2	M9	PIO	2
PIO2	N3	PIO	2
PIO2	N4	PIO	2
PIO2	N5	PIO	2
PIO2	N6	PIO	2

Pinout Differences between iCE65L04 and iCE65L08 in CB196 Package

Table 43 lists the package balls that are different between the pinouts for iCE65L04 and the iCE65L08 in the CB196 package. The table also describes the functional differences between these pins, which is critical when designing a CB196 footprint that supports both the iCE65L04 and the iCE65L08 devices. In some cases, only the differential inputs are swapped; single-ended I/Os are not affected. A swapped differential pair can be inverted internally for functional equivalence. In other cases, a global buffer input is swapped with another PIO pin in the same bank.

***Table 43:* Pinout Differences between iCE65L04 and iCE65L08 in CB196 Package**

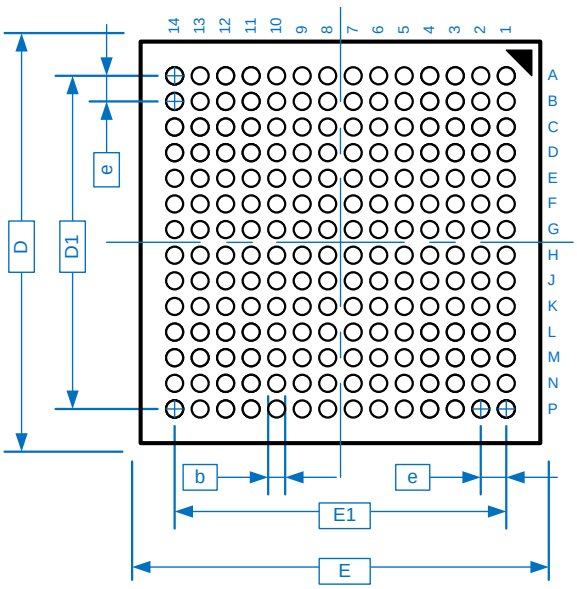
Ball Number	iCE65L04	iCE65L08	Functional Difference
E1	PIO3/DP03A	PIO3/DP03B	Differential inputs swapped, single-ended I/Os not affected
E2	PIO3/DP03B	PIO3/DP03A	
F3	PIO3/DP05A	PIO3/DP05B	Differential inputs swapped, single-ended I/Os not affected
F4	PIO3/DP05B	PIO3/DP05A	
G1	GBIN7/PIO3/DP07B	PIO3/DP11A	Global buffer input GBIN7 and its associated differential input is swapped with another differential pair in I/O Bank 3
G2	PIO3/DP07A	PIO3/DP11B	
H3	PIO3/DP11B	GBIN7/PIO3/DP07B	
H4	PIO3/DP11A	PIO3/DP07A	
K3	PIO3/DP16A	PIO3/DP16B	Differential inputs swapped, single-ended I/Os not affected
K4	PIO3/DP16B	PIO3/DP16A	
L7	GBIN4/PIO2	PIO2	Global buffer input GBIN4 swapped with another PIO pin in I/O Bank 2
N8	PIO2	GBIN4/PIO2	
M7	PIO2	GBIN5/PIO2	Global buffer input GBIN5 swapped with another PIO pin in I/O Bank 2
P5	GBIN5/PIO2	PIO2	

(b) iCE65L08 CB196 Package Mechanical Drawing

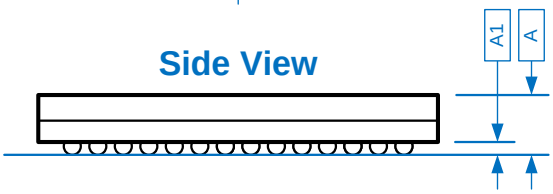
CB196: 8 x8 mm, 196-ball, 0.5 mm ball-pitch, fully-populated, chip-scale ball grid array

Top View

Bottom View



Side View



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			14		Columns
Number of Ball Rows	Y			14		Rows
Number of Signal Balls		n		196		Balls
Body Size	X	E	7.90	8.00	8.10	mm
	Y	D	7.90	8.00	8.10	
Ball Pitch		e	—	0.50	—	
Ball Diameter		b	0.27	—	0.37	
Edge Ball Center to Center	X	E1	—	6.50	—	
	Y	D1	—	6.50	—	
Package Height		A	—	—	1.00	
Stand Off		A1	0.16	—	0.26	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65L08F	Part number
	-T	Power/Speed
3	CB196C	Package type
	ENG	Engineering
4	NXXXXXXX	Lot Number
5	YYWW	Date Code
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
42	34

Ball Function	Ball Number iCE65L04 iCE65L08	Pin Type by Device iCE65L04	iCE65L08	Bank	CB132 Ball Equivalent
PIO1	L15	PIO	PIO	1	G11
PIO1	L16	PIO	PIO	1	G12
PIO1 (●)	L22	N.C.	PIO	1	—
PIO1	M15	PIO	PIO	1	H11
PIO1	M16	PIO	PIO	1	H12
PIO1	M20	PIO	PIO	1	—
PIO1 (●)	M22	N.C.	PIO	1	—
PIO1	N15	PIO	PIO	1	J11
PIO1	N16	PIO	PIO	1	J12
PIO1	N22	PIO	PIO	1	—
PIO1	P15	PIO	PIO	1	K11
PIO1	P16	PIO	PIO	1	K12
PIO1	P18	PIO	PIO	1	K14
PIO1	P20	PIO	PIO	1	—
PIO1	P22	PIO	PIO	1	—
PIO1	R18	PIO	PIO	1	L14
PIO1	R20	PIO	PIO	1	—
PIO1	R22	PIO	PIO	1	—
PIO1	T20	PIO	PIO	1	—
PIO1	T22	PIO	PIO	1	—
PIO1	U20	PIO	PIO	1	—
PIO1 (●)	U22	N.C.	PIO	1	—
PIO1	V20	PIO	PIO	1	—
PIO1 (●)	V22	N.C.	PIO	1	—
PIO1	W20	PIO	PIO	1	—
PIO1 (●)	W22	N.C.	PIO	1	—
PIO1 (●)	Y22	N.C.	PIO	1	—
TCK	R16	JTAG	JTAG	1	L12
TDI	T16	JTAG	JTAG	1	M12
TDO	U18	JTAG	JTAG	1	N14
TMS	V18	JTAG	JTAG	1	P14
TRST_B	T18	JTAG	JTAG	1	M14
VCCIO_1	H22	VCCIO	VCCIO	1	—
VCCIO_1	J20	VCCIO	VCCIO	1	—
VCCIO_1	K13	VCCIO	VCCIO	1	F9
VCCIO_1	M18	VCCIO	VCCIO	1	H14
CDONE	T14	CONFIG	CONFIG	2	M10
CRESET_B	R14	CONFIG	CONFIG	2	L10
GBIN4/PIO2	V12	GBIN	GBIN	2	P7
GBIN5/PIO2	V11	GBIN	GBIN	2	P8
PIO2	R8	PIO	PIO	2	L4
PIO2	R9	PIO	PIO	2	L5
PIO2	R10	PIO	PIO	2	L6
PIO2	R11	PIO	PIO	2	L7
PIO2	R12	PIO	PIO	2	L8
PIO2	T7	PIO	PIO	2	M3
PIO2	T8	PIO	PIO	2	M4
PIO2	T10	PIO	PIO	2	M6
PIO2	T11	PIO	PIO	2	M7
PIO2	T12	PIO	PIO	2	M8

Die Cross Reference

The tables in this section list all the pads on a specific die type and provide a cross reference on how a specific pad connects to a ball or pin in each of the available package offerings. Similarly, the tables provide the pad coordinates for the die-based version of the product (DiePlus). These tables also provide a way to prototype with one package option and then later move to a different package or die.

As described in "Input and Output Register Control per PIO Pair" on page 16, PIO pairs share register control inputs. Similarly, as described in "Differential Inputs and Outputs" on page 12, a PIO pair can form a differential input or output. PIO pairs in I/O Bank 3 are optionally differential inputs or differential outputs. PIO pairs in all other I/O Banks are optionally differential outputs. In the tables, differential pairs are surrounded by a heavy blue box.

iCE65L04

Table 45 lists all the pads on the iCE65L04 die and how these pads connect to the balls or pins in the supported package styles. Most VCC, VCCIO, and GND pads are double-bonded inside the package although the table shows only a single connection.

For additional information on the iCE65L04 DiePlus product, please refer to the following data sheet.

DiePlus Advantage FPGA Known Good Die

Table 45: iCE65L04 Die Cross Reference

iCE65L04	DiePlus						
Pad Name	VQ100	CB132	CB196	CB284	Pad	X (µm)	Y (µm)
PIO3_00/DP00A	1	B1	C1	F5	1	129.40	2,687.75
PIO3_01/DP00B	2	C1	B1	G5	2	231.40	2,642.74
PIO3_02/DP01A	3	C3	D3	G7	3	129.40	2,597.75
PIO3_03/DP01B	4	D3	C3	H7	4	231.40	2,552.74
GND	5	F1	F1	K5	5	129.40	2,507.75
GND	—	—	—	—	6	231.40	2,462.74
VCCIO_3	6	E3	E3	J7	7	129.40	2,417.75
VCCIO_3	—	—	—	—	8	231.40	2,372.74
PIO3_04/DP02A	7	D4	D1	H8	9	129.40	2,327.75
PIO3_05/DP02B	8	E4	D2	J8	10	231.40	2,292.74
PIO3_06/DP03A	—	D1	E1	H5	11	129.40	2,257.75
PIO3_07/DP03B	—	E1	E2	J5	12	231.40	2,222.74
VCC	—	—	H9	D3	13	129.40	2,187.75
PIO3_08/DP04A	9	F4	D4	K8	14	231.40	2,152.74
PIO3_09/DP04B	10	F3	E4	K7	15	129.40	2,117.75
PIO3_10/DP05A	—	—	F3	E3	16	231.40	2,082.74
PIO3_11/DP05B	—	—	F4	F3	17	129.40	2,047.75
GND	—	H6	A9	M10	18	231.40	2,012.74
PIO3_12/DP06A	—	—	F5	G3	19	129.40	1,977.75
PIO3_13/DP06B	—	—	E5	H3	20	231.40	1,942.74
GND	—	—	A9	J3	21	129.40	1,907.75
GND	—	—	—	—	22	231.40	1,872.74
PIO3_14/DP07A	—	—	—	H1	23	129.40	1,837.75
PIO3_15/DP07B	—	—	—	J1	24	231.40	1,802.74
VCCIO_3	—	—	K1	K3	25	129.40	1,767.75
VCC	11	G6	G6	L10	26	231.40	1,732.74
PIO3_16/DP08A	—	—	—	K1	27	129.40	1,697.75
PIO3_17/DP08B	—	—	—	L1	28	231.40	1,662.74

Electrical Characteristics

All parameter limits are specified under worst-case supply voltage, temperature, and processing conditions.

Absolute Maximum Ratings

Stresses beyond those listed under Table 47 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 47: Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
VCC	Core supply Voltage	–0.5	1.42	V
VPP_2V5	VPP_2V5 NVCM programming and operating supply			V
VPP_FAST	Optional fast NVCM programming supply			V
VCCIO_0 **VCCIO_1** **VCCIO_2** **SPI_VCC**	I/O bank supply voltage (I/O Banks 0, 1, and 2 plus SPI interface)	–0.5	4.00	V
VCCIO_3	I/O Bank 3 supply voltage	–0.5	iCE65L01: 4.00 iCE65L04/08: 3.6	V
VIN_0 **VIN_1** **VIN_2** **VIN_SPI**	Voltage applied to PIO pin within a specific I/O bank (I/O Banks 0, 1, and 2 plus SPI interface)	–1.0	5.5	V
VIN_3 **VIN_VREF**	Voltage applied to PIO pin within I/O Bank 3	–0.5	iCE65L01: 4.00 iCE65L04/08: 3.6	V
IOUT	DC output current per pin	—	20	mA
T_J	Junction temperature	–55	125	°C
T_{STG}	Storage temperature, no bias	–65	150	°C

Recommended Operating Conditions

Table 48: **Recommended Operating Conditions**

Symbol	Description		Minimum	Nominal	Maximum	Units
VCC	Core supply voltage	–L: Ultra-Low Power mode	0.95	1.00	1.05	V
		–L: Low Power –T: High Performance	1.14	1.20	1.26	V
VPP_2V5	VPP_2V5 NVCM programming and operating supply	Release from Power-on Reset	1.30	—	3.47	V
		Configure from NVCM	2.30	—	3.47	V
		NVCM programming	2.30	—	3.00	V
VPP_FAST	Optional fast NVCM programming supply		Leave unconnected in application			
SPI_VCC	SPI interface supply voltage		1.71	—	3.47	V
VCCIO_0 VCCIO_1 VCCIO_2 VCCIO_3 SPI_VCC	I/O standards, all banks*	**LVCMOS33**	3.14	3.30	3.47	V
		Non-standard voltage: in between 2.5V and 3.3V use LVCMOS25 in iCEcube2	Nominal -5%	2.5< Nominal <3.3	Nominal +5%	V
		LVCMOS25, LVDS	2.38	2.50	2.63	V
		LVCMOS18, SubLVDS	1.71	1.80	1.89	V
		LVCMOS15	1.43	1.50	1.58	V
VCCIO_3	I/O standards only available in iCE65L04/08 I/O Bank 3*	**SSTL2**	2.38	2.50	2.63	V
		SSTL18	1.71	1.80	1.89	V
		MDDR	1.71	1.80	1.89	V
T_A	Ambient temperature	Commercial (C)	0	—	70	°C
		Industrial (I)	–40	—	85	°C
T_{PROG}	NVCM programming temperature		10	25	30	°C

NOTE:

VPP_FAST is only used for fast production programming. Leave floating or unconnected in application. When the iCE65 device is active, VPP_2V5 must be connected to a valid voltage.

		minimum temperature to –40°C in Figure 2 and Table 48. Added NVCM programming temperature to Table 48.
1.3	17-DEC-2008	Added footprint and pinout information for the CS110 Wafer-Level Chip-Scale Ball Grid Array. Clarified that the CB196 footprint shown is for the iCE65L04; the iCE65L08 footprint for the CB196 package is similar but different. Added updated information on Differential Inputs and Outputs, including support for SubLVDS. Updated Electrical Characteristics and AC Timing Guidelines sections. Added support for the LVCMOS15 I/O standard. Corrected the diagram showing the direct differential clock input, Figure 16. Updated the number of I/Os by package in Table 34. Updated company address. Other minor updates throughout.
1.2	11-OCT-2008	Updated I/O Bank 3 characteristics in Table 7 and Table 51. Corrected label in Figure 14. Added JTAG configuration to Table 20. Added pull-up resistor information in Table 22 and Figure 21. Added "Internal Device Reset" section. Updated internal oscillator performance in and Table 57. Updated configuration timing in Table 58 based on new oscillator timing. Completely reorganized the "Package and Pinout Information" section. Added information on CS63 and CB196 packages. Updated information on VPP_2V5 signal in Table 36. Reduced package height for CB132 and CB284 packages to 1.0 mm. Added "Differential Inputs" and "Differential Outputs" sections.
1.1	4-SEPT-2008	Updated package roadmap (Table 2) and updated ordering codes (Figure 2). Updated Figure 7. Updated Figure 24. Added CS63 package footprint (Figure 36), pinout (Table 39) and Package.
1.0	31-MAY-2008	Initial public release.