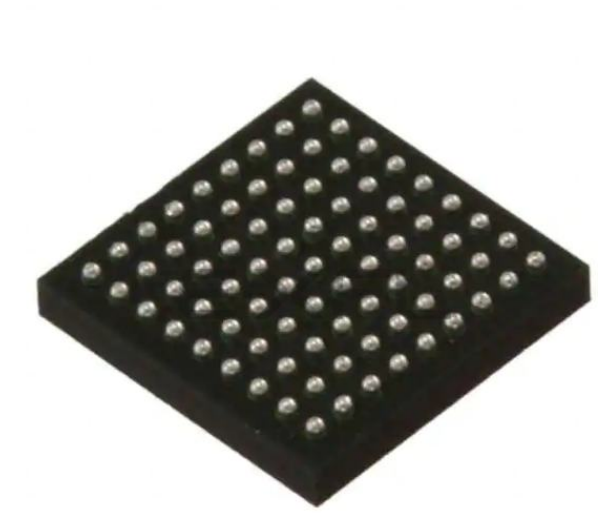

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

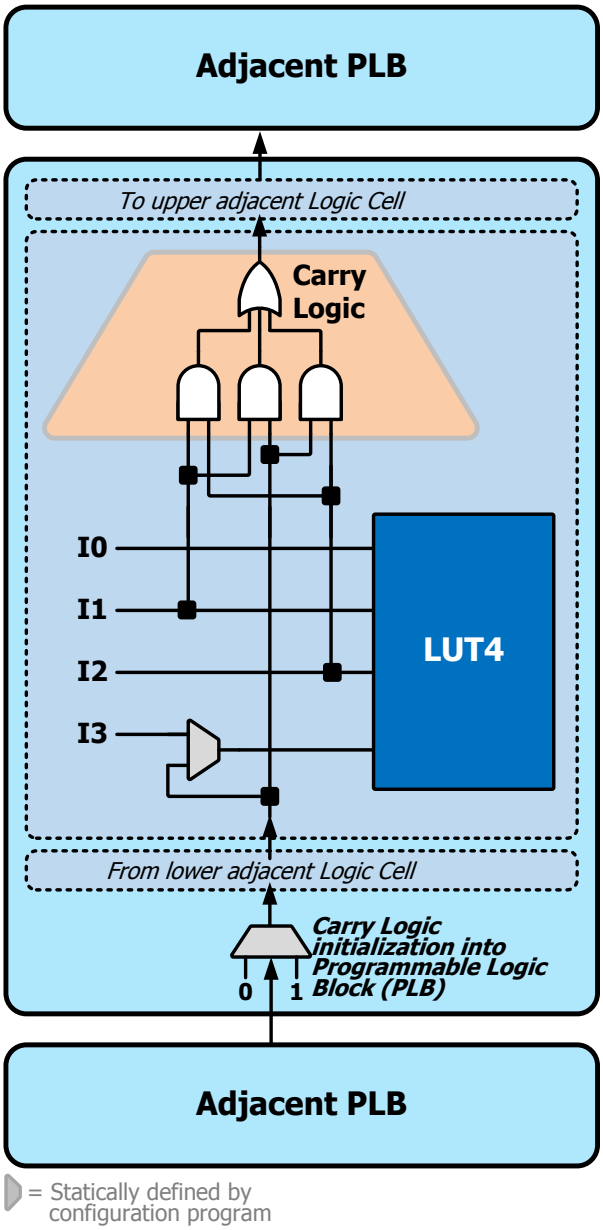
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	160
Number of Logic Elements/Cells	1280
Total RAM Bits	65536
Number of I/O	63
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	81-VFBGA, CSPBGA
Supplier Device Package	81-CSBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice65l01f-lcb81i

The Carry Logic generates the carry value to feed the next bit in the adder. The calculated carry value replaces the I3 input to the next LUT4 in the upper Logic Cell.

If required by the application, the carry output from the final stage of the adder is available by passing it through the final LUT4.

Figure 5: **Carry Logic Structure within a Logic Cell and between PLBs**



For best possible performance, the global buffer inputs (GBIN[7:0]) connect directly to the their associated global buffers (GBUF[7:0]), bypassing the PIO logic and iCEgate circuitry as shown in Figure 7. Consequently, the direct GBIN-to-GBUF connection cannot be blocked by the iCEgate circuitry. However, it is possible to use iCEgate to block PIO-to-GBUF clock connections.

For additional information on using the iCEgate feature, please refer to the following application note.

AN002: Using iCEgate Blocking for Ultra-Low Power

Input Pull-Up Resistors on I/O Banks 0, 1, and 2

The PIO pins in I/O Banks 0, 1, and 2 have an optional input pull-up resistor. Pull-up resistors are not provided in iCE65L04 and iCE65L08 I/O Bank 3. During the iCE65 configuration process, the input pull-up resistor is unconditionally enabled and pulls the input to within a diode drop of the associated I/O bank supply voltage (VCCIO_#). This prevents any signals from floating on the circuit board during configuration.

After iCE65 configuration is complete, the input pull-up resistor is optional, defined by a configuration bit. The pull-up resistor is also useful to tie off unused PIO pins. The Lattice iCEcube development software defines all unused PIO pins in I/O Banks 0, 1 and 2 as inputs with the pull-up resistor turned on. The pull-up resistor value depends on the VCCIO voltage applied to the bank, as shown in Table 49.

Note: JTAG inputs TCK, TDI and TMS do not have the input pull-up resistor and must be tied off to GND when unused, else VCCIO_1 draws current.

No Input Pull-up Resistors on I/O Bank 3 of iCE65L04 and iCE65L08

The PIO pins in I/O Bank 3 do not have an internal pull-up resistor. To minimize power consumption, tie unused PIO pins in Bank 3 to a known logic level or drive them as a disabled high-impedance output.

Input Hysteresis

Inputs typically have about 50 mV of hysteresis, as indicated in Table 49.

Output and Output Enable Signal Path

As shown in Figure 7, a signal from programmable interconnect feeds the OUT signal on a Programmable I/O pad. This output connects either directly to the associated package pin or is held in an optional output flip-flop. Because all flip-flops are automatically reset after configuration, the output from the output flip-flop can be optionally inverted so that an active-Low output signal is held in the disabled (High) state immediately after configuration.

Similarly, each Programmable I/O pin has an output enable or three-state control called OE. When OE = High, the OUT output signal drives the associated pad, as described in Table 10. When OE = Low, the output driver is in the high-impedance (Hi-Z) state. The OE output enable control signal itself connects either directly to the output buffer or is held in an optional register. The output buffer is optionally permanently enabled or permanently disabled, either to unconditionally drive output signals, or to allow input-only signals.

Table 10: **PIO Output Operations (non-registered operation, no inversions)**

Operation	OUT Data Output	OE Enable	PAD
Three-State	X	0	Hi-Z
Drive Output Data	OUT	1*	OUT

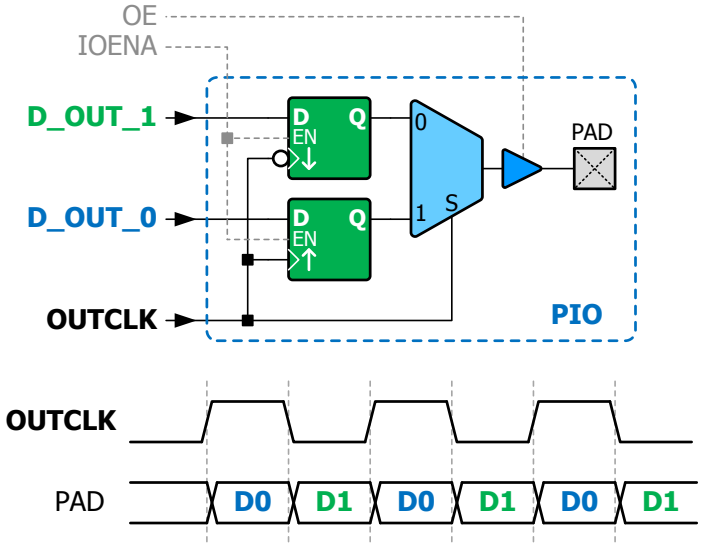
X = don't care, 1* = High or unused, Hi-Z = high-impedance, three-stated, floating.

See Input and Output Register Control per PIO Pair for information about the registered input path.

Double Data Rate (DDR) Flip-Flops

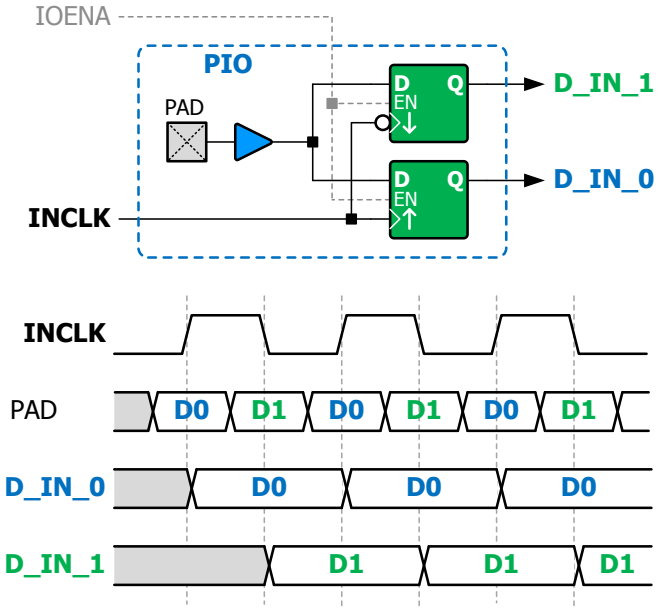
Each individual PIO pin optionally has two sets of double data rate (DDR) flip-flops; one input pair and one output pair. Figure 12 demonstrates the functionality of the output DDR flip-flop. Two signals from within the iCE65 device drive the DDR output flip-flop. The D_OUT_0 signal is clocked by the rising edge of the OUTCLK signal while the D_OUT_1 signal is clocked by the falling edge of the OUTCLK signal, assuming no optional clock polarity inversion. Internally, the two individual flip-flops are multiplexed together before the data appears at the pad, effectively doubling the output data rate.

Figure 12: DDR Output Flip-Flop



Similarly, Figure 13 demonstrates the DDR input flip-flop functionality. A double data rate (DDR) signal arrives at the pad. Internally, one value is clocked by the rising edge of the INCLK signal and another value is clocked by the falling edge of the INCLK signal. The DDR data stream is effectively de-multiplexed within the PIO pin and presented to the programmable interconnect on D_IN_0 and D_IN_1.

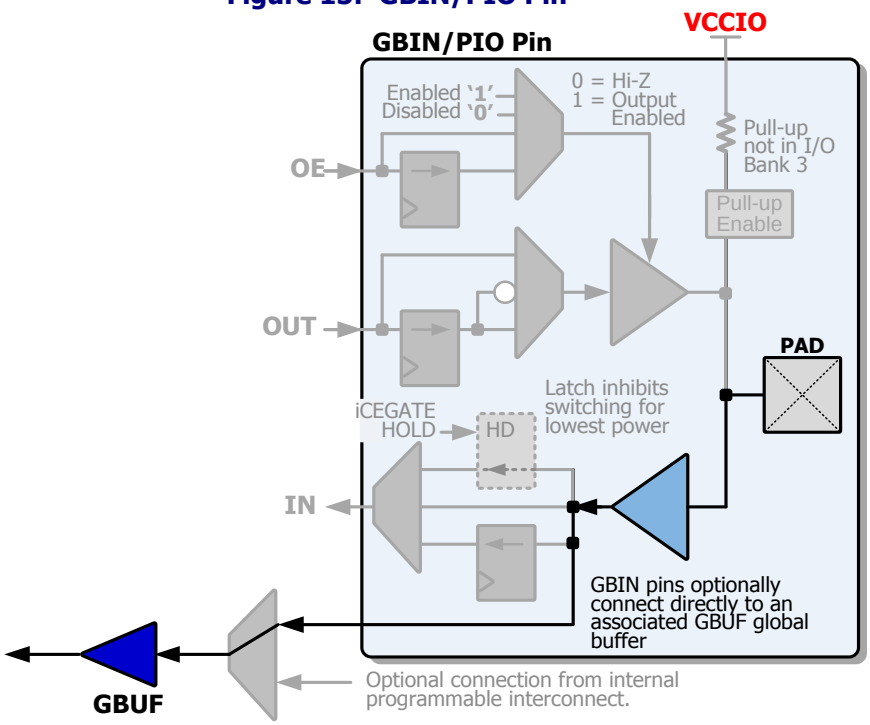
Figure 13: DDR Input Flip-Flop



The DDR flip-flops provide several design advantages. Internally within the iCE65 device, the clock frequency is half the effective external data rate. The lower clock frequency eases internal timing, doubling the clock period, and slashes the clock-related power in half.

Note the clock differences between the iCE65L04 and iCE65L08 in the CB196 package.

Figure 15: GBIN/PIO Pin



Differential Global Buffer Input

All eight global buffer inputs support single-ended I/O standards such as LVCMOS. Global buffer GBUF7 in I/O Bank 3 also provides an optional direct SubLVDS, LVDS, or LVPECL differential clock input, as shown in Figure 16. The GBIN7 and its associated differential I/O pad accept a differential clock signal. A 100 Ω termination resistor is required across the two pads. Optionally, swap the outputs from the LVDS or LVPECL clock driver to invert the clock as it enters the iCE65 device.

Figure 16: LVDS or LVPECL Clock Input

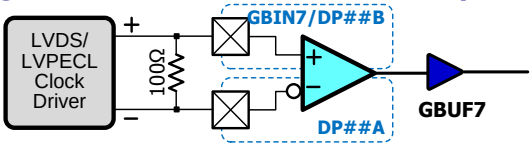


Table 15 lists the pin or ball numbers for the differential global buffer input by package style. Although this differential input is the only one that connects directly to a global buffer, other differential inputs can connect to a global buffer using general-purpose interconnect, with slightly more signal delay.

***Table 15:* Differential Global Buffer Input Ball/Pin Number by Package**

Differential Global Buffer Input (GBIN)	I/O Bank	VQ100	CB132	'L04 CB196	'L08 CB196	CB284
GBIN7/DPxxB	3	13	N/A	G1	H3	L5
DPxxA		12	N/A	G2	H4	L3

The differential global buffer input is not available for iCE65 devices in the CB132 package. This restriction is an artifact of the pin compatibility between the CB132 and CB284 package.

Note the clock differences between the iCE65L04 and iCE65L08 in the CB196 package.

Figure 19: RAM4K Read Logic

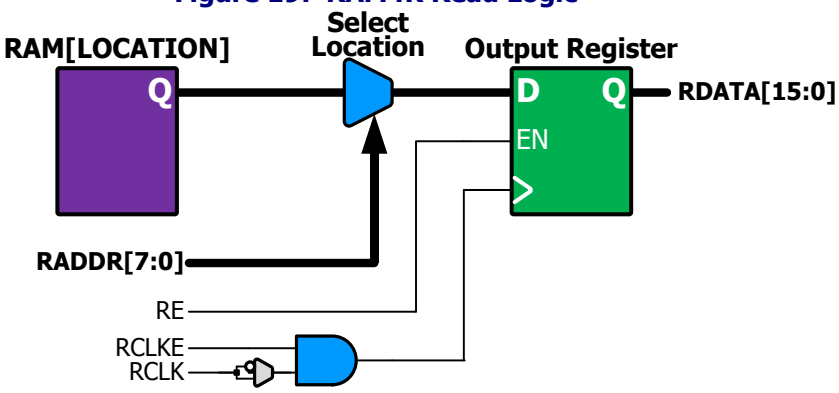


Table 19: RAM4K Read Operations

Operation	RADDR[7:0] Address	RE Read Enable	RCLKE Clock Enabe	RCLK Clock	RDATA[15:0]
After configuration, before first valid Read Data operation	X	X	X	X	Undefined
Disabled	X	X	X	0	No Change
Disabled		X	0	X	No Change
Disabled	X	0	X	X	No change
Read Data	RADDR	1	1	↑	RAM[RADDR]

To read data from the RAM4K block, perform the following operations.

- Supply a valid address on the RADDR[7:0] address input port
- Enable the RAM4K read port (RE = 1)
- Enable the RAM4K read clock (RCLKE = 1)
- Apply a rising clock edge on RCLK
- After the clock edge, the RAM contents located at the specified address (RADDR) appear on the RDATA output port

Read Data Register Undefined Immediately after Configuration

Unlike the flip-flops in the Programmable Logic Blocks and Programmable I/O pins, the RDATA[15:0] read data output register is not automatically reset after configuration. Consequently, immediately following configuration and before the first valid Read Data operation, the initial RDATA[15:0] read value is undefined.

Pre-loading RAM Data

The data contents for a RAM4K block can be optionally pre-loaded during iCE65 configuration. If not pre-loaded during configuration, then the RAM contents must be initialized by the iCE65 application before the RAM contents are valid.

Pre-loading the RAM data in the configuration bitstream increases the size of the configuration image accordingly.

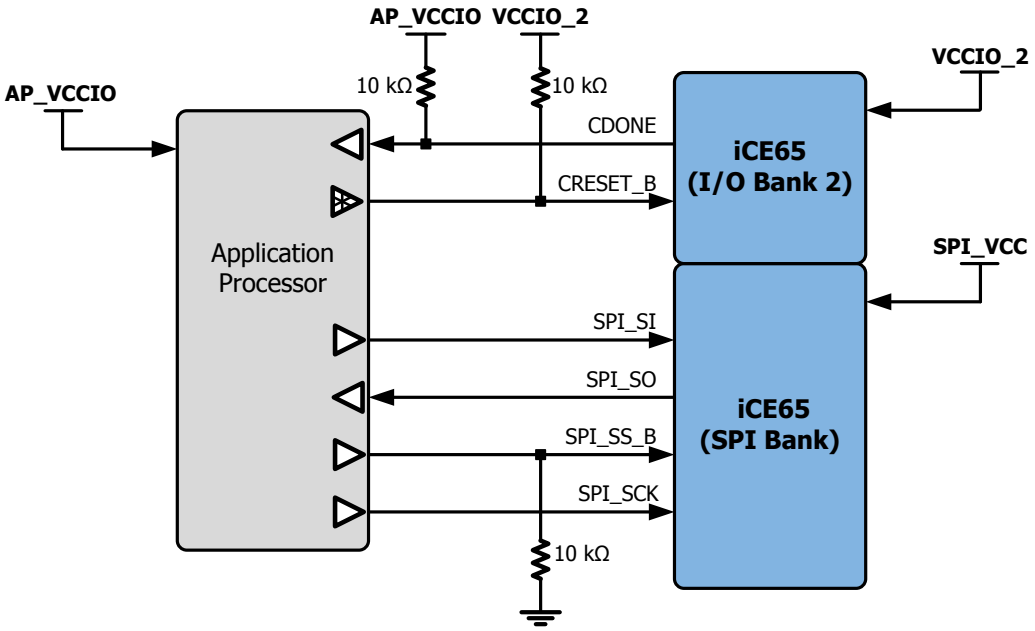
RAM Contents Preserved during Configuration

RAM contents are preserved (write protected) during configuration, assuming that voltage supplies are maintained throughout. Consequently, data can be passed between multiple iCE65 configurations by leaving it in a RAM4K block and then skipping pre-loading during the subsequent reconfiguration. See "Cold Boot Configuration Option" and "Warm Boot Configuration Option" for more information.

Low-Power Setting

To place a RAM4K block in its lowest power mode, keep WCLKE = 0 and RCLKE = 0. In other words, when not actively using a RAM4K block, disable the clock inputs.

Figure 28: **iCE65 SPI Peripheral Configuration Interface**



The SPI control signals are defined in Table 25.

Table 29: **SPI Peripheral Configuration Interface Pins (SPI_SS_B Low when CRESET_B Released)**

Signal Name	Direction	iCE65 I/O Supply	Description
CDONE	AP ← iCE65	VCCIO_2	Configuration Done output from iCE65. Connect to a 10kΩ pull-up resistor to the application processor I/O voltage, AP_VCC.
CRESET_B	AP → iCE65		Configuration Reset input on iCE65. Typically driven by AP using an open-drain driver, which also requires a 10kΩ pull-up resistor to VCCIO_2.
SPI_VCC	Supply	SPI_VCC	SPI Flash PROM voltage supply input.
SPI_SI	AP → iCE65		SPI Serial Input to the iCE65 FPGA, driven by the application processor.
SPI_SO	AP ← iCE65		SPI Serial Output from CE65 device to the application processor. Not actually used during SPI peripheral mode configuration but required if the SPI interface is also used to program the NVCM.
SPI_SS_B	AP → iCE65		SPI Slave Select output from the application processor. Active Low. Optionally hold Low prior to configuration using a 10kΩ pull-down resistor to ground.
SPI_SCK	AP → iCE65		SPI Slave Clock output from the application processor.

After configuration, the SPI port pins are available to the user-application as additional PIO pins, supplied by the SPI_VCC input voltage, essentially providing a fifth "mini" I/O bank.

Enabling SPI Configuration Interface

The optional 10 kΩ pull-down resistor on the SPI_SS_B signal ensures that the iCE65 FPGA powers up in the SPI peripheral mode. Optionally, the application processor drives the SPI_SS_B pin Low when CRESET_B is released, forcing the iCE65 FPGA into SPI peripheral mode.

SPI Peripheral Configuration Process

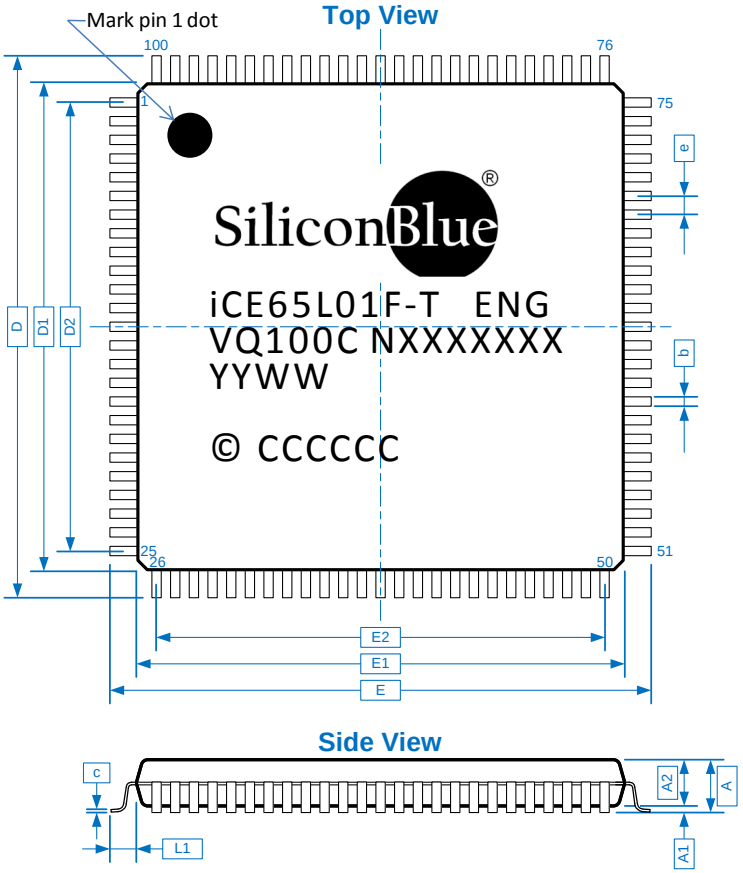
Figure 29 illustrates the interface timing for the SPI peripheral mode and Figure 30 outlines the resulting configuration process. The actual timing specifications appear in Table 60. The application processor (AP) begins by driving the iCE65 CRESET_B pin Low, resetting the iCE65 FPGA. Similarly, the AP holds the iCE65's SPI_SS_B pin Low. The AP must hold the CRESET_B pin Low for at least 200 ns. Ultimately, the AP either releases the CRESET_B pin and allows it to float High via the 10 kΩ pull-up resistor to VCCIO_2 or drives CRESET_B High. The iCE65 FPGA enters SPI peripheral mode when the CRESET_B pin returns High while the SPI_SS_B pin is Low.

Pin Function	Pin Number	Type	Bank
PIO2	28	PIO	2
PIO2	29	PIO	2
PIO2	30	PIO	2
PIO2	iCE65L01: 34 iCE65L04: 36	PIO	2
PIO2	37	PIO	2
PIO2	40	PIO	2
PIO2/CBSEL0	41	PIO	2
PIO2/CBSEL1	42	PIO	2
VCCIO_2	31	VCCIO	2
VCCIO_2	38	VCCIO	2
PIO3/DP00A	1	PIO/DPIO	3
PIO3/DP00B	2	PIO/DPIO	3
PIO3/DP01A	3	PIO/DPIO	3
PIO3/DP01B	4	PIO/DPIO	3
PIO3/DP02A	7	PIO/DPIO	3
PIO3/DP02B	8	PIO/DPIO	3
PIO3/DP03A	9	PIO/DPIO	3
PIO3/DP03B	10	PIO/DPIO	3
PIO3/DP04A	12	PIO/DPIO	3
GBIN7/PIO3/DP04B	13	GBIN/DPIO	3
GBIN6/PIO3/DP05A	15	GBIN/DPIO	3
PIO3/DP05B	16	PIO/DPIO	3
PIO3/DP06A	18	PIO/DPIO	3
PIO3/DP06B	19	PIO/DPIO	3
PIO3/DP07A	20	PIO/DPIO	3
PIO3/DP07B	21	PIO/DPIO	3
PIO3/DP08A	24	PIO/DPIO	3
PIO3/DP08B	25	PIO/DPIO	3
VCCIO_3	6	VCCIO	3
VCCIO_3	14	VCCIO	3
VCCIO_3	22	VCCIO	3
PIOS/SPI_SO	45	SPI	SPI
PIOS/SPI_SI	46	SPI	SPI
PIOS/SPI_SCK	48	SPI	SPI
PIOS/SPI_SS_B	49	SPI	SPI
SPI_VCC	50	SPI	SPI
GND	5	GND	GND
GND	17	GND	GND
GND	23	GND	GND
GND	32	GND	GND
GND	39	GND	GND
GND	47	GND	GND
GND	55	GND	GND
GND	70	GND	GND
GND	84	GND	GND
GND	98	GND	GND
VCC	11	VCC	VCC
VCC	35	VCC	VCC

Pin Function	Pin Number	Type	Bank
VCC	61	VCC	VCC
VCC	77	VCC	VCC
VPP_2V5	75	VPP	VPP
VPP_FAST	76	VPP	VPP

Package Mechanical Drawing

Figure 37: VQ100 Package Mechanical Drawing: Standard Device Marking



Description		Symbol	Min.	Nominal	Max.	Units
Leads per Edge	X			25		Leads
	Y			25		
Number of Signal Leads		n		100		
Maximum Size (lead tip to lead tip)	X	E	—	16.0	—	mm
	Y	D	—	16.0	—	
Body Size	X	E1	—	14.0	—	
	Y	D1	—	14.0	—	
Edge Pin Center to Center	X	E2	—	12.0	—	
	Y	D2	—	12.0	—	
Lead Pitch		e	—	0.50	—	
Lead Width		b	0.17	0.20	0.27	
Total Package Height		A	—	1.20	—	
Stand Off		A1	0.05	—	0.15	
Body Thickness		A2	0.95	1.00	1.05	
Lead Length		L1	—	1.00	—	
Lead Thickness		c	0.09	—	0.20	
Coplanarity			—	0.08	—	

Top Marking Format

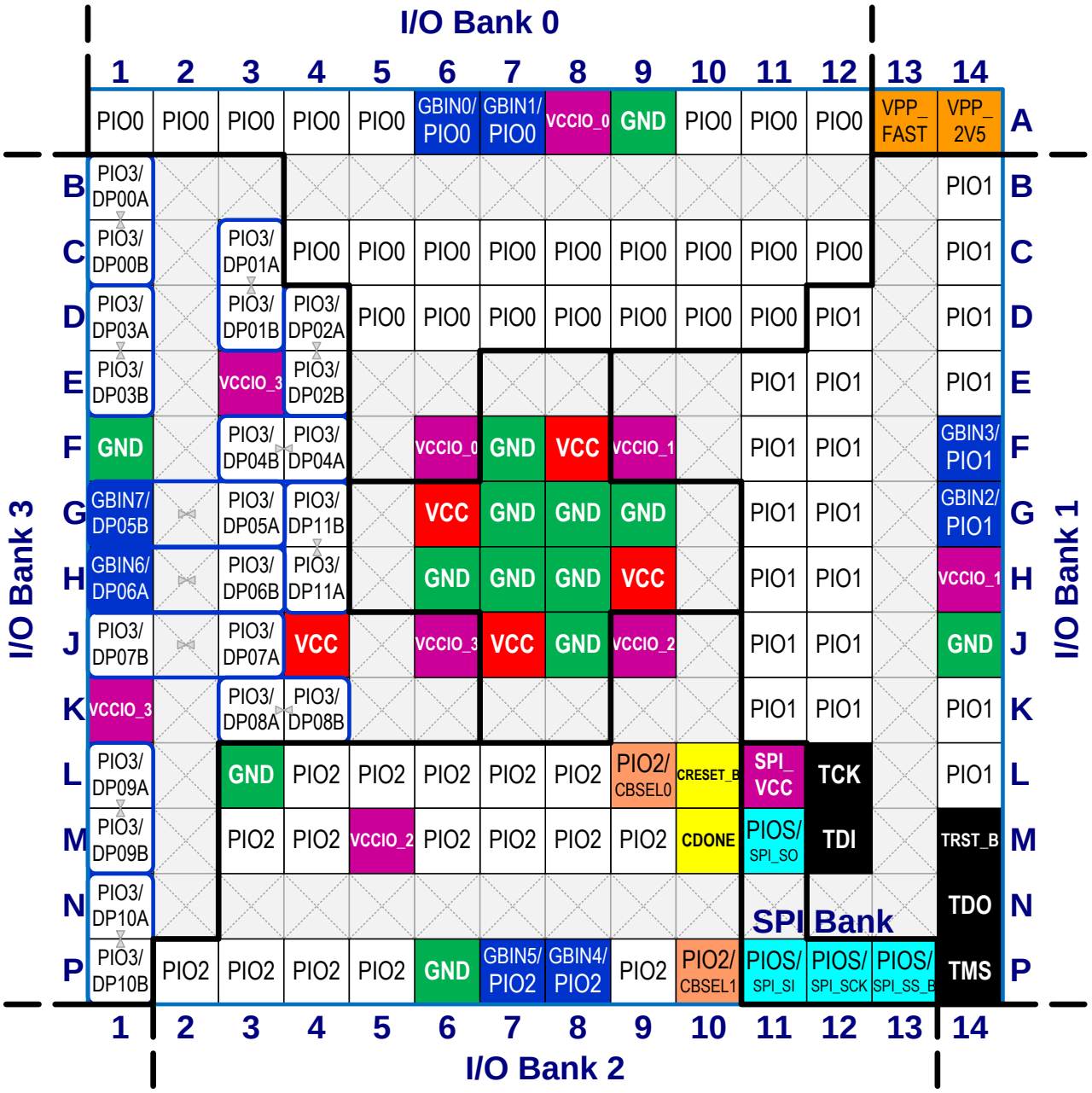
Line	Content	Description
1	Logo	Logo
2	iCE65L01F	Part number
	-T	Power/Speed
	ENG	Engineering
3	VQ100C NXXXXXXX	Package type and Lot number
4	YYWW	Date Code
5	N/A	Blank
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θJA (°C/W)	
0 LFM	200 LFM
38	32

Ball Function	Ball Number	Pin Type	Bank
GND	K2	GND	GND
GND	K10	GND	GND
VCC	B6	VCC	VCC
VCC	F1	VCC	VCC
VCC	F11	VCC	VCC
VCC	K6	VCC	VCC
VPP_2V5	C10	VPP	VPP
VPP_FAST	A9	VPP	VPP

Figure 43: **iCE65L08 CB132 Chip-Scale BGA Footprint (Top View)**



Ball Function	Ball Number	Pin Type	Bank
L01/L04: GBIN7/PIO3 L08: GBIN7/DP05B	G1	GBIN	3
L01/L04: PIO3/DP05A L08: PIO3/DP05A	G3	DPIO	3
L01/L04: PIO3/DP05B L08: PIO3/DP11B	G4	DPIO	3
L01/L04: PIO3/DP06A L08: PIO3/DP06B	H3	DPIO	3
L01/L04: PIO3/DP06B L08: PIO3/DP11A	H4	DPIO	3
PIO3/DP07A	J3	DPIO	3
PIO3/DP07B	J1	DPIO	3
PIO3/DP08A	K3	DPIO	3
PIO3/DP08B	K4	DPIO	3
PIO3/DP09A	L1	DPIO	3
PIO3/DP09B	M1	DPIO	3
PIO3/DP10A	N1	DPIO	3
PIO3/DP10B	P1	DPIO	3
VCCIO_3	E3	VCCIO	3
VCCIO_3	J6	VCCIO	3
VCCIO_3	K1	VCCIO	3
PIOS/SPI_SO	M11	SPI	SPI
PIOS/SPI_SI	P11	SPI	SPI
PIOS/SPI_SCK	P12	SPI	SPI
PIOS/SPI_SS_B	P13	SPI	SPI
SPI_VCC	L11	SPI	SPI
GND	A9	GND	GND
GND	F1	GND	GND
GND	F7	GND	GND
GND	G7	GND	GND
GND	G8	GND	GND
GND	G9	GND	GND
GND	H6	GND	GND
GND	H7	GND	GND
GND	H8	GND	GND
GND	J8	GND	GND
GND	J14	GND	GND
GND	L3	GND	GND
GND	P6	GND	GND
VCC	F8	VCC	VCC
VCC	G6	VCC	VCC
VCC	H9	VCC	VCC
VCC	J4	VCC	VCC
VCC	J7	VCC	VCC
VPP_2V5	A14	VPP	VPP
VPP_FAST	A13	VPP	VPP

CB284 Chip-Scale Ball-Grid Array

The CB284 package, partially-populated 0.5 mm pitch, ball grid array simplifies PCB layout with empty ball rings.

Footprint Diagram

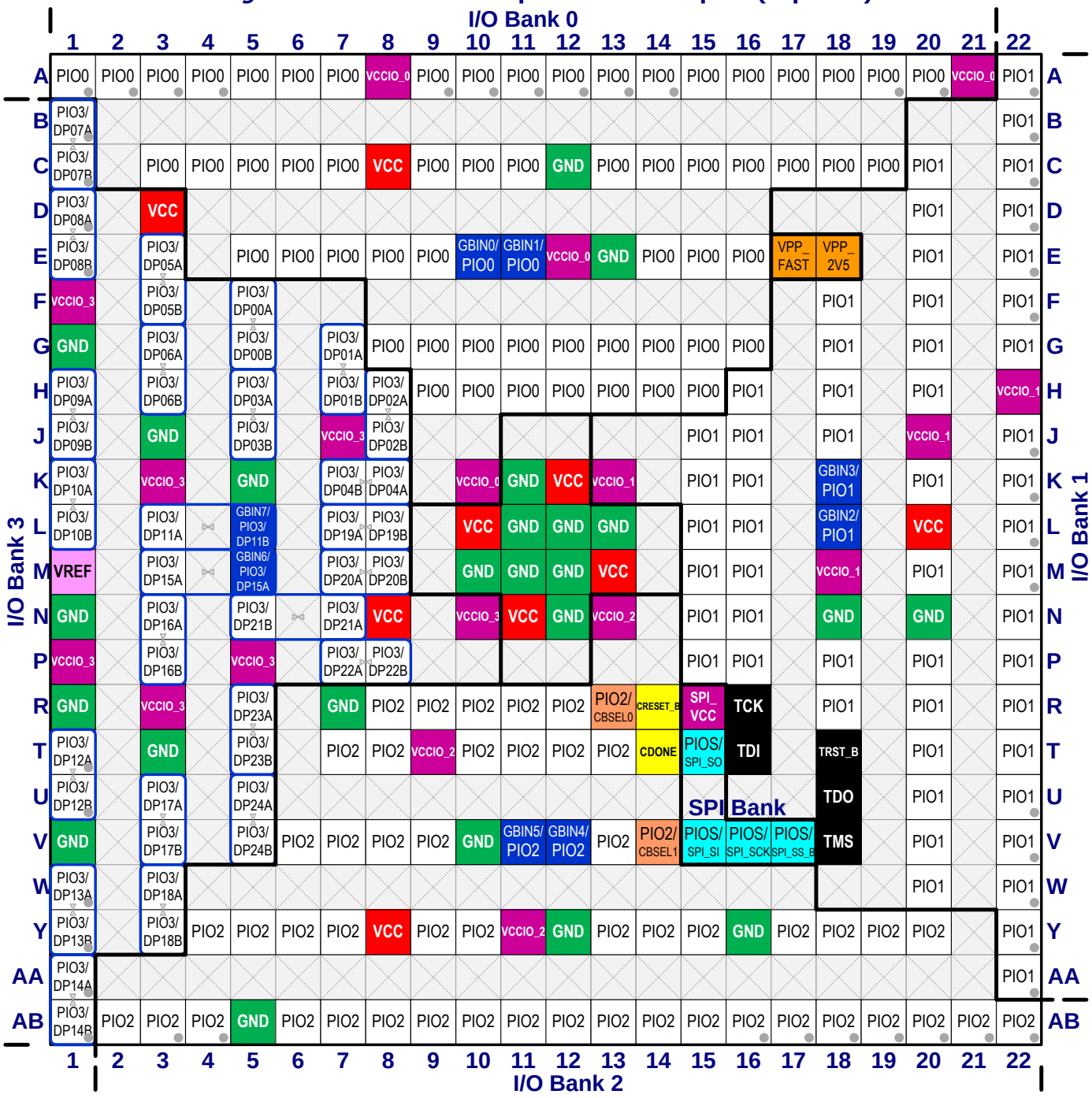
Figure 48 shows the CB284 chip-scale BGA footprint. The 8 x 8 mm CB132 package fits within the same ball pattern as the 12 x 12 mm CB284 package. In other words, the central 8 x 8 section of the CB284 footprint matches the CB132 footprint.

Figure 31 shows the conventions used in the diagram.

Also see Table 44 for a complete, detailed pinout for the 132-ball and 284-ball chip-scale BGA packages.

The signal pins are also grouped into the four I/O Banks and the SPI interface.

Figure 48: **iCE65 CB284 Chip-Scale BGA Footprint (Top View)**



Ball Function	Ball Number iCE65L04 iCE65L08	Pin Type by Device iCE65L04	Pin Type by Device iCE65L08	Bank	CB132 Ball Equivalent
PIO0	E15	PIO	PIO	0	A11
PIO0	E16	PIO	PIO	0	A12
PIO0	G8	PIO	PIO	0	C4
PIO0	G9	PIO	PIO	0	C5
PIO0	G10	PIO	PIO	0	C6
PIO0	G11	PIO	PIO	0	C7
PIO0	G12	PIO	PIO	0	C8
PIO0	G13	PIO	PIO	0	C9
PIO0	G14	PIO	PIO	0	C10
PIO0	G15	PIO	PIO	0	C11
PIO0	G16	PIO	PIO	0	C12
PIO0	H9	PIO	PIO	0	D5
PIO0	H10	PIO	PIO	0	D6
PIO0	H11	PIO	PIO	0	D7
PIO0	H12	PIO	PIO	0	D8
PIO0	H13	PIO	PIO	0	D9
PIO0	H14	PIO	PIO	0	D10
PIO0	H15	PIO	PIO	0	D11
VCCIO_0	A8	VCCIO	VCCIO	0	—
VCCIO_0	A21	VCCIO	VCCIO	0	—
VCCIO_0	E12	VCCIO	VCCIO	0	A8
VCCIO_0	K10	VCCIO	VCCIO	0	F6
GBIN2/PIO1	L18	GBIN	GBIN	1	G14
GBIN3/PIO1	K18	GBIN	GBIN	1	F14
PIO1 (●)	A22	N.C.	PIO	1	—
PIO1 (●)	AA22	N.C.	PIO	1	—
PIO1 (●)	B22	N.C.	PIO	1	—
PIO1	C20	PIO	PIO	1	—
PIO1 (●)	C22	N.C.	PIO	1	—
PIO1	D20	PIO	PIO	1	—
PIO1 (●)	D22	N.C.	PIO	1	—
PIO1	E20	PIO	PIO	1	—
PIO1 (●)	E22	N.C.	PIO	1	—
PIO1	F18	PIO	PIO	1	B14
PIO1	F20	PIO	PIO	1	—
PIO1 (●)	F22	N.C.	PIO	1	—
PIO1	G18	PIO	PIO	1	C14
PIO1	G20	PIO	PIO	1	—
PIO1	G22	PIO	PIO	1	—
PIO1	H16	PIO	PIO	1	D12
PIO1	H18	PIO	PIO	1	D14
PIO1	H20	PIO	PIO	1	—
PIO1	J15	PIO	PIO	1	E11
PIO1	J16	PIO	PIO	1	E12
PIO1	J18	PIO	PIO	1	E14
PIO1 (●)	J22	N.C.	PIO	1	—
PIO1	K15	PIO	PIO	1	F11
PIO1	K16	PIO	PIO	1	F12
PIO1	K20	PIO	PIO	1	—
PIO1 (●)	K22	N.C.	PIO	1	—

Ball Function	Ball Number iCE65L04 iCE65L08	Pin Type by Device iCE65L04	iCE65L08	Bank	CB132 Ball Equivalent
PIO1	L15	PIO	PIO	1	G11
PIO1	L16	PIO	PIO	1	G12
PIO1 (●)	L22	N.C.	PIO	1	—
PIO1	M15	PIO	PIO	1	H11
PIO1	M16	PIO	PIO	1	H12
PIO1	M20	PIO	PIO	1	—
PIO1 (●)	M22	N.C.	PIO	1	—
PIO1	N15	PIO	PIO	1	J11
PIO1	N16	PIO	PIO	1	J12
PIO1	N22	PIO	PIO	1	—
PIO1	P15	PIO	PIO	1	K11
PIO1	P16	PIO	PIO	1	K12
PIO1	P18	PIO	PIO	1	K14
PIO1	P20	PIO	PIO	1	—
PIO1	P22	PIO	PIO	1	—
PIO1	R18	PIO	PIO	1	L14
PIO1	R20	PIO	PIO	1	—
PIO1	R22	PIO	PIO	1	—
PIO1	T20	PIO	PIO	1	—
PIO1	T22	PIO	PIO	1	—
PIO1	U20	PIO	PIO	1	—
PIO1 (●)	U22	N.C.	PIO	1	—
PIO1	V20	PIO	PIO	1	—
PIO1 (●)	V22	N.C.	PIO	1	—
PIO1	W20	PIO	PIO	1	—
PIO1 (●)	W22	N.C.	PIO	1	—
PIO1 (●)	Y22	N.C.	PIO	1	—
TCK	R16	JTAG	JTAG	1	L12
TDI	T16	JTAG	JTAG	1	M12
TDO	U18	JTAG	JTAG	1	N14
TMS	V18	JTAG	JTAG	1	P14
TRST_B	T18	JTAG	JTAG	1	M14
VCCIO_1	H22	VCCIO	VCCIO	1	—
VCCIO_1	J20	VCCIO	VCCIO	1	—
VCCIO_1	K13	VCCIO	VCCIO	1	F9
VCCIO_1	M18	VCCIO	VCCIO	1	H14
CDONE	T14	CONFIG	CONFIG	2	M10
CRESET_B	R14	CONFIG	CONFIG	2	L10
GBIN4/PIO2	V12	GBIN	GBIN	2	P7
GBIN5/PIO2	V11	GBIN	GBIN	2	P8
PIO2	R8	PIO	PIO	2	L4
PIO2	R9	PIO	PIO	2	L5
PIO2	R10	PIO	PIO	2	L6
PIO2	R11	PIO	PIO	2	L7
PIO2	R12	PIO	PIO	2	L8
PIO2	T7	PIO	PIO	2	M3
PIO2	T8	PIO	PIO	2	M4
PIO2	T10	PIO	PIO	2	M6
PIO2	T11	PIO	PIO	2	M7
PIO2	T12	PIO	PIO	2	M8

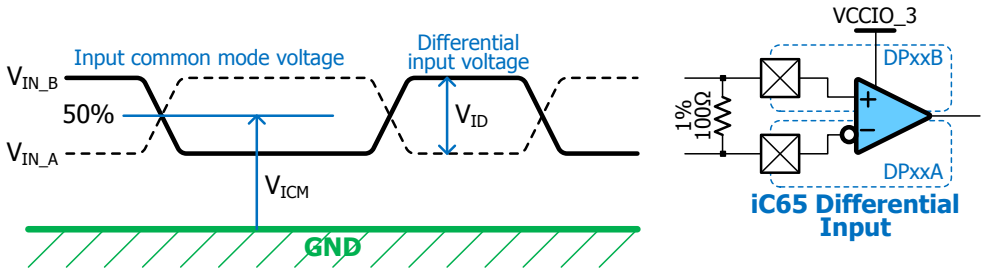
iCE65L04 Pad Name	DiePlus VQ100	CB132	CB196	CB284	Pad	X (µm)	Y (µm)
PIO3_18/DP09A	12	—	G2	L3	29	129.40	1,627.75
GBIN7/PIO3_19/DP09B	13	G1	G1	L5	30	231.40	1,592.74
VCCIO_3	14	J6	J6	N10	31	129.40	1,557.75
VREF	N/A	N/A	N/A	M1	32	231.40	1,522.74
GND	—	—	A9	N1	33	129.40	1,487.75
GBIN6/PIO3_20/DP10A	15	H1	H1	M5	34	231.40	1,452.74
PIO3_21/DP10B	16	—	H2	M3	35	129.40	1,417.75
GND	17	H7	A9	M11	36	231.40	1,382.74
PIO3_22/DP11A	—	—	G3	N3	37	129.40	1,347.75
PIO3_23/DP11B	—	—	G4	P3	38	231.40	1,312.74
VCCIO_3	—	—	K1	R3	39	129.40	1,277.75
VCCIO_3	—	—	—	—	40	231.40	1,242.74
GND	—	—	A9	T3	41	129.40	1,207.75
GND	—	—	—	—	42	231.40	1,172.74
PIO3_24/DP12A	—	—	J1	U3	43	129.40	1,137.75
PIO3_25/DP12B	—	—	J2	V3	44	231.40	1,102.74
GND	—	—	A9	V1	45	129.40	1,067.75
PIO3_26/DP13A	—	—	H4	W3	46	231.40	1,032.74
PIO3_27/DP13B	—	—	H3	Y3	47	129.40	997.75
PIO3_28/DP14A	18	G3	K2	L7	48	231.40	962.74
PIO3_29/DP14B	19	G4	J3	L8	49	129.40	927.75
PIO3_30/DP15A	—	H3	H5	M7	50	231.40	892.74
PIO3_31/DP15B	—	H4	G5	M8	51	129.40	857.75
VCC	—	J4	F2	N8	52	231.40	822.74
PIO3_32/DP16A	20	J3	L1	N7	53	129.40	787.75
PIO3_33/DP16B	21	J1	L2	N5	54	231.40	752.74
VCCIO_3	22	K1	K1	P5	55	129.40	717.75
VCCIO_3	—	—	—	—	56	231.40	682.74
GND	23	L3	L3	R7	57	129.40	637.75
GND	—	—	—	—	58	231.40	592.74
PIO3_34/DP17A	—	K3	M1	P7	59	129.40	547.75
PIO3_35/DP17B	—	K4	M2	P8	60	231.40	502.74
PIO3_36/DP18A	24	L1	K3	R5	61	129.40	457.75
PIO3_37/DP18B	25	M1	K4	T5	62	231.40	412.74
PIO3_38/DP19A	—	N1	N1	U5	63	129.40	367.75
PIO3_39/DP19B	—	P1	N2	V5	64	231.40	322.74
PIO2_00	—	—	—	AB2	65	545.00	139.20
PIO2_01	—	P2	L4	V6	66	595.00	37.20
PIO2_02	—	M3	M3	T7	67	645.00	139.20
GND	—	—	C2	AB5	68	695.00	37.20
PIO2_03	26	L4	P1	R8	69	745.00	139.20
PIO2_04	27	P3	N3	V7	70	795.00	37.20
PIO2_05	28	M4	P2	T8	71	845.00	139.20
PIO2_06	29	L5	L5	R9	72	895.00	37.20
PIO2_07	30	P4	M4	V8	73	930.00	139.20

iCE65L04 Pad Name	DiePlus VQ100	CB132	CB196	CB284	Pad	X (µm)	Y (µm)
PIO1_24	—	—	G11	F20	167	3,712.80	1,812.00
PIO1_25	—	—	F11	E20	168	3,610.80	1,847.00
PIO1_26	—	—	E10	D20	169	3,712.80	1,882.00
PIO1_27	—	—	E14	C20	170	3,610.80	1,917.00
GND	—	G8	G8	L12	171	3,712.80	1,952.00
GND	—	—	—	—	172	3,610.80	1,987.00
PIO1_28	—	—	F12	G22	173	3,712.80	2,022.00
PIO1_29	—	G12	D14	L16	174	3,610.80	2,057.00
PIO1_30	64	G11	E13	L15	175	3,712.80	2,092.00
PIO1_31	65	F12	C14	K16	176	3,610.80	2,127.00
VCC	—	—	K13	L20	177	3,712.80	2,162.00
VCC	—	—	—	—	178	3,610.80	2,197.00
PIO1_32	66	E14	E11	J18	179	3,712.80	2,232.00
PIO1_33	—	F11	C13	K15	180	3,610.80	2,267.00
VCCIO_1	67	F9	F9	K13	181	3,712.80	2,302.00
VCCIO_1	—	—	—	—	182	3,610.80	2,337.00
PIO1_34	68	E12	E12	J16	183	3,712.80	2,377.00
PIO1_35	69	D14	B14	H18	184	3,610.80	2,427.00
GND	70	G9	G9	L13	185	3,712.80	2,477.00
PIO1_36	71	E11	B13	J15	186	3,610.80	2,527.00
PIO1_37	72	D12	D12	H16	187	3,712.80	2,577.00
PIO1_38	73	C14	C12	G18	188	3,610.80	2,627.00
PIO1_39	74	B14	D11	F18	189	3,712.80	2,677.00
VPP_2V5	75	A14	A14	E18	190	3,610.80	2,739.68
VPP_FAST	76	A13	A13	E17	191	3,097.00	2,962.80
VCC	77	F8	F8	K12	192	2,997.00	2,860.80
VCC	77	F8	F8	K12	193	2,947.00	2,962.80
PIO0_00	78	A12	C11	E16	194	2,897.00	2,860.80
PIO0_01	—	C12	—	G16	195	2,847.00	2,962.80
PIO0_02	79	A11	A12	E15	196	2,797.00	2,860.80
PIO0_03	80	C11	B11	G15	197	2,747.00	2,962.80
PIO0_04	—	D11	—	H15	198	2,697.00	2,860.80
PIO0_05	81	A10	D10	E14	199	2,647.00	2,962.80
PIO0_06	82	C10	A11	G14	200	2,612.00	2,860.80
PIO0_07	83	D10	D9	H14	201	2,577.00	2,962.80
GND	84	A9	H6	E13	202	2,542.00	2,860.80
GND	—	—	—	—	203	2,507.00	2,962.80
PIO0_08	85	C9	C10	G13	204	2,472.00	2,860.80
PIO0_09	86	D9	A10	H13	205	2,437.00	2,962.80
PIO0_10	87	C8	B10	G12	206	2,402.00	2,860.80
PIO0_11	—	D8	E9	H12	207	2,367.00	2,962.80
PIO0_12	—	—	—	A18	208	2,332.00	2,860.80
PIO0_13	—	—	—	A17	209	2,297.00	2,962.80
PIO0_14	—	—	—	A16	210	2,262.00	2,860.80
PIO0_15	—	—	—	A15	211	2,227.00	2,962.80
VCCIO_0	88	A8	A8	E12	212	2,192.00	2,860.80
VCCIO_0	—	—	—	—	213	2,157.00	2,962.80

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO3_44/DP22A	M1	U3	86	231.735	777.67
PIO3_45/DP22B	M2	V3	87	129.735	732.67
PIO3_46/DP23A	N1	U5	88	231.735	687.67
PIO3_47/DP23B	N2	V5	89	129.735	642.67
PIO3_48/DP24A	—	W3	90	231.735	597.67
PIO3_49/DP24B	—	Y3	91	129.735	552.665
PIO2_00	P1	AB2	92	510.0	139.5
PIO2_01	M3	R8	93	560.0	37.5
PIO2_02	P2	Y4	94	610.0	139.5
GND	P6	AB5	95	660.0	37.5
GND	—	—	96	710.0	139.5
PIO2_03	M4	T7	97	760.0	37.5
PIO2_04	N3	AB3	98	810.0	139.5
PIO2_05	—	R9	99	859.3	37.5
PIO2_06	—	Y5	100	910.0	139.5
PIO2_07	L4	T8	101	960.0	37.5
PIO2_08	P3	V6	102	1,012.5	139.5
VCCIO_2	M5	T9	103	1,047.5	37.5
VCCIO_2	—	—	104	1,082.5	139.5
PIO2_09	P4	R10	105	1,117.5	37.5
PIO2_10	N4	AB4	106	1,152.5	139.5
GND	H8	V10	107	1,187.5	37.5
GND	—	—	108	1,222.5	139.5
PIO2_11	K5	V7	109	1,257.5	37.5
PIO2_12	P5	Y7	110	1,292.5	139.5
PIO2_13	—	V9	111	1,327.5	37.5
PIO2_14	—	Y6	112	1,362.5	139.5
PIO2_15	—	AB7	113	1,397.5	37.5
PIO2_16	—	AB6	114	1,432.5	139.5
PIO2_17	L5	Y9	115	1,467.5	37.5
PIO2_18	N5	V8	116	1,502.3	139.5
GND	P6	N12	117	1,537.3	37.5
GND	—	—	118	1,572.5	139.5
PIO2_19	N6	AB8	119	1,607.5	37.5
PIO2_20	K6	AB9	120	1,642.5	139.5
VCC	J7	Y8	121	1,677.5	37.5
VCC	—	—	122	1,712.5	139.5
PIO2_21	L6	T10	123	1,747.5	37.5
PIO2_22	M6	AB10	124	1,782.5	139.5
PIO2_23	—	AB11	125	1,817.5	37.5
PIO2_24	—	AB12	126	1,852.5	139.5
PIO2_25	L7	Y10	127	1,887.5	37.5
PIO2_26	P7	AB13	128	1,922.5	139.5
PIO2_27	K7	AB14	129	1,957.5	37.5
VCCIO_2	N10	Y11	130	1,992.5	139.5
VCCIO_2	—	—	131	2,027.5	37.5

Differential Inputs

Figure 50: Differential Input Specifications



Input common mode voltage: $$V_{ICM} = \frac{VCCIO\_3}{2} \pm \Delta V_{ICM}$$

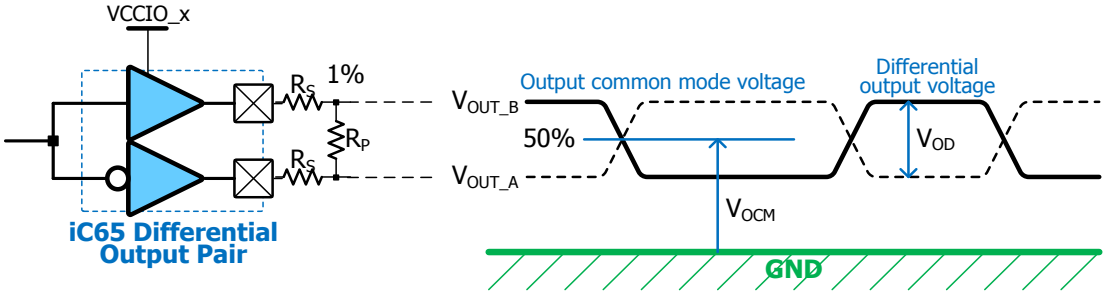
Differential input voltage: $$V_{ID} = |V_{IN\_B} - V_{IN\_A}|$$

Table 52: **Recommended Operating Conditions for Differential Inputs**

I/O Standard	VCCIO_3 (V)			V_{ID} (mV)			V_{ICM} (V)		
	Min	**Nom**	**Max**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
LVDS	2.38	2.50	2.63	250	350	450	$\frac{VCCIO\_3}{2} - 0.30$	$\frac{VCCIO\_3}{2}$	$\frac{VCCIO\_3}{2} + 0.30$
SubLVDS	1.71	1.80	1.89	100	150	200	$\frac{VCCIO\_3}{2} - 0.25$	$\frac{VCCIO\_3}{2}$	$\frac{VCCIO\_3}{2} + 0.25$

Differential Outputs

Figure 51: Differential Output Specifications



Output common mode voltage: $$V_{OCM} = \frac{VCCIO\_x}{2} \pm \Delta V_{OCM}$$

Differential output voltage: $$V_{OD} = |V_{OUT\_B} - V_{OUT\_A}|$$

Table 53: **Recommended Operating Conditions for Differential Outputs**

I/O Standard	VCCIO_x (V)			Ω		V_{OD} (mV)			V_{OCM} (V)		
	Min	**Nom**	**Max**	**R_S**	**R_P**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
LVDS	2.38	2.50	2.63	150	140	300	350	400	$\frac{VCCIO}{2} - 0.15$	$\frac{VCCIO}{2}$	$\frac{VCCIO}{2} + 0.15$
SubLVDS	1.71	1.80	1.89	270	120	100	150	200	$\frac{VCCIO}{2} - 0.10$	$\frac{VCCIO}{2}$	$\frac{VCCIO}{2} + 0.10$

I/O Banks 0, 1, 2 and SPI Bank Characteristic Curves

Figure 52: **Typical LVCMOS Output Low Characteristics (I/O Banks 0, 1, 2, and SPI)**

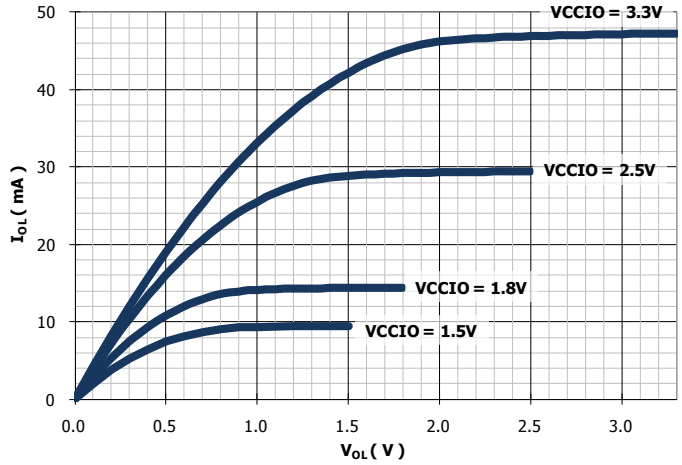


Figure 53: **Typical LVCMOS Output High Characteristics (I/O Banks 0, 1, 2, and SPI)**

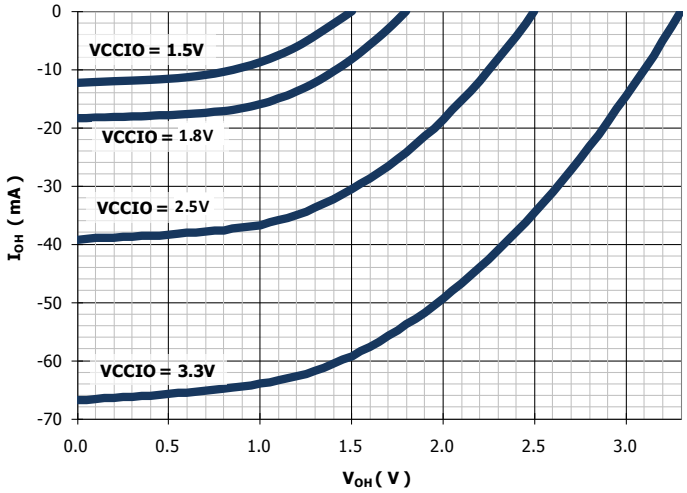
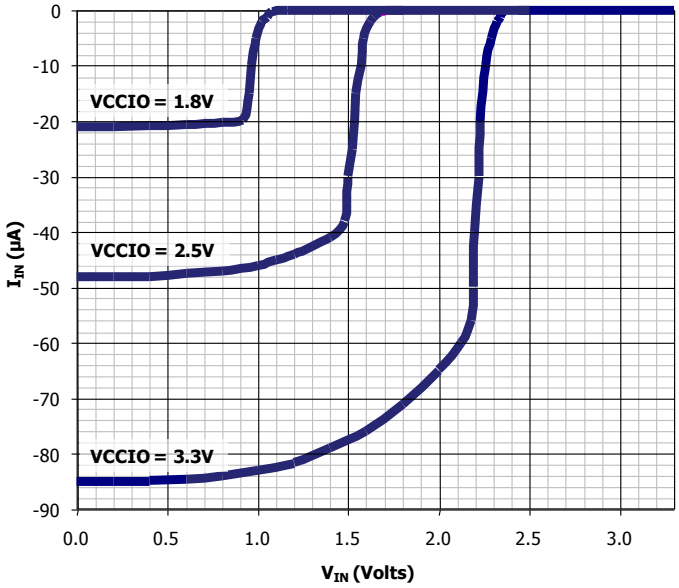


Figure 54: **Input with Internal Pull-Up Resistor Enabled (I/O Banks 0, 1, 2, and SPI)**



Notes