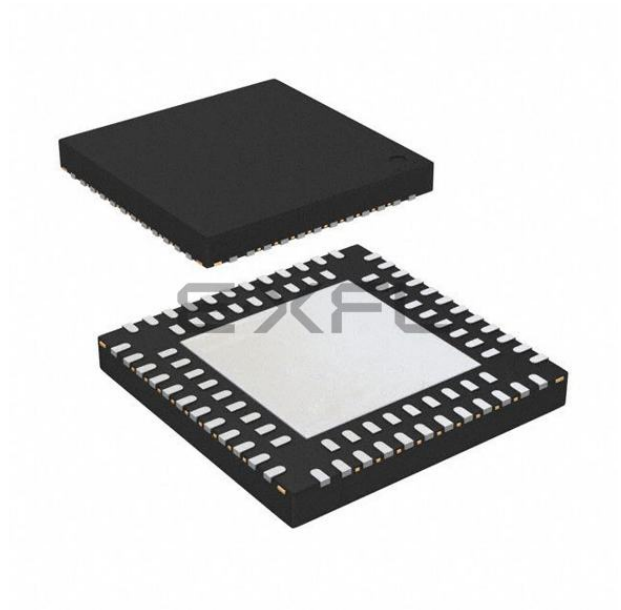
Lattice Semiconductor Corporation - ICE65L01F-LQN84I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	160
Number of Logic Elements/Cells	1280
Total RAM Bits	65536
Number of I/O	67
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	84-VFQFN Dual Rows, Exposed Pad
Supplier Device Package	84-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice65l01f-lqn84i

Programmable Logic Block (PLB)

Generally, a logic design for an iCE65 component is created using a high-level hardware description language such as Verilog or VHDL. The Lattice Semiconductor development software then synthesizes the high-level description into equivalent functions built using the programmable logic resources within each iCE65 device. Both sequential and combinational functions are constructed from an array of Programmable Logic Blocks (PLBs). Each PLB contains eight Logic Cells (LCs), as pictured in Figure 4, and share common control inputs, such as clocks, reset, and enable controls.

PLBs are connected to one another and other logic functions using the rich Programmable Interconnect resources.

Logic Cell (LC)

Each iCE65 device contains thousands of Logic Cells (LCs), as listed in Table 1. Each Logic Cell includes three primary logic elements, shown in Figure 4.

- A four-input Look-Up Table (LUT4) builds any combinational logic function, of any complexity, of up to four inputs. Similarly, the LUT4 element behaves as a 16x1 Read-Only Memory (ROM). Combine and cascade multiple LUT4s to create wider logic functions.

Figure 4: **Programmable Logic Block and Logic Cell**

- A 'D'-style Flip-Flop (DFF), with an optional clock-enable and reset control input, builds sequential logic functions. Each DFF also connects to a global reset signal that is automatically asserted immediately following device configuration.
- Carry Logic boosts the logic efficiency and performance of arithmetic functions, including adders, subtracters, comparators, binary counters and some wide, cascaded logic functions.

The output from a Logic Cell is available to all inputs to all eight Logic Cells within the Programmable Logic Block. Similarly, the Logic Cell output feeds into fabric to connect to other features on the iCE65 device.

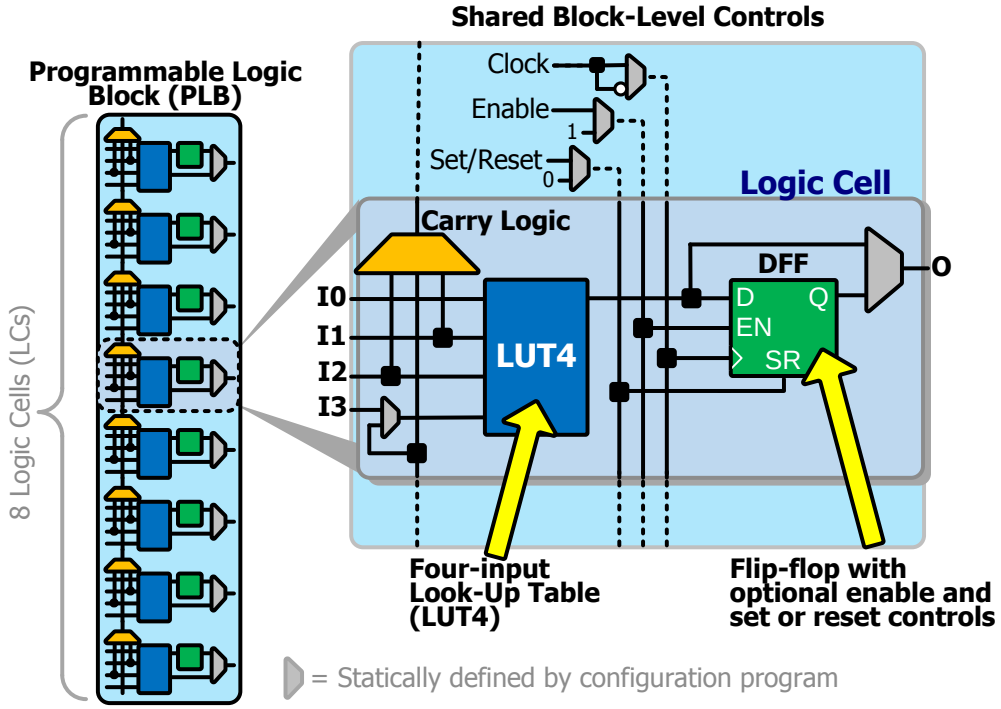
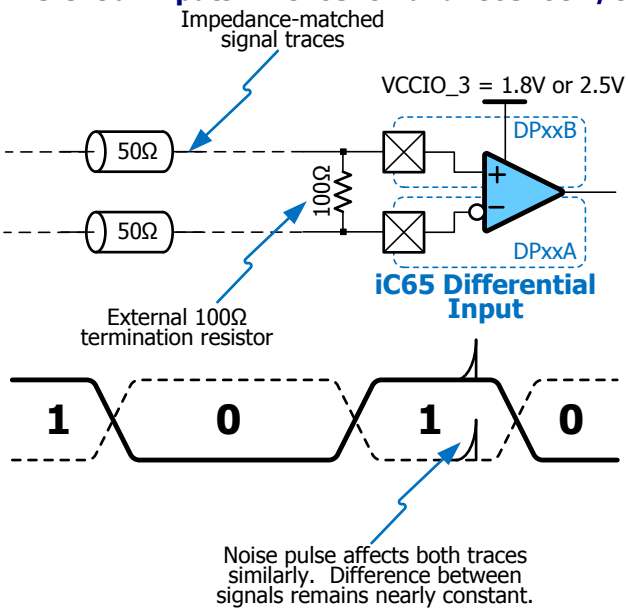


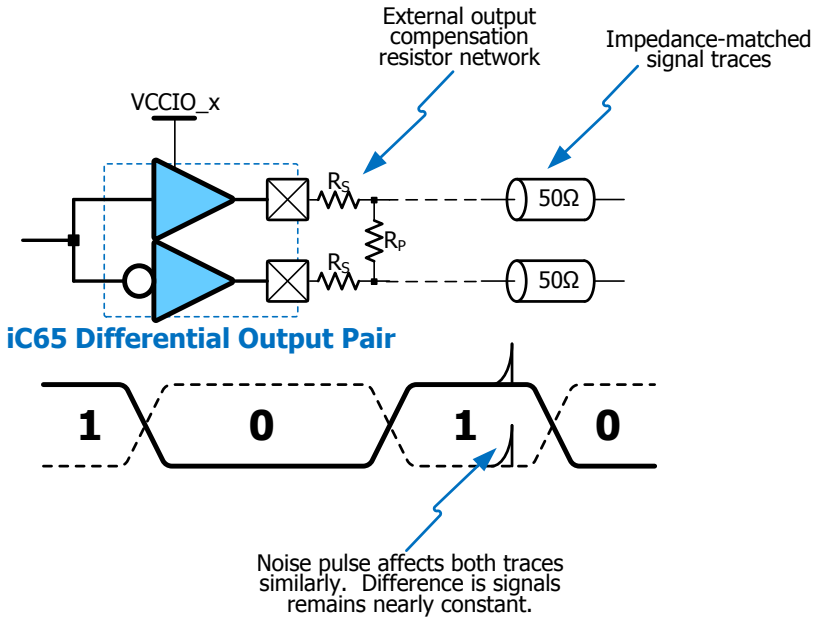
Figure 8: **Differential Inputs in iCE65L04 and iC65L08 I/O Bank 3**



Differential Outputs in Any Bank

Differential outputs are built using a pair of single-ended PIO pins as shown in Figure 9. Each differential I/O pair requires a three-resistor termination network to adjust output characteristic to match those for the specific differential I/O standard. The output characteristics depend on the values of the parallel resistors (RP) and series resistor (RS). Differential outputs must be located in the same I/O tile.

Figure 9: Differential Output Pair



For electrical characteristics, see "Differential Outputs" on page 100.

The PIO pins that make up a differential output pair are indicated with a blue bounding box in the in the tables in "Die Cross Reference" starting on page 84.

Table 12 and Table 13 list the connections between a specific global buffer and the inputs on a Programmable I/O (PIO) pair. Although there is no direct connection between a global buffer and a PIO output, such a connection is possible by first connecting through a PLB LUT4 function. Again, all global buffers optionally drive all clock inputs. However, even-numbered global buffers optionally drive the clock-enable input on a PIO pair.

The PIO clock enable connect is different between the iCE65L01/iCE65L04 and iCE65L08.

Table 12: **iCE65L01 & iCE65L04: Global Buffer (GBUF) Connections to Programmable I/O (PIO) Pair**

Global Buffer	Output Connections	Input Clock	Output Clock	Clock Enable
GBUF0	No (connect through PLB LUT)	Yes	Yes	No
GBUF1		Yes	Yes	Yes
GBUF2		Yes	Yes	No
GBUF3		Yes	Yes	Yes
GBUF4		Yes	Yes	No
GBUF5		Yes	Yes	Yes
GBUF6		Yes	Yes	No
GBUF7		Yes	Yes	Yes

Table 13: **iCE64L08: Global Buffer (GBUF) Connections to Programmable I/O (PIO) Pair**

Global Buffer	Output Connections	Input Clock	Output Clock	Clock Enable
GBUF0	No (connect through PLB LUT)	Yes	Yes	Yes
GBUF1		Yes	Yes	No
GBUF2		Yes	Yes	Yes
GBUF3		Yes	Yes	No
GBUF4		Yes	Yes	Yes
GBUF5		Yes	Yes	No
GBUF6		Yes	Yes	Yes
GBUF7		Yes	Yes	No

Global Buffer Inputs

The iCE65 component has eight specialized GBIN/PIO pins that are optionally direct inputs to the global buffers, offering the best overall clock characteristics. As shown in Figure 15, each GBIN/PIO pin is a full-featured I/O pin but also provides a direct connection to its associated global buffer. The direct connection to the global buffer bypasses the iCEgate input-blocking latch and other PIO input logic. These special PIO pins are allocated two to an I/O Bank, a total of eight. These pins are labeled GBIN0 through GBIN7, as shown in Figure 14 and the pin locations for each GBIN input appear in Table 14.

Table 14: **Global Buffer Input Ball/Pin Number by Package**

Global Buffer Input (GBIN)	I/O Bank	VQ100	CB132	'L04 CB196	'L08 CB196	CB284
GBIN0	0	90	A6	A7	A7	E10
GBIN1		89	A7	E7	E7	E11
GBIN2	1	63	G14	F10	F10	L18
GBIN3		62	F14	G12	G12	K18
GBIN4	2	34	P8	L7	N8	V12
GBIN5		33	P7	P5	M7	V11
GBIN6	3	15	H1	H1	H1	M5
GBIN7		13	G1	G1	H3	L5

Device Configuration

As described in Table 20, iCE65 components are configured for a specific application by loading a binary configuration bitstream image, generated by the Lattice development system. For high-volume applications, the bitstream image is usually permanently programmed in the on-chip NVCM, However, the bitstream image can also be stored external in a standard, low-cost commodity SPI serial Flash PROM. The iCE65 component can automatically load the image using the SPI Master Configuration Interface. Similarly, the iCE65 configuration data can be downloaded from an external processor, microcontroller, or DSP processor using an SPI-like serial interface or an IEEE 1149 JTAG interface.

Table 20: **iCE65 Device Configuration Modes**

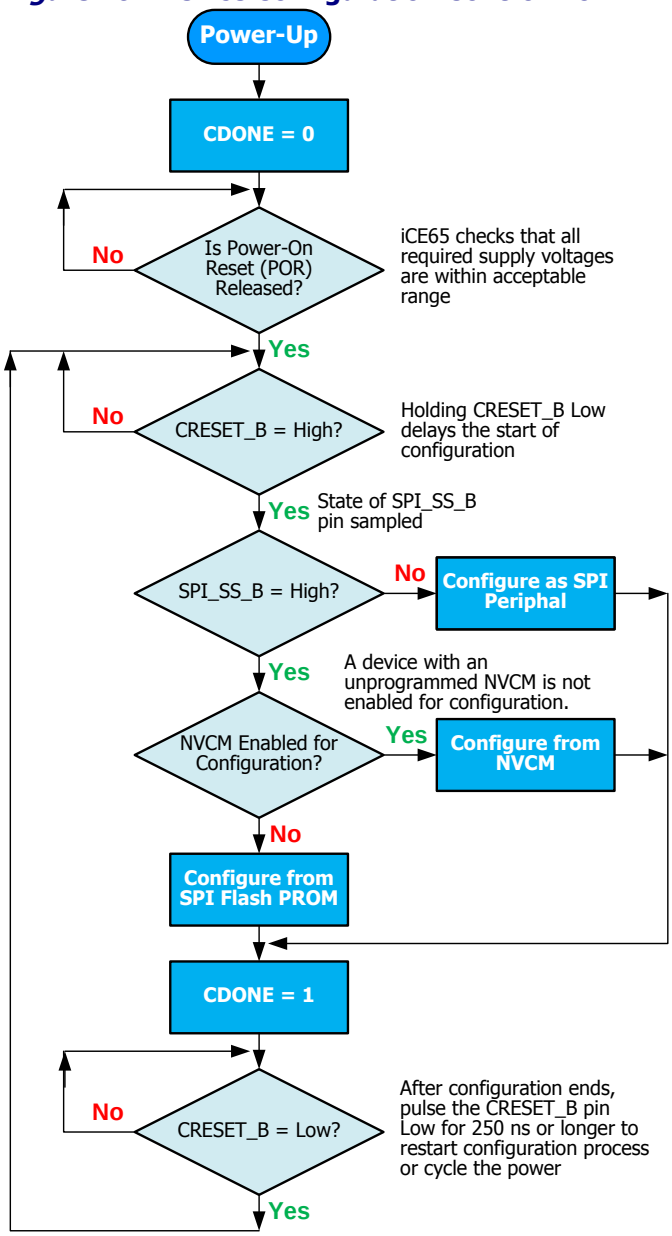
Mode	Analogy	Configuration Data Source
NVCM	ASIC	Internal, lowest-cost, secure, one-time programmable Nonvolatile Configuration Memory (NVCM)
SPI Flash	Microprocessor	External, low-cost, commodity, SPI serial Flash PROM
SPI Peripheral	Processor Peripheral	Configured by external device, such as a processor, microcontroller, or DSP using practically any data source, such as system Flash, a disk image, or over a network connection.
JTAG	JTAG	JTAG configuration requires sending a special command sequence on the SPI interface to enable JTAG configuration. Configuration is controlled by and external device.

Configuration Mode Selection

The iCE65 configuration mode is selected according to the following priority described below and illustrated in Figure 20.

- After exiting the Power-On Reset (POR) state or when CRESET_B returns High after being held Low for 250 ns or more, the iCE65 FPGA samples the logical value on its SPI_SS_B pin. Like other programmable I/O pins, the SPI_SS_B pin has an internal pull-up resistor (see Input Pull-Up Resistors on I/O Banks 0, 1, and 2).
- If the SPI_SS_B pin is sampled as a logic '1' (High), then …
  - Check if the iCE65 is enabled to configure from the Nonvolatile Configuration Memory (NVCM). If the iCE65 device has NVCM memory ('**F**' ordering code) but the NVCM is yet unprogrammed, then the iCE65 device is not enabled to configure from NVCM. Conversely, if the NVCM is programmed, the iCE65 device will configure from NVCM.
    - If enabled to configure from NVCM, the iCE65 device configures itself using NVCM.
    - If not enabled to configure from NVCM, then the iCE65 FPGA configures using the SPI Master Configuration Interface.
- If the SPI_SS_B pin is sampled as a logic '0' (Low), then the iCE65 device waits to be configured from an external controller or from another iCE65 device in SPI Master Configuration Mode using an SPI-like interface.

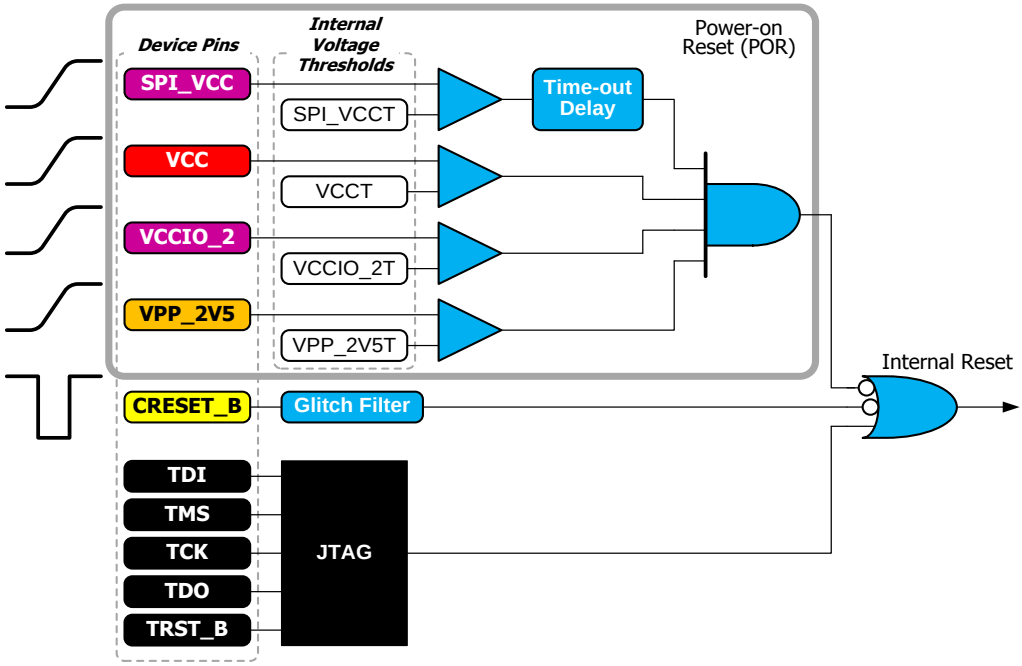
Figure 20: **Device Configuration Control Flow**



Configuration Image Size

Table 23 shows the number of memory bits required to configure an iCE65 device. Two values are provided for each device. The "Logic Only" value indicates the minimum configuration size, the number of bits required to configure only the logic fabric, leaving the RAM4K blocks uninitialized. The "Logic + RAM4K" column indicates the maximum configuration size, the number of bits to configure the logic fabric and to pre-initialize all the RAM4K blocks.

Figure 22: iCE65 Internal Reset Circuitry



Power-On Reset (POR)

The Power-on Reset (POR) circuit monitors specific voltage supply inputs and holds the device in reset until all the relevant supplies exceed the internal voltage thresholds. The SPI_VCC supply also has an additional time-out delay to allow an attached SPI serial PROM to power up properly. Table 24 shows the POR supply inputs. The Nonvolatile Configuration Memory (NVCM) requires that the VPP_2V5 supply be connected, even if the application does not use the NVCM.

***Table 24:* Power-on Reset (POR) Voltage Resources**

Supply Rail	iCE65 Production Devices
VCC	Yes
SPI_VCC	Yes
VCCIO_1	No
VCCIO_2	Yes
VPP_2V5	Yes

CRESET_B Pin

The CRESET_B pin resets the iCE65 internal logic when Low.

JTAG Interface

Specific command sequences also reset the iCE65 internal logic.

SPI Master Configuration Interface

All iCE65 devices, including those with NVCM, can be configured from an external, commodity SPI serial Flash PROM, as shown in Figure 23. The SPI configuration interface is essentially its own independent I/O bank, powered by the VCC_SPI supply input. Presently, most commercially-available SPI serial Flash PROMs require a 3.3V supply.

QN84 Quad Flat Pack No-Lead

The QN84 is a Quad Flat Pack No-Lead package with a 0.5 mm pad pitch.

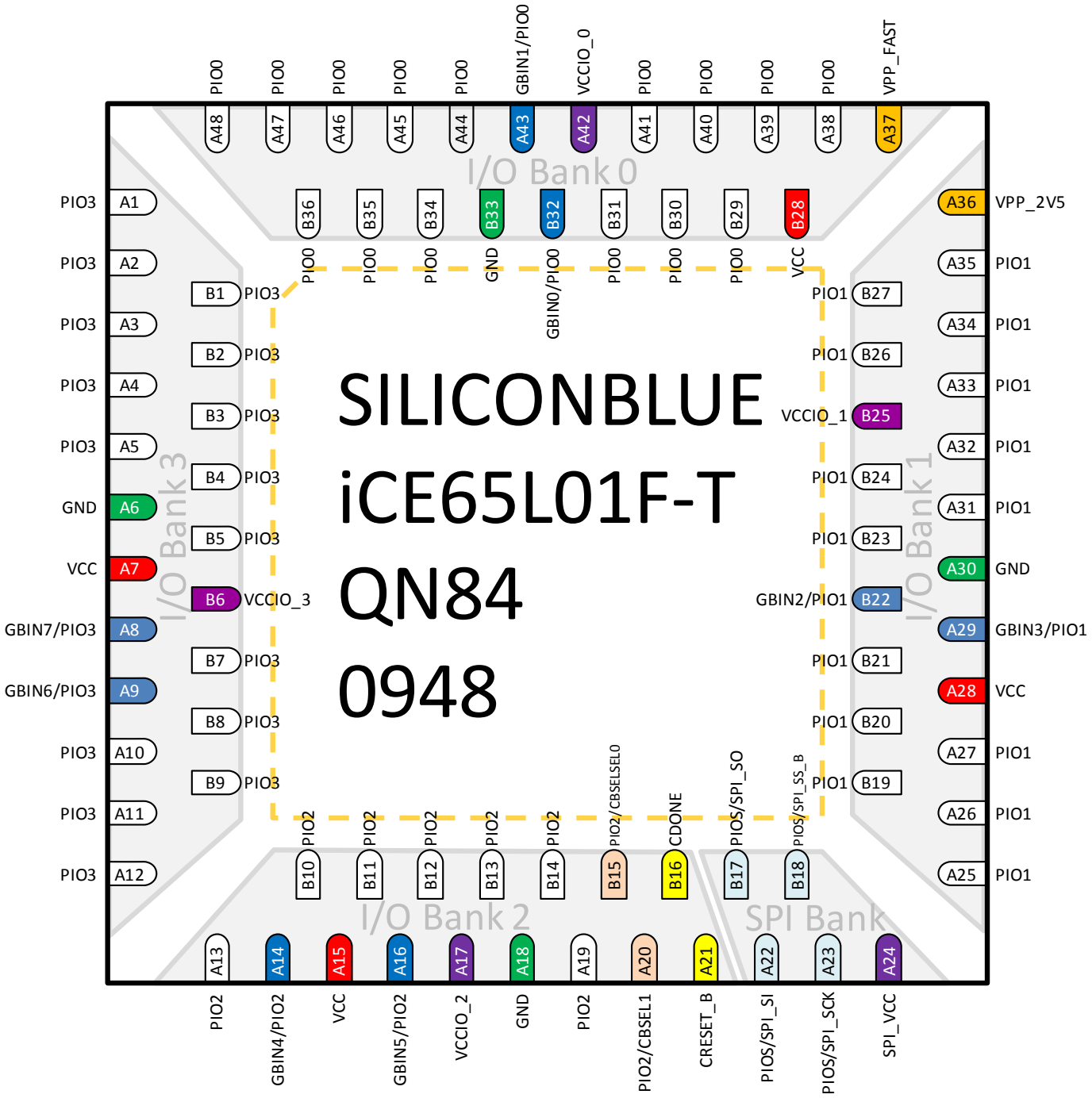
Footprint Diagram

Figure 34 shows the iCE65 footprint diagram for the QN84 package.

Also see Table 38 for a complete, detailed pinout for the QN84 package.

The signal pins are also grouped into the four I/O Banks and the SPI interface.

Figure 34: **iCE65 QN84 Quad Flat Pack No-Lead Footprint (Top View)**



CB121 Chip-Scale Ball-Grid Array

The CB121 package is a chip-scale, fully-populated, ball-grid array with 0.5 mm ball pitch.

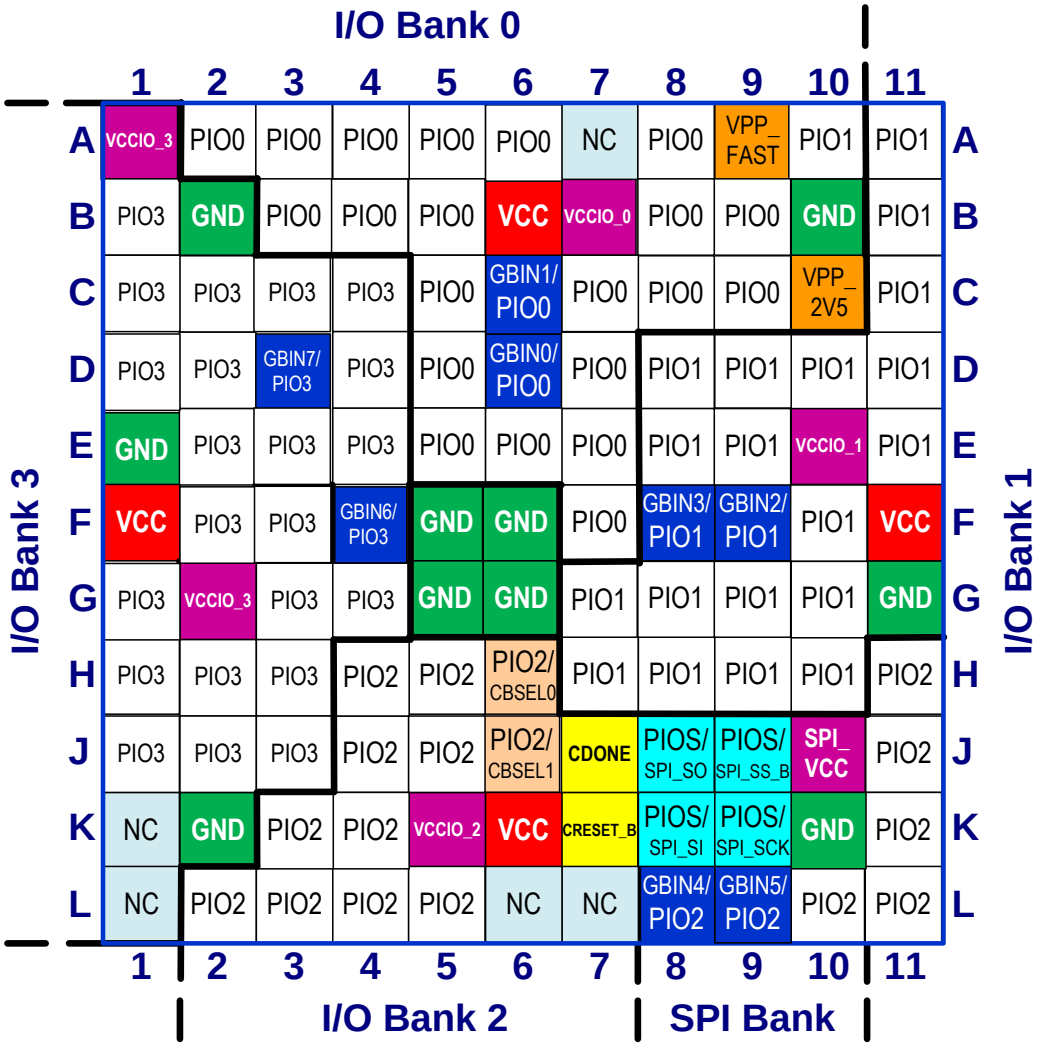
Footprint Diagram

Figure 39 shows the iCE65L01 chip-scale BGA footprint for the 6 x 6 mm CB121 package.

Also see Table 40 for a complete, detailed pinout for the 121-ball chip-scale BGA packages.

The signal pins are also grouped into the four I/O Banks and the SPI interface.

Figure 39: **iCE65L01 CB121 Chip-Scale BGA Footprint (Top View)**



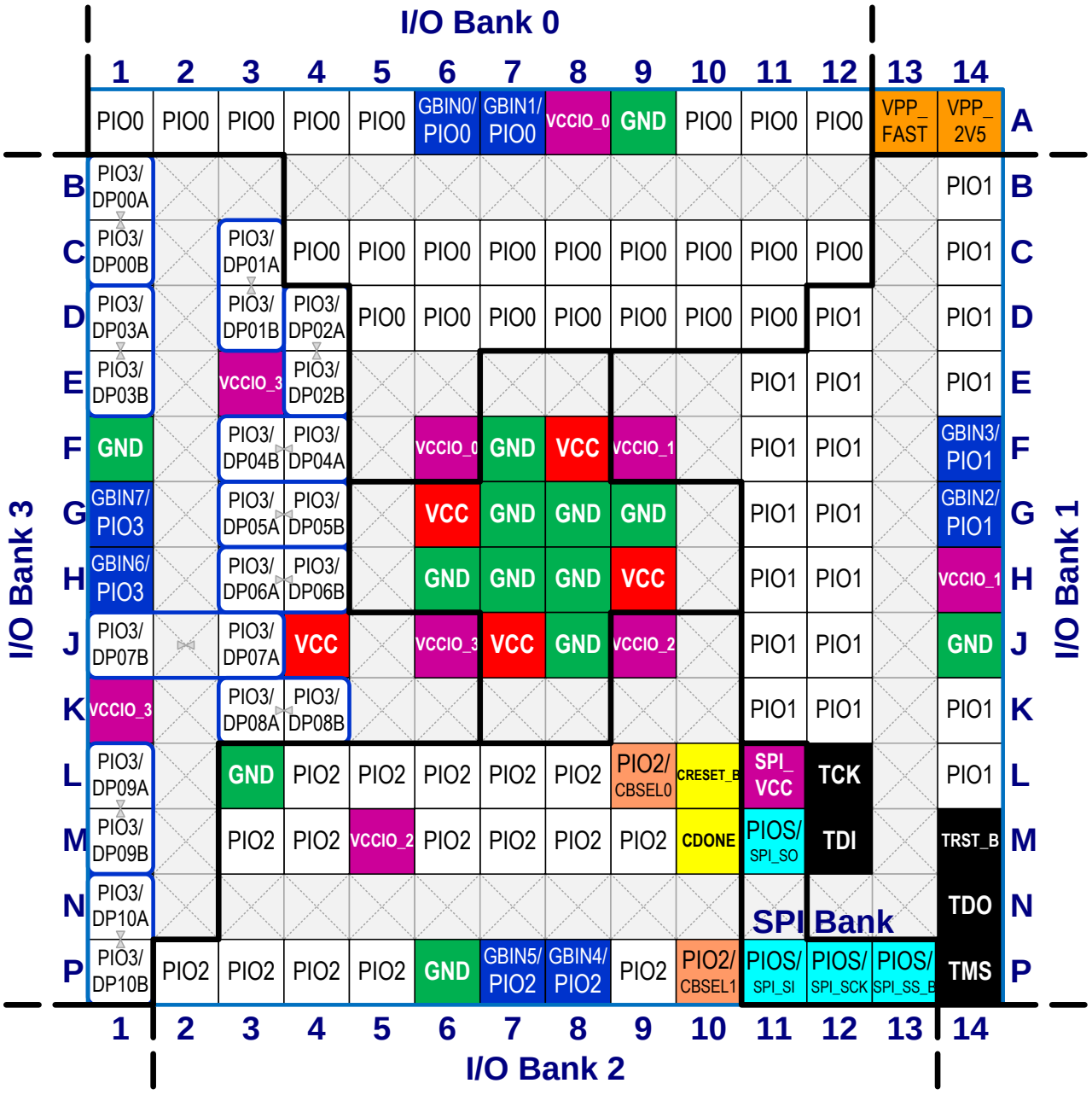
Pinout Table

Table 40 provides a detailed pinout table for the iCE65L01 in the CB121 chip-scale BGA package. Pins are generally arranged by I/O bank, then by ball function.

Table 40: **iCE65L01 CB121 Chip-scale BGA Pinout Table**

Ball Function	Ball Number	Pin Type	Bank
GBIN0/PIO0	D6	GBIN	0
GBIN1/PIO0	C6	GBIN	0
PIO0	A2	PIO	0
PIO0	A3	PIO	0
PIO0	A4	PIO	0

Figure 42: **iCE65L04 CB132 Chip-Scale BGA Footprint (Top View)**



Ball Function	Ball Number	Pin Type	Bank
PIO1	H12	PIO	1
PIO1	J11	PIO	1
PIO1	J12	PIO	1
PIO1	K11	PIO	1
PIO1	K12	PIO	1
PIO1	K14	PIO	1
PIO1	L14	PIO	1
TCK	L12	JTAG	1
TDI	M12	JTAG	1
TDO	N14	JTAG	1
TMS	P14	JTAG	1
TRST_B	M14	JTAG	1
VCCIO_1	F9	VCCIO	1
VCCIO_1	H14	VCCIO	1
CDONE	M10	CONFIG	2
CRESET_B	L10	CONFIG	2
GBIN4/PIO2	P8	GBIN	2
GBIN5/PIO2	P7	GBIN	2
PIO2	L4	PIO	2
PIO2	L5	PIO	2
PIO2	L6	PIO	2
PIO2	L7	PIO	2
PIO2	L8	PIO	2
PIO2	M3	PIO	2
PIO2	M4	PIO	2
PIO2	M6	PIO	2
PIO2	M7	PIO	2
PIO2	M8	PIO	2
PIO2	M9	PIO	2
PIO2	P2	PIO	2
PIO2	P3	PIO	2
PIO2	P4	PIO	2
PIO2	P5	PIO	2
PIO2	P9	PIO	2
PIO2/CBSEL0	L9	PIO	2
PIO2/CBSEL1	P10	PIO	2
VCCIO_2	J9	PIO	2
VCCIO_2	M5	PIO	2
PIO3/DP00A	B1	DPIO	3
PIO3/DP00B	C1	DPIO	3
PIO3/DP01A	C3	DPIO	3
PIO3/DP01B	D3	DPIO	3
PIO3/DP02A	D4	DPIO	3
PIO3/DP02B	E4	DPIO	3
PIO3/DP03A	D1	DPIO	3
PIO3/DP03B	E1	DPIO	3
PIO3/DP04A	F4	DPIO	3
PIO3/DP04B	F3	DPIO	3
L01/L04: GBIN6/PIO3 L08: GBIN6/DP06A	H1	GBIN	3

Ball Function	Ball Number iCE65L04 iCE65L08	Pin Type by Device iCE65L04	iCE65L08	Bank	CB132 Ball Equivalent
PIO1	L15	PIO	PIO	1	G11
PIO1	L16	PIO	PIO	1	G12
PIO1 (●)	L22	N.C.	PIO	1	—
PIO1	M15	PIO	PIO	1	H11
PIO1	M16	PIO	PIO	1	H12
PIO1	M20	PIO	PIO	1	—
PIO1 (●)	M22	N.C.	PIO	1	—
PIO1	N15	PIO	PIO	1	J11
PIO1	N16	PIO	PIO	1	J12
PIO1	N22	PIO	PIO	1	—
PIO1	P15	PIO	PIO	1	K11
PIO1	P16	PIO	PIO	1	K12
PIO1	P18	PIO	PIO	1	K14
PIO1	P20	PIO	PIO	1	—
PIO1	P22	PIO	PIO	1	—
PIO1	R18	PIO	PIO	1	L14
PIO1	R20	PIO	PIO	1	—
PIO1	R22	PIO	PIO	1	—
PIO1	T20	PIO	PIO	1	—
PIO1	T22	PIO	PIO	1	—
PIO1	U20	PIO	PIO	1	—
PIO1 (●)	U22	N.C.	PIO	1	—
PIO1	V20	PIO	PIO	1	—
PIO1 (●)	V22	N.C.	PIO	1	—
PIO1	W20	PIO	PIO	1	—
PIO1 (●)	W22	N.C.	PIO	1	—
PIO1 (●)	Y22	N.C.	PIO	1	—
TCK	R16	JTAG	JTAG	1	L12
TDI	T16	JTAG	JTAG	1	M12
TDO	U18	JTAG	JTAG	1	N14
TMS	V18	JTAG	JTAG	1	P14
TRST_B	T18	JTAG	JTAG	1	M14
VCCIO_1	H22	VCCIO	VCCIO	1	—
VCCIO_1	J20	VCCIO	VCCIO	1	—
VCCIO_1	K13	VCCIO	VCCIO	1	F9
VCCIO_1	M18	VCCIO	VCCIO	1	H14
CDONE	T14	CONFIG	CONFIG	2	M10
CRESET_B	R14	CONFIG	CONFIG	2	L10
GBIN4/PIO2	V12	GBIN	GBIN	2	P7
GBIN5/PIO2	V11	GBIN	GBIN	2	P8
PIO2	R8	PIO	PIO	2	L4
PIO2	R9	PIO	PIO	2	L5
PIO2	R10	PIO	PIO	2	L6
PIO2	R11	PIO	PIO	2	L7
PIO2	R12	PIO	PIO	2	L8
PIO2	T7	PIO	PIO	2	M3
PIO2	T8	PIO	PIO	2	M4
PIO2	T10	PIO	PIO	2	M6
PIO2	T11	PIO	PIO	2	M7
PIO2	T12	PIO	PIO	2	M8

Ball Function	Ball Number iCE65L04 iCE65L08	Pin Type by Device iCE65L04	Pin Type by Device iCE65L08	Bank	CB132 Ball Equivalent
PIO2	T13	PIO	PIO	2	M9
PIO2	V6	PIO	PIO	2	P2
PIO2	V7	PIO	PIO	2	P3
PIO2	V8	PIO	PIO	2	P4
PIO2	V9	PIO	PIO	2	P5
PIO2	V13	PIO	PIO	2	P9
PIO2	Y4	PIO	PIO	2	—
PIO2	Y5	PIO	PIO	2	—
PIO2	Y6	PIO	PIO	2	—
PIO2	Y7	PIO	PIO	2	—
PIO2	Y9	PIO	PIO	2	—
PIO2	Y10	PIO	PIO	2	—
PIO2	Y13	PIO	PIO	2	—
PIO2	Y14	PIO	PIO	2	—
PIO2	Y15	PIO	PIO	2	—
PIO2	Y17	PIO	PIO	2	—
PIO2	Y18	PIO	PIO	2	—
PIO2	Y19	PIO	PIO	2	—
PIO2	Y20	PIO	PIO	2	—
PIO2	AB2	PIO	PIO	2	—
PIO2 (●)	AB3	N.C.	PIO	2	—
PIO2 (●)	AB4	N.C.	PIO	2	—
PIO2	AB6	PIO	PIO	2	—
PIO2	AB7	PIO	PIO	2	—
PIO2	AB8	PIO	PIO	2	—
PIO2	AB9	PIO	PIO	2	—
PIO2	AB10	PIO	PIO	2	—
PIO2	AB11	PIO	PIO	2	—
PIO2	AB12	PIO	PIO	2	—
PIO2	AB13	PIO	PIO	2	—
PIO2	AB14	PIO	PIO	2	—
PIO2	AB15	PIO	PIO	2	—
PIO2 (●)	AB16	N.C.	PIO	2	—
PIO2 (●)	AB17	N.C.	PIO	2	—
PIO2 (●)	AB18	N.C.	PIO	2	—
PIO2 (●)	AB19	N.C.	PIO	2	—
PIO2 (●)	AB20	N.C.	PIO	2	—
PIO2 (●)	AB21	N.C.	PIO	2	—
PIO2 (●)	AB22	N.C.	PIO	2	—
PIO2/CBSEL0	R13	PIO	PIO	2	L9
PIO2/CBSEL1	V14	PIO	PIO	2	P10
VCCIO_2	N13	VCCIO	VCCIO	2	J9
VCCIO_2	T9	VCCIO	VCCIO	2	M5
VCCIO_2	Y11	VCCIO	VCCIO	2	—
PIO3/DP00A	F5	DPIO	DPIO	3	B1
PIO3/DP00B	G5	DPIO	DPIO	3	C1
PIO3/DP01A	G7	DPIO	DPIO	3	C3
PIO3/DP01B	H7	DPIO	DPIO	3	D3
PIO3/DP02A	H8	DPIO	DPIO	3	D4
PIO3/DP02B	J8	DPIO	DPIO	3	E4

Die Cross Reference

The tables in this section list all the pads on a specific die type and provide a cross reference on how a specific pad connects to a ball or pin in each of the available package offerings. Similarly, the tables provide the pad coordinates for the die-based version of the product (DiePlus). These tables also provide a way to prototype with one package option and then later move to a different package or die.

As described in "Input and Output Register Control per PIO Pair" on page 16, PIO pairs share register control inputs. Similarly, as described in "Differential Inputs and Outputs" on page 12, a PIO pair can form a differential input or output. PIO pairs in I/O Bank 3 are optionally differential inputs or differential outputs. PIO pairs in all other I/O Banks are optionally differential outputs. In the tables, differential pairs are surrounded by a heavy blue box.

iCE65L04

Table 45 lists all the pads on the iCE65L04 die and how these pads connect to the balls or pins in the supported package styles. Most VCC, VCCIO, and GND pads are double-bonded inside the package although the table shows only a single connection.

For additional information on the iCE65L04 DiePlus product, please refer to the following data sheet.

DiePlus Advantage FPGA Known Good Die

Table 45: iCE65L04 Die Cross Reference

iCE65L04	DiePlus						
Pad Name	VQ100	CB132	CB196	CB284	Pad	X (µm)	Y (µm)
PIO3_00/DP00A	1	B1	C1	F5	1	129.40	2,687.75
PIO3_01/DP00B	2	C1	B1	G5	2	231.40	2,642.74
PIO3_02/DP01A	3	C3	D3	G7	3	129.40	2,597.75
PIO3_03/DP01B	4	D3	C3	H7	4	231.40	2,552.74
GND	5	F1	F1	K5	5	129.40	2,507.75
GND	—	—	—	—	6	231.40	2,462.74
VCCIO_3	6	E3	E3	J7	7	129.40	2,417.75
VCCIO_3	—	—	—	—	8	231.40	2,372.74
PIO3_04/DP02A	7	D4	D1	H8	9	129.40	2,327.75
PIO3_05/DP02B	8	E4	D2	J8	10	231.40	2,292.74
PIO3_06/DP03A	—	D1	E1	H5	11	129.40	2,257.75
PIO3_07/DP03B	—	E1	E2	J5	12	231.40	2,222.74
VCC	—	—	H9	D3	13	129.40	2,187.75
PIO3_08/DP04A	9	F4	D4	K8	14	231.40	2,152.74
PIO3_09/DP04B	10	F3	E4	K7	15	129.40	2,117.75
PIO3_10/DP05A	—	—	F3	E3	16	231.40	2,082.74
PIO3_11/DP05B	—	—	F4	F3	17	129.40	2,047.75
GND	—	H6	A9	M10	18	231.40	2,012.74
PIO3_12/DP06A	—	—	F5	G3	19	129.40	1,977.75
PIO3_13/DP06B	—	—	E5	H3	20	231.40	1,942.74
GND	—	—	A9	J3	21	129.40	1,907.75
GND	—	—	—	—	22	231.40	1,872.74
PIO3_14/DP07A	—	—	—	H1	23	129.40	1,837.75
PIO3_15/DP07B	—	—	—	J1	24	231.40	1,802.74
VCCIO_3	—	—	K1	K3	25	129.40	1,767.75
VCC	11	G6	G6	L10	26	231.40	1,732.74
PIO3_16/DP08A	—	—	—	K1	27	129.40	1,697.75
PIO3_17/DP08B	—	—	—	L1	28	231.40	1,662.74

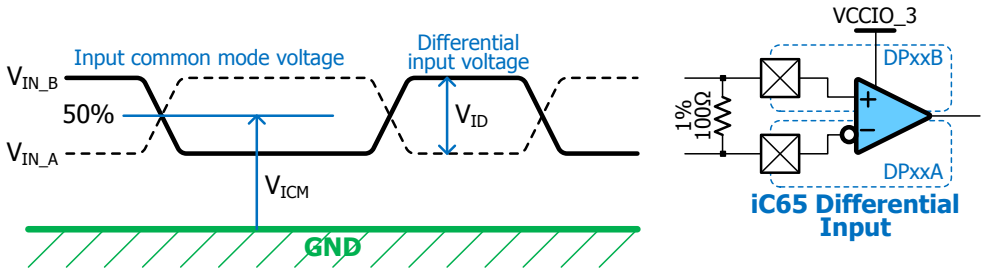
iCE65L04 Pad Name	DiePlus VQ100	CB132	CB196	CB284	Pad	X (µm)	Y (µm)
PIO3_18/DP09A	12	—	G2	L3	29	129.40	1,627.75
GBIN7/PIO3_19/DP09B	13	G1	G1	L5	30	231.40	1,592.74
VCCIO_3	14	J6	J6	N10	31	129.40	1,557.75
VREF	N/A	N/A	N/A	M1	32	231.40	1,522.74
GND	—	—	A9	N1	33	129.40	1,487.75
GBIN6/PIO3_20/DP10A	15	H1	H1	M5	34	231.40	1,452.74
PIO3_21/DP10B	16	—	H2	M3	35	129.40	1,417.75
GND	17	H7	A9	M11	36	231.40	1,382.74
PIO3_22/DP11A	—	—	G3	N3	37	129.40	1,347.75
PIO3_23/DP11B	—	—	G4	P3	38	231.40	1,312.74
VCCIO_3	—	—	K1	R3	39	129.40	1,277.75
VCCIO_3	—	—	—	—	40	231.40	1,242.74
GND	—	—	A9	T3	41	129.40	1,207.75
GND	—	—	—	—	42	231.40	1,172.74
PIO3_24/DP12A	—	—	J1	U3	43	129.40	1,137.75
PIO3_25/DP12B	—	—	J2	V3	44	231.40	1,102.74
GND	—	—	A9	V1	45	129.40	1,067.75
PIO3_26/DP13A	—	—	H4	W3	46	231.40	1,032.74
PIO3_27/DP13B	—	—	H3	Y3	47	129.40	997.75
PIO3_28/DP14A	18	G3	K2	L7	48	231.40	962.74
PIO3_29/DP14B	19	G4	J3	L8	49	129.40	927.75
PIO3_30/DP15A	—	H3	H5	M7	50	231.40	892.74
PIO3_31/DP15B	—	H4	G5	M8	51	129.40	857.75
VCC	—	J4	F2	N8	52	231.40	822.74
PIO3_32/DP16A	20	J3	L1	N7	53	129.40	787.75
PIO3_33/DP16B	21	J1	L2	N5	54	231.40	752.74
VCCIO_3	22	K1	K1	P5	55	129.40	717.75
VCCIO_3	—	—	—	—	56	231.40	682.74
GND	23	L3	L3	R7	57	129.40	637.75
GND	—	—	—	—	58	231.40	592.74
PIO3_34/DP17A	—	K3	M1	P7	59	129.40	547.75
PIO3_35/DP17B	—	K4	M2	P8	60	231.40	502.74
PIO3_36/DP18A	24	L1	K3	R5	61	129.40	457.75
PIO3_37/DP18B	25	M1	K4	T5	62	231.40	412.74
PIO3_38/DP19A	—	N1	N1	U5	63	129.40	367.75
PIO3_39/DP19B	—	P1	N2	V5	64	231.40	322.74
PIO2_00	—	—	—	AB2	65	545.00	139.20
PIO2_01	—	P2	L4	V6	66	595.00	37.20
PIO2_02	—	M3	M3	T7	67	645.00	139.20
GND	—	—	C2	AB5	68	695.00	37.20
PIO2_03	26	L4	P1	R8	69	745.00	139.20
PIO2_04	27	P3	N3	V7	70	795.00	37.20
PIO2_05	28	M4	P2	T8	71	845.00	139.20
PIO2_06	29	L5	L5	R9	72	895.00	37.20
PIO2_07	30	P4	M4	V8	73	930.00	139.20

iCE65L04 Pad Name	DiePlus VQ100	CB132	CB196	CB284	Pad	X (µm)	Y (µm)
PIO1_24	—	—	G11	F20	167	3,712.80	1,812.00
PIO1_25	—	—	F11	E20	168	3,610.80	1,847.00
PIO1_26	—	—	E10	D20	169	3,712.80	1,882.00
PIO1_27	—	—	E14	C20	170	3,610.80	1,917.00
GND	—	G8	G8	L12	171	3,712.80	1,952.00
GND	—	—	—	—	172	3,610.80	1,987.00
PIO1_28	—	—	F12	G22	173	3,712.80	2,022.00
PIO1_29	—	G12	D14	L16	174	3,610.80	2,057.00
PIO1_30	64	G11	E13	L15	175	3,712.80	2,092.00
PIO1_31	65	F12	C14	K16	176	3,610.80	2,127.00
VCC	—	—	K13	L20	177	3,712.80	2,162.00
VCC	—	—	—	—	178	3,610.80	2,197.00
PIO1_32	66	E14	E11	J18	179	3,712.80	2,232.00
PIO1_33	—	F11	C13	K15	180	3,610.80	2,267.00
VCCIO_1	67	F9	F9	K13	181	3,712.80	2,302.00
VCCIO_1	—	—	—	—	182	3,610.80	2,337.00
PIO1_34	68	E12	E12	J16	183	3,712.80	2,377.00
PIO1_35	69	D14	B14	H18	184	3,610.80	2,427.00
GND	70	G9	G9	L13	185	3,712.80	2,477.00
PIO1_36	71	E11	B13	J15	186	3,610.80	2,527.00
PIO1_37	72	D12	D12	H16	187	3,712.80	2,577.00
PIO1_38	73	C14	C12	G18	188	3,610.80	2,627.00
PIO1_39	74	B14	D11	F18	189	3,712.80	2,677.00
VPP_2V5	75	A14	A14	E18	190	3,610.80	2,739.68
VPP_FAST	76	A13	A13	E17	191	3,097.00	2,962.80
VCC	77	F8	F8	K12	192	2,997.00	2,860.80
VCC	77	F8	F8	K12	193	2,947.00	2,962.80
PIO0_00	78	A12	C11	E16	194	2,897.00	2,860.80
PIO0_01	—	C12	—	G16	195	2,847.00	2,962.80
PIO0_02	79	A11	A12	E15	196	2,797.00	2,860.80
PIO0_03	80	C11	B11	G15	197	2,747.00	2,962.80
PIO0_04	—	D11	—	H15	198	2,697.00	2,860.80
PIO0_05	81	A10	D10	E14	199	2,647.00	2,962.80
PIO0_06	82	C10	A11	G14	200	2,612.00	2,860.80
PIO0_07	83	D10	D9	H14	201	2,577.00	2,962.80
GND	84	A9	H6	E13	202	2,542.00	2,860.80
GND	—	—	—	—	203	2,507.00	2,962.80
PIO0_08	85	C9	C10	G13	204	2,472.00	2,860.80
PIO0_09	86	D9	A10	H13	205	2,437.00	2,962.80
PIO0_10	87	C8	B10	G12	206	2,402.00	2,860.80
PIO0_11	—	D8	E9	H12	207	2,367.00	2,962.80
PIO0_12	—	—	—	A18	208	2,332.00	2,860.80
PIO0_13	—	—	—	A17	209	2,297.00	2,962.80
PIO0_14	—	—	—	A16	210	2,262.00	2,860.80
PIO0_15	—	—	—	A15	211	2,227.00	2,962.80
VCCIO_0	88	A8	A8	E12	212	2,192.00	2,860.80
VCCIO_0	—	—	—	—	213	2,157.00	2,962.80

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO2_28	—	Y13	132	2,062.5	139.5
GBIN5/PIO2_29	M7	V11	133	2,097.5	37.5
GBIN4/PIO2_30	N8	V12	134	2,132.5	139.5
GND	J8	Y12	135	2,167.5	37.5
GND	—	—	136	2,202.5	139.5
PIO2_31	P8	Y14	137	2,237.5	37.5
PIO2_32	—	AB15	138	2,272.5	139.5
PIO2_33	M8	V13	139	2,307.5	37.5
PIO2_34	—	AB16	140	2,342.5	139.5
PIO2_35	L8	Y15	141	2,377.5	37.5
PIO2_36	—	AB17	142	2,412.5	139.5
PIO2_37	N9	AB18	143	2,447.5	37.5
PIO2_38	—	AB19	144	2,482.5	139.5
PIO2_39	—	AB20	145	2,517.5	37.5
PIO2_40	—	AB21	146	2,552.5	139.5
PIO2_41	—	Y17	147	2,587.5	37.5
PIO2_42	—	AB22	148	2,622.5	139.5
PIO2_43	—	Y18	149	2,657.5	37.5
PIO2_44	P9	Y19	150	2,692.5	139.5
VCC	N7	N11	151	2,727.5	37.5
VCC	—	—	152	2,762.5	139.5
PIO2_45	M9	Y20	153	2,797.5	37.5
PIO2_46	K8	T11	154	2,832.5	139.5
VCCIO_2	J9	N13	155	2,867.5	37.5
VCCIO_2	—	—	156	2,902.5	139.5
PIO2_47	N11	R11	157	2,937.5	37.5
GND	J8	M12	158	2,972.5	139.5
GND	—	—	159	3,007.5	37.5
PIO2_48	N12	T12	160	3,042.5	139.5
PIO2_49	K9	R12	161	3,077.5	37.5
PIO2_50	N13	T13	162	3,112.5	139.5
PIO2_51/CBSEL0	L9	R13	163	3,147.5	37.5
PIO2_52/CBSEL1	P10	V14	164	3,182.5	139.5
CDONE	M10	T14	165	3,217.5	37.5
CRESET_B	L10	R14	166	3,260.0	139.5
PIOS_00/SPI_SO	M11	T15	167	3,320.0	37.5
PIOS_01/SPI_SI	P11	V15	168	3,370.0	139.5
GND	J8	Y16	169	3,420.0	37.5
GND	—	—	170	3,470.0	139.5
PIOS_02/SPI_SCK	P12	V16	171	3,520.0	37.5
PIOS_03/SPI_SS_B	P13	V17	172	3,570.0	139.5
VCC	—	—	173	3,620.0	37.5
VCC	—	—	174	3,670.0	139.5
SPI_VCC	L11	R15	175	3,720.0	37.5
SPI_VCC	—	—	176	3,770.0	139.5

Differential Inputs

Figure 50: Differential Input Specifications



Input common mode voltage: $$V_{ICM} = \frac{VCCIO\_3}{2} \pm \Delta V_{ICM}$$

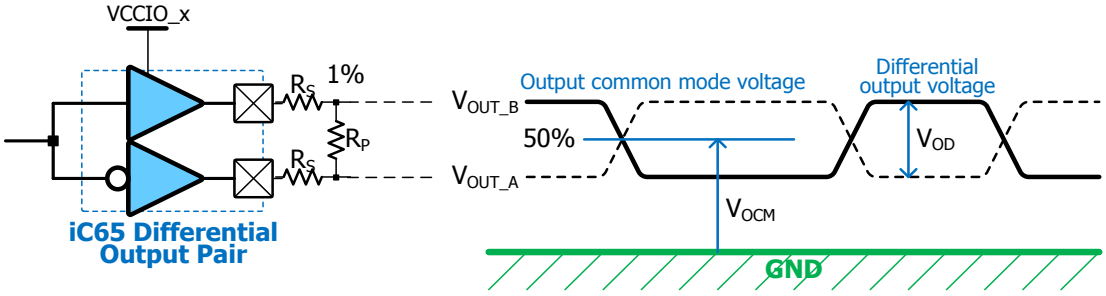
Differential input voltage: $$V_{ID} = |V_{IN\_B} - V_{IN\_A}|$$

Table 52: **Recommended Operating Conditions for Differential Inputs**

I/O Standard	VCCIO_3 (V)			V_{ID} (mV)			V_{ICM} (V)		
	Min	**Nom**	**Max**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
LVDS	2.38	2.50	2.63	250	350	450	$\frac{VCCIO\_3}{2} - 0.30$	$\frac{VCCIO\_3}{2}$	$\frac{VCCIO\_3}{2} + 0.30$
SubLVDS	1.71	1.80	1.89	100	150	200	$\frac{VCCIO\_3}{2} - 0.25$	$\frac{VCCIO\_3}{2}$	$\frac{VCCIO\_3}{2} + 0.25$

Differential Outputs

Figure 51: Differential Output Specifications



Output common mode voltage: $$V_{OCM} = \frac{VCCIO\_x}{2} \pm \Delta V_{OCM}$$

Differential output voltage: $$V_{OD} = |V_{OUT\_B} - V_{OUT\_A}|$$

Table 53: **Recommended Operating Conditions for Differential Outputs**

I/O Standard	VCCIO_x (V)			Ω		V_{OD} (mV)			V_{OCM} (V)		
	Min	**Nom**	**Max**	**R_S**	**R_P**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
LVDS	2.38	2.50	2.63	150	140	300	350	400	$\frac{VCCIO}{2} - 0.15$	$\frac{VCCIO}{2}$	$\frac{VCCIO}{2} + 0.15$
SubLVDS	1.71	1.80	1.89	270	120	100	150	200	$\frac{VCCIO}{2} - 0.10$	$\frac{VCCIO}{2}$	$\frac{VCCIO}{2} + 0.10$

Programmable Input/Output (PIO) Block

Table 55 provides timing information for the logic in a Programmable Logic Block (PLB), which includes the paths shown in Figure 57 and Figure 58. The timing shown is for the LVCMOS25 I/O standard in all I/O banks. The iCEcube development software reports timing adjustments for other I/O standards.

Figure 57: **Programmable I/O (PIO) Pad-to-Pad Timing Circuit**

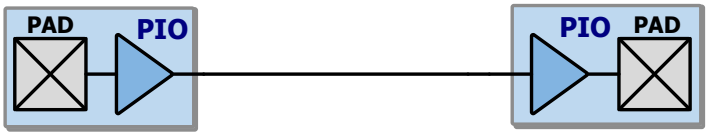


Figure 58: **Programmable I/O (PIO) Sequential Timing Circuit**

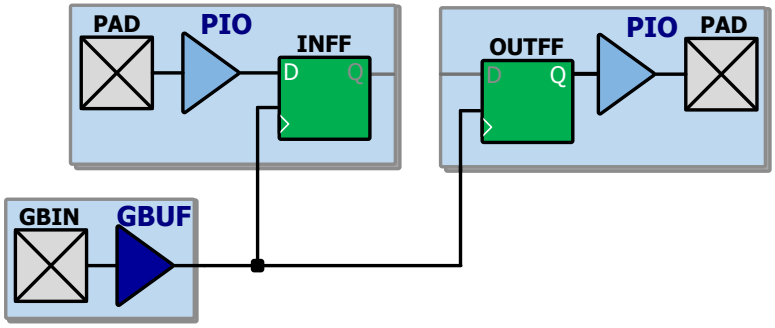


Table 55: **Typical Programmable Input/Output (PIO) Timing (LVCMOS25)**

Symbol	From	To	Device: iCE65	L01	L04, L08			Units
			Power/Speed Grad	–T	–L		–T	
			Nominal VCC	1.2 V	1.0 V	1.2 V	1.2 V	
			Description	Typ.	Typ.	Typ.	Typ.	
		Synchronous Output Paths						
t_{OCKO}	OUTFF clock input	PIO output	Delay from clock input on OUTFF output flip-flop to PIO output pad.	4.7	13.8	7.3	5.6	ns
t_{GBCKIO}	GBIN input	OUTFF clock input	Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to clock input on the PIO OUTFF output flip-flop.	2.1	7.3	3.8	2.6	ns
		Synchronous Input Paths						
t_{SUPDIN}	PIO input	GBIN input	Setup time on PIO input pin to INFF input flip-flop before active clock edge on GBIN input, including interconnect delay.	0	0	0	0	ns
t_{HDPDIN}	GBIN input	PIO input	Hold time on PIO input to INFF input flip-flop after active clock edge on the GBIN input, including interconnect delay.	2.7	7.1	3.6	2.8	ns
		Pad to Pad						
t_{PADIN}	PIO input	Inter-connect	Asynchronous delay from PIO input pad to adjacent interconnect.	2.5	9.5	5.0	3.2	ns
t_{PADO}	Inter-connect	PIO output	Asynchronous delay from adjacent interconnect to PIO output pad including interconnect delay.	4.5	14.6	7.7	6.2	ns

		minimum temperature to –40°C in Figure 2 and Table 48. Added NVCM programming temperature to Table 48.
1.3	17-DEC-2008	Added footprint and pinout information for the CS110 Wafer-Level Chip-Scale Ball Grid Array. Clarified that the CB196 footprint shown is for the iCE65L04; the iCE65L08 footprint for the CB196 package is similar but different. Added updated information on Differential Inputs and Outputs, including support for SubLVDS. Updated Electrical Characteristics and AC Timing Guidelines sections. Added support for the LVCMOS15 I/O standard. Corrected the diagram showing the direct differential clock input, Figure 16. Updated the number of I/Os by package in Table 34. Updated company address. Other minor updates throughout.
1.2	11-OCT-2008	Updated I/O Bank 3 characteristics in Table 7 and Table 51. Corrected label in Figure 14. Added JTAG configuration to Table 20. Added pull-up resistor information in Table 22 and Figure 21. Added "Internal Device Reset" section. Updated internal oscillator performance in and Table 57. Updated configuration timing in Table 58 based on new oscillator timing. Completely reorganized the "Package and Pinout Information" section. Added information on CS63 and CB196 packages. Updated information on VPP_2V5 signal in Table 36. Reduced package height for CB132 and CB284 packages to 1.0 mm. Added "Differential Inputs" and "Differential Outputs" sections.
1.1	4-SEPT-2008	Updated package roadmap (Table 2) and updated ordering codes (Figure 2). Updated Figure 7. Updated Figure 24. Added CS63 package footprint (Figure 36), pinout (Table 39) and Package.
1.0	31-MAY-2008	Initial public release.

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