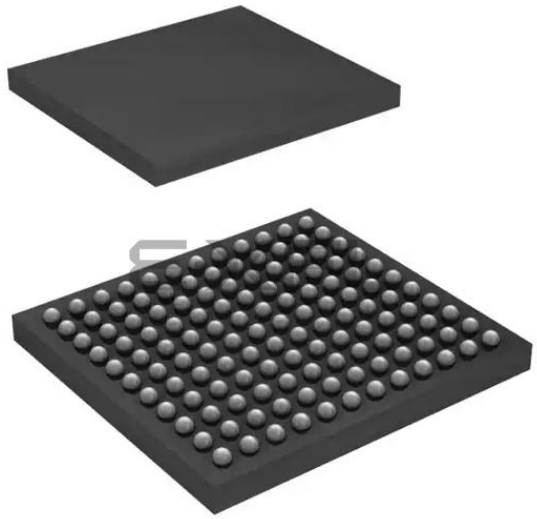
Lattice Semiconductor Corporation - ICE65L01F-TCB132C Datasheet



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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	160
Number of Logic Elements/Cells	1280
Total RAM Bits	65536
Number of I/O	93
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	132-VFBGA, CSPBGA
Supplier Device Package	132-CSBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice65l01f-tcb132c

Look-Up Table (LUT4)

The four-input Look-Up Table (LUT4) function implements any and all combinational logic functions, regardless of complexity, of between zero and four inputs. Zero-input functions include "High" (1) and "Low" (0). The LUT4 function has four inputs, labeled I0, I1, I2, and I3. Three of the four inputs are shared with the Carry Logic function, as shown in Figure 4. The bottom-most LUT4 input connects either to the I3 input or to the Carry Logic output from the previous Logic Cell.

The output from the LUT4 function connects to the flip-flop within the same Logic Cell. The LUT4 output or the flip-flop output then connects to the programmable interconnect.

For detailed LUT4 internal timing, see Table 54.

'D'-style Flip-Flop (DFF)

The 'D'-style flip-flop (DFF) optionally stores state information for the application.

The flip-flop has a data input, 'D', and a data output, 'Q'. Additionally, each flip-flop has up to three control signals that are shared among all flip-flops in all Logic Cells within the PLB, as shown in Figure 4. Table 3 describes the behavior of the flip-flop based on inputs and upon the specific DFF design primitive used or synthesized.

Table 3: 'D'-Style Flip-Flop Behavior

DFF Primitive	Operation	Flip-Flop Mode	Inputs				Output
			D	EN	SR	CLK	Q
All	Cleared Immediately after Configuration	X	X	X	X	X	0
	Hold Present Value (Disabled)		X	0	X	X	Q
	Hold Present Value (Static Clock)		X	X	X	1 or 0	Q
	Load with Input Data		D	1*	0*	↑	D
SB_DFFR	Asynchronous Reset	Asynchronous Reset	X	X	1	X	0
SB_DFFS	Asynchronous Set	Asynchronous Set	X	X	1	X	1
SB_DFFSR	Synchronous Reset	Synchronous Reset	X	1*	1	↑	0
SB_DFFSS	Synchronous Set	Synchronous Set	X	1*	1	↑	1

X = don't care, ↑ = rising clock edge (default polarity), 1* = High or unused, 0* = Low or unused

The CLK clock signal is not optional and is shared among all flip-flops in a Programmable Logic Block. By default, flip-flops are clocked by the rising edge of the PLB clock input, although the clock polarity can be inverted for all the flip-flops in the PLB.

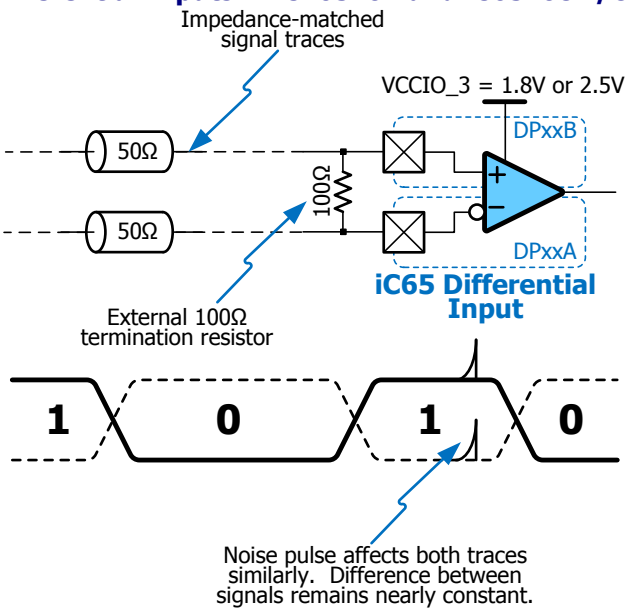
The CLK input optionally connects to one of the following clock sources.

- The output from any one of the eight Global Buffers, or
- A connection from the general-purpose interconnect fabric

The EN clock-enable signal is common to all Logic Cells in a Programmable Logic Block. If the enable signal is not used, then the flip-flop is always enabled. This condition is indicated as "1*" in Table 3. The asterisk indicates that this is the default state if the control signal is not connected in the application.

Similarly, the SR set/reset signal is common to all Logic Cells in a Programmable Logic Block. If not used, then the flip-flop is never set/reset, except when cleared immediately after configuration or by the Global Reset signal. This condition is indicated as "0*" in Table 3. The asterisk indicates that this is the default state if the control signal is not connected in the application.

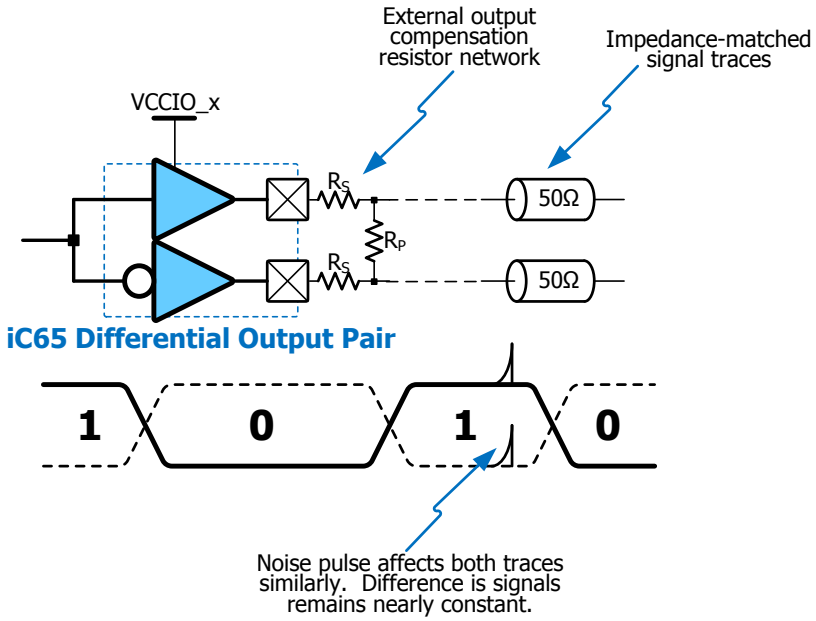
Figure 8: **Differential Inputs in iCE65L04 and iC65L08 I/O Bank 3**



Differential Outputs in Any Bank

Differential outputs are built using a pair of single-ended PIO pins as shown in Figure 9. Each differential I/O pair requires a three-resistor termination network to adjust output characteristic to match those for the specific differential I/O standard. The output characteristics depend on the values of the parallel resistors (RP) and series resistor (RS). Differential outputs must be located in the same I/O tile.

Figure 9: Differential Output Pair



For electrical characteristics, see "Differential Outputs" on page 100.

The PIO pins that make up a differential output pair are indicated with a blue bounding box in the in the tables in "Die Cross Reference" starting on page 84.

For best possible performance, the global buffer inputs (GBIN[7:0]) connect directly to the their associated global buffers (GBUF[7:0]), bypassing the PIO logic and iCEgate circuitry as shown in Figure 7. Consequently, the direct GBIN-to-GBUF connection cannot be blocked by the iCEgate circuitry. However, it is possible to use iCEgate to block PIO-to-GBUF clock connections.

For additional information on using the iCEgate feature, please refer to the following application note.

AN002: Using iCEgate Blocking for Ultra-Low Power

Input Pull-Up Resistors on I/O Banks 0, 1, and 2

The PIO pins in I/O Banks 0, 1, and 2 have an optional input pull-up resistor. Pull-up resistors are not provided in iCE65L04 and iCE65L08 I/O Bank 3. During the iCE65 configuration process, the input pull-up resistor is unconditionally enabled and pulls the input to within a diode drop of the associated I/O bank supply voltage (VCCIO_#). This prevents any signals from floating on the circuit board during configuration.

After iCE65 configuration is complete, the input pull-up resistor is optional, defined by a configuration bit. The pull-up resistor is also useful to tie off unused PIO pins. The Lattice iCEcube development software defines all unused PIO pins in I/O Banks 0, 1 and 2 as inputs with the pull-up resistor turned on. The pull-up resistor value depends on the VCCIO voltage applied to the bank, as shown in Table 49.

Note: JTAG inputs TCK, TDI and TMS do not have the input pull-up resistor and must be tied off to GND when unused, else VCCIO_1 draws current.

No Input Pull-up Resistors on I/O Bank 3 of iCE65L04 and iCE65L08

The PIO pins in I/O Bank 3 do not have an internal pull-up resistor. To minimize power consumption, tie unused PIO pins in Bank 3 to a known logic level or drive them as a disabled high-impedance output.

Input Hysteresis

Inputs typically have about 50 mV of hysteresis, as indicated in Table 49.

Output and Output Enable Signal Path

As shown in Figure 7, a signal from programmable interconnect feeds the OUT signal on a Programmable I/O pad. This output connects either directly to the associated package pin or is held in an optional output flip-flop. Because all flip-flops are automatically reset after configuration, the output from the output flip-flop can be optionally inverted so that an active-Low output signal is held in the disabled (High) state immediately after configuration.

Similarly, each Programmable I/O pin has an output enable or three-state control called OE. When OE = High, the OUT output signal drives the associated pad, as described in Table 10. When OE = Low, the output driver is in the high-impedance (Hi-Z) state. The OE output enable control signal itself connects either directly to the output buffer or is held in an optional register. The output buffer is optionally permanently enabled or permanently disabled, either to unconditionally drive output signals, or to allow input-only signals.

Table 10: **PIO Output Operations (non-registered operation, no inversions)**

Operation	OUT Data Output	OE Enable	PAD
Three-State	X	0	Hi-Z
Drive Output Data	OUT	1*	OUT

X = don't care, 1* = High or unused, Hi-Z = high-impedance, three-stated, floating.

See Input and Output Register Control per PIO Pair for information about the registered input path.

Table 12 and Table 13 list the connections between a specific global buffer and the inputs on a Programmable I/O (PIO) pair. Although there is no direct connection between a global buffer and a PIO output, such a connection is possible by first connecting through a PLB LUT4 function. Again, all global buffers optionally drive all clock inputs. However, even-numbered global buffers optionally drive the clock-enable input on a PIO pair.

The PIO clock enable connect is different between the iCE65L01/iCE65L04 and iCE65L08.

Table 12: **iCE65L01 & iCE65L04: Global Buffer (GBUF) Connections to Programmable I/O (PIO) Pair**

Global Buffer	Output Connections	Input Clock	Output Clock	Clock Enable
GBUF0	No (connect through PLB LUT)	Yes	Yes	No
GBUF1		Yes	Yes	Yes
GBUF2		Yes	Yes	No
GBUF3		Yes	Yes	Yes
GBUF4		Yes	Yes	No
GBUF5		Yes	Yes	Yes
GBUF6		Yes	Yes	No
GBUF7		Yes	Yes	Yes

Table 13: **iCE64L08: Global Buffer (GBUF) Connections to Programmable I/O (PIO) Pair**

Global Buffer	Output Connections	Input Clock	Output Clock	Clock Enable
GBUF0	No (connect through PLB LUT)	Yes	Yes	Yes
GBUF1		Yes	Yes	No
GBUF2		Yes	Yes	Yes
GBUF3		Yes	Yes	No
GBUF4		Yes	Yes	Yes
GBUF5		Yes	Yes	No
GBUF6		Yes	Yes	Yes
GBUF7		Yes	Yes	No

Global Buffer Inputs

The iCE65 component has eight specialized GBIN/PIO pins that are optionally direct inputs to the global buffers, offering the best overall clock characteristics. As shown in Figure 15, each GBIN/PIO pin is a full-featured I/O pin but also provides a direct connection to its associated global buffer. The direct connection to the global buffer bypasses the iCEgate input-blocking latch and other PIO input logic. These special PIO pins are allocated two to an I/O Bank, a total of eight. These pins are labeled GBIN0 through GBIN7, as shown in Figure 14 and the pin locations for each GBIN input appear in Table 14.

Table 14: **Global Buffer Input Ball/Pin Number by Package**

Global Buffer Input (GBIN)	I/O Bank	VQ100	CB132	'L04 CB196	'L08 CB196	CB284
GBIN0	0	90	A6	A7	A7	E10
GBIN1		89	A7	E7	E7	E11
GBIN2	1	63	G14	F10	F10	L18
GBIN3		62	F14	G12	G12	K18
GBIN4	2	34	P8	L7	N8	V12
GBIN5		33	P7	P5	M7	V11
GBIN6	3	15	H1	H1	H1	M5
GBIN7		13	G1	G1	H3	L5

- Register file and scratchpad RAM
- First-In, First-Out (FIFO) memory for data buffering applications
- Circuit buffer
- A 256-deep by 16-wide ROM with registered outputs, contents loaded during configuration
  - Sixteen different 8-input look-up tables
  - Function or waveform tables such as sine, cosine, etc.
  - Correlators or pattern matching operations
- Counters, sequencers

As pictured in Figure 17, a RAM4K block has separate write and read ports, each with independent control signals. Table 17 lists the signals for both ports. Additionally, the write port has an active-Low bit-line write-enable control; optionally mask write operations on individual bits. By default, input and output data is 16 bits wide, although the data width is configurable using programmable logic and, if needed, multiple RAM4K blocks.

The WCLK and RCLK inputs optionally connect to one of the following clock sources.

- The output from any one of the eight Global Buffers, or
- A connection from the general-purpose interconnect fabric

The data contents of the RAM4K block are optionally pre-loaded during iCE65 device configuration. If the RAM4K blocks are not pre-loaded during configuration, then the resulting configuration bitstream image is smaller. However, if an uninitialized RAM4K block is used in the application, then the application must initialize the RAM contents to guarantee the data value.

See Table 56 for detailed timing information.

Signals

Table 17 lists the signal names, direction, and function of each connection to the RAM4K block. See also Figure 17.

Table 17: RAM4K Block RAM Signals

Signal Name	Direction	Description
WDATA[15:0]	Input	Write Data input.
MASK[15:0]	Input	Masks write operations for individual data bit-lines. 0 = Write bit; 1 = Don't write bit
WADDR[7:0]	Input	Write Address input. Selects one of 256 possible RAM locations.
WE	Input	Write Enable input.
WCLKE	Input	Write Clock Enable input.
WCLK	Input	Write Clock input. Default rising-edge, but with falling-edge option.
RDATA[15:0]	Output	Read Data output.
RADDR[7:0]	Input	Read Address input. Selects one of 256 possible RAM locations.
RE	Input	Read Enable input.
RCLKE	Input	Read Clock Enable input.
RCLK	Input	Read Clock input. Default rising-edge, but with falling-edge option.

Write Operations

Figure 18 shows the logic involved in writing a data bit to a RAM location. Table 18 describes various write operations for a RAM4K block. By default, all RAM4K write operations are synchronized to the rising edge of WCLK although the clock is invertible as shown in Figure 18.

Figure 19: RAM4K Read Logic

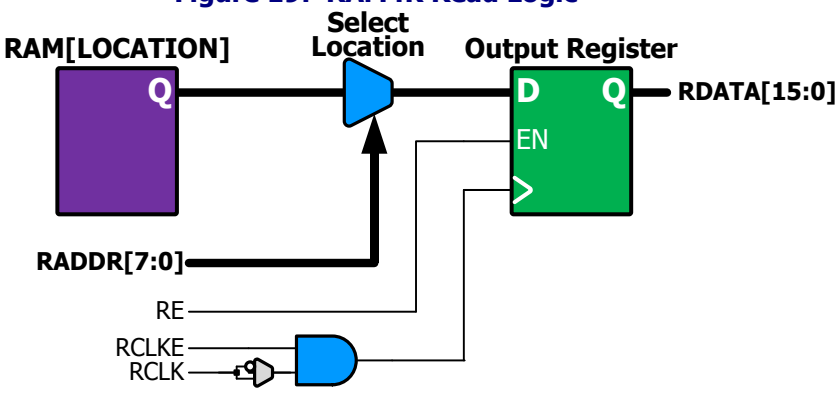


Table 19: RAM4K Read Operations

Operation	RADDR[7:0] Address	RE Read Enable	RCLKE Clock Enabe	RCLK Clock	RDATA[15:0]
After configuration, before first valid Read Data operation	X	X	X	X	Undefined
Disabled	X	X	X	0	No Change
Disabled		X	0	X	No Change
Disabled	X	0	X	X	No change
Read Data	RADDR	1	1	↑	RAM[RADDR]

To read data from the RAM4K block, perform the following operations.

- Supply a valid address on the RADDR[7:0] address input port
- Enable the RAM4K read port (RE = 1)
- Enable the RAM4K read clock (RCLKE = 1)
- Apply a rising clock edge on RCLK
- After the clock edge, the RAM contents located at the specified address (RADDR) appear on the RDATA output port

Read Data Register Undefined Immediately after Configuration

Unlike the flip-flops in the Programmable Logic Blocks and Programmable I/O pins, the RDATA[15:0] read data output register is not automatically reset after configuration. Consequently, immediately following configuration and before the first valid Read Data operation, the initial RDATA[15:0] read value is undefined.

Pre-loading RAM Data

The data contents for a RAM4K block can be optionally pre-loaded during iCE65 configuration. If not pre-loaded during configuration, then the RAM contents must be initialized by the iCE65 application before the RAM contents are valid.

Pre-loading the RAM data in the configuration bitstream increases the size of the configuration image accordingly.

RAM Contents Preserved during Configuration

RAM contents are preserved (write protected) during configuration, assuming that voltage supplies are maintained throughout. Consequently, data can be passed between multiple iCE65 configurations by leaving it in a RAM4K block and then skipping pre-loading during the subsequent reconfiguration. See "Cold Boot Configuration Option" and "Warm Boot Configuration Option" for more information.

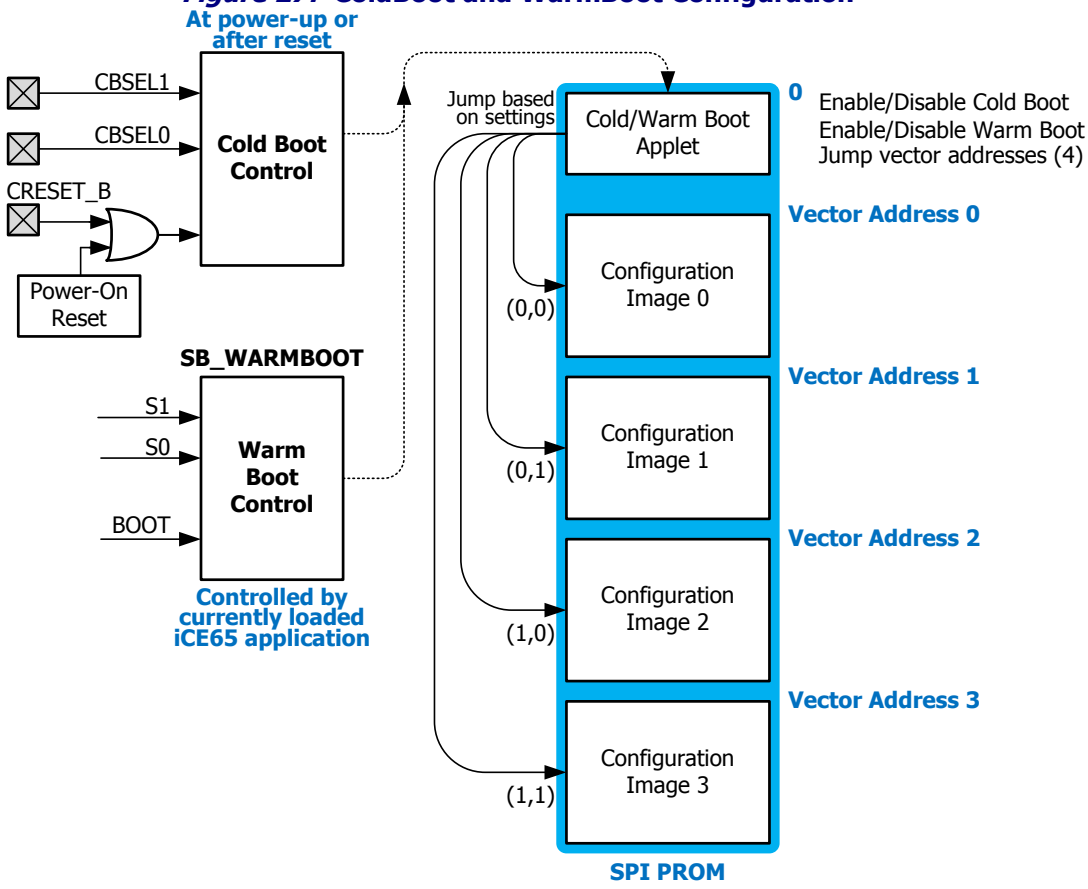
Low-Power Setting

To place a RAM4K block in its lowest power mode, keep WCLKE = 0 and RCLKE = 0. In other words, when not actively using a RAM4K block, disable the clock inputs.

Cold Boot Configuration Option

By default, the iCE65 FPGA is programmed with a single configuration image, either from internal NVCM memory, from an external SPI Flash PROM, or externally from a processor or microcontroller.

Figure 27: **ColdBoot and WarmBoot Configuration**



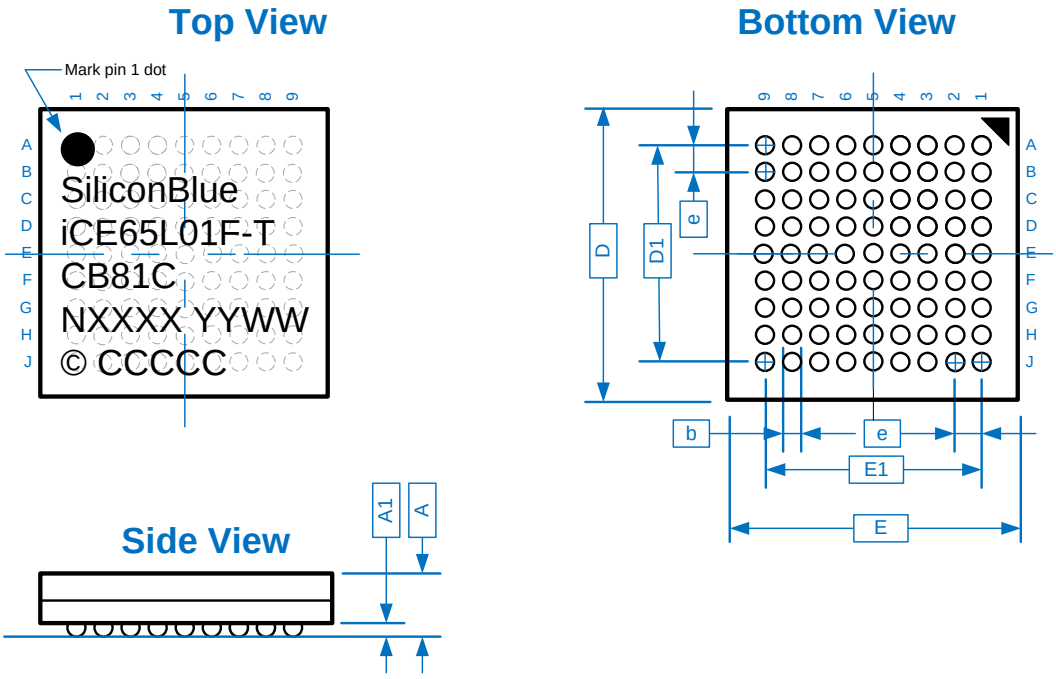
When self loading from NVCM or from an SPI Flash PROM, there is an additional configuration option called Cold Boot mode. When this option is enabled in the configuration bitstream, the iCE65 FPGA boots normally from power-on or a master reset (CRESET_B = Low pulse), but monitors the value on two PIO pins that are borrowed during configuration, as shown in Figure 27. These pins, labeled PIO2/CBSEL0 and PIO2/CBSEL1, tell the FPGA which of the four possible SPI configurations to load into the device. Table 30 provides the pin or ball locations for these pins.

- Load from initial location, either from NVCM or from address 0 in SPI Flash PROM. For Cold Boot or Warm Boot applications, the initial configuration image contains the cold boot/warm boot applet.
- Check if Cold Boot configuration feature is enabled in the bitstream.
  - If not enabled, FPGA configures normally.
  - If Cold Boot is enabled, then the FPGA reads the logic values on pins CBSEL[1:0]. The FPGA uses the value as a vector and then reads from the indicated vector address.
  - At the selected CBSEL[1:0] vector address, there is a starting address for the selected configuration image.
    - For SPI Flash PROMs, the new address is a 24-bit start address in Flash.
    - If the selected bitstream is in NVCM, then the address points to the internal NVCM.
- Using the new start address, the FPGA restarts reading configuration memory from the new location.

Ball Function	Ball Number	Pin Type	Bank
PIO3	B1	PIO	3
PIO3	B2	PIO	3
PIO3	B3	PIO	3
PIO3	C1	PIO	3
PIO3	C2	PIO	3
PIO3	C3	PIO	3
GBIN7/PIO3	D1	GBIN	3
PIO3	D2	PIO	3
PIO3	D3	PIO	3
GBIN6/PIO3	E1	GBIN	3
PIO3	E2	PIO	3
PIO3	E3	PIO	3
PIO3	F2	PIO	3
PIO3	F3	PIO	3
PIO3	G1	PIO	3
PIO3	G2	PIO	3
PIO3	H1	PIO	3
PIO3	H2	PIO	3
VCCIO_3	F1	VCCIO	3
PIOS/SPI_SO	H7	SPI	SPI
PIOS/SPI_SI	J7	SPI	SPI
PIOS/SPI_SCK	J8	SPI	SPI
PIOS/SPI_SS_B	H8	SPI	SPI
SPI_VCC	H9	SPI	SPI
GND	A1	GND	GND
GND	A9	GND	GND
GND	J9	GND	GND
GND	J1	GND	GND
GND	E4	GND	GND
GND	E5	GND	GND
GND	F4	GND	GND
GND	F5	GND	GND
VCC	A5	VCC	VCC
VCC	J5	VCC	VCC
VPP_2V5	B9	VPP	VPP

***Figure 33:* CB81 Package Mechanical Drawing**

CB81: 5 x 5 mm, 81-ball, 0.5 mm ball-pitch, chip-scale ball grid array



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			9		Columns
Number of Ball Rows	Y			9		Rows
Number of Signal Balls		n		81		Balls
Body Size	X	E	4.90	5.00	5.10	mm
	Y	D	4.90	5.00	5.10	
Ball Pitch		e	—	0.50	—	
Ball Diameter		b	0.2	—	0.3	
Edge Ball Center to Center	X	E1	—	4.00	—	
	Y	D1	—	4.00	—	
Package Height		A	—	—	1.00	
Stand Off		A1	0.15	—	0.25	

Top Marking Format

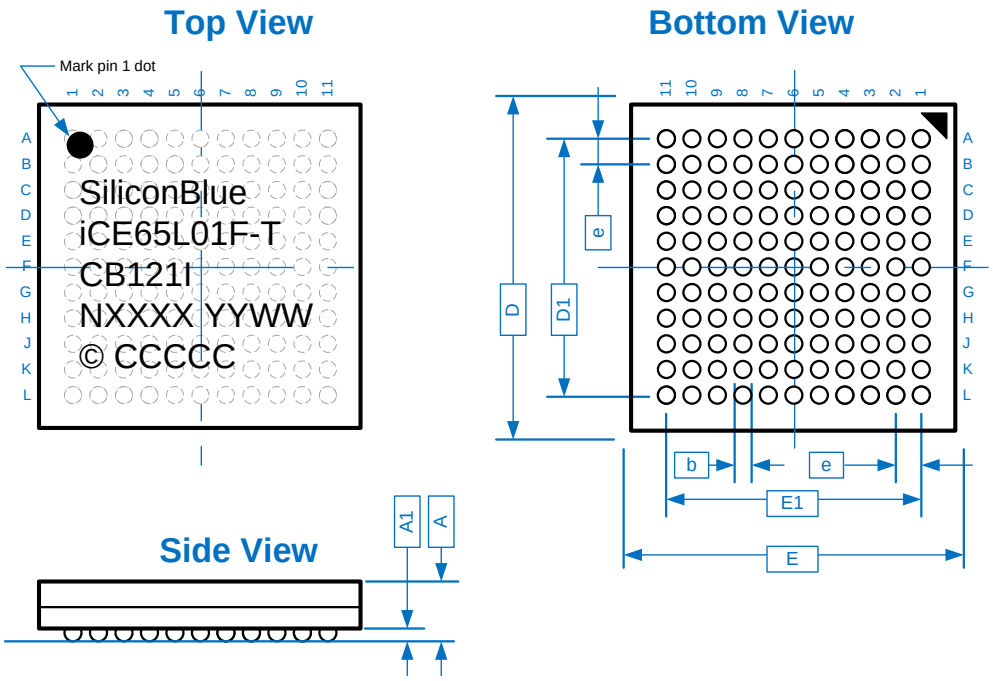
Line	Content	Description
1	Logo	Logo
2	iCE65P01F	Part number
	-T	Power/Speed
3	CB81C	Package type
	ENG	Engineering
4	NXXXX	Lot Number
5	YYWW	Date Code
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
67	57

***Figure 40:* CB121 Package Mechanical Drawing**

CB121: 6 x 6 mm, 121-ball, 0.5 mm ball-pitch, fully-populated, chip-scale ball grid array



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			11		Columns
Number of Ball Rows	Y			11		Rows
Number of Signal Balls		n		121		Balls
Body Size	X	E	5.90	6.00	6.10	mm
	Y	D	5.90	6.00	6.10	
Ball Pitch		e	—	0.50	—	
Ball Diameter		b	0.2	—	0.3	
Edge Ball Center to Center	X	E1	—	5.00	—	
	Y	D1	—	5.00	—	
Package Height		A	—	—	1.00	
Stand Off		A1	0.12	—	0.20	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65L01F	Part number
	-T	Power/Speed
3	CB121I	Package type
	ENG	Engineering
4	NXXXX	Lot Number
5	YYWW	Date Code
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
64	55

Ball Function	Ball Number	Pin Type	Bank
PIO3/DP13A	H5	DPIO	3
PIO3/DP13B	G5	DPIO	3
PIO3/DP14A	L1	DPIO	3
PIO3/DP14B	L2	DPIO	3
PIO3/DP15A	M1	DPIO	3
PIO3/DP15B	M2	DPIO	3
PIO3/DP16A (◆)	***iCE65L04:*** K3 ***iCE65L08:*** K4	DPIO	3
PIO3/DP16B (◆)	***iCE65L08:*** K4 ***iCE65L08:*** K3	DPIO	3
PIO3/DP17A	N1	DPIO	3
PIO3/DP17B	N2	DPIO	3
VCCIO_3	E3	VCCIO	3
VCCIO_3	J6	VCCIO	3
VCCIO_3	K1	VCCIO	3
PIOS/SPI_SO	M11	SPI	SPI
PIOS/SPI_SI	P11	SPI	SPI
PIOS/SPI_SCK	P12	SPI	SPI
PIOS/SPI_SS_B	P13	SPI	SPI
SPI_VCC	L11	SPI	SPI
GND	A9	GND	GND
GND	B12	GND	GND
GND	C2	GND	GND
GND	F1	GND	GND
GND	F7	GND	GND
GND	G7	GND	GND
GND	G8	GND	GND
GND	G9	GND	GND
GND	H6	GND	GND
GND	H7	GND	GND
GND	H8	GND	GND
GND	J5	GND	GND
GND	J8	GND	GND
GND	J14	GND	GND
GND	K10	GND	GND
GND	L3	GND	GND
GND	P6	GND	GND
VCC	B7	VCC	VCC
VCC	F2	VCC	VCC
VCC	F8	VCC	VCC
VCC	G6	VCC	VCC
VCC	H9	VCC	VCC
VCC	J4	VCC	VCC
VCC	J7	VCC	VCC
VCC	K13	VCC	VCC
VCC	N7	VCC	VCC
VPP_2V5	A14	VPP	VPP
VPP_FAST	A13	VPP	VPP

Pinout Differences between iCE65L04 and iCE65L08 in CB196 Package

Table 43 lists the package balls that are different between the pinouts for iCE65L04 and the iCE65L08 in the CB196 package. The table also describes the functional differences between these pins, which is critical when designing a CB196 footprint that supports both the iCE65L04 and the iCE65L08 devices. In some cases, only the differential inputs are swapped; single-ended I/Os are not affected. A swapped differential pair can be inverted internally for functional equivalence. In other cases, a global buffer input is swapped with another PIO pin in the same bank.

***Table 43:* Pinout Differences between iCE65L04 and iCE65L08 in CB196 Package**

Ball Number	iCE65L04	iCE65L08	Functional Difference
E1	PIO3/DP03A	PIO3/DP03B	Differential inputs swapped, single-ended I/Os not affected
E2	PIO3/DP03B	PIO3/DP03A	
F3	PIO3/DP05A	PIO3/DP05B	Differential inputs swapped, single-ended I/Os not affected
F4	PIO3/DP05B	PIO3/DP05A	
G1	GBIN7/PIO3/DP07B	PIO3/DP11A	Global buffer input GBIN7 and its associated differential input is swapped with another differential pair in I/O Bank 3
G2	PIO3/DP07A	PIO3/DP11B	
H3	PIO3/DP11B	GBIN7/PIO3/DP07B	
H4	PIO3/DP11A	PIO3/DP07A	
K3	PIO3/DP16A	PIO3/DP16B	Differential inputs swapped, single-ended I/Os not affected
K4	PIO3/DP16B	PIO3/DP16A	
L7	GBIN4/PIO2	PIO2	Global buffer input GBIN4 swapped with another PIO pin in I/O Bank 2
N8	PIO2	GBIN4/PIO2	
M7	PIO2	GBIN5/PIO2	Global buffer input GBIN5 swapped with another PIO pin in I/O Bank 2
P5	GBIN5/PIO2	PIO2	

Ball Function	Ball Number iCE65L04 iCE65L08	Pin Type by Device iCE65L04	Pin Type by Device iCE65L08	Bank	CB132 Ball Equivalent
PIO0	E15	PIO	PIO	0	A11
PIO0	E16	PIO	PIO	0	A12
PIO0	G8	PIO	PIO	0	C4
PIO0	G9	PIO	PIO	0	C5
PIO0	G10	PIO	PIO	0	C6
PIO0	G11	PIO	PIO	0	C7
PIO0	G12	PIO	PIO	0	C8
PIO0	G13	PIO	PIO	0	C9
PIO0	G14	PIO	PIO	0	C10
PIO0	G15	PIO	PIO	0	C11
PIO0	G16	PIO	PIO	0	C12
PIO0	H9	PIO	PIO	0	D5
PIO0	H10	PIO	PIO	0	D6
PIO0	H11	PIO	PIO	0	D7
PIO0	H12	PIO	PIO	0	D8
PIO0	H13	PIO	PIO	0	D9
PIO0	H14	PIO	PIO	0	D10
PIO0	H15	PIO	PIO	0	D11
VCCIO_0	A8	VCCIO	VCCIO	0	—
VCCIO_0	A21	VCCIO	VCCIO	0	—
VCCIO_0	E12	VCCIO	VCCIO	0	A8
VCCIO_0	K10	VCCIO	VCCIO	0	F6
GBIN2/PIO1	L18	GBIN	GBIN	1	G14
GBIN3/PIO1	K18	GBIN	GBIN	1	F14
PIO1 (●)	A22	N.C.	PIO	1	—
PIO1 (●)	AA22	N.C.	PIO	1	—
PIO1 (●)	B22	N.C.	PIO	1	—
PIO1	C20	PIO	PIO	1	—
PIO1 (●)	C22	N.C.	PIO	1	—
PIO1	D20	PIO	PIO	1	—
PIO1 (●)	D22	N.C.	PIO	1	—
PIO1	E20	PIO	PIO	1	—
PIO1 (●)	E22	N.C.	PIO	1	—
PIO1	F18	PIO	PIO	1	B14
PIO1	F20	PIO	PIO	1	—
PIO1 (●)	F22	N.C.	PIO	1	—
PIO1	G18	PIO	PIO	1	C14
PIO1	G20	PIO	PIO	1	—
PIO1	G22	PIO	PIO	1	—
PIO1	H16	PIO	PIO	1	D12
PIO1	H18	PIO	PIO	1	D14
PIO1	H20	PIO	PIO	1	—
PIO1	J15	PIO	PIO	1	E11
PIO1	J16	PIO	PIO	1	E12
PIO1	J18	PIO	PIO	1	E14
PIO1 (●)	J22	N.C.	PIO	1	—
PIO1	K15	PIO	PIO	1	F11
PIO1	K16	PIO	PIO	1	F12
PIO1	K20	PIO	PIO	1	—
PIO1 (●)	K22	N.C.	PIO	1	—

Ball Function	Ball Number iCE65L04 iCE65L08	Pin Type by Device iCE65L04	Pin Type by Device iCE65L08	Bank	CB132 Ball Equivalent
PIO2	T13	PIO	PIO	2	M9
PIO2	V6	PIO	PIO	2	P2
PIO2	V7	PIO	PIO	2	P3
PIO2	V8	PIO	PIO	2	P4
PIO2	V9	PIO	PIO	2	P5
PIO2	V13	PIO	PIO	2	P9
PIO2	Y4	PIO	PIO	2	—
PIO2	Y5	PIO	PIO	2	—
PIO2	Y6	PIO	PIO	2	—
PIO2	Y7	PIO	PIO	2	—
PIO2	Y9	PIO	PIO	2	—
PIO2	Y10	PIO	PIO	2	—
PIO2	Y13	PIO	PIO	2	—
PIO2	Y14	PIO	PIO	2	—
PIO2	Y15	PIO	PIO	2	—
PIO2	Y17	PIO	PIO	2	—
PIO2	Y18	PIO	PIO	2	—
PIO2	Y19	PIO	PIO	2	—
PIO2	Y20	PIO	PIO	2	—
PIO2	AB2	PIO	PIO	2	—
PIO2 (●)	AB3	N.C.	PIO	2	—
PIO2 (●)	AB4	N.C.	PIO	2	—
PIO2	AB6	PIO	PIO	2	—
PIO2	AB7	PIO	PIO	2	—
PIO2	AB8	PIO	PIO	2	—
PIO2	AB9	PIO	PIO	2	—
PIO2	AB10	PIO	PIO	2	—
PIO2	AB11	PIO	PIO	2	—
PIO2	AB12	PIO	PIO	2	—
PIO2	AB13	PIO	PIO	2	—
PIO2	AB14	PIO	PIO	2	—
PIO2	AB15	PIO	PIO	2	—
PIO2 (●)	AB16	N.C.	PIO	2	—
PIO2 (●)	AB17	N.C.	PIO	2	—
PIO2 (●)	AB18	N.C.	PIO	2	—
PIO2 (●)	AB19	N.C.	PIO	2	—
PIO2 (●)	AB20	N.C.	PIO	2	—
PIO2 (●)	AB21	N.C.	PIO	2	—
PIO2 (●)	AB22	N.C.	PIO	2	—
PIO2/CBSEL0	R13	PIO	PIO	2	L9
PIO2/CBSEL1	V14	PIO	PIO	2	P10
VCCIO_2	N13	VCCIO	VCCIO	2	J9
VCCIO_2	T9	VCCIO	VCCIO	2	M5
VCCIO_2	Y11	VCCIO	VCCIO	2	—
PIO3/DP00A	F5	DPIO	DPIO	3	B1
PIO3/DP00B	G5	DPIO	DPIO	3	C1
PIO3/DP01A	G7	DPIO	DPIO	3	C3
PIO3/DP01B	H7	DPIO	DPIO	3	D3
PIO3/DP02A	H8	DPIO	DPIO	3	D4
PIO3/DP02B	J8	DPIO	DPIO	3	E4

iCE65L04 Pad Name	DiePlus VQ100	CB132	CB196	CB284	Pad	X (µm)	Y (µm)
PIO3_18/DP09A	12	—	G2	L3	29	129.40	1,627.75
GBIN7/PIO3_19/DP09B	13	G1	G1	L5	30	231.40	1,592.74
VCCIO_3	14	J6	J6	N10	31	129.40	1,557.75
VREF	N/A	N/A	N/A	M1	32	231.40	1,522.74
GND	—	—	A9	N1	33	129.40	1,487.75
GBIN6/PIO3_20/DP10A	15	H1	H1	M5	34	231.40	1,452.74
PIO3_21/DP10B	16	—	H2	M3	35	129.40	1,417.75
GND	17	H7	A9	M11	36	231.40	1,382.74
PIO3_22/DP11A	—	—	G3	N3	37	129.40	1,347.75
PIO3_23/DP11B	—	—	G4	P3	38	231.40	1,312.74
VCCIO_3	—	—	K1	R3	39	129.40	1,277.75
VCCIO_3	—	—	—	—	40	231.40	1,242.74
GND	—	—	A9	T3	41	129.40	1,207.75
GND	—	—	—	—	42	231.40	1,172.74
PIO3_24/DP12A	—	—	J1	U3	43	129.40	1,137.75
PIO3_25/DP12B	—	—	J2	V3	44	231.40	1,102.74
GND	—	—	A9	V1	45	129.40	1,067.75
PIO3_26/DP13A	—	—	H4	W3	46	231.40	1,032.74
PIO3_27/DP13B	—	—	H3	Y3	47	129.40	997.75
PIO3_28/DP14A	18	G3	K2	L7	48	231.40	962.74
PIO3_29/DP14B	19	G4	J3	L8	49	129.40	927.75
PIO3_30/DP15A	—	H3	H5	M7	50	231.40	892.74
PIO3_31/DP15B	—	H4	G5	M8	51	129.40	857.75
VCC	—	J4	F2	N8	52	231.40	822.74
PIO3_32/DP16A	20	J3	L1	N7	53	129.40	787.75
PIO3_33/DP16B	21	J1	L2	N5	54	231.40	752.74
VCCIO_3	22	K1	K1	P5	55	129.40	717.75
VCCIO_3	—	—	—	—	56	231.40	682.74
GND	23	L3	L3	R7	57	129.40	637.75
GND	—	—	—	—	58	231.40	592.74
PIO3_34/DP17A	—	K3	M1	P7	59	129.40	547.75
PIO3_35/DP17B	—	K4	M2	P8	60	231.40	502.74
PIO3_36/DP18A	24	L1	K3	R5	61	129.40	457.75
PIO3_37/DP18B	25	M1	K4	T5	62	231.40	412.74
PIO3_38/DP19A	—	N1	N1	U5	63	129.40	367.75
PIO3_39/DP19B	—	P1	N2	V5	64	231.40	322.74
PIO2_00	—	—	—	AB2	65	545.00	139.20
PIO2_01	—	P2	L4	V6	66	595.00	37.20
PIO2_02	—	M3	M3	T7	67	645.00	139.20
GND	—	—	C2	AB5	68	695.00	37.20
PIO2_03	26	L4	P1	R8	69	745.00	139.20
PIO2_04	27	P3	N3	V7	70	795.00	37.20
PIO2_05	28	M4	P2	T8	71	845.00	139.20
PIO2_06	29	L5	L5	R9	72	895.00	37.20
PIO2_07	30	P4	M4	V8	73	930.00	139.20

iCE65L04 Pad Name	DiePlus VQ100	CB132	CB196	CB284	Pad	X (µm)	Y (µm)
PIO2_08	—	L6	P3	R10	74	965.00	37.20
VCCIO_2	31	M5	M5	T9	75	1,000.00	139.20
PIO2_09	—	P5	K5	V9	76	1,035.00	37.20
PIO2_10	—	M6	N4	T10	77	1,070.00	139.20
GND	32	P6	H7	V10	78	1,105.00	37.20
PIO2_11	—	—	P4	Y4	79	1,140.00	139.20
PIO2_12	—	—	L6	Y5	80	1,175.00	37.20
PIO2_13	—	—	—	AB6	81	1,210.00	139.20
PIO2_14	—	—	—	AB7	82	1,245.00	37.20
PIO2_15	—	—	—	AB8	83	1,280.00	139.20
PIO2_16	—	—	—	AB9	84	1,315.00	37.20
PIO2_17	—	—	—	AB10	85	1,350.00	139.20
PIO2_18	—	—	—	AB11	86	1,385.00	37.20
GND	—	J8	H8	N12	87	1,420.00	139.20
PIO2_19	—	—	K6	Y6	88	1,455.00	37.20
PIO2_20	—	—	N5	Y7	89	1,490.00	139.20
VCC	—	—	J4	Y8	90	1,525.00	37.20
PIO2_21	—	—	M6	Y9	91	1,560.00	139.20
PIO2_22	—	—	N6	Y10	92	1,595.00	37.20
GBIN5/PIO2_23	33	P7	P5	V11	93	1,630.00	139.20
GBIN4/PIO2_24	34	P8	L7	V12	94	1,665.00	37.20
PIO2_25	—	—	—	AB12	95	1,700.00	139.20
VCCIO_2	—	—	J9	Y11	96	1,735.00	37.20
PIO2_26	—	—	—	AB13	97	1,770.00	139.20
PIO2_27	—	—	K7	AB14	98	1,805.00	37.20
GND	—	—	J5	Y12	99	1,840.00	139.20
PIO2_28	—	—	K9	AB15	100	1,875.00	37.20
PIO2_29	—	—	M7	Y13	101	1,910.00	139.20
PIO2_30	—	—	K8	Y14	102	1,945.00	37.20
PIO2_31	—	—	P7	Y15	103	1,980.00	139.20
PIO2_32	—	—	L8	Y17	104	2,015.00	37.20
PIO2_33	—	—	P8	Y18	105	2,050.00	139.20
PIO2_34	—	—	N8	Y19	106	2,085.00	37.20
PIO2_35	—	—	M8	Y20	107	2,120.00	139.20
VCC	35	J7	J7	N11	108	2,155.00	37.20
VCC	—	—	—	—	109	2,190.00	139.20
PIO2_36	36	P9	P9	V13	110	2,225.00	37.20
PIO2_37	37	M7	N9	T11	111	2,260.00	139.20
VCCIO_2	38	J9	N10	N13	112	2,295.00	37.20
PIO2_38	—	L7	M9	R11	113	2,330.00	139.20
GND	39	H8	J8	M12	114	2,365.00	37.20
PIO2_39	—	M8	N12	T12	115	2,400.00	139.20
PIO2_40	—	L8	N11	R12	116	2,435.00	37.20
PIO2_41	40	M9	N13	T13	117	2,470.00	139.20
PIO2_42/CBSEL0	41	L9	L9	R13	118	2,505.00	37.20
PIO2_43/CBSEL1	42	P10	P10	V14	119	2,540.00	139.20
CDONE	43	M10	M10	T14	120	2,575.00	37.20

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO3_20/DP10A	—	H8	39	129.735	2,462.665
PIO3_21/DP10B	—	J8	40	231.735	2,427.665
PIO3_22/DP11A	G1	T1	41	129.735	2,392.665
PIO3_23/DP11B	G2	U1	42	231.735	2,357.665
VCCIO_3	K1	N10	43	129.735	2,322.665
VCCIO_3	—	—	44	231.735	2,287.665
VREF	N/A	M1	45	129.735	2,252.665
VREF	N/A	—	46	231.735	2,217.665
GND	J5	N1	47	129.735	2,182.665
GND	—	—	48	231.735	2,147.665
VCCIO_3	J6	P1	49	129.735	2,112.665
VCCIO_3	—	—	50	231.735	2,077.665
GND	H6	R1	51	129.735	2,042.665
GND	—	—	52	231.735	2,007.665
PIO3_24/DP12A	H4	L3	53	129.735	1,972.665
GBIN7/PIO3_25/DP12B	H3	L5	54	231.735	1,937.665
GND	H7	V1	55	129.735	1,902.665
GBIN6/PIO3_26/DP13A	H1	M5	56	231.735	1,867.665
PIO3_27/DP13B	H2	M3	57	129.735	1,832.665
PIO3_28/DP14A	—	N7	58	231.735	1,798.665
PIO3_29/DP14B	—	N5	59	129.735	1,762.665
PIO3_30/DP15A	J1	N3	60	231.735	1,727.665
PIO3_31/DP15B	J2	P3	61	129.735	1,692.665
GND	J5	M11	62	231.735	1,657.665
GND	—	—	63	129.735	1,622.665
PIO3_32/DP16A	H5	W1	64	231.735	1,587.665
PIO3_33/DP16B	G5	Y1	65	129.735	1,552.665
VCCIO_3	J6	R3	66	231.735	1,517.665
VCCIO_3	—	—	67	129.735	1,482.665
GND	J5	T3	68	231.735	1,447.665
GND	—	—	69	129.735	1,412.665
PIO3_34/DP17A	K2	AA1	70	231.735	1,377.665
PIO3_35/DP17B	J3	AB1	71	129.735	1,342.665
PIO3_36/DP18A	—	L7	72	231.735	1,307.665
PIO3_37/DP18B	—	L8	73	129.735	1,272.665
PIO3_38/DP19A	—	M7	74	231.735	1,237.665
PIO3_39/DP19B	—	M8	75	129.735	1,202.665
PIO3_40/DP20A	L1	P7	76	231.735	1,167.665
PIO3_41/DP20B	L2	P8	77	129.735	1,132.665
VCC	J4	N8	78	231.735	1,097.665
VCC	—	—	79	129.735	1,062.665
PIO3_42/DP21A	K4	R5	80	231.735	1,027.665
PIO3_43/DP21B	K3	T5	81	129.735	992.665
VCCIO_3	K1	P5	82	231.735	957.665
VCCIO_3	—	—	83	129.735	912.665
GND	L3	R7	84	231.735	867.665
GND	—	—	85	129.735	822.67

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO2_28	—	Y13	132	2,062.5	139.5
GBIN5/PIO2_29	M7	V11	133	2,097.5	37.5
GBIN4/PIO2_30	N8	V12	134	2,132.5	139.5
GND	J8	Y12	135	2,167.5	37.5
GND	—	—	136	2,202.5	139.5
PIO2_31	P8	Y14	137	2,237.5	37.5
PIO2_32	—	AB15	138	2,272.5	139.5
PIO2_33	M8	V13	139	2,307.5	37.5
PIO2_34	—	AB16	140	2,342.5	139.5
PIO2_35	L8	Y15	141	2,377.5	37.5
PIO2_36	—	AB17	142	2,412.5	139.5
PIO2_37	N9	AB18	143	2,447.5	37.5
PIO2_38	—	AB19	144	2,482.5	139.5
PIO2_39	—	AB20	145	2,517.5	37.5
PIO2_40	—	AB21	146	2,552.5	139.5
PIO2_41	—	Y17	147	2,587.5	37.5
PIO2_42	—	AB22	148	2,622.5	139.5
PIO2_43	—	Y18	149	2,657.5	37.5
PIO2_44	P9	Y19	150	2,692.5	139.5
VCC	N7	N11	151	2,727.5	37.5
VCC	—	—	152	2,762.5	139.5
PIO2_45	M9	Y20	153	2,797.5	37.5
PIO2_46	K8	T11	154	2,832.5	139.5
VCCIO_2	J9	N13	155	2,867.5	37.5
VCCIO_2	—	—	156	2,902.5	139.5
PIO2_47	N11	R11	157	2,937.5	37.5
GND	J8	M12	158	2,972.5	139.5
GND	—	—	159	3,007.5	37.5
PIO2_48	N12	T12	160	3,042.5	139.5
PIO2_49	K9	R12	161	3,077.5	37.5
PIO2_50	N13	T13	162	3,112.5	139.5
PIO2_51/CBSEL0	L9	R13	163	3,147.5	37.5
PIO2_52/CBSEL1	P10	V14	164	3,182.5	139.5
CDONE	M10	T14	165	3,217.5	37.5
CRESET_B	L10	R14	166	3,260.0	139.5
PIOS_00/SPI_SO	M11	T15	167	3,320.0	37.5
PIOS_01/SPI_SI	P11	V15	168	3,370.0	139.5
GND	J8	Y16	169	3,420.0	37.5
GND	—	—	170	3,470.0	139.5
PIOS_02/SPI_SCK	P12	V16	171	3,520.0	37.5
PIOS_03/SPI_SS_B	P13	V17	172	3,570.0	139.5
VCC	—	—	173	3,620.0	37.5
VCC	—	—	174	3,670.0	139.5
SPI_VCC	L11	R15	175	3,720.0	37.5
SPI_VCC	—	—	176	3,770.0	139.5

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
GND	F7	E13	270	3,216.98	4,054.5
GND	—	—	271	3,166.98	4,156.5
PIO0_08	D9	E15	272	3,116.98	4,054.5
PIO0_09	C10	G14	273	3,064.48	4,156.5
PIO0_10	A10	A20	274	3,029.48	4,054.5
PIO0_11	B10	H13	275	2,994.48	4,156.5
PIO0_12	—	A19	276	2,959.48	4,054.5
PIO0_13	E9	G13	277	2,924.48	4,156.5
PIO0_14	—	C16	278	2,889.48	4,054.5
PIO0_15	—	E14	279	2,854.48	4,156.5
VCCIO_0	F6	E12	280	2,819.48	4,054.5
VCCIO_0	—	—	281	2,784.48	4,156.5
PIO0_16	—	A18	282	2,749.48	4,054.5
PIO0_17	—	A17	283	2,714.48	4,156.5
PIO0_18	C9	C15	284	2,679.48	4,054.5
PIO0_19	—	A16	285	2,644.48	4,156.5
PIO0_20	B9	C14	286	2,609.48	4,054.5
PIO0_21	—	H12	287	2,574.48	4,156.5
PIO0_22	D8	A15	288	2,539.48	4,054.5
PIO0_23	C8	H11	289	2,504.48	4,156.5
PIO0_24	E8	C13	290	2,469.48	4,054.5
PIO0_25	—	A14	291	2,434.48	4,156.5
GND	B12	C12	292	2,399.48	4,054.5
GND	—	—	293	2,364.48	4,156.5
PIO0_26	B8	A13	294	2,329.48	4,054.5
PIO0_27	D7	A12	295	2,294.48	4,156.5
PIO0_28	—	C11	296	2,259.48	4,054.5
GBIN1/PIO0_29	E7	E11	297	2,224.48	4,156.5
GBIN0/PIO0_30	A7	E10	298	2,189.48	4,054.5
PIO0_31	—	G12	299	2,154.48	4,156.5
VCCIO_0	A8	A8	300	2,119.48	4,054.5
VCCIO_0	—	—	301	2,084.48	4,156.5
PIO0_32	C7	A11	302	2,049.48	4,054.5
PIO0_33	—	G11	303	2,014.48	4,156.5
PIO0_34	E6	A10	304	1,979.48	4,054.5
PIO0_35	—	C10	305	1,944.48	4,156.5
VCC	B7	C8	306	1,909.48	4,054.5
VCC	—	—	307	1,874.48	4,156.5
PIO0_36	—	A9	308	1,839.48	4,054.5
PIO0_37	A6	A7	309	1,804.48	4,156.5
PIO0_38	B6	C9	310	1,769.48	4,054.5
PIO0_39	A5	A6	311	1,734.48	4,156.5
GND	G7	K11	312	1,699.48	4,054.5
GND	—	—	313	1,664.48	4,156.5
PIO0_40	D6	E9	314	1,629.48	4,054.5
PIO0_41	C6	G10	315	1,594.48	4,156.5

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO0_42	C5	A5	316	1,559.48	4,054.5
PIO0_43	B5	G9	317	1,524.48	4,156.5
PIO0_44	A4	A3	318	1,489.48	4,054.5
PIO0_45	—	A4	319	1,454.48	4,156.5
PIO0_46	—	A2	320	1,419.48	4,054.5
PIO0_47	—	C7	321	1,384.48	4,156.5
PIO0_48	—	C6	322	1,331.98	4,054.5
VCCIO_0	A8	K10	323	1,281.98	4,156.5
VCCIO_0	—	—	324	1,231.98	4,054.5
PIO0_49	—	E8	325	1,181.98	4,156.5
PIO0_50	B4	A1	326	1,131.98	4,054.5
PIO0_51	C4	E7	327	1,081.98	4,156.5
PIO0_52	A3	C5	328	1,031.98	4,054.5
PIO0_53	B3	E6	329	981.98	4,156.5
PIO0_54	D5	C3	330	931.98	4,054.5
GND	A9	L11	331	881.98	4,156.5
GND	—	—	332	831.98	4,054.5
PIO0_55	B2	G8	333	781.98	4,156.5
PIO0_56	A2	C4	334	731.98	4,054.5
PIO0_57	A1	H10	335	681.98	4,156.5
PIO0_58	—	E5	336	631.98	4,054.5
PIO0_59	—	H9	337	581.98	4,156.5