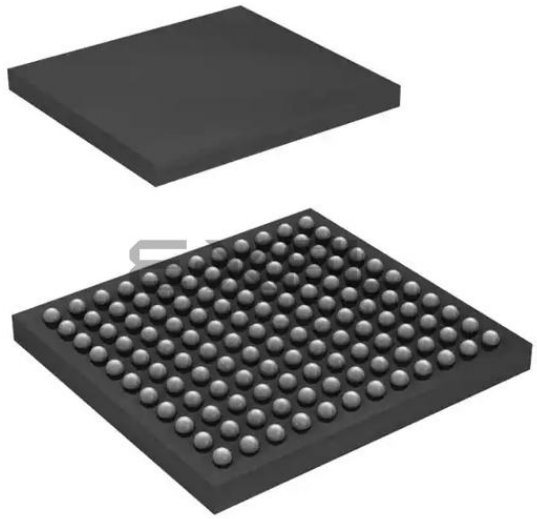
Lattice Semiconductor Corporation - ICE65L01F-TCB132I Datasheet



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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	160
Number of Logic Elements/Cells	1280
Total RAM Bits	65536
Number of I/O	93
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	132-VFBGA, CSPBGA
Supplier Device Package	132-CSBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice65l01f-tcb132i

Input and Output Register Control per PIO Pair

PIO pins are grouped into pairs for synchronous control. Registers within pairs of PIO pins share common input clock, output clock, and I/O clock enable control signals, as illustrated in Figure 11. The combinational logic paths are removed from the drawing for clarity.

The INCLK clock signal only controls the input flip-flops within the PIO pair.

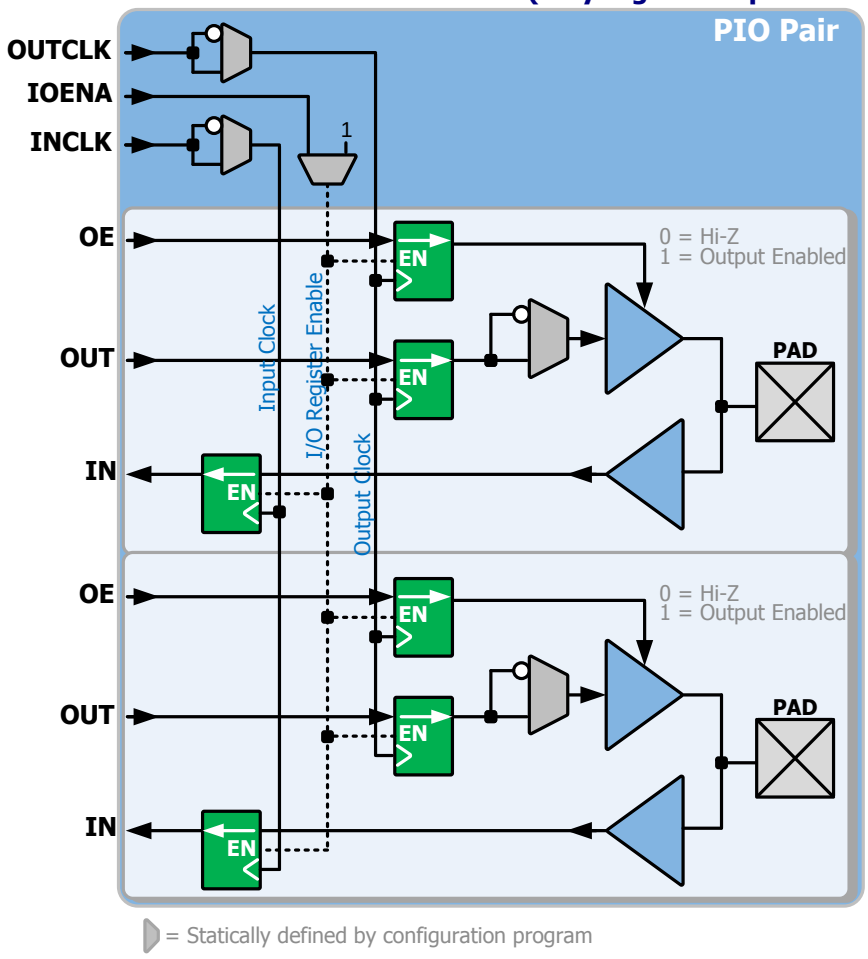
The OUTCLK clock signal controls the output flip-flops and the output-enable flip-flops within the PIO pair.

If desired in the iCE65 application, the INCLK and OUTCLK signals can be connected together.

The IOENA clock-enable input, if used, enables all registers in the PIO pair, as shown in Figure 11. By default, the registers are always enabled.

Before laying out your printed-circuit board, run the design through the iCEcube development software to verify that your selected pinout complies with these I/O register pairing requirements. See tables in "Die Cross Reference" starting on page 84.

Figure 11: **PIO Pairs Share Clock and Clock Enable Controls (only registered paths shown for clarity)**

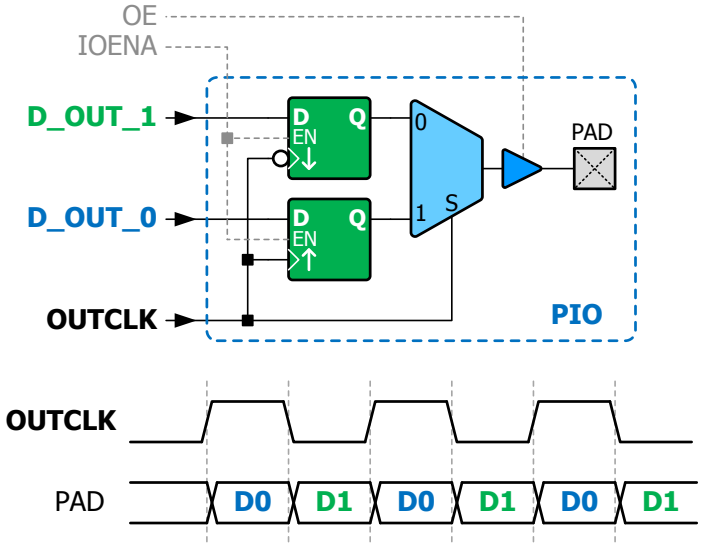


The pairing of PIO pairs is most evident in the tables in "Die Cross Reference" starting on page 84.

Double Data Rate (DDR) Flip-Flops

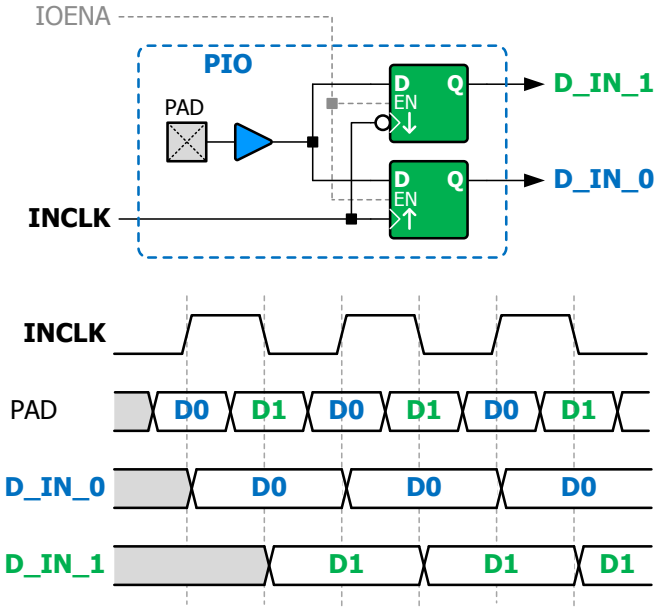
Each individual PIO pin optionally has two sets of double data rate (DDR) flip-flops; one input pair and one output pair. Figure 12 demonstrates the functionality of the output DDR flip-flop. Two signals from within the iCE65 device drive the DDR output flip-flop. The D_OUT_0 signal is clocked by the rising edge of the OUTCLK signal while the D_OUT_1 signal is clocked by the falling edge of the OUTCLK signal, assuming no optional clock polarity inversion. Internally, the two individual flip-flops are multiplexed together before the data appears at the pad, effectively doubling the output data rate.

Figure 12: DDR Output Flip-Flop



Similarly, Figure 13 demonstrates the DDR input flip-flop functionality. A double data rate (DDR) signal arrives at the pad. Internally, one value is clocked by the rising edge of the INCLK signal and another value is clocked by the falling edge of the INCLK signal. The DDR data stream is effectively de-multiplexed within the PIO pin and presented to the programmable interconnect on D_IN_0 and D_IN_1.

Figure 13: DDR Input Flip-Flop



The DDR flip-flops provide several design advantages. Internally within the iCE65 device, the clock frequency is half the effective external data rate. The lower clock frequency eases internal timing, doubling the clock period, and slashes the clock-related power in half.

Table 12 and Table 13 list the connections between a specific global buffer and the inputs on a Programmable I/O (PIO) pair. Although there is no direct connection between a global buffer and a PIO output, such a connection is possible by first connecting through a PLB LUT4 function. Again, all global buffers optionally drive all clock inputs. However, even-numbered global buffers optionally drive the clock-enable input on a PIO pair.

The PIO clock enable connect is different between the iCE65L01/iCE65L04 and iCE65L08.

Table 12: **iCE65L01 & iCE65L04: Global Buffer (GBUF) Connections to Programmable I/O (PIO) Pair**

Global Buffer	Output Connections	Input Clock	Output Clock	Clock Enable
GBUF0	No (connect through PLB LUT)	Yes	Yes	No
GBUF1		Yes	Yes	Yes
GBUF2		Yes	Yes	No
GBUF3		Yes	Yes	Yes
GBUF4		Yes	Yes	No
GBUF5		Yes	Yes	Yes
GBUF6		Yes	Yes	No
GBUF7		Yes	Yes	Yes

Table 13: **iCE64L08: Global Buffer (GBUF) Connections to Programmable I/O (PIO) Pair**

Global Buffer	Output Connections	Input Clock	Output Clock	Clock Enable
GBUF0	No (connect through PLB LUT)	Yes	Yes	Yes
GBUF1		Yes	Yes	No
GBUF2		Yes	Yes	Yes
GBUF3		Yes	Yes	No
GBUF4		Yes	Yes	Yes
GBUF5		Yes	Yes	No
GBUF6		Yes	Yes	Yes
GBUF7		Yes	Yes	No

Global Buffer Inputs

The iCE65 component has eight specialized GBIN/PIO pins that are optionally direct inputs to the global buffers, offering the best overall clock characteristics. As shown in Figure 15, each GBIN/PIO pin is a full-featured I/O pin but also provides a direct connection to its associated global buffer. The direct connection to the global buffer bypasses the iCEgate input-blocking latch and other PIO input logic. These special PIO pins are allocated two to an I/O Bank, a total of eight. These pins are labeled GBIN0 through GBIN7, as shown in Figure 14 and the pin locations for each GBIN input appear in Table 14.

Table 14: **Global Buffer Input Ball/Pin Number by Package**

Global Buffer Input (GBIN)	I/O Bank	VQ100	CB132	'L04 CB196	'L08 CB196	CB284
GBIN0	0	90	A6	A7	A7	E10
GBIN1		89	A7	E7	E7	E11
GBIN2	1	63	G14	F10	F10	L18
GBIN3		62	F14	G12	G12	K18
GBIN4	2	34	P8	L7	N8	V12
GBIN5		33	P7	P5	M7	V11
GBIN6	3	15	H1	H1	H1	M5
GBIN7		13	G1	G1	H3	L5

Figure 21: iCE65 Configuration Control Pins

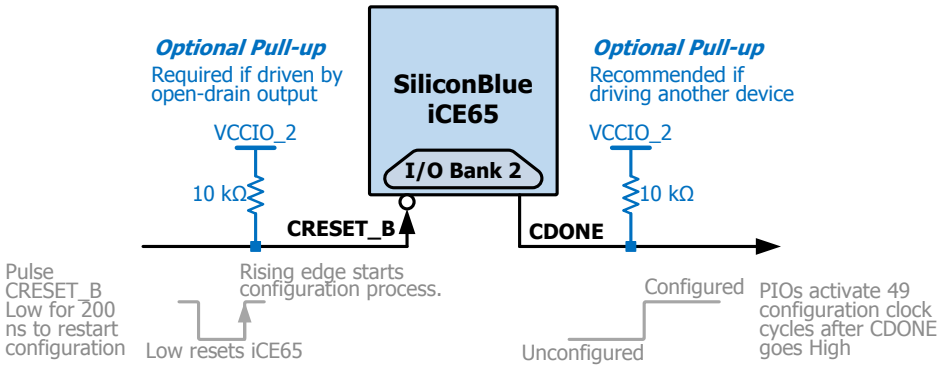


Figure 21 shows the two iCE65 configuration control pins, CRESET_B and CDONE. Table 23 lists the ball/pin numbers for the configuration control pins by package. When driven Low for at least 200 ns, the dedicated Configuration Reset input, CRESET_B, resets the iCE65 device. When CRESET_B returns High, the iCE65 FPGA restarts the configuration process from its power-on conditions (Cold Boot). The CRESET_B pin is a pure input with no internal pull-up resistor. If driven by open-drain driver or un-driven, then connect the CRESET_B pin to a 10 kΩ pull-up resistor connected to the VCCIO_2 supply.

***Table 23:* Configuration Control Ball/Pin Numbers by Package**

Configuration Control Pins	CB81	QN84	VQ100	CB132	CB196	CB284
CRESET_B	J6	A21	44	L10	L10	R14
CDONE	H6	B16	43	M10	M10	T14

The iCE65 device signals the end of the configuration process by actively turning off the internal pull-down transistor on the Configuration Done output pin, CDONE. The pin has a permanent, weak internal pull-up resistor to the VCCIO_2 rail. If the iCE65 device drives other devices, then optionally connect the CDONE pin to a 10 kΩ pull-up resistor connected to the VCCIO_2 supply.

The PIO pins activate according to their configured function after 49 configuration clock cycles. The internal oscillator is the configuration clock source for the SPI Master Configuration Interface and when configuring from

* Note: only 14 of the 16 RAM4K Memory Blocks may be pre-initialized in the iCE65L01.

Nonvolatile Configuration Memory (NVCM). When using the SPI Peripheral Configuration Interface, the configuration clock source is the SPI_SCK clock input pin.

Internal Oscillator

During SPI Master or NVCM configuration mode, the controlling clock signal is generated from an internal oscillator. The oscillator starts operating at the Default frequency. During the configuration process, however, bit settings within the configuration bitstream can specify a higher-frequency mode in order to maximize SPI bandwidth and reduce overall configuration time. See Table 57: Internal Oscillator Frequency on page 105 for the specified oscillator frequency range.

Using the SPI Master Configuration Interface, internal oscillator controls all the interface timing and clocks the SPI serial Flash PROM via the SPI_SCK clock output pin.

The oscillator output, which also supplies the SPI SCK clock output during the SPI Flash configuration process, has a 50% duty cycle.

Internal Device Reset

Figure 22 presents the various signals that internally reset the iCE65 internal logic.

- Power-On Reset (POR)
- CRESET_B Pin
- JTAG Interface

CB81 Chip-Scale Ball-Grid Array

The CB81 package is a full ball grid array with 0.5 mm ball pitch. The iCE65L01 device is available in this package.

Footprint Diagram

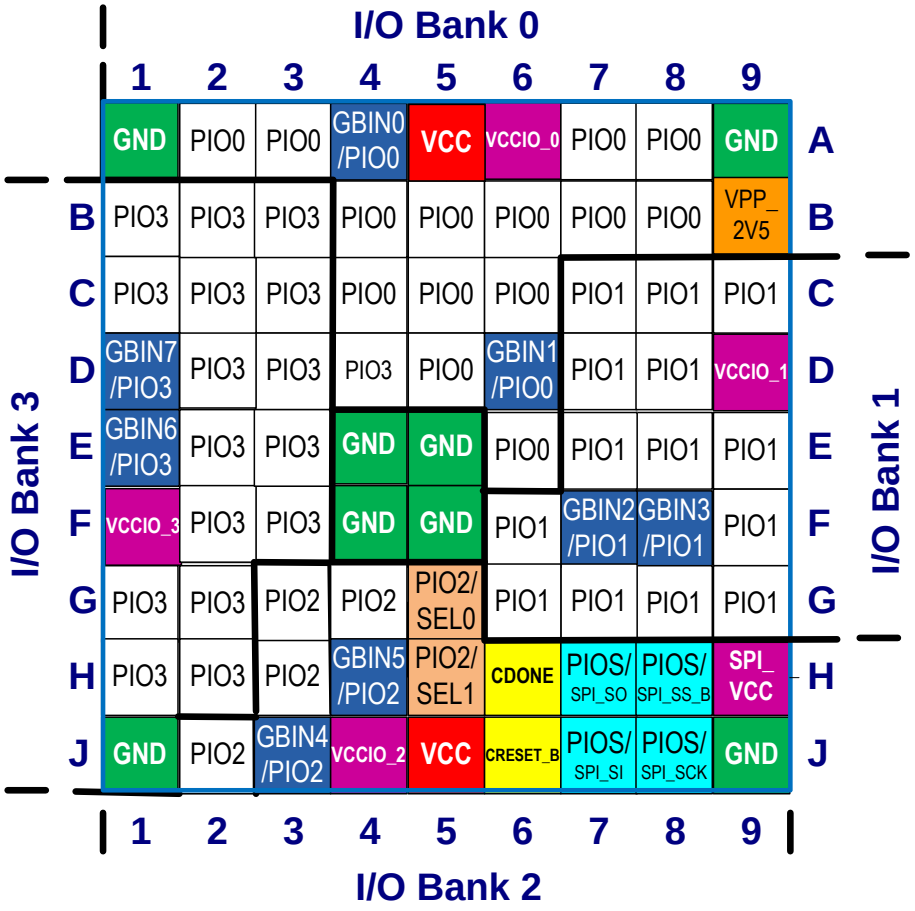
Figure 32 shows the iCE65 footprint diagram for the CB81 package.

Figure 31 shows the conventions used in the diagram.

Also see Table 37 for a complete, detailed pinout for the 81-ball BGA package.

The signal pins are also grouped into the four I/O Banks and the SPI interface.

***Figure 32*: iCE65L01 CB81 Chip-Scale BGA Footprint (Top View)**



Pinout Table

Table 37 provides a detailed pinout table for the CB81 package. Pins are generally arranged by I/O bank, then by ball function.

Table 37: iCE65 CB81 Chip-scale BGA Pinout Table

Ball Function	Ball Number	Pin Type	Bank
PIO0	A2	PIO	0
PIO0	A3	PIO	0
GBIN0/PIO0	A4	GBIN	0
PIO0	A7	PIO	0
PIO0	A8	PIO	0
PIO0	B4	PIO	0
PIO0	B5	PIO	0
PIO0	B6	PIO	0
PIO0	B7	PIO	0
PIO0	B8	PIO	0
PIO0	C4	PIO	0
PIO0	C5	PIO	0
PIO0	C6	PIO	0
PIO0	D4	PIO	0
PIO0	D5	PIO	0
GBIN1/PIO0	D6	GBIN	0
PIO0	E6	PIO	0
VCCIO_0	A6	VCCIO	0
PIO1	C7	PIO	1
PIO1	C8	PIO	1
PIO1	C9	PIO	1
PIO1	D7	PIO	1
PIO1	D8	PIO	1
PIO1	E7	PIO	1
PIO1	E8	PIO	1
PIO1	E9	PIO	1
PIO1	F6	PIO	1
GBIN2/PIO1	F7	GBIN	1
GBIN3/PIO1	F8	GBIN	1
PIO1	F9	PIO	1
PIO1	G6	PIO	1
PIO1	G7	PIO	1
PIO1	G8	PIO	1
PIO1	G9	PIO	1
VCCIO_1	D9	VCCIO	1
CDONE	H6	CONFIG	2
CRESET_B	J6	CONFIG	2
PIO2	G3	PIO	2
PIO2	G4	PIO	2
PIO2/CBSEL0	G5	PIO	2
PIO2	H3	PIO	2
GBIN5/PIO2	H4	PIO	2
PIO2/CBSEL1	H5	PIO	2
PIO2	J2	PIO	2
GBIN4/PIO2	J3	PIO	2
VCCIO_2	J4	PIO	2

Ball Function	Ball Number	Pin Type	Bank
PIO2	B14	PIO	2
PIO2/CBSEL0	B15	PIO	2
PIO2/CBSEL1	A20	PIO	2
VCCIO_2	A17	PIO	2
GBIN6/PIO3	A9	GBIN	3
GBIN7/PIO3	A8	GBIN	3
PIO3	A1	PIO	3
PIO3	A2	PIO	3
PIO3	A3	PIO	3
PIO3	A4	PIO	3
PIO3	A5	PIO	3
PIO3	A10	PIO	3
PIO3	A11	PIO	3
PIO3	A12	PIO	3
PIO3	B1	PIO	3
PIO3	B2	PIO	3
PIO3	B3	PIO	3
PIO3	B4	PIO	3
PIO3	B5	PIO	3
PIO3	B7	PIO	3
PIO3	B8	PIO	3
PIO3	B9	PIO	3
VCCIO_3	B6	VCCIO	3
PIOS/SPI_SO	B17	SPI	SPI
PIOS/SPI_SI	A22	SPI	SPI
PIOS/SPI_SCK	A23	SPI	SPI
PIOS/SPI_SS_B	B18	SPI	SPI
SPI_VCC	A24	SPI	SPI
GND	A6	GND	GND
GND	A18	GND	GND
GND	A30	GND	GND
GND	B33	GND	GND
VCC	A7	VCC	VCC
VCC	A15	VCC	VCC
VCC	A28	VCC	VCC
VCC	B28	VCC	VCC
VPP_2V5	A36	VPP	VPP
VPP_FAST	A37	VPP	VPP

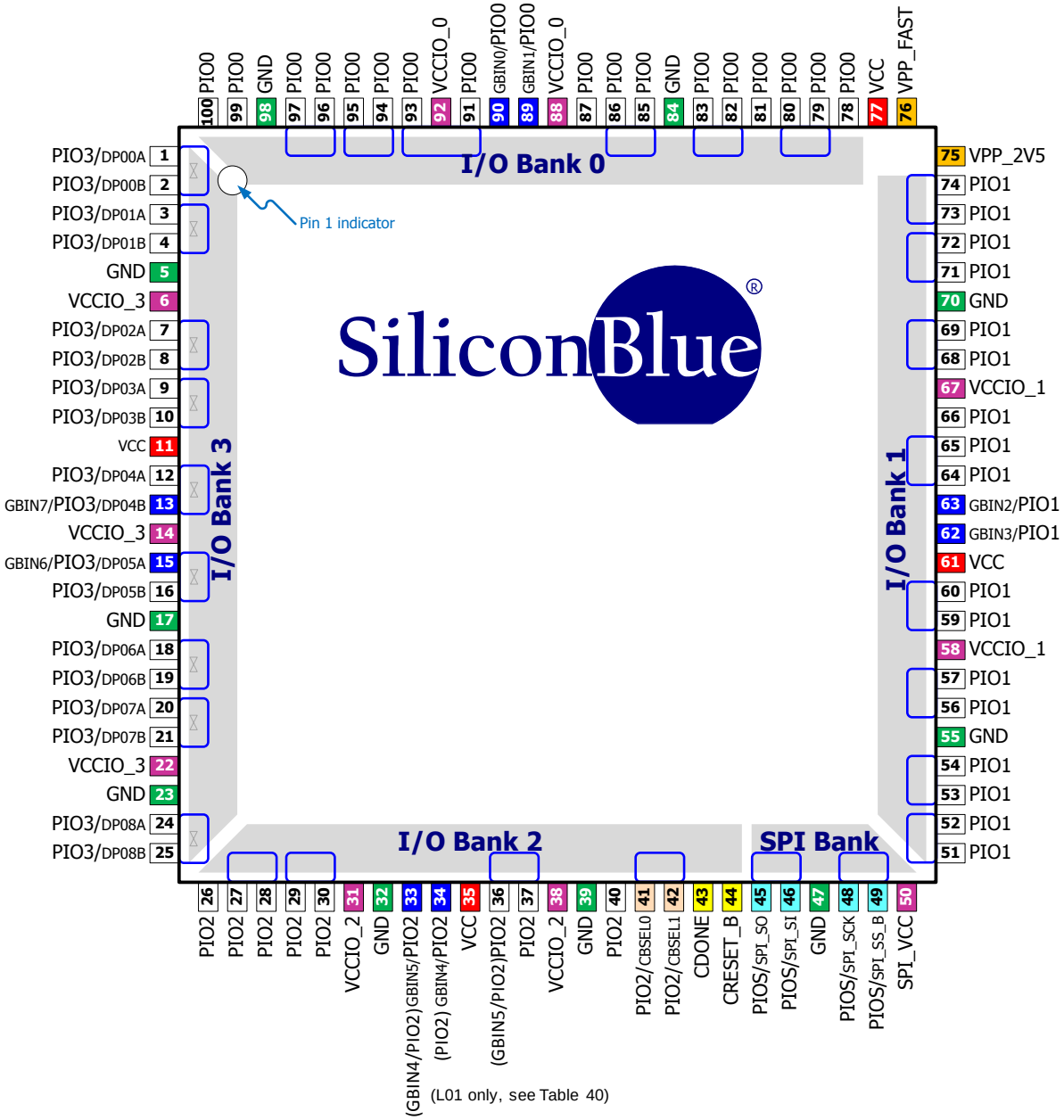
VQ100 Very-thin Quad Flat Package

The VQ100 package is a very-thin quad-flat package with 0.5 mm lead pitch. The iCE65L01 and iCE65L04 devices are available in this package.

Footprint Diagram

Figure 36 shows the footprint diagram for the 100-lead very-thin quad-flat package (VQ100). See Table 40 for a complete, detailed pinout for the 100-lead very-thin quad-flat package. The signal pins are also grouped into the four I/O Banks and the SPI interface.

Figure 36: iCE65 VQ100 Footprint (Top View)

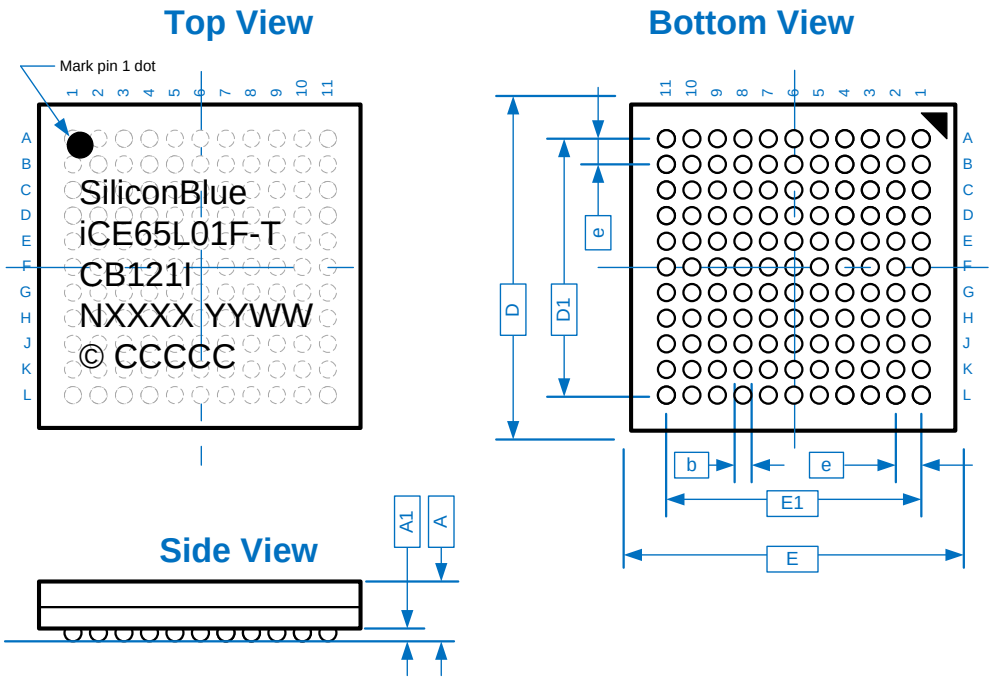


Pinout Table

Table 39 provides a detailed pinout table for the VQ100 package. Pins are generally arranged by I/O bank, then by pin function. The table also highlights the differential I/O pairs in I/O Bank 3. The VQ100 package has no JTAG pins.

***Figure 40:* CB121 Package Mechanical Drawing**

CB121: 6 x 6 mm, 121-ball, 0.5 mm ball-pitch, fully-populated, chip-scale ball grid array



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			11		Columns
Number of Ball Rows	Y			11		Rows
Number of Signal Balls		n		121		Balls
Body Size	X	E	5.90	6.00	6.10	mm
	Y	D	5.90	6.00	6.10	
Ball Pitch		e	—	0.50	—	
Ball Diameter		b	0.2	—	0.3	
Edge Ball Center to Center	X	E1	—	5.00	—	
	Y	D1	—	5.00	—	
Package Height		A	—	—	1.00	
Stand Off		A1	0.12	—	0.20	

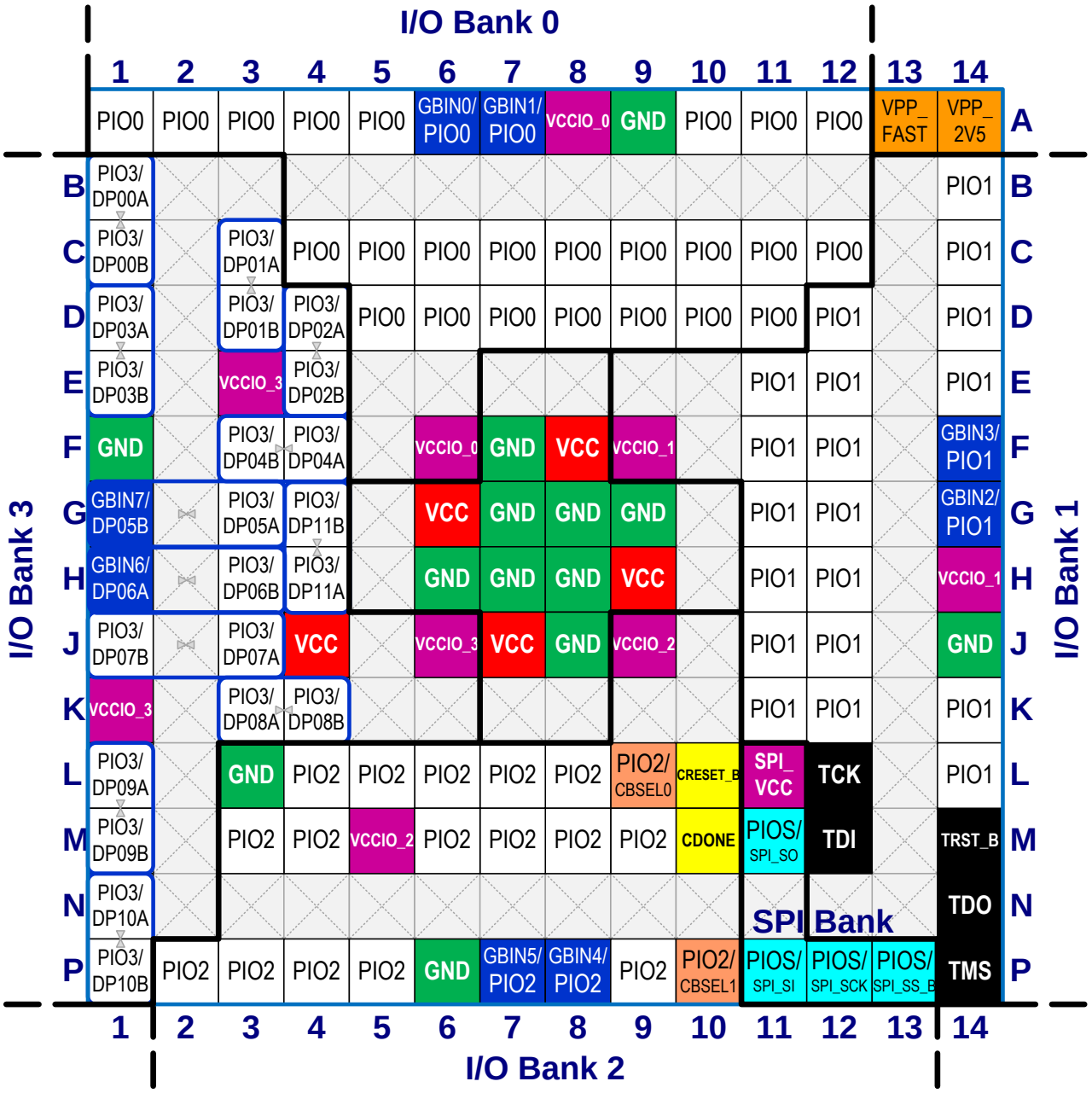
Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65L01F	Part number
	-T	Power/Speed
3	CB121I	Package type
	ENG	Engineering
4	NXXXX	Lot Number
5	YYWW	Date Code
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
64	55

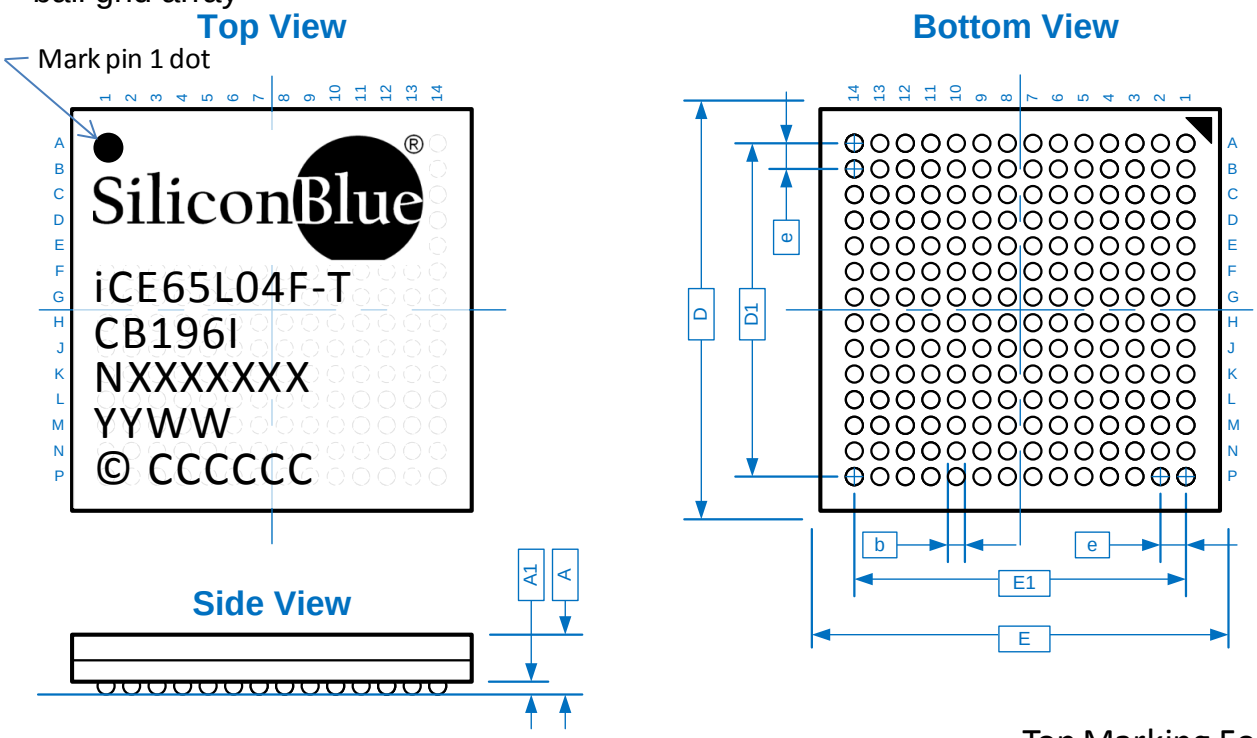
Figure 43: **iCE65L08 CB132 Chip-Scale BGA Footprint (Top View)**



Package Mechanical Drawing

Figure 47:
(a) iCE65L04 CB196 Package Mechanical Drawing

CB196: 8 x8 mm, 196-ball, 0.5 mm ball-pitch, fully-populated, chip-scale ball grid array



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			14		Columns
Number of Ball Rows	Y			14		Rows
Number of Signal Balls		n		196		Balls
Body Size	X	E	7.90	8.00	8.10	mm
	Y	D	7.90	8.00	8.10	
Ball Pitch		e	—	0.50	—	
Ball Diameter		b	0.27	—	0.37	
Edge Ball Center to Center	X	E1	—	6.50	—	
	Y	D1	—	6.50	—	
Package Height		A	—	—	1.00	
Stand Off		A1	0.16	—	0.26	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65L04F	Part number
	-T	Power/Speed
3	CB196I	Package type
	ENG	Engineering
4	NXXXXXXX	Lot Number
5	YYWW	Date Code
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
42	34

iCE65L04 Pad Name	DiePlus VQ100	CB132	CB196	CB284	Pad	X (µm)	Y (µm)
PIO3_18/DP09A	12	—	G2	L3	29	129.40	1,627.75
GBIN7/PIO3_19/DP09B	13	G1	G1	L5	30	231.40	1,592.74
VCCIO_3	14	J6	J6	N10	31	129.40	1,557.75
VREF	N/A	N/A	N/A	M1	32	231.40	1,522.74
GND	—	—	A9	N1	33	129.40	1,487.75
GBIN6/PIO3_20/DP10A	15	H1	H1	M5	34	231.40	1,452.74
PIO3_21/DP10B	16	—	H2	M3	35	129.40	1,417.75
GND	17	H7	A9	M11	36	231.40	1,382.74
PIO3_22/DP11A	—	—	G3	N3	37	129.40	1,347.75
PIO3_23/DP11B	—	—	G4	P3	38	231.40	1,312.74
VCCIO_3	—	—	K1	R3	39	129.40	1,277.75
VCCIO_3	—	—	—	—	40	231.40	1,242.74
GND	—	—	A9	T3	41	129.40	1,207.75
GND	—	—	—	—	42	231.40	1,172.74
PIO3_24/DP12A	—	—	J1	U3	43	129.40	1,137.75
PIO3_25/DP12B	—	—	J2	V3	44	231.40	1,102.74
GND	—	—	A9	V1	45	129.40	1,067.75
PIO3_26/DP13A	—	—	H4	W3	46	231.40	1,032.74
PIO3_27/DP13B	—	—	H3	Y3	47	129.40	997.75
PIO3_28/DP14A	18	G3	K2	L7	48	231.40	962.74
PIO3_29/DP14B	19	G4	J3	L8	49	129.40	927.75
PIO3_30/DP15A	—	H3	H5	M7	50	231.40	892.74
PIO3_31/DP15B	—	H4	G5	M8	51	129.40	857.75
VCC	—	J4	F2	N8	52	231.40	822.74
PIO3_32/DP16A	20	J3	L1	N7	53	129.40	787.75
PIO3_33/DP16B	21	J1	L2	N5	54	231.40	752.74
VCCIO_3	22	K1	K1	P5	55	129.40	717.75
VCCIO_3	—	—	—	—	56	231.40	682.74
GND	23	L3	L3	R7	57	129.40	637.75
GND	—	—	—	—	58	231.40	592.74
PIO3_34/DP17A	—	K3	M1	P7	59	129.40	547.75
PIO3_35/DP17B	—	K4	M2	P8	60	231.40	502.74
PIO3_36/DP18A	24	L1	K3	R5	61	129.40	457.75
PIO3_37/DP18B	25	M1	K4	T5	62	231.40	412.74
PIO3_38/DP19A	—	N1	N1	U5	63	129.40	367.75
PIO3_39/DP19B	—	P1	N2	V5	64	231.40	322.74
PIO2_00	—	—	—	AB2	65	545.00	139.20
PIO2_01	—	P2	L4	V6	66	595.00	37.20
PIO2_02	—	M3	M3	T7	67	645.00	139.20
GND	—	—	C2	AB5	68	695.00	37.20
PIO2_03	26	L4	P1	R8	69	745.00	139.20
PIO2_04	27	P3	N3	V7	70	795.00	37.20
PIO2_05	28	M4	P2	T8	71	845.00	139.20
PIO2_06	29	L5	L5	R9	72	895.00	37.20
PIO2_07	30	P4	M4	V8	73	930.00	139.20

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO3_20/DP10A	—	H8	39	129.735	2,462.665
PIO3_21/DP10B	—	J8	40	231.735	2,427.665
PIO3_22/DP11A	G1	T1	41	129.735	2,392.665
PIO3_23/DP11B	G2	U1	42	231.735	2,357.665
VCCIO_3	K1	N10	43	129.735	2,322.665
VCCIO_3	—	—	44	231.735	2,287.665
VREF	N/A	M1	45	129.735	2,252.665
VREF	N/A	—	46	231.735	2,217.665
GND	J5	N1	47	129.735	2,182.665
GND	—	—	48	231.735	2,147.665
VCCIO_3	J6	P1	49	129.735	2,112.665
VCCIO_3	—	—	50	231.735	2,077.665
GND	H6	R1	51	129.735	2,042.665
GND	—	—	52	231.735	2,007.665
PIO3_24/DP12A	H4	L3	53	129.735	1,972.665
GBIN7/PIO3_25/DP12B	H3	L5	54	231.735	1,937.665
GND	H7	V1	55	129.735	1,902.665
GBIN6/PIO3_26/DP13A	H1	M5	56	231.735	1,867.665
PIO3_27/DP13B	H2	M3	57	129.735	1,832.665
PIO3_28/DP14A	—	N7	58	231.735	1,798.665
PIO3_29/DP14B	—	N5	59	129.735	1,762.665
PIO3_30/DP15A	J1	N3	60	231.735	1,727.665
PIO3_31/DP15B	J2	P3	61	129.735	1,692.665
GND	J5	M11	62	231.735	1,657.665
GND	—	—	63	129.735	1,622.665
PIO3_32/DP16A	H5	W1	64	231.735	1,587.665
PIO3_33/DP16B	G5	Y1	65	129.735	1,552.665
VCCIO_3	J6	R3	66	231.735	1,517.665
VCCIO_3	—	—	67	129.735	1,482.665
GND	J5	T3	68	231.735	1,447.665
GND	—	—	69	129.735	1,412.665
PIO3_34/DP17A	K2	AA1	70	231.735	1,377.665
PIO3_35/DP17B	J3	AB1	71	129.735	1,342.665
PIO3_36/DP18A	—	L7	72	231.735	1,307.665
PIO3_37/DP18B	—	L8	73	129.735	1,272.665
PIO3_38/DP19A	—	M7	74	231.735	1,237.665
PIO3_39/DP19B	—	M8	75	129.735	1,202.665
PIO3_40/DP20A	L1	P7	76	231.735	1,167.665
PIO3_41/DP20B	L2	P8	77	129.735	1,132.665
VCC	J4	N8	78	231.735	1,097.665
VCC	—	—	79	129.735	1,062.665
PIO3_42/DP21A	K4	R5	80	231.735	1,027.665
PIO3_43/DP21B	K3	T5	81	129.735	992.665
VCCIO_3	K1	P5	82	231.735	957.665
VCCIO_3	—	—	83	129.735	912.665
GND	L3	R7	84	231.735	867.665
GND	—	—	85	129.735	822.67

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO2_28	—	Y13	132	2,062.5	139.5
GBIN5/PIO2_29	M7	V11	133	2,097.5	37.5
GBIN4/PIO2_30	N8	V12	134	2,132.5	139.5
GND	J8	Y12	135	2,167.5	37.5
GND	—	—	136	2,202.5	139.5
PIO2_31	P8	Y14	137	2,237.5	37.5
PIO2_32	—	AB15	138	2,272.5	139.5
PIO2_33	M8	V13	139	2,307.5	37.5
PIO2_34	—	AB16	140	2,342.5	139.5
PIO2_35	L8	Y15	141	2,377.5	37.5
PIO2_36	—	AB17	142	2,412.5	139.5
PIO2_37	N9	AB18	143	2,447.5	37.5
PIO2_38	—	AB19	144	2,482.5	139.5
PIO2_39	—	AB20	145	2,517.5	37.5
PIO2_40	—	AB21	146	2,552.5	139.5
PIO2_41	—	Y17	147	2,587.5	37.5
PIO2_42	—	AB22	148	2,622.5	139.5
PIO2_43	—	Y18	149	2,657.5	37.5
PIO2_44	P9	Y19	150	2,692.5	139.5
VCC	N7	N11	151	2,727.5	37.5
VCC	—	—	152	2,762.5	139.5
PIO2_45	M9	Y20	153	2,797.5	37.5
PIO2_46	K8	T11	154	2,832.5	139.5
VCCIO_2	J9	N13	155	2,867.5	37.5
VCCIO_2	—	—	156	2,902.5	139.5
PIO2_47	N11	R11	157	2,937.5	37.5
GND	J8	M12	158	2,972.5	139.5
GND	—	—	159	3,007.5	37.5
PIO2_48	N12	T12	160	3,042.5	139.5
PIO2_49	K9	R12	161	3,077.5	37.5
PIO2_50	N13	T13	162	3,112.5	139.5
PIO2_51/CBSEL0	L9	R13	163	3,147.5	37.5
PIO2_52/CBSEL1	P10	V14	164	3,182.5	139.5
CDONE	M10	T14	165	3,217.5	37.5
CRESET_B	L10	R14	166	3,260.0	139.5
PIOS_00/SPI_SO	M11	T15	167	3,320.0	37.5
PIOS_01/SPI_SI	P11	V15	168	3,370.0	139.5
GND	J8	Y16	169	3,420.0	37.5
GND	—	—	170	3,470.0	139.5
PIOS_02/SPI_SCK	P12	V16	171	3,520.0	37.5
PIOS_03/SPI_SS_B	P13	V17	172	3,570.0	139.5
VCC	—	—	173	3,620.0	37.5
VCC	—	—	174	3,670.0	139.5
SPI_VCC	L11	R15	175	3,720.0	37.5
SPI_VCC	—	—	176	3,770.0	139.5

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
TDI	M12	T16	177	4,470.5	634.615
TMS	P14	V18	178	4,572.5	684.615
TCK	L12	R16	179	4,470.5	734.615
TDO	N14	U18	180	4,572.5	784.615
TRST_B	M14	T18	181	4,470.5	834.615
PIO1_00	M13	R18	182	4,572.5	884.615
PIO1_01	K11	P16	183	4,470.5	934.615
PIO1_02	L13	P15	184	4,572.5	984.615
PIO1_03	L14	P18	185	4,470.5	1,034.615
GND	G9	N18	186	4,572.5	1,084.615
GND	—	—	187	4,470.5	1,134.615
PIO1_04	J11	N16	188	4,572.5	1,184.615
PIO1_05	K12	N15	189	4,470.5	1,234.62
VCCIO_1	F9	M18	190	4,572.5	1,287.115
VCCIO_1	—	—	191	4,470.5	1,322.115
PIO1_06	J12	M15	192	4,572.5	1,357.115
PIO1_07	K14	M16	193	4,470.5	1,392.115
PIO1_08	—	T20	194	4,572.5	1,427.115
PIO1_09	—	W20	195	4,470.5	1,462.115
PIO1_10	—	V20	196	4,572.5	1,497.115
VCC	H9	M13	197	4,470.5	1,532.115
VCC	—	—	198	4,572.5	1,567.115
PIO1_11	—	R20	199	4,470.5	1,602.115
PIO1_12	—	Y22	200	4,572.5	1,637.115
PIO1_13	—	AA22	201	4,470.5	1,672.115
PIO1_14	—	U20	202	4,572.5	1,707.115
PIO1_15	J13	W22	203	4,470.5	1,742.115
PIO1_16	H11	P20	204	4,572.5	1,777.115
PIO1_17	J10	V22	205	4,470.5	1,812.115
PIO1_18	H12	U22	206	4,572.5	1,847.115
GND	K10	N20	207	4,470.5	1,882.115
GND	—	—	208	4,572.5	1,917.110
PIO1_19	H13	T22	209	4,470.5	1,952.115
PIO1_20	—	M20	210	4,572.5	1,987.115
PIO1_21	H10	R22	211	4,470.5	2,022.115
PIO1_22	—	P22	212	4,572.5	2,057.115
VCCIO_1	F9	J20	213	4,470.5	2,092.115
VCCIO_1	—	—	214	4,572.5	2,127.115
PIO1_23	G10	M22	215	4,470.5	2,162.115
PIO1_24	G11	N22	216	4,572.5	2,197.115
PIO1_25	—	K22	217	4,470.5	2,232.115
PIO1_26	—	L22	218	4,572.5	2,267.115
GBIN3/PIO1_27	G12	K18	219	4,470.5	2,302.11
GBIN2/PIO1_28	F10	L18	220	4,572.5	2,337.115
PIO1_29	—	J22	221	4,470.5	2,372.115

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO1_30	—	K20	222	4,572.5	2,407.115
PIO1_31	G14	F22	223	4,470.5	2,442.115
PIO1_32	—	G22	224	4,572.5	2,477.115
PIO1_33	F11	E22	225	4,470.5	2,512.115
PIO1_34	F12	L16	226	4,572.5	2,547.115
PIO1_35	G13	D22	227	4,470.5	2,582.115
GND	G8	L12	228	4,572.5	2,617.115
GND	—	—	229	4,470.5	2,652.115
PIO1_36	E10	K16	230	4,572.5	2,687.12
VCCIO_1	H14	H22	231	4,470.5	2,722.12
VCCIO_1	—	—	232	4,572.5	2,757.12
PIO1_37	F14	H20	233	4,470.5	2,792.12
PIO1_38	E11	J18	234	4,572.5	2,827.12
PIO1_39	D12	C22	235	4,470.5	2,862.12
PIO1_40	F13	J16	236	4,572.5	2,897.12
PIO1_41	E13	B22	237	4,470.5	2,932.12
PIO1_42	E12	H18	238	4,572.5	2,967.12
PIO1_43	E14	G20	239	4,470.5	3,002.12
PIO1_44	—	L15	240	4,572.5	3,037.12
PIO1_45	—	A22	241	4,470.5	3,072.12
PIO1_46	—	H16	242	4,572.5	3,107.12
VCC	K13	L20	243	4,470.5	3,142.12
VCC	—	—	244	4,572.5	3,177.12
PIO1_47	D14	F20	245	4,470.5	3,229.615
PIO1_48	D11	K15	246	4,572.5	3,279.615
VCCIO_1	H14	K13	247	4,470.5	3,329.615
VCCIO_1	—	—	248	4,572.5	3,379.615
PIO1_49	C14	E20	249	4,470.5	3,429.62
PIO1_50	D13	J15	250	4,572.5	3,479.615
GND	J14	L13	251	4,470.5	3,529.615
GND	—	—	252	4,572.5	3,579.615
PIO1_51	B14	D20	253	4,470.5	3,629.615
PIO1_52	C13	G18	254	4,572.5	3,679.595
PIO1_53	B13	C20	255	4,470.5	3,729.595
PIO1_54	C12	F18	256	4,572.5	3,779.595
VPP_2V5	A14	E18	257	4,470.5	3,879.575
VPP_FAST	A13	E17	258	3,866.975	4,054.5
VCC	F8	K12	259	3,766.98	4,156.5
VCC	—	—	260	3,716.98	4,054.5
PIO0_00	—	G16	261	3,666.98	4,156.5
PIO0_01	—	C19	262	3,616.98	4,054.5
PIO0_02	C11	H15	263	3,566.98	4,156.5
PIO0_03	—	C18	264	3,516.98	4,054.5
PIO0_04	A12	H14	265	3,466.98	4,156.5
VCCIO_0	F6	A21	266	3,416.98	4,054.5
PIO0_05	B11	C17	267	3,366.98	4,156.5
PIO0_06	D10	E16	268	3,316.98	4,054.5
PIO0_07	A11	G15	269	3,266.98	4,156.5

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO0_42	C5	A5	316	1,559.48	4,054.5
PIO0_43	B5	G9	317	1,524.48	4,156.5
PIO0_44	A4	A3	318	1,489.48	4,054.5
PIO0_45	—	A4	319	1,454.48	4,156.5
PIO0_46	—	A2	320	1,419.48	4,054.5
PIO0_47	—	C7	321	1,384.48	4,156.5
PIO0_48	—	C6	322	1,331.98	4,054.5
VCCIO_0	A8	K10	323	1,281.98	4,156.5
VCCIO_0	—	—	324	1,231.98	4,054.5
PIO0_49	—	E8	325	1,181.98	4,156.5
PIO0_50	B4	A1	326	1,131.98	4,054.5
PIO0_51	C4	E7	327	1,081.98	4,156.5
PIO0_52	A3	C5	328	1,031.98	4,054.5
PIO0_53	B3	E6	329	981.98	4,156.5
PIO0_54	D5	C3	330	931.98	4,054.5
GND	A9	L11	331	881.98	4,156.5
GND	—	—	332	831.98	4,054.5
PIO0_55	B2	G8	333	781.98	4,156.5
PIO0_56	A2	C4	334	731.98	4,054.5
PIO0_57	A1	H10	335	681.98	4,156.5
PIO0_58	—	E5	336	631.98	4,054.5
PIO0_59	—	H9	337	581.98	4,156.5

I/O Characteristics

Table 49: PIO Pin Electrical Characteristics

Symbol	Description		Conditions	Minimum	Nominal	Maximum	Units
I_I	Input pin leakage current	I/O Bank 0, 1, 2	V_{IN} = $VCCIO_{max}$ to 0 V			±10	µA
		I/O Bank 3	V_{IN} = $VCCIO_{max}$				
I_{OZ}	Three-state I/O pin (Hi-Z) leakage current		V_O = $VCCIO_{max}$ to 0 V			±10	µA
C_{PIO}	PIO pin input capacitance				6		pF
C_{GBIN}	GBIN global buffer pin input capacitance				6		pF
R_{PULLUP}	Internal PIO pull-up resistance during configuration		VCCIO = 3.3V		40		kΩ
			VCCIO = 2.5V		50		kΩ
			VCCIO = 1.8V		90		kΩ
			VCCIO = 1.5V				kΩ
			VCCIO = 1.2V				kΩ
V_{HYST}	Input hysteresis		VCCIO = 1.5V to 3.3V		50		mV

NOTE: All characteristics are characterized and may or may not be tested on each pin on each device.

Single-ended I/O Characteristics

Table 50: I/O Characteristics (I/O Banks 0, 1, 2 and SPI only) (I/O Bank 3 iCE65L01 only)

I/O Standard	Nominal I/O Bank Supply Voltage	Input Voltage (V)		Output Voltage (V)		Output Current at Voltage (mA)	
		V_{IL}	V_{IH}	V_{OL}	V_{OH}	I_{OL}	I_{OH}
LVCMOS33	3.3V	0.80	2.00	0.4	2.40	8	8
LVCMOS25	2.5V	0.70	1.70	0.4	2.00	6	6
LVCMOS18	1.8V	35% VCCIO	65% VCCIO	0.4	1.40	4	4
LVCMOS15	1.5V	Not supported Use I/O Bank 3		0.4	1.20	2	2

Table 51: I/O Characteristics (I/O Bank 3 and iCE65L04/08 only)

I/O Standard	Supply Voltage	Input Voltage (V)		Output Voltage (V)		I/O Attribute Name	mA at Voltage
		Max. V_{IL}	Min. V_{IH}	Max. V_{OL}	Min. V_{OH}		I_{OL}, I_{OH}
LVCMOS33	3.3V	0.80	2.20	0.4	2.40	SL_LVCMOS33_8	±8
LVCMOS25	2.5V	0.70	1.70	0.4	2.00	SB_LVCMOS25_16	±16
						SB_LVCMOS25_12	±12
						SB_LVCMOS25_8 *	±8
						SB_LVCMOS25_4	±4
LVCMOS18	1.8V	35% VCCIO	65% VCCIO	0.4	VCCIO–0.45	SB_LVCMOS18_10	±10
						SB_LVCMOS18_8	±8
						SB_LVCMOS18_4 *	±4
						SB_LVCMOS18_2	±2
LVCMOS15	1.5V	35% VCCIO	65% VCCIO	25% VCCIO	75% VCCIO	SB_LVCMOS15_4	±4
						SB_LVCMOS15_2 *	±2
MDDR	1.8V	35% VCCIO	65% VCCIO	0.4	VCCIO–0.45	SB_MDDR10	±10
						SB_MDDR8	±8
						SB_MDDR4 *	±4
						SB_MDDR2	±2
SSTL2 (Class 2)	2.5V	VREF–0.180	VREF+0.180	0.35	VTT+0.430	SB_SSTL2_CLASS_2	±16.2
SSTL2 (Class 1)				0.54		SB_SSTL2_CLASS_1	±8.1
SSTL18 (Full)	1.8V	VREF–0.125	VREF+0.125	0.28	VTT+0.280	SB_SSTL18_FULL	±13.4
SSTL18 (Half)				VTT–0.475	VTT+0.475	SB_SSTL18_HALF	±6.7

NOTES:
SSTL2 and SSTL18 I/O standards require the VREF input pin, which is only available on the CB284 package and die-based products.

Programmable Input/Output (PIO) Block

Table 55 provides timing information for the logic in a Programmable Logic Block (PLB), which includes the paths shown in Figure 57 and Figure 58. The timing shown is for the LVCMOS25 I/O standard in all I/O banks. The iCEcube development software reports timing adjustments for other I/O standards.

Figure 57: **Programmable I/O (PIO) Pad-to-Pad Timing Circuit**

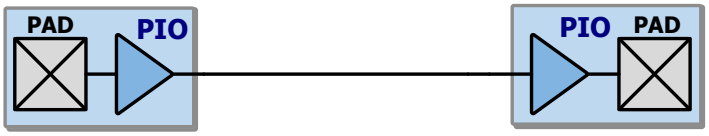


Figure 58: **Programmable I/O (PIO) Sequential Timing Circuit**

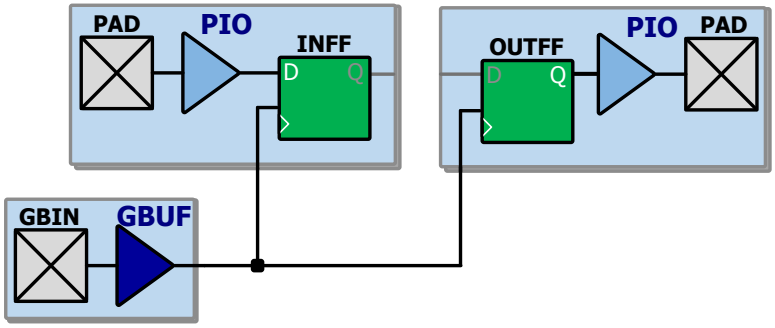


Table 55: **Typical Programmable Input/Output (PIO) Timing (LVCMOS25)**

Symbol	From	To	Device: iCE65	L01	L04, L08			Units
			Power/Speed Grad	–T	–L		–T	
			Nominal VCC	1.2 V	1.0 V	1.2 V	1.2 V	
			Description	Typ.	Typ.	Typ.	Typ.	
		Synchronous Output Paths						
t_{OCKO}	OUTFF clock input	PIO output	Delay from clock input on OUTFF output flip-flop to PIO output pad.	4.7	13.8	7.3	5.6	ns
t_{GBCKIO}	GBIN input	OUTFF clock input	Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to clock input on the PIO OUTFF output flip-flop.	2.1	7.3	3.8	2.6	ns
		Synchronous Input Paths						
t_{SUPDIN}	PIO input	GBIN input	Setup time on PIO input pin to INFF input flip-flop before active clock edge on GBIN input, including interconnect delay.	0	0	0	0	ns
t_{HDPDIN}	GBIN input	PIO input	Hold time on PIO input to INFF input flip-flop after active clock edge on the GBIN input, including interconnect delay.	2.7	7.1	3.6	2.8	ns
		Pad to Pad						
t_{PADIN}	PIO input	Inter-connect	Asynchronous delay from PIO input pad to adjacent interconnect.	2.5	9.5	5.0	3.2	ns
t_{PADO}	Inter-connect	PIO output	Asynchronous delay from adjacent interconnect to PIO output pad including interconnect delay.	4.5	14.6	7.7	6.2	ns

Revision History

Version	Date	Description
2.42	30-MAR-2012	Changed company name. Updated Table 1
2.41	1-AUG-2011	Added VQ100 marking for NVCM programming.
2.4	13-MAY-2011	Added L01 CB121 package Figure 39. Added note "else VCCIO_1 draws current" to JTAG inputs TCK, TDI and TMS do not have the input pull-up resistor and must be tied off to GND when unused, Table 32. Input pin leakage current Table 49 split by bank. QN84 package drawing, Figure 35, added note "underside metal is at ground potential", increased thermal resistance. Added Marking Format and Thermal resistance to CB81 Packag Mechanical Drawing Figure 33. Added coplanarity specification to VQ100 Package Mechanical Drawing Figure 37
2.3	18-OCT-2010	Added L01 CB81 and L08 CB132 packages.
2.2.3	12-OCT-2010	Changed Figure 29: Application Processor Waveforms for SPI Peripheral Mode Configuration Process and Table 60 from 300 µs CRESET_B to 800 µs for iCE65L01/04 and 1200 µs for iCE65L08.
2.2.2	8-OCT-2010	Added iCE65L04 marking specification to Figure 47 CB196 Package Mechanical Drawing.
2.2.1	5-OCT-2010	Changed FSPI_SCK from 0.125 MHz to 1 MHz in SPI Peripheral Configuration Interface and in Table 60.
2.2	6-AUG-2010	Programmable Interconnect section removed.
2.1.1	26-MAY-2010	Switched labels on Figure 53 LVCMOS Output High, VCCIO = 1.8V with VCCIO = 2.5V.
2.1	15-MAR-2010	Added JTAG unused input tie off guideline. Added marking specification and thermal characteristics to package drawings. Added production datasheet for iCE65L01 with timing update, including QN84, VQ100 and CB132. Added NVCM shut-off on SPI configuration. Added non-standard VCCIO operating conditions. Increased the minimum voltage supply specification for LVCMOS33 to 3.14V in Table 48.
2.0.1	12-NOV-2009	Recommended Operation Conditions, Table 47, replaced junction with ambient.
2.0	14-SEPT-2009	Finalized production data sheet for iCE65L04 and iCE65L08. Improved SubLVDS input specification V_{ICM} in Table 52. CS63 and CC72 packages removed and placed in iCE DiCE KGD, Known Good Die datasheet. Added "IBIS Models for I/O Banks 0, 1, 2 and the SPI Bank". Added "Printed Circuit Board Layout Information".
1.5.1	13-JUL-2009	Updated the text in "SPI PROM Requirements" section. Minor label change in Figure 48.
1.5	20-JUN-2009	Updated timing information and added –T high-speed device option (affected Figure 2, Table 48, Table 54, Table 55, Table 56, and Table 61). Added support for 3.3V LVCMOS I/Os in I/O Bank 3 (affected Figure 7, Table 5, Table 7, Table 8, Table 47, Table 48, and Table 51). Added a section about the SPI Peripheral Configuration Interface and timing in Table 60. Added a warning that a Warm Boot operation can only jump to another configuration image that has Warm Boot disabled. Updated configuration image size and configuration time for the iCE65L02 in Table 27 and Table 58. Reduced the minimum voltage supply specification for LVCMOS33 to 2.7V in Table 48. Added information about which power rails can be disconnected without effecting the Power-On Reset (POR) circuit and clarified description of VPP_2V5 pin in Table 36. Added I/O characterization curves (Figure 52, Figure 53, and Figure 54). Minor changes to Figure 20 and Figure 21. Changed timing per Figures 54-58 and Tables 55-57.
1.4.4	25-MAR-2009	Clarified the voltage requirements for the VPP_2V5 pin in Table 36 and notes under Table 48.
1.4.3	9-MAR-2009	Removed volatile-only (-V) product offering from Figure 2. Corrected NC on ball V22, removed it for ball T22 on CB284 package (Figure 48).
1.4.2	27-FEB-2009	Updated Table 14, Table 23, Table 26, Table 30, Table 33, Table 35, and Table 46. Updated I/O Bank 3 information in Table 7 and Table 48.
1.4.1	24-FEB-2009	Based on characterization data, reduced 32KHz operating current by 40% in Table 1, Table 61, and Figure 1. Corrected that SSTL18 standards require VREF pin in Table 7. Correct ball numbers for GBIN4/GBIN5 for CS110 package.
1.4	9-FEB-2009	Added footprint and pinout information for the VQ100 Very-thin Quad Flat Package. Added footprint for iCE65L08 in CB196 (Figure 46) and added Table 43 showing the differences between the 'L04 and 'L08 in the CB196 package. Unified the package footprint nomenclature in the Package and Pinout Information section. Added note to Global Buffer Inputs that the differential clock direct input is not available on the CB132 package. Added tables showing the ball/pin number for various control functions, by package (Table 14, Table 23, Table 26, Table 30, and Table 33). Corrected the GBIN/GBUF designations. GBIN4 and GBIN5 were swapped as were GBIN6 and GBIN7. This change affected all pinout tables and footprint diagrams. Updated and corrected "Differential Global Buffer Input." Tested and corrected the clock-enable and reset connections between global buffers and various resources (Table 11, Table 12, and Table 13). Added "Automatic Global Buffer Insertion, Manual Insertion." Added "Die Cross Reference" section. Improved industrial temperature range by lowering