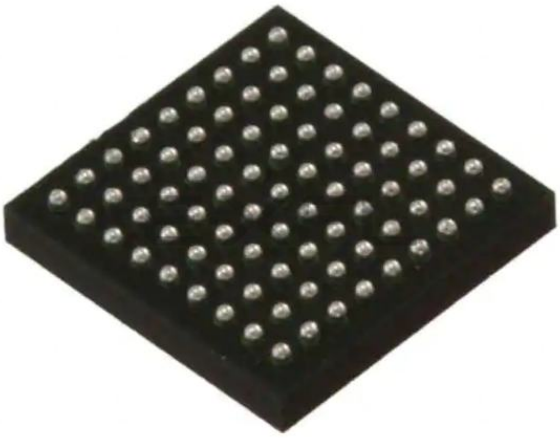

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	160
Number of Logic Elements/Cells	1280
Total RAM Bits	65536
Number of I/O	63
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	81-VFBGA, CSPBGA
Supplier Device Package	81-CSBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice65l01f-tcb81c

Overview

The Lattice Semiconductor iCE65 programmable logic family is specifically designed to deliver the lowest static and dynamic power consumption of any comparable CPLD or FPGA device. iCE65 devices are designed for cost-sensitive, high-volume applications and provide on-chip, nonvolatile configuration memory (NVCM) to customize for a specific application. iCE65 devices can self-configure from a configuration image stored in an external commodity SPI serial Flash PROM or be downloaded from an external processor over an SPI-like serial port.

The three iCE65 components, highlighted in Table 1, deliver from approximately 1K to nearly 8K logic cells and flip-flops while consuming a fraction of the power of comparable programmable logic devices. Each iCE65 device includes between 16 to 32 RAM blocks, each with 4Kbits of storage, for on-chip data storage and data buffering.

As pictured in Figure 1, each iCE65 device consists of four primary architectural elements.

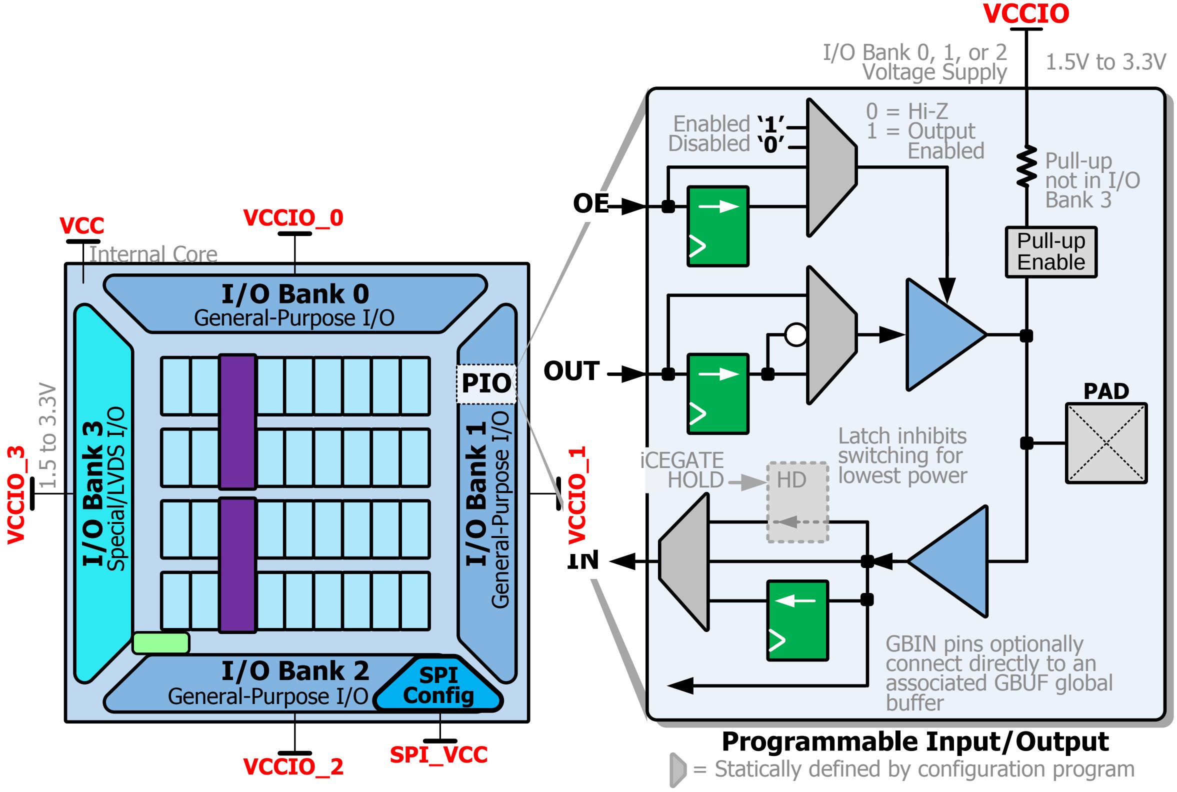
- An array of Programmable Logic Blocks (PLBs)
  - Each PLB contains eight Logic Cells (LCs); each Logic Cell consists of …
    - A fast, four-input look-up table (LUT4) capable of implementing any combinational logic function of up to four inputs, regardless of complexity
    - A 'D'-type flip-flop with an optional clock-enable and set/reset control
    - Fast carry logic to accelerate arithmetic functions such as adders, subtracters, comparators, and counters.
  - Common clock input with polarity control, clock-enable input, and optional set/reset control input to the PLB is shared among all eight Logic Cells
- Two-port, 4Kbit RAM blocks (RAM4K)
  - 256x16 default configuration; selectable data width using programmable logic resources
  - Simultaneous read and write access; ideal for FIFO memory and data buffering applications
  - RAM contents pre-loadable during configuration
- Four I/O banks with independent supply voltage, each with multiple Programmable Input/Output (PIO) blocks
  - LVCMOS I/O standards and LVDS outputs supported in all banks
  - I/O Bank 3 supports additional SSTL, MDDR, LVDS, and SubLVDS I/O standards
- Programmable interconnections between the blocks
  - Flexible connections between all programmable logic functions
  - Eight dedicated low-skew, high-fanout clock distribution networks

Programmable Input/Output Block (PIO)

Programmable Input/Output (PIO) blocks surround the periphery of the device and connect external components to the Programmable Logic Blocks (PLBs) and RAM4K blocks via programmable interconnect. Individual PIO pins are grouped into one of four I/O banks, as shown in Figure 7. I/O Bank 3 has additional capabilities, including LVDS differential I/O and the ability to interface to Mobile DDR memories.

Figure 7 also shows the logic within a PIO pin. When used in an application, a PIO pin becomes a signal input, an output, or a bidirectional I/O pin with a separate direction control input.

Figure 7: Programmable Input/Output (PIO) Pin



I/O Banks

PIO blocks are organized into four separate I/O banks, each with its own voltage supply input, as shown in Table 5. The voltage applied to the VCCIO pin on a bank defines the I/O standard used within the bank. Table 50 and Table 51 describe the I/O drive capabilities and switching thresholds by I/O standard. On iCE65L04 and iCE65L08 devices, I/O Bank 3, along the left edge of the die, is different than the others and supports specialized I/O standards.

I/O Bank Voltage Supply Inputs Support Different I/O Standards

Because each I/O bank has its own voltage supply, iCE65 components become the ideal bridging device between different interface standards. For example, the iCE65 device allows a 1.8V-only processor to interface cleanly with a 3.3V bus interface. The iCE65 device replaces external voltage translators.

Table 5: Supported Voltages by I/O Bank

Bank	Device Edge	Supply Input	3.3V	2.5V	1.8V	1.5V
0	Top	VCCIO_0	Yes	Yes	Yes	Outputs only
1	Right	VCCIO_1	Yes	Yes	Yes	Outputs only
2	Bottom	VCCIO_2	Yes	Yes	Yes	Outputs only
3	Left	VCCIO_3	Yes	Yes	Yes	iCE65L01: Outputs only iCE65L04/08: Yes
SPI	Bottom Right	SPI_VCC	Yes	Yes	Yes	No

Table 8 lists the I/O standards that can co-exist in I/O Bank 3, depending on the VCCIO_3 voltage.

Table 8: **Compatible I/O Standards in I/O Bank 3 of iCE65L04 and iCE65L08**

VCCIO_3 Voltage	3.3V	2.5V	1.8V	1.5V
Compatible I/O Standards	SB_LVCMOS33_8	Any SB_LVCMOS25 SB_SSTL2_Class_2 SB_SSTL2_Class_1 SB_LVDS_INPUT	Any SB_LVCMOS18 SB_SSTL18_FULL SB_SSTL18_HALF SB_MDDR10 SB_MDDR8 SB_MDDR4 SB_MDDR2 SB_LVDS_INPUT	Any SB_LVCMOS15

Programmable Output Drive Strength

Each PIO in I/O Bank 3 offers programmable output drive strength, as listed in Table 8. For the LVCMOS and MDDR I/O standards, the output driver has settings for static drive currents ranging from 2 mA to 16 mA output drive current, depending on the I/O standard and supply voltage.

The SSTL18 and SSTL2 I/O standards offer full- and half-strength drive current options

Differential Inputs and Outputs

All PIO pins support "single-ended" I/O standards, such as LVCMOS. However, iCE65 FPGAs also support differential I/O standards where a single data value is represented by two complementary signals transmitted or received using a pair of PIO pins. The PIO pins in I/O Bank 3 of iCE65L04 and iCE65L08L08 support Low-Voltage Differential Swing (LVDS) and SubLVDS inputs as shown in Figure 8. Differential outputs are available in all four I/O banks.

Differential Inputs Only on I/O Bank 3 of iCE65L04 and iCE65L08

Differential receivers are required for popular applications such as LVDS and LVPECL clock inputs, camera interfaces, and for various telecommunications standards.

Specific pairs of PIO pins in I/O Bank 3 form a differential input. Each pair consists of a DPxxA and DPxxB pin, where "xx" represents the pair number. The DPxxB receives the true version of the signal while the DPxxA receives the complement of the signal. Typically, the resulting signal pair is routed on the printed circuit board (PCB) with matched 50Ω signal impedance. The differential signaling, the low voltage swing, and the matched signal routing are ideal for communicating very-high frequency signals. Differential signals are generally also more tolerant of system noise and generate little EMI themselves.

The LVDS input circuitry requires 2.5V on the VCCIO_3 voltage supply. Similarly, the SubLVDS input circuitry requires 1.8V on the VCCIO_3 voltage supply. For electrical specifications, see "Differential Inputs" on page 100.

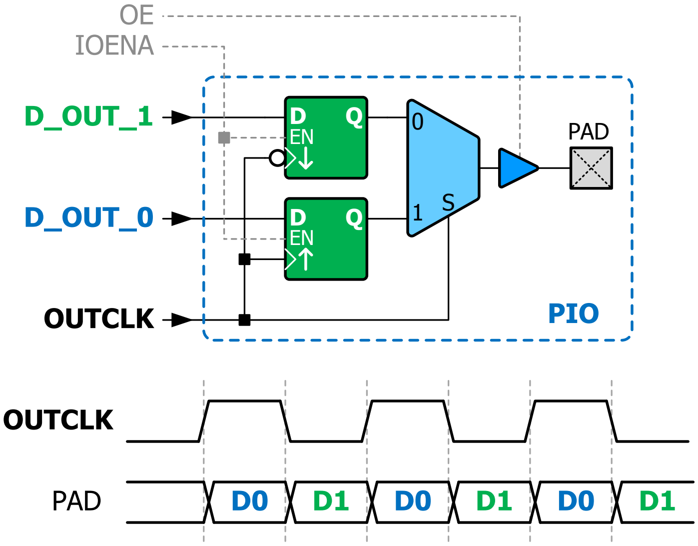
Each differential input pair requires an external 100 Ω termination resistor, as shown in Figure 8.

The PIO pins that make up a differential input pair are indicated with a blue bounding box in the footprint diagrams and in the pinout tables.

Double Data Rate (DDR) Flip-Flops

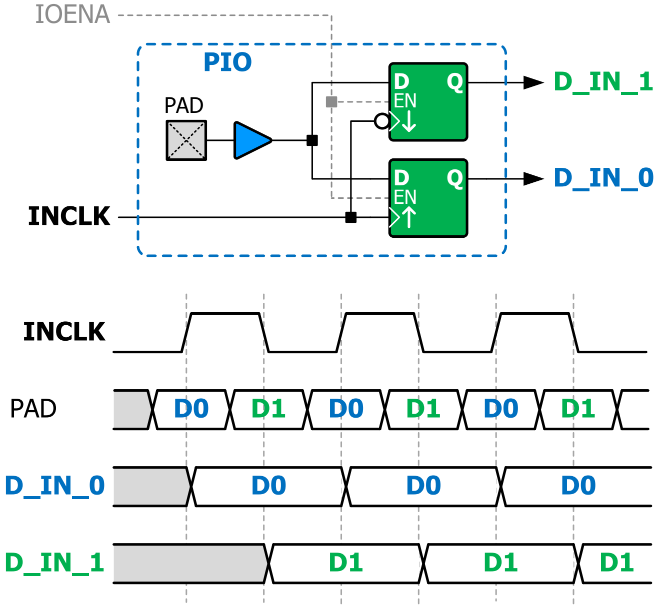
Each individual PIO pin optionally has two sets of double data rate (DDR) flip-flops; one input pair and one output pair. Figure 12 demonstrates the functionality of the output DDR flip-flop. Two signals from within the iCE65 device drive the DDR output flip-flop. The D_OUT_0 signal is clocked by the rising edge of the OUTCLK signal while the D_OUT_1 signal is clocked by the falling edge of the OUTCLK signal, assuming no optional clock polarity inversion. Internally, the two individual flip-flops are multiplexed together before the data appears at the pad, effectively doubling the output data rate.

Figure 12: DDR Output Flip-Flop



Similarly, Figure 13 demonstrates the DDR input flip-flop functionality. A double data rate (DDR) signal arrives at the pad. Internally, one value is clocked by the rising edge of the INCLK signal and another value is clocked by the falling edge of the INCLK signal. The DDR data stream is effectively de-multiplexed within the PIO pin and presented to the programmable interconnect on D_IN_0 and D_IN_1.

Figure 13: DDR Input Flip-Flop



The DDR flip-flops provide several design advantages. Internally within the iCE65 device, the clock frequency is half the effective external data rate. The lower clock frequency eases internal timing, doubling the clock period, and slashes the clock-related power in half.

Table 12 and Table 13 list the connections between a specific global buffer and the inputs on a Programmable I/O (PIO) pair. Although there is no direct connection between a global buffer and a PIO output, such a connection is possible by first connecting through a PLB LUT4 function. Again, all global buffers optionally drive all clock inputs. However, even-numbered global buffers optionally drive the clock-enable input on a PIO pair.

> ⚠ The PIO clock enable connect is different between the iCE65L01/iCE65L04 and iCE65L08.

Table 12: iCE65L01 & iCE65L04: Global Buffer (GBUF) Connections to Programmable I/O (PIO) Pair

Global Buffer	Output Connections	Input Clock	Output Clock	Clock Enable
GBUF0	No (connect through PLB LUT)	Yes	Yes	No
GBUF1		Yes	Yes	Yes
GBUF2		Yes	Yes	No
GBUF3		Yes	Yes	Yes
GBUF4		Yes	Yes	No
GBUF5		Yes	Yes	Yes
GBUF6		Yes	Yes	No
GBUF7		Yes	Yes	Yes

Table 13: iCE64L08: Global Buffer (GBUF) Connections to Programmable I/O (PIO) Pair

Global Buffer	Output Connections	Input Clock	Output Clock	Clock Enable
GBUF0	No (connect through PLB LUT)	Yes	Yes	Yes
GBUF1		Yes	Yes	No
GBUF2		Yes	Yes	Yes
GBUF3		Yes	Yes	No
GBUF4		Yes	Yes	Yes
GBUF5		Yes	Yes	No
GBUF6		Yes	Yes	Yes
GBUF7		Yes	Yes	No

Global Buffer Inputs

The iCE65 component has eight specialized GBIN/PIO pins that are optionally direct inputs to the global buffers, offering the best overall clock characteristics. As shown in Figure 15, each GBIN/PIO pin is a full-featured I/O pin but also provides a direct connection to its associated global buffer. The direct connection to the global buffer bypasses the iCEgate input-blocking latch and other PIO input logic. These special PIO pins are allocated two to an I/O Bank, a total of eight. These pins are labeled GBIN0 through GBIN7, as shown in Figure 14 and the pin locations for each GBIN input appear in Table 14.

Table 14: Global Buffer Input Ball/Pin Number by Package

Global Buffer Input (GBIN)	I/O Bank	**VQ100**	**CB132**	**`L04 CB196**	**`L08 CB196**	**CB284**
GBIN0	0	90	A6	A7	A7	E10
GBIN1		89	A7	E7	E7	E11
GBIN2	1	63	G14	F10	F10	L18
GBIN3		62	F14	G12	G12	K18
GBIN4	2	34	P8	L7	N8	V12
GBIN5		33	P7	P5	M7	V11
GBIN6	3	15	H1	H1	H1	M5
GBIN7		13	G1	G1	H3	L5

- For lowest possible power consumption after configuration, the PROM should also support the `0xB9` Deep Power Down command and the `0xAB` Release from Deep Power-down Command (see Figure 24 and Figure 26). The low-power mode is optional.
- The PROM must be ready to accept commands 10 µs after meeting its power-on conditions. In the PROM data sheet, this may be specified as t_{VSL} or t_{VCSL}. It is possible to use slower PROMs by holding the CRESET_B input Low until the PROM is ready, then releasing CRESET_B, either under program control or using an external power-on reset circuit.

The Lattice iCEman65 development board and associated programming software uses an ST Micro/Numonyx M25Pxx SPI serial Flash PROM.

SPI PROM Size Requirements

Table 27 lists the minimum SPI PROM size required to configure an iCE65 device. Larger PROM sizes are allowed, but not required unless the end application uses the additional space. SPI serial PROM sizes are specified in bits. For each device size, the table shows the required minimum PROM size for "Logic Only" (no BRAM initialization) and "Logic + RAM4K" (RAM4K blocks pre-initialized). Furthermore, the table shows the PROM size for varying numbers of configuration images. Most applications will use a single image. Applications that use the Cold Boot or Warm Boot features may use more than one image.

Table 27: Smallest SPI PROM Size (bits), by Device, by Number of Images

	1 Image		2 Images		3 Images		4 Images	
Device	**Logic Only**	**Logic + RAM4K**	**Logic Only**	**Logic + RAM4K**	**Logic Only**	**Logic + RAM4K**	**Logic Only**	**Logic + RAM4K**
iCE65L01	256K	256K	512K	512K	1M	1M	1M	1M
iCE65L04	512K	1M	1M	2M	2M	2M	2M	4M
iCE65L08	1M	2M	2M	4M	4M	4M	4M	8M

Enabling SPI Configuration Interface

To enable the SPI configuration mode, the SPI_SS_B pin must be allowed to float High. The SPI_SS_B pin has an internal pull-up resistor. If SPI_SS_B is Low, then the iCE65 component defaults to the SPI Slave configuration mode.

SPI Master Configuration Process

The iCE65 SPI Master Configuration Interface supports a variety of modern, high-density, low-cost SPI serial Flash PROMs. Most modern SPI PROMs include a power-saving Deep Power-down mode. The iCE65 component exploits this mode for additional system power savings.

The iCE65 SPI interface starts by driving SPI_SS_B Low, and then sends a Release from Power-down command to the SPI PROM, hexadecimal command code `0xAB`. Figure 24 provides an example waveform. This initial command wakes up the SPI PROM if it is already in Deep Power-down mode. If the PROM is not in Deep Power-down mode, the extra command has no adverse affect other than that it requires a few additional microseconds during the configuration process. The iCE65 device transmits data on the SPI_SO output, on the falling edge of the SPI_SCK output. The SPI PROM does not provide any data to the iCE65 device's SPI_SI input. After sending the last command bit, the iCE65 device de-asserts SPI_SS_B High, completing the command. The iCE65 device then waits a minimum of 10 µS before sending the next SPI PROM command.

Supported JTAG Commands

The JTAG interface supports the IEEE 1149.1 mandatory instructions, including EXTEST, SAMPLE/PRELOAD, and BYPASS.

Package and Pinout Information

Maximum User I/O Pins by Package and by I/O Bank

Table 34 lists the maximum number of user-programmable I/O pins by package, with additional detail showing user I/O pins by I/O bank. In some cases, a smaller iCE65 device is packaged in a larger package with unconnected (N.C.) pins or balls, resulting in fewer overall I/O pins. See Table 35 for device-specific I/O counts by package.

Table 34: **User I/O by Package, by I/O Bank**

	CB81	QN84	VQ100	CB132	CB196	CB284
Package Leads	81	84	100	132	196	284
Package Body (mm)	5 x 5	7 x 7	14 x 14	8 x 8	8 x 8	12 x 12
Ball Array (balls)	9 x 9	N/A	N/A	14 x 14	14 x 14	22 x 22
Ball/Lead Pitch (mm)	0.5	0.5	0.5	0.5	0.5	0.5
Maximum user I/O, all I/O banks	63	67	72	95	150	222
PIO Pins in Bank 0	17	17	19	26	37	60
PIO Pins in Bank 1	16	17	19	21	38	55
PIO Pins in Bank 2	12	11	12	20	35	53
PIO Pins in Bank 3	18	18	18	24	36	50
PIO Pins in SPI Interface	4	4	4	4	4	4

Printed Circuit Board Layout Information

For information on how to use the iCE65 packages on a printed circuit board (PCB) design, consult the following application note.

- AN010: iCE65 Printed Circuit Board (PCB Layout) Guidelines

Maximum User I/O by Device and Package

Table 35 lists the maximum available user I/O by device and by and package type. Not all devices are available in all packages. Similarly, smaller iCE65 devices may have unconnected balls in some packages. Devices sharing a common package have similar footprints.

Table 35: **Maximum User I/O by Device and Package**

Package	Device		
	iCE65L01	**iCE65L04**	**iCE65L08**
CB81	63	—	—
QN84	67	—	—
VQ100	72	72	
CB132	93	95	—
CB196	—	150	150
CB284	—	176	222

CB81 Chip-Scale Ball-Grid Array

The CB81 package is a full ball grid array with 0.5 mm ball pitch. The iCE65L01 device is available in this package.

Footprint Diagram

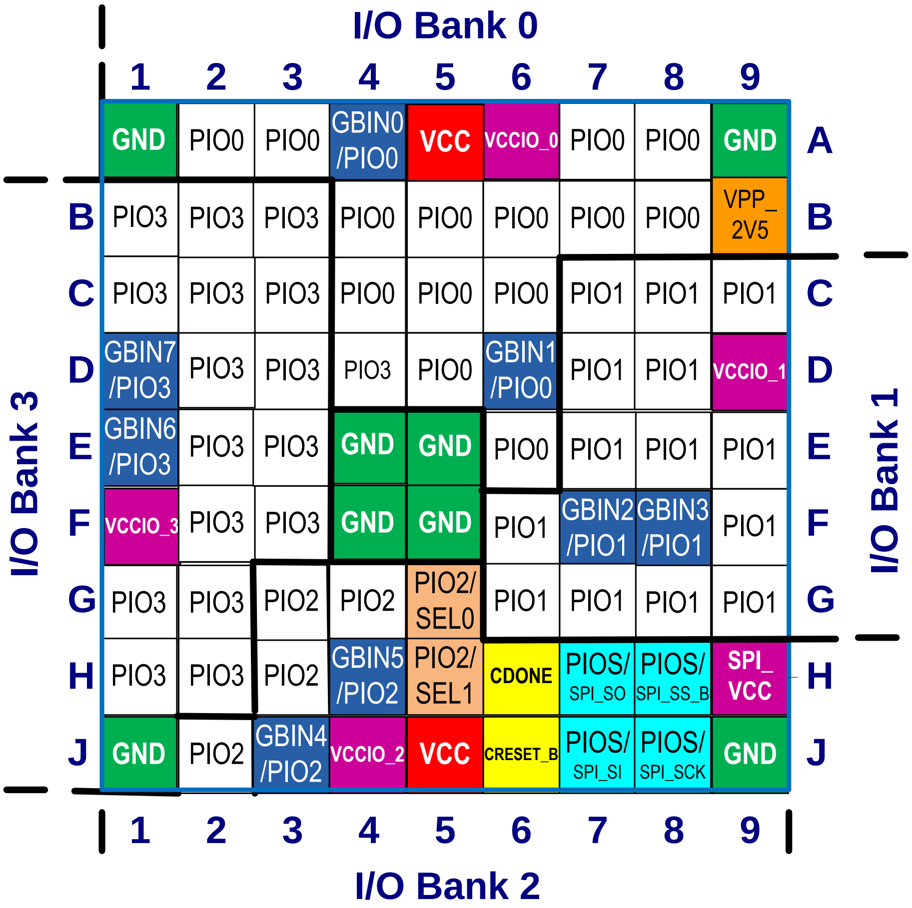
Figure 32 shows the iCE65 footprint diagram for the CB81 package.

Figure 31 shows the conventions used in the diagram.

Also see Table 37 for a complete, detailed pinout for the 81-ball BGA package.

The signal pins are also grouped into the four I/O Banks and the SPI interface.

***Figure 32*: iCE65L01 CB81 Chip-Scale BGA Footprint (Top View)**



	1	2	3	4	5	6	7	8	9
A	GND	PIO0	PIO0	GBIN0/PIO0	VCC	VCCIO_0	PIO0	PIO0	GND
B	PIO3	PIO3	PIO3	PIO0	PIO0	PIO0	PIO0	PIO0	VPP_2V5
C	PIO3	PIO3	PIO3	PIO0	PIO0	PIO0	PIO1	PIO1	PIO1
D	GBIN7/PIO3	PIO3	PIO3	PIO3	PIO0	GBIN1/PIO0	PIO1	PIO1	VCCIO_1
E	GBIN6/PIO3	PIO3	PIO3	GND	GND	PIO0	PIO1	PIO1	PIO1
F	VCCIO_3	PIO3	PIO3	GND	GND	PIO1	GBIN2/PIO1	GBIN3/PIO1	PIO1
G	PIO3	PIO3	PIO2	PIO2	PIO2/SEL0	PIO1	PIO1	PIO1	PIO1
H	PIO3	PIO3	PIO2	GBIN5/PIO2	PIO2/SEL1	CDONE	PIOS/SPI_SO	PIOS/SPI_SS_B	SPI_VCC
J	GND	PIO2	GBIN4/PIO2	VCCIO_2	VCC	CRESET_B	PIOS/SPI_SI	PIOS/SPI_SCK	GND

QN84 Quad Flat Pack No-Lead

The QN84 is a Quad Flat Pack No-Lead package with a 0.5 mm pad pitch.

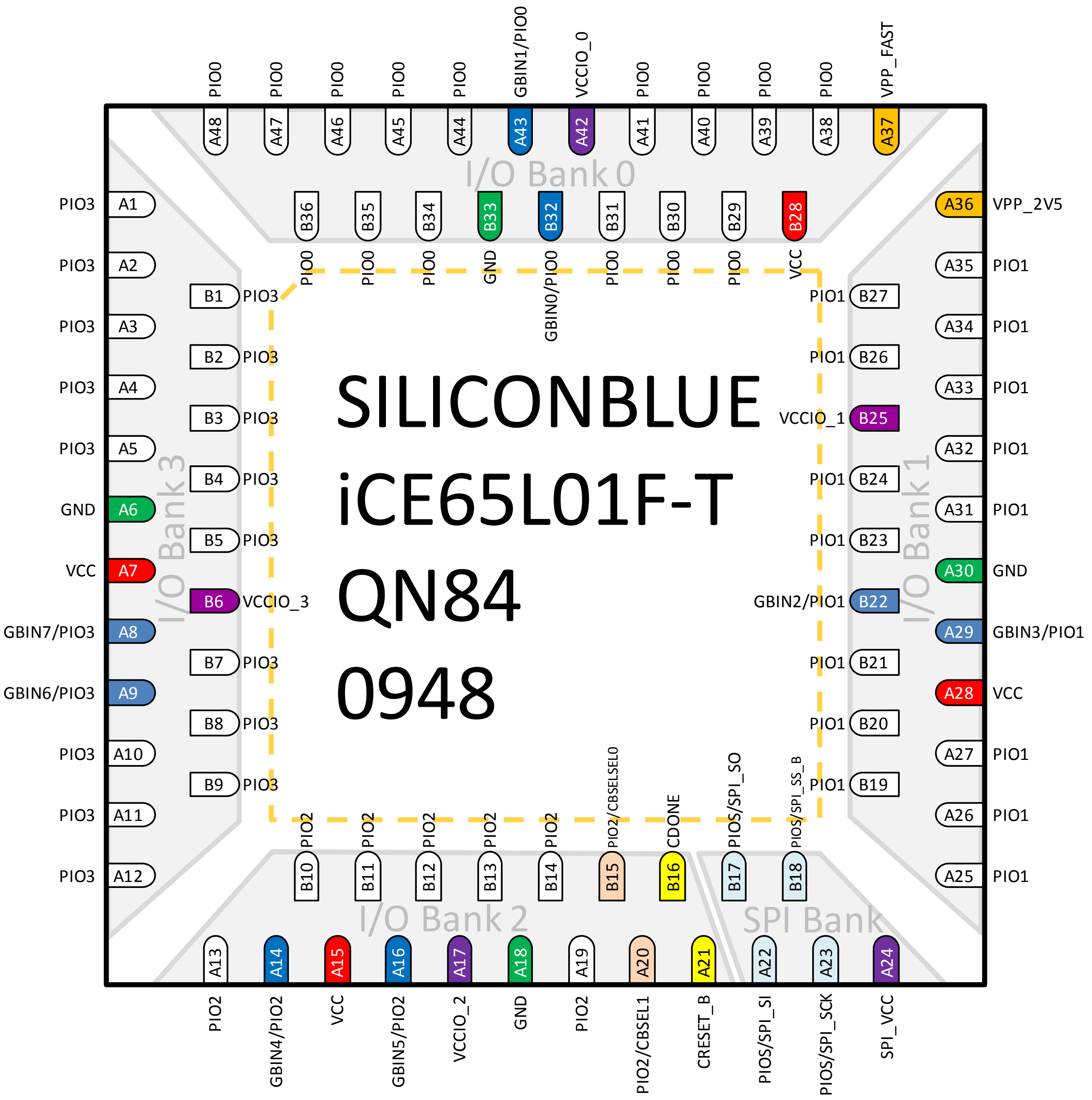
Footprint Diagram

Figure 34 shows the iCE65 footprint diagram for the QN84 package.

Also see Table 38 for a complete, detailed pinout for the QN84 package.

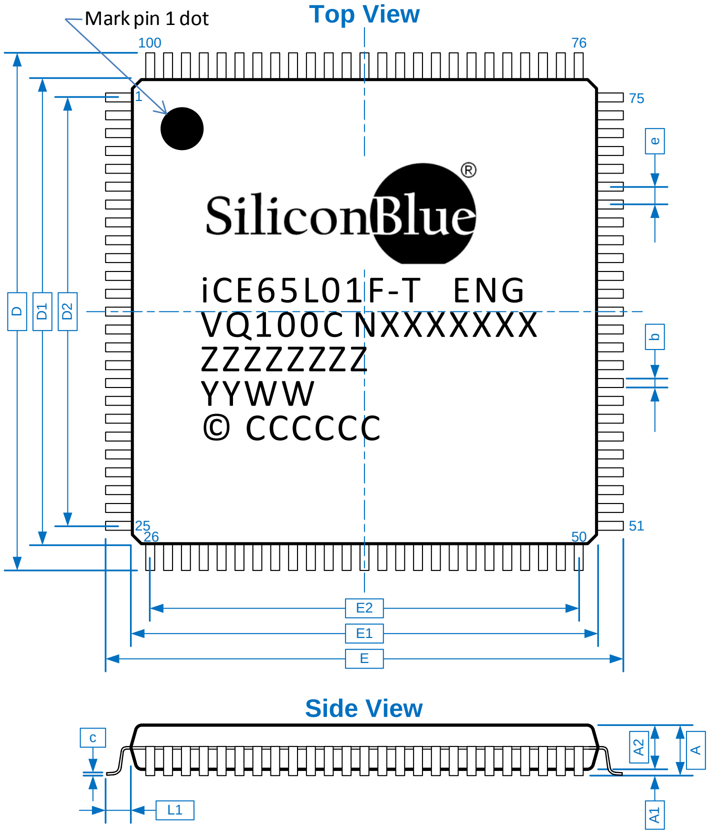
The signal pins are also grouped into the four I/O Banks and the SPI interface.

Figure 34: **iCE65 QN84 Quad Flat Pack No-Lead Footprint (Top View)**



Ball Function	Ball Number	Pin Type	Bank
PIO2	B14	PIO	2
PIO2/CBSEL0	B15	PIO	2
PIO2/CBSEL1	A20	PIO	2
VCCIO_2	A17	PIO	2
GBIN6/PIO3	A9	GBIN	3
GBIN7/PIO3	A8	GBIN	3
PIO3	A1	PIO	3
PIO3	A2	PIO	3
PIO3	A3	PIO	3
PIO3	A4	PIO	3
PIO3	A5	PIO	3
PIO3	A10	PIO	3
PIO3	A11	PIO	3
PIO3	A12	PIO	3
PIO3	B1	PIO	3
PIO3	B2	PIO	3
PIO3	B3	PIO	3
PIO3	B4	PIO	3
PIO3	B5	PIO	3
PIO3	B7	PIO	3
PIO3	B8	PIO	3
PIO3	B9	PIO	3
VCCIO_3	B6	VCCIO	3
PIOS/SPI_SO	B17	SPI	SPI
PIOS/SPI_SI	A22	SPI	SPI
PIOS/SPI_SCK	A23	SPI	SPI
PIOS/SPI_SS_B	B18	SPI	SPI
SPI_VCC	A24	SPI	SPI
GND	A6	GND	GND
GND	A18	GND	GND
GND	A30	GND	GND
GND	B33	GND	GND
VCC	A7	VCC	VCC
VCC	A15	VCC	VCC
VCC	A28	VCC	VCC
VCC	B28	VCC	VCC
VPP_2V5	A36	VPP	VPP
VPP_FAST	A37	VPP	VPP

Figure 38: VQ100 Package Mechanical Drawing: NVCM Programmed Device Marking



Description		Symbol	Min.	Nominal	Max.	Units
Leads per Edge	X			25		Leads
	Y			25		
Number of Signal Leads		n		100		
Maximum Size (lead tip to lead tip)	X	E	—	16.0	—	mm
	Y	D	—	16.0	—	
Body Size	X	E1	—	14.0	—	
	Y	D1	—	14.0	—	
Edge Pin Center to Center	X	E2	—	12.0	—	
	Y	D2	—	12.0	—	
Lead Pitch		e	—	0.50	—	
Lead Width		b	0.17	0.20	0.27	
Total Package Height		A	—	1.20	—	
Stand Off		A1	0.05	—	0.15	
Body Thickness		A2	0.95	1.00	1.05	
Lead Length		L1	—	1.00	—	
Lead Thickness		c	0.09	—	0.20	
Coplanarity			—	0.08	—	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65L01F	Part number
	-T	Power/Speed
	ENG	Engineering
3	VQ100C NXXXXXXX	Package type and Lot number
4	ZZZZZZZZ	NVCM Program. code
5	YYWW	Date Code
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θJA (°C/W)	
0 LFM	200 LFM
38	32

CB132 Chip-Scale Ball-Grid Array

The CB132 package is a partially-populated ball grid array with 0.5 mm ball pitch. The empty ball rings simplify PCB layout. The iCE65L01, iCE65L04 and iCE65L08 devices are available in this package.

Footprint Diagram

Figure 41, Figure 42 and

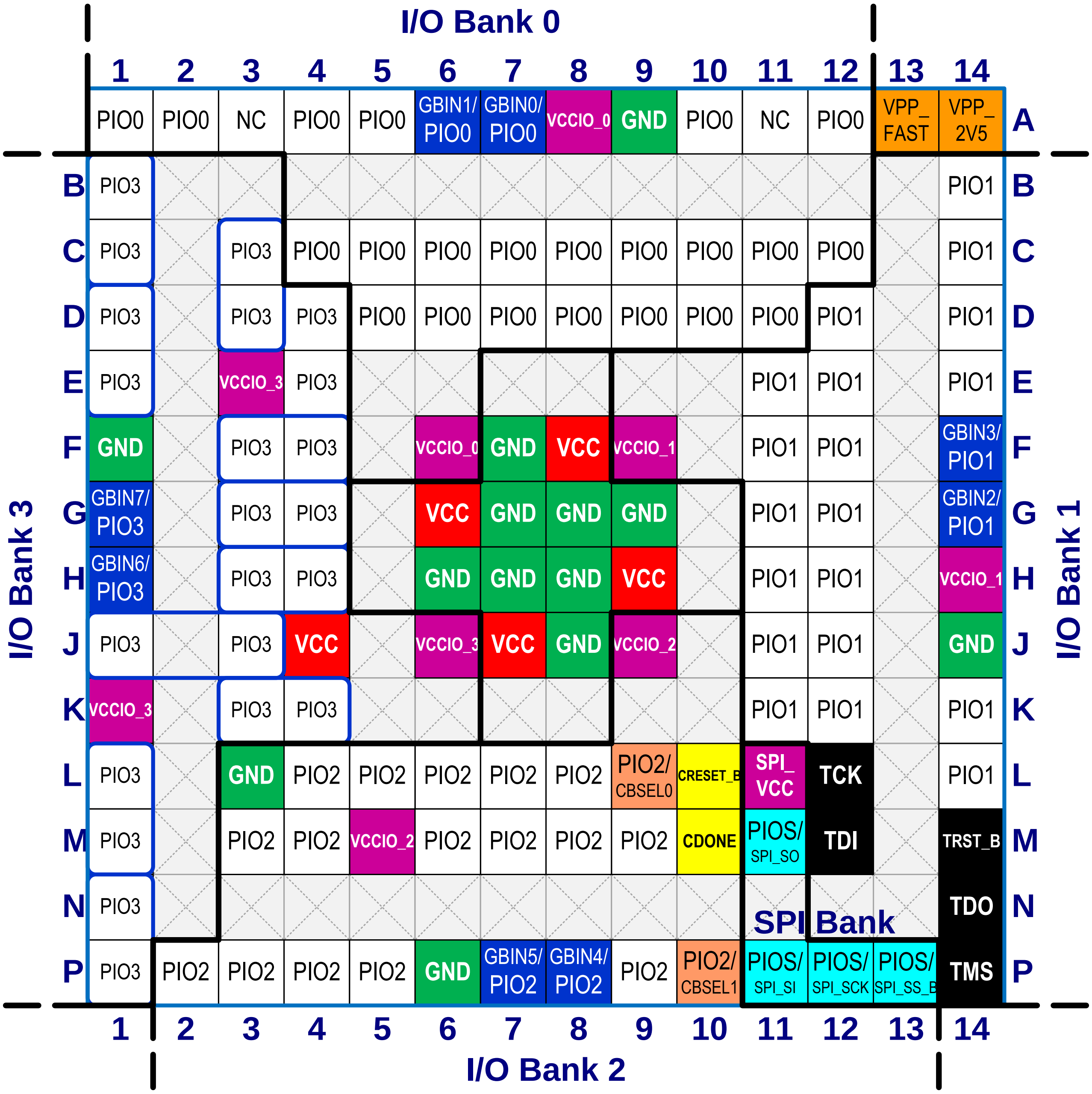
Figure 43 show the iCE65 footprint diagrams for the CB132 package in iCE65L01, iCE65L04 and iCE65L08 devices. See Figure 48 for the “universal” chip-scale BGA footprint for the CB132 and CB284 packages. The 8 x 8 mm CB132 package fits within the same ball pattern as the 12 x 12 mm CB284 package.

Figure 31 shows the conventions used in the diagram.

Also see Table 41 for a complete, detailed pinout for the 132-ball BGA package.

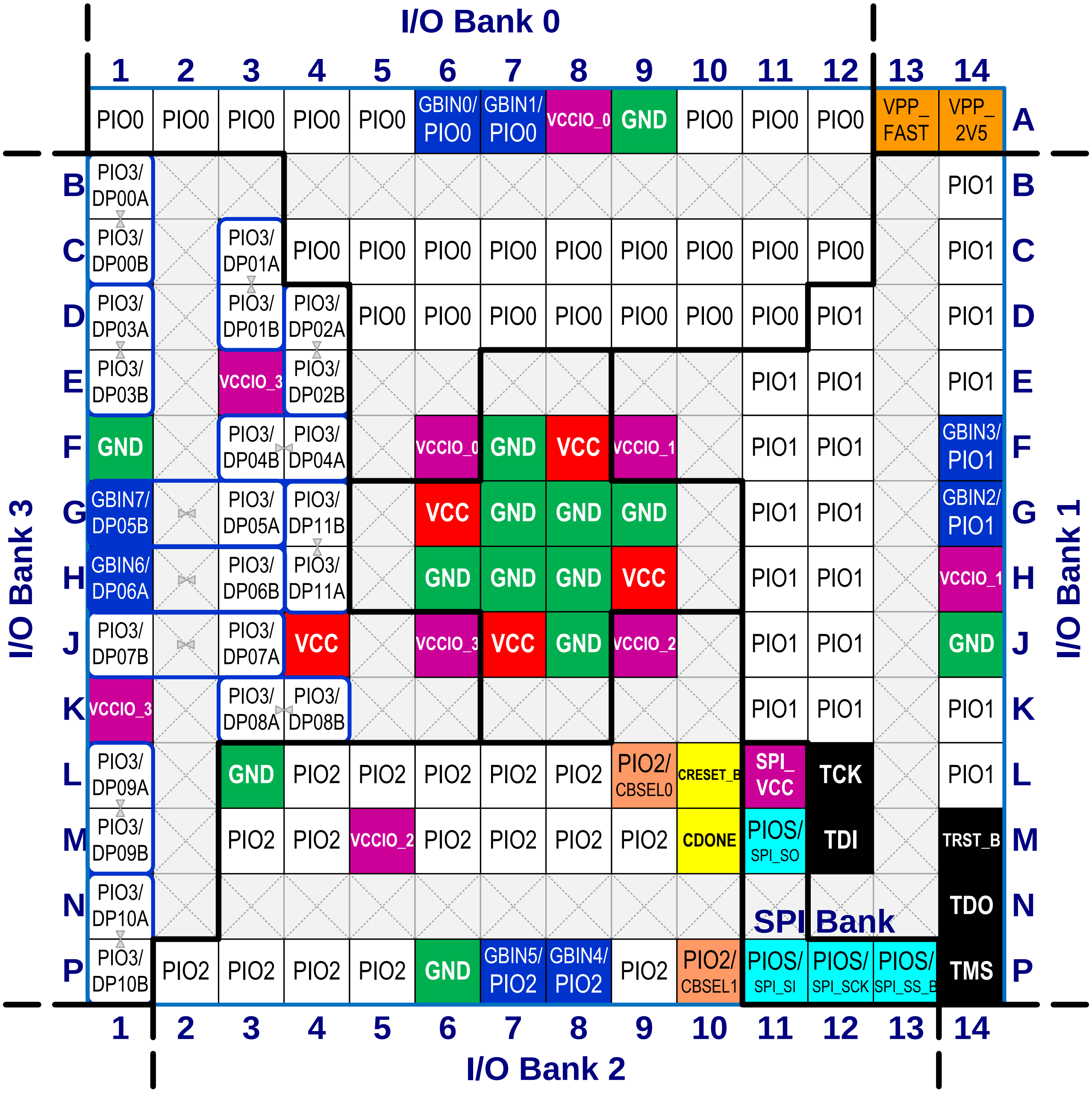
The signal pins are also grouped into the four I/O Banks and the SPI interface.

***Figure 41*: iCE65L01 CB132 Chip-Scale BGA Footprint (Top View)**



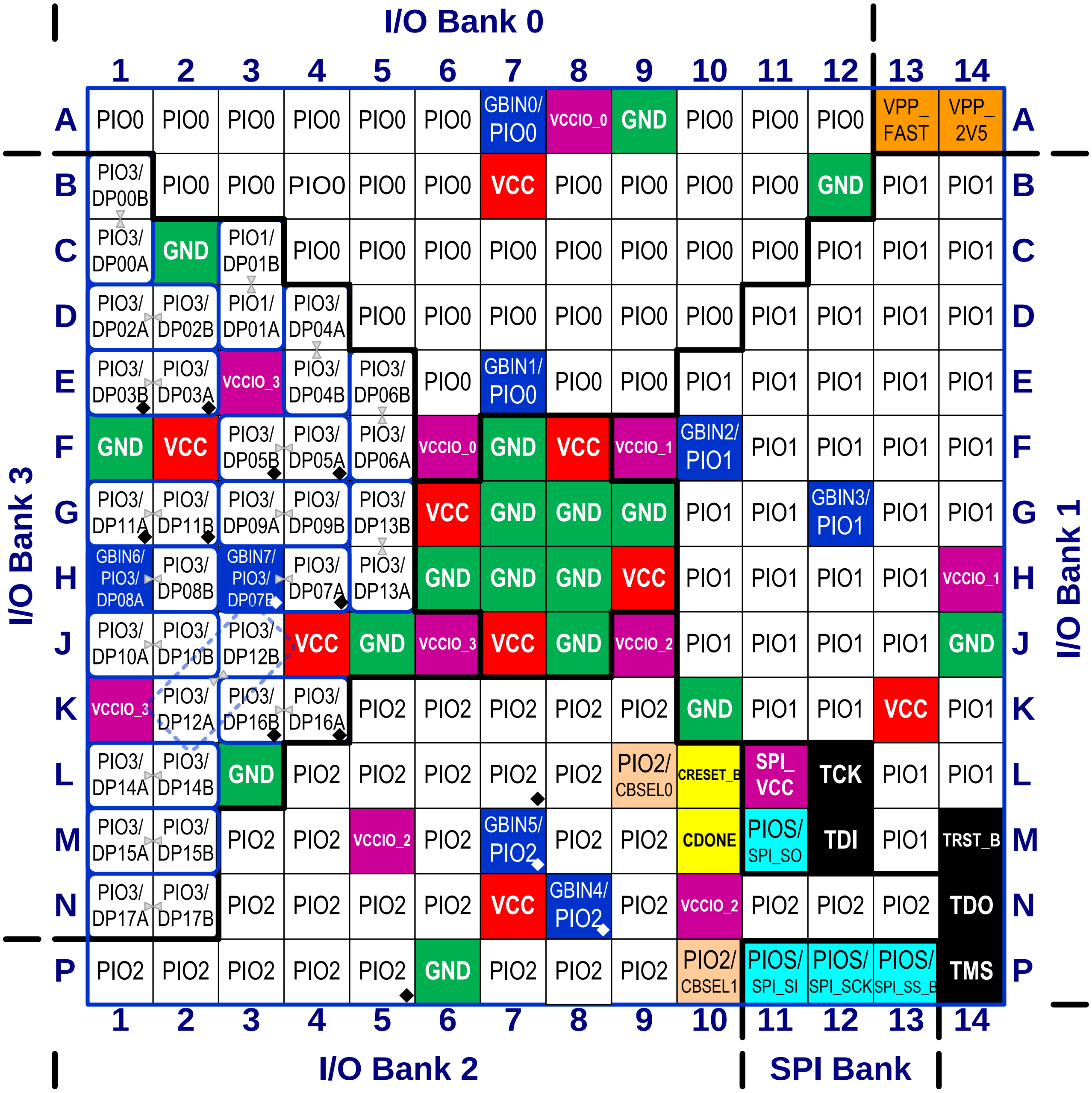
	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	PIO0	PIO0	NC	PIO0	PIO0	GBIN1/ PIO0	GBIN0/ PIO0	VCCIO_0	GND	PIO0	NC	PIO0	VPP_ FAST	VPP_ 2V5
B	PIO3													PIO1
C	PIO3		PIO3	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0		PIO1
D	PIO3		PIO3	PIO3	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0	PIO1		PIO1
E	PIO3		VCCIO_3	PIO3							PIO1	PIO1		PIO1
F	GND		PIO3	PIO3		VCCIO_0	GND	VCC	VCCIO_1		PIO1	PIO1		GBIN3/ PIO1
G	GBIN7/ PIO3		PIO3	PIO3		VCC	GND	GND	GND		PIO1	PIO1		GBIN2/ PIO1
H	GBIN6/ PIO3		PIO3	PIO3		GND	GND	GND	VCC		PIO1	PIO1		VCCIO_1
J	PIO3		PIO3	VCC		VCCIO_3	VCC	GND	VCCIO_2		PIO1	PIO1		GND
K	VCCIO_3		PIO3	PIO3							PIO1	PIO1		PIO1
L	PIO3		GND	PIO2	PIO2	PIO2	PIO2	PIO2	PIO2/ CBSEL0	CRESET_B	SPI_ VCC	TCK		PIO1
M	PIO3		PIO2	PIO2	VCCIO_2	PIO2	PIO2	PIO2	PIO2	CDONE	PIOS/ SPI_SO	TDI		TRST_B
N	PIO3													TDO
P	PIO3	PIO2	PIO2	PIO2	PIO2	GND	GBIN5/ PIO2	GBIN4/ PIO2	PIO2	PIO2/ CBSEL1	PIOS/ SPI_SI	PIOS/ SPI_SCK	PIOS/ SPI_SS_B	TMS

Figure 43: **iCE65L08 CB132 Chip-Scale BGA Footprint (Top View)**



	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	PIO0	PIO0	PIO0	PIO0	PIO0	GBIN0/ PIO0	GBIN1/ PIO0	VCCIO_0	GND	PIO0	PIO0	PIO0	VPP_ FAST	VPP_ 2V5
B	PIO3/ DP00A													PIO1
C	PIO3/ DP00B		PIO3/ DP01A	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0		PIO1
D	PIO3/ DP03A		PIO3/ DP01B	PIO3/ DP02A	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0	PIO1		PIO1
E	PIO3/ DP03B		VCCIO_3	PIO3/ DP02B							PIO1	PIO1		PIO1
F	GND		PIO3/ DP04B	PIO3/ DP04A		VCCIO_0	GND	VCC	VCCIO_1		PIO1	PIO1		GBIN3/ PIO1
G	GBIN7/ DP05B		PIO3/ DP05A	PIO3/ DP11B		VCC	GND	GND	GND		PIO1	PIO1		GBIN2/ PIO1
H	GBIN6/ DP06A		PIO3/ DP06B	PIO3/ DP11A		GND	GND	GND	VCC		PIO1	PIO1		VCCIO_1
J	PIO3/ DP07B		PIO3/ DP07A	VCC		VCCIO_3	VCC	GND	VCCIO_2		PIO1	PIO1		GND
K	VCCIO_3		PIO3/ DP08A	PIO3/ DP08B							PIO1	PIO1		PIO1
L	PIO3/ DP09A		GND	PIO2	PIO2	PIO2	PIO2	PIO2	PIO2/ CBSEL0	CRESET_B	SPI_ VCC	TCK		PIO1
M	PIO3/ DP09B		PIO2	PIO2	VCCIO_2	PIO2	PIO2	PIO2	PIO2	CDONE	PIOS/ SPI_SO	TDI		TRST_B
N	PIO3/ DP10A													TDO
P	PIO3/ DP10B	PIO2	PIO2	PIO2	PIO2	GND	GBIN5/ PIO2	GBIN4/ PIO2	PIO2	PIO2/ CBSEL1	PIOS/ SPI_SI	PIOS/ SPI_SCK	PIOS/ SPI_SS_B	TMS

Figure 46: **iCE65L08 CB196 Chip-Scale BGA Footprint (Top View)**



	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0	GBIN0/ PIO0	VCCIO_0	GND	PIO0	PIO0	PIO0	VPP_ FAST	VPP_ 2V5
B	PIO3/ DP00B	PIO0	PIO0	PIO0	PIO0	PIO0	VCC	PIO0	PIO0	PIO0	PIO0	GND	PIO1	PIO1
C	PIO3/ DP00A	GND	PIO1/ DP01B	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0	PIO1	PIO1	PIO1
D	PIO3/ DP02A	PIO3/ DP02B	PIO1/ DP01A	PIO3/ DP04A	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0	PIO1	PIO1	PIO1	PIO1
E	PIO3/ DP03B	PIO3/ DP03A	VCCIO_3	PIO3/ DP04B	PIO3/ DP06B	PIO0	GBIN1/ PIO0	PIO0	PIO0	PIO1	PIO1	PIO1	PIO1	PIO1
F	GND	VCC	PIO3/ DP05B	PIO3/ DP05A	PIO3/ DP06A	VCCIO_0	GND	VCC	VCCIO_1	GBIN2/ PIO1	PIO1	PIO1	PIO1	PIO1
G	PIO3/ DP11A	PIO3/ DP11B	PIO3/ DP09A	PIO3/ DP09B	PIO3/ DP13B	VCC	GND	GND	GND	PIO1	PIO1	GBIN3/ PIO1	PIO1	PIO1
H	GBIN6/ PIO3/ DP08A	PIO3/ DP08B	GBIN7/ PIO3/ DP07B	PIO3/ DP07A	PIO3/ DP13A	GND	GND	GND	VCC	PIO1	PIO1	PIO1	PIO1	VCCIO_1
J	PIO3/ DP10A	PIO3/ DP10B	PIO3/ DP12B	VCC	GND	VCCIO_3	VCC	GND	VCCIO_2	PIO1	PIO1	PIO1	PIO1	GND
K	VCCIO_3	PIO3/ DP12A	PIO3/ DP16B	PIO3/ DP16A	PIO2	PIO2	PIO2	PIO2	PIO2	GND	PIO1	PIO1	VCC	PIO1
L	PIO3/ DP14A	PIO3/ DP14B	GND	PIO2	PIO2	PIO2	PIO2	PIO2	PIO2/ CBSEL0	CRESET_B	SPI_ VCC	TCK	PIO1	PIO1
M	PIO3/ DP15A	PIO3/ DP15B	PIO2	PIO2	VCCIO_2	PIO2	GBIN5/ PIO2	PIO2	PIO2	CDONE	PIOS/ SPI_SO	TDI	PIO1	TRST_B
N	PIO3/ DP17A	PIO3/ DP17B	PIO2	PIO2	PIO2	PIO2	VCC	GBIN4/ PIO2	PIO2	VCCIO_2	PIO2	PIO2	PIO2	TDO
P	PIO2	PIO2	PIO2	PIO2	PIO2	GND	PIO2	PIO2	PIO2	PIO2/ CBSEL1	PIOS/ SPI_SI	PIOS/ SPI_SCK	PIOS/ SPI_SS_B	TMS

Pinout Table

Table 42 provides a detailed pinout table for the iCE65L04 in the CB196 chip-scale BGA package. Pins are generally arranged by I/O bank, then by ball function. The pinout for the iCE65L08 is different than the iCE64L04 pinout.

⚠ Although both the iCE65L04 and iCE65L08 are both available in the CB196 package and *almost* completely pin compatible, there are differences as shown in Table 43.

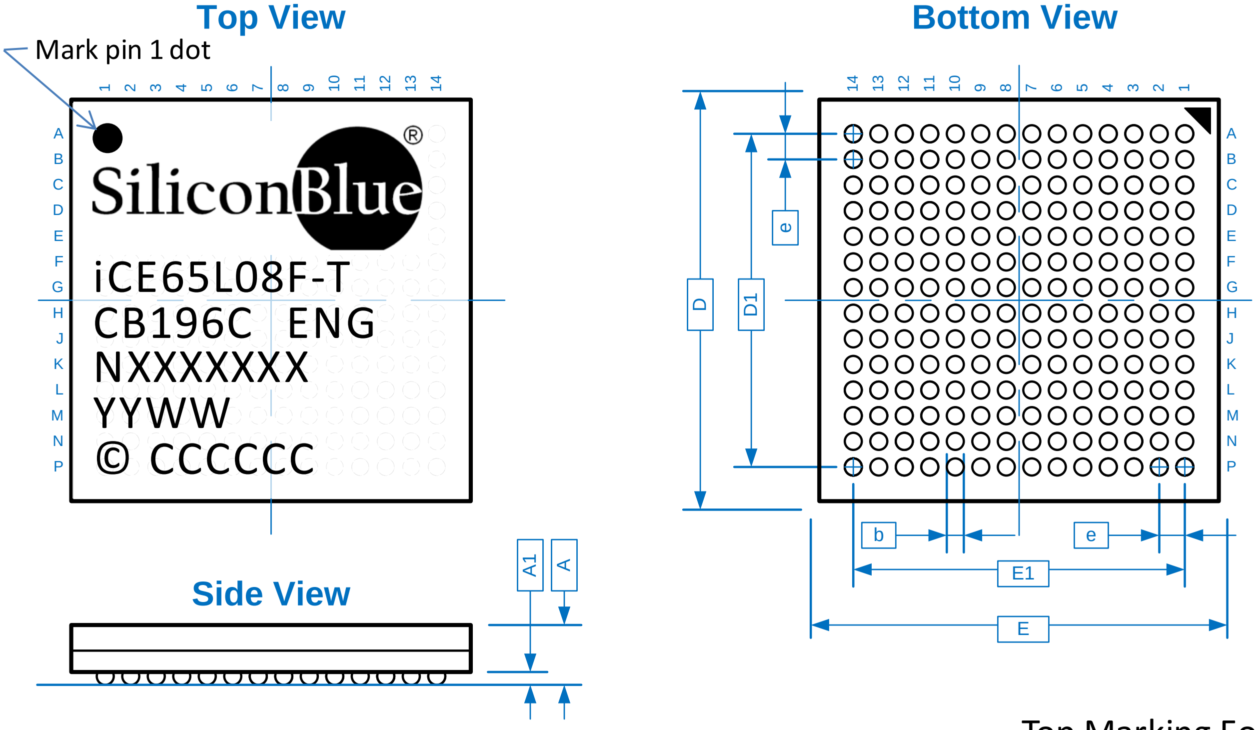
Table 42: **iCE65L04 CB196 Chip-scale BGA Pinout Table**

Ball Function	Ball Number	Pin Type	Bank
GBIN0/PIO0	A7	GBIN	0
GBIN1/PIO0	E7	GBIN	0
PIO0	A1	PIO	0
PIO0	A2	PIO	0
PIO0	A3	PIO	0
PIO0	A4	PIO	0

Ball Function	Ball Number	Pin Type	Bank
PIO3/DP13A	H5	DPIO	3
PIO3/DP13B	G5	DPIO	3
PIO3/DP14A	L1	DPIO	3
PIO3/DP14B	L2	DPIO	3
PIO3/DP15A	M1	DPIO	3
PIO3/DP15B	M2	DPIO	3
PIO3/DP16A (◆)	***iCE65L04:*** K3 ***iCE65L08:*** K4	DPIO	3
PIO3/DP16B (◆)	***iCE65L08:*** K4 ***iCE65L08:*** K3	DPIO	3
PIO3/DP17A	N1	DPIO	3
PIO3/DP17B	N2	DPIO	3
VCCIO_3	E3	VCCIO	3
VCCIO_3	J6	VCCIO	3
VCCIO_3	K1	VCCIO	3
PIOS/SPI_SO	M11	SPI	SPI
PIOS/SPI_SI	P11	SPI	SPI
PIOS/SPI_SCK	P12	SPI	SPI
PIOS/SPI_SS_B	P13	SPI	SPI
SPI_VCC	L11	SPI	SPI
GND	A9	GND	GND
GND	B12	GND	GND
GND	C2	GND	GND
GND	F1	GND	GND
GND	F7	GND	GND
GND	G7	GND	GND
GND	G8	GND	GND
GND	G9	GND	GND
GND	H6	GND	GND
GND	H7	GND	GND
GND	H8	GND	GND
GND	J5	GND	GND
GND	J8	GND	GND
GND	J14	GND	GND
GND	K10	GND	GND
GND	L3	GND	GND
GND	P6	GND	GND
VCC	B7	VCC	VCC
VCC	F2	VCC	VCC
VCC	F8	VCC	VCC
VCC	G6	VCC	VCC
VCC	H9	VCC	VCC
VCC	J4	VCC	VCC
VCC	J7	VCC	VCC
VCC	K13	VCC	VCC
VCC	N7	VCC	VCC
VPP_2V5	A14	VPP	VPP
VPP_FAST	A13	VPP	VPP

(b) iCE65L08 CB196 Package Mechanical Drawing

CB196: 8 x8 mm, 196-ball, 0.5 mm ball-pitch, fully-populated, chip-scale ball grid array



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			14		Columns
Number of Ball Rows	Y			14		Rows
Number of Signal Balls		n		196		Balls
Body Size	X	E	7.90	8.00	8.10	mm
	Y	D	7.90	8.00	8.10	
Ball Pitch		e	—	0.50	—	
Ball Diameter		b	0.27	—	0.37	
Edge Ball Center to Center	X	E1	—	6.50	—	
	Y	D1	—	6.50	—	
Package Height		A	—	—	1.00	
Stand Off		A1	0.16	—	0.26	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65L08F	Part number
	-T	Power/Speed
3	CB196C	Package type
	ENG	Engineering
4	NXXXXXXX	Lot Number
5	YYWW	Date Code
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
42	34

	Ball Number	Pin Type by Device			
Ball Function	iCE65L04 iCE65L08	iCE65L04	iCE65L08	Bank	CB132 Ball Equivalent
PIO0	E15	PIO	PIO	0	A11
PIO0	E16	PIO	PIO	0	A12
PIO0	G8	PIO	PIO	0	C4
PIO0	G9	PIO	PIO	0	C5
PIO0	G10	PIO	PIO	0	C6
PIO0	G11	PIO	PIO	0	C7
PIO0	G12	PIO	PIO	0	C8
PIO0	G13	PIO	PIO	0	C9
PIO0	G14	PIO	PIO	0	C10
PIO0	G15	PIO	PIO	0	C11
PIO0	G16	PIO	PIO	0	C12
PIO0	H9	PIO	PIO	0	D5
PIO0	H10	PIO	PIO	0	D6
PIO0	H11	PIO	PIO	0	D7
PIO0	H12	PIO	PIO	0	D8
PIO0	H13	PIO	PIO	0	D9
PIO0	H14	PIO	PIO	0	D10
PIO0	H15	PIO	PIO	0	D11
VCCIO_0	A8	VCCIO	VCCIO	0	—
VCCIO_0	A21	VCCIO	VCCIO	0	—
VCCIO_0	E12	VCCIO	VCCIO	0	A8
VCCIO_0	K10	VCCIO	VCCIO	0	F6
GBIN2/PIO1	L18	GBIN	GBIN	1	G14
GBIN3/PIO1	K18	GBIN	GBIN	1	F14
PIO1 (●)	A22	N.C.	PIO	1	—
PIO1 (●)	AA22	N.C.	PIO	1	—
PIO1 (●)	B22	N.C.	PIO	1	—
PIO1	C20	PIO	PIO	1	—
PIO1 (●)	C22	N.C.	PIO	1	—
PIO1	D20	PIO	PIO	1	—
PIO1 (●)	D22	N.C.	PIO	1	—
PIO1	E20	PIO	PIO	1	—
PIO1 (●)	E22	N.C.	PIO	1	—
PIO1	F18	PIO	PIO	1	B14
PIO1	F20	PIO	PIO	1	—
PIO1 (●)	F22	N.C.	PIO	1	—
PIO1	G18	PIO	PIO	1	C14
PIO1	G20	PIO	PIO	1	—
PIO1	G22	PIO	PIO	1	—
PIO1	H16	PIO	PIO	1	D12
PIO1	H18	PIO	PIO	1	D14
PIO1	H20	PIO	PIO	1	—
PIO1	J15	PIO	PIO	1	E11
PIO1	J16	PIO	PIO	1	E12
PIO1	J18	PIO	PIO	1	E14
PIO1 (●)	J22	N.C.	PIO	1	—
PIO1	K15	PIO	PIO	1	F11
PIO1	K16	PIO	PIO	1	F12
PIO1	K20	PIO	PIO	1	—
PIO1 (●)	K22	N.C.	PIO	1	—

I/O Characteristics

Table 49: PIO Pin Electrical Characteristics

Symbol	Description		Conditions	Minimum	Nominal	Maximum	Units
I_I	Input pin leakage current	I/O Bank 0, 1, 2	V_{IN} = $VCCIO_{max}$ to 0 V			±10	µA
		I/O Bank 3	V_{IN} = $VCCIO_{max}$				
I_{OZ}	Three-state I/O pin (Hi-Z) leakage current		V_O = $VCCIO_{max}$ to 0 V			±10	µA
C_{PIO}	PIO pin input capacitance				6		pF
C_{GBIN}	GBIN global buffer pin input capacitance				6		pF
R_{PULLUP}	Internal PIO pull-up resistance during configuration		VCCIO = 3.3V		40		kΩ
			VCCIO = 2.5V		50		kΩ
			VCCIO = 1.8V		90		kΩ
			VCCIO = 1.5V				kΩ
			VCCIO = 1.2V				kΩ
V_{HYST}	Input hysteresis		VCCIO = 1.5V to 3.3V		50		mV

NOTE: All characteristics are characterized and may or may not be tested on each pin on each device.

Single-ended I/O Characteristics

Table 50: I/O Characteristics (I/O Banks 0, 1, 2 and SPI only) (I/O Bank 3 iCE65L01 only)

I/O Standard	Nominal I/O Bank Supply Voltage	Input Voltage (V)		Output Voltage (V)		Output Current at Voltage (mA)	
		V_{IL}	V_{IH}	V_{OL}	V_{OH}	I_{OL}	I_{OH}
LVCMOS33	3.3V	0.80	2.00	0.4	2.40	8	8
LVCMOS25	2.5V	0.70	1.70	0.4	2.00	6	6
LVCMOS18	1.8V	35% VCCIO	65% VCCIO	0.4	1.40	4	4
LVCMOS15	1.5V	Not supported Use I/O Bank 3		0.4	1.20	2	2

Table 51: I/O Characteristics (I/O Bank 3 and iCE65L04/08 only)

I/O Standard	Supply Voltage	Input Voltage (V)		Output Voltage (V)		I/O Attribute Name	mA at Voltage
		Max. V_{IL}	Min. V_{IH}	Max. V_{OL}	Min. V_{OH}		I_{OL}, I_{OH}
LVCMOS33	3.3V	0.80	2.20	0.4	2.40	SL_LVCMOS33_8	±8
LVCMOS25	2.5V	0.70	1.70	0.4	2.00	SB_LVCMOS25_16	±16
						SB_LVCMOS25_12	±12
						SB_LVCMOS25_8 *	±8
						SB_LVCMOS25_4	±4
LVCMOS18	1.8V	35% VCCIO	65% VCCIO	0.4	VCCIO–0.45	SB_LVCMOS18_10	±10
						SB_LVCMOS18_8	±8
						SB_LVCMOS18_4 *	±4
						SB_LVCMOS18_2	±2
LVCMOS15	1.5V	35% VCCIO	65% VCCIO	25% VCCIO	75% VCCIO	SB_LVCMOS15_4	±4
						SB_LVCMOS15_2 *	±2
MDDR	1.8V	35% VCCIO	65% VCCIO	0.4	VCCIO–0.45	SB_MDDR10	±10
						SB_MDDR8	±8
						SB_MDDR4 *	±4
						SB_MDDR2	±2
SSTL2 (Class 2)	2.5V	VREF–0.180	VREF+0.180	0.35	VTT+0.430	SB_SSTL2_CLASS_2	±16.2
SSTL2 (Class 1)				0.54		SB_SSTL2_CLASS_1	±8.1
SSTL18 (Full)	1.8V	VREF–0.125	VREF+0.125	0.28	VTT+0.280	SB_SSTL18_FULL	±13.4
SSTL18 (Half)				VTT–0.475	VTT+0.475	SB_SSTL18_HALF	±6.7

NOTES:

SSTL2 and SSTL18 I/O standards require the VREF input pin, which is only available on the CB284 package and die-based products.

Programmable Input/Output (PIO) Block

Table 55 provides timing information for the logic in a Programmable Logic Block (PLB), which includes the paths shown in Figure 57 and Figure 58. The timing shown is for the LVCMOS25 I/O standard in all I/O banks. The iCEcube development software reports timing adjustments for other I/O standards.

Figure 57: Programmable I/O (PIO) Pad-to-Pad Timing Circuit

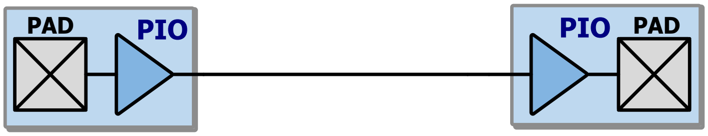


Figure 58: Programmable I/O (PIO) Sequential Timing Circuit

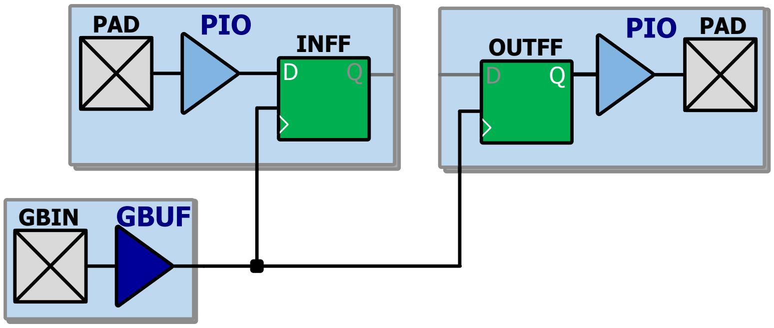


Table 55: Typical Programmable Input/Output (PIO) Timing (LVCMOS25)

			Device: iCE65	L01	L04, L08			
			Power/Speed Grad	–T	–L		–T	
			Nominal VCC	1.2 V	1.0 V	1.2 V	1.2 V	
Symbol	From	To	Description	Typ.	Typ.	Typ.	Typ.	Units
		Synchronous Output Paths						
t_{OCKO}	OUTFF clock input	PIO output	Delay from clock input on OUTFF output flip-flop to PIO output pad.	4.7	13.8	7.3	5.6	ns
t_{GBCKIO}	GBIN input	OUTFF clock input	Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to clock input on the PIO OUTFF output flip-flop.	2.1	7.3	3.8	2.6	ns
		Synchronous Input Paths						
t_{SUPDIN}	PIO input	GBIN input	Setup time on PIO input pin to INFF input flip-flop before active clock edge on GBIN input, including interconnect delay.	0	0	0	0	ns
t_{HDPDIN}	GBIN input	PIO input	Hold time on PIO input to INFF input flip-flop after active clock edge on the GBIN input, including interconnect delay.	2.7	7.1	3.6	2.8	ns
		Pad to Pad						
t_{PADIN}	PIO input	Inter-connect	Asynchronous delay from PIO input pad to adjacent interconnect.	2.5	9.5	5.0	3.2	ns
t_{PADO}	Inter-connect	PIO output	Asynchronous delay from adjacent interconnect to PIO output pad including interconnect delay.	4.5	14.6	7.7	6.2	ns

Internal Configuration Oscillator Frequency

Table 57 shows the operating frequency for the iCE65's internal configuration oscillator.

Table 57: Internal Oscillator Frequency

Symbol	Oscillator Mode	Frequency (MHz)		Description
		Min.	Max.	
f_{OSCD}	**Default**	4.0	6.8	Default oscillator frequency. Slow enough to safely operate with any SPI serial PROM.
f_{OSCL}	**Low Frequency**	14	21	Supported by most SPI serial Flash PROMs
f_{OSCH}	**High Frequency**	21	31	Supported by some high-speed SPI serial Flash PROMs
	Off	0	0	Oscillator turned off by default after configuration to save power.

Configuration Timing

Table 58 shows the maximum time to configure an iCE65 device, by oscillator mode. The calculations use the slowest frequency for a given oscillator mode from Table 57 and the maximum configuration bitstream size from Table 1 which includes full RAM4K block initialization. The configuration bitstream selects the desired oscillator mode based on the performance of the configuration data source.

Table 58: **Maximum SPI Master or NVCM Configuration Timing by Oscillator Mode**

Symbol	Description	Device	Default	Low Freq.	High Freq.	Units
$t_{CONFIGL}$	Time from when minimum Power-on Reset (POR) threshold is reached until user application starts.	**iCE65L01**	53	25	11	ms
		iCE65L04	115	55	25	ms
		iCE65L08	230	110	50	ms

Table 59 provides timing for the CRESET_B and CDONE pins.

Table 59: General Configuration Timing

Symbol	From	To	Description		All Grades		Units
					Min.	Max.	
t_{CRESET_B}	CREST_B	CREST_B	Minimum CRESET_B Low pulse width required to restart configuration, from falling edge to rising edge		200	—	ns
t_{DONE_IO}	CDONE High	PIO pins active	Number of configuration clock cycles after CDONE goes High before the PIO pins are activated.		—	49	Clock cycles
			SPI Peripheral Mode (Clock = SPI_SCK, cycles measured rising-edge to rising-edge)		Depends on SPI_SCK frequency		
			NVCM or SPI Master Mode by internal oscillator frequency setting (Clock = internal oscillator)	Default	7.20	12.25	µs
				Low	2.34	3.50	µs
				High	1.59	2.33	µs