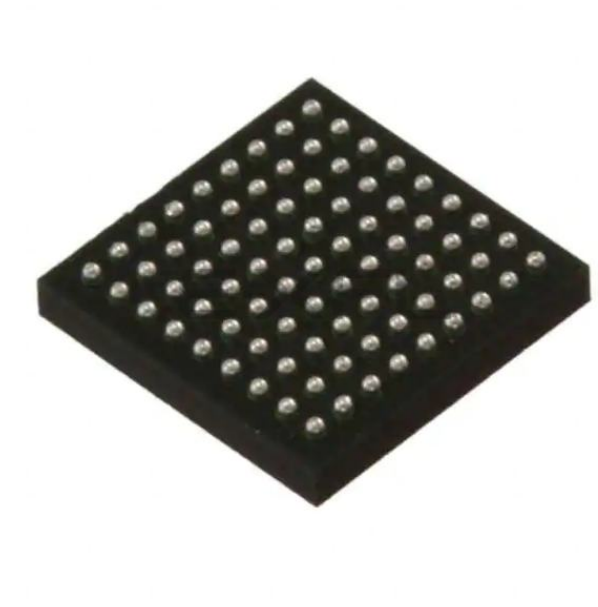

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 160 |
| Number of Logic Elements/Cells | 1280 |
| Total RAM Bits | 65536 |
| Number of I/O | 63 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 81-VFBGA, CSPBGA |
| Supplier Device Package | 81-CSBGA (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/ice65l01f-tcb81i |

## Overview

The Lattice Semiconductor iCE65 programmable logic family is specifically designed to deliver the lowest static and dynamic power consumption of any comparable CPLD or FPGA device. iCE65 devices are designed for cost-sensitive, high-volume applications and provide on-chip, nonvolatile configuration memory (NVCM) to customize for a specific application. iCE65 devices can self-configure from a configuration image stored in an external commodity SPI serial Flash PROM or be downloaded from an external processor over an SPI-like serial port.

The three iCE65 components, highlighted in Table 1, deliver from approximately 1K to nearly 8K logic cells and flip-flops while consuming a fraction of the power of comparable programmable logic devices. Each iCE65 device includes between 16 to 32 RAM blocks, each with 4Kbits of storage, for on-chip data storage and data buffering.

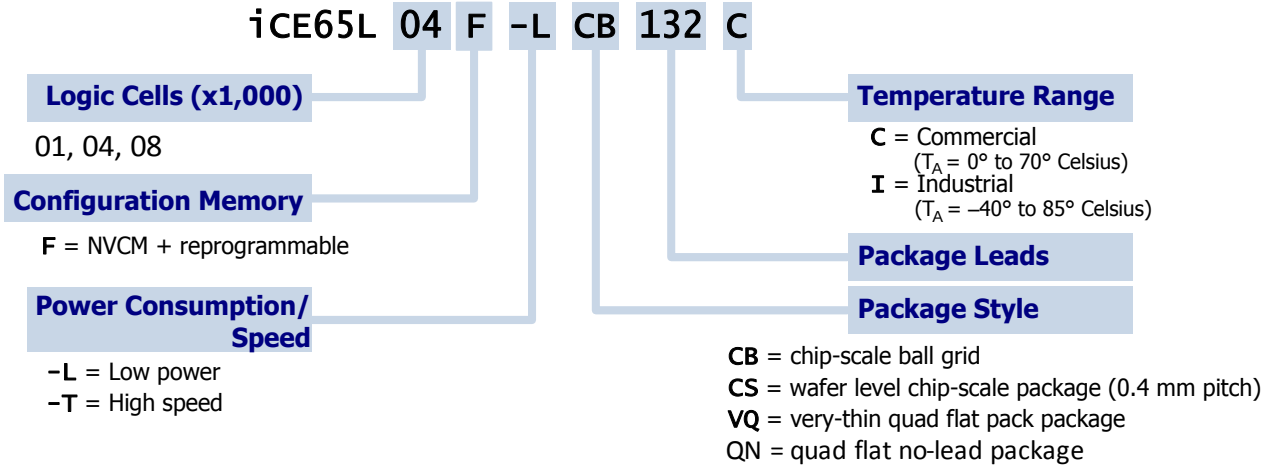
As pictured in Figure 1, each iCE65 device consists of four primary architectural elements.

- An array of Programmable Logic Blocks (PLBs)
  - Each PLB contains eight Logic Cells (LCs); each Logic Cell consists of ...
    - A fast, four-input look-up table (LUT4) capable of implementing any combinational logic function of up to four inputs, regardless of complexity
    - A 'D'-type flip-flop with an optional clock-enable and set/reset control
    - Fast carry logic to accelerate arithmetic functions such as adders, subtracters, comparators, and counters.
  - Common clock input with polarity control, clock-enable input, and optional set/reset control input to the PLB is shared among all eight Logic Cells
- Two-port, 4Kbit RAM blocks (RAM4K)
  - 256x16 default configuration; selectable data width using programmable logic resources
  - Simultaneous read and write access; ideal for FIFO memory and data buffering applications
  - RAM contents pre-loadable during configuration
- Four I/O banks with independent supply voltage, each with multiple Programmable Input/Output (PIO) blocks
  - LVCMOS I/O standards and LVDS outputs supported in all banks
  - I/O Bank 3 supports additional SSTL, MDDR, LVDS, and SubLVDS I/O standards
- Programmable interconnections between the blocks
  - Flexible connections between all programmable logic functions
  - Eight dedicated low-skew, high-fanout clock distribution networks

## Ordering Information

Figure 2 describes the iCE65 ordering codes for all packaged, non-NVCM Programed components. See the separate DiePlus data sheets when ordering die-based products.

***Figure 2:*** **iCE65 Ordering Codes Standard Device**

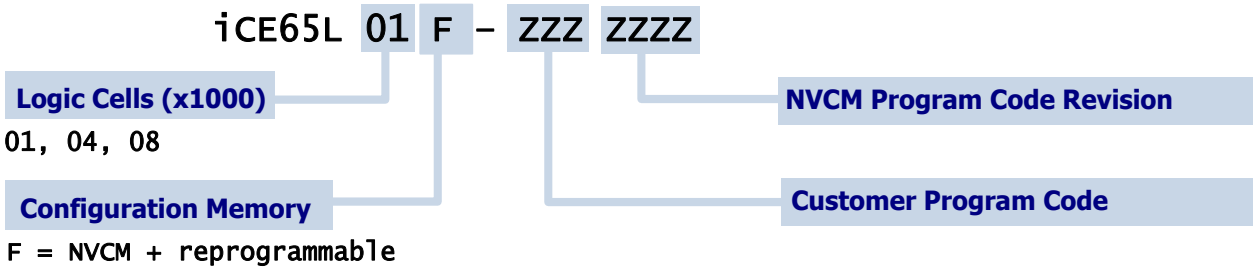



iCE65 devices offer two power consumption, speed options. Standard products ("-L" ordering code) have low standby and dynamic power consumption. The "-T" provides higher-speed logic.

Similarly, iCE65 devices are available in two operating temperature ranges, one for typical commercial applications, the other with an extended temperature range for industrial and telecommunications applications. The ordering code also specifies the device package option, as described further in Table 2.

Figure 3 describes the iCE65 ordering codes for all packaged, NVCM Programmed components.

***Figure 3:*** **iCE65 Ordering Codes NVCM Programmed Device**



### *Implementing Subtracters, Decrementers*

As mentioned earlier, the Carry Logic generates a High output whenever the sum of `I1 + I2 + CARRY_IN` generates a carry. The Carry Logic does not specifically have a subtract mode. To implement a subtract function or decrement function, logically invert either the I1 or I2 input and invert the initial carry input. This performs a 2s complement subtract operation.

**Figure 6: Two-bit Adder Example**

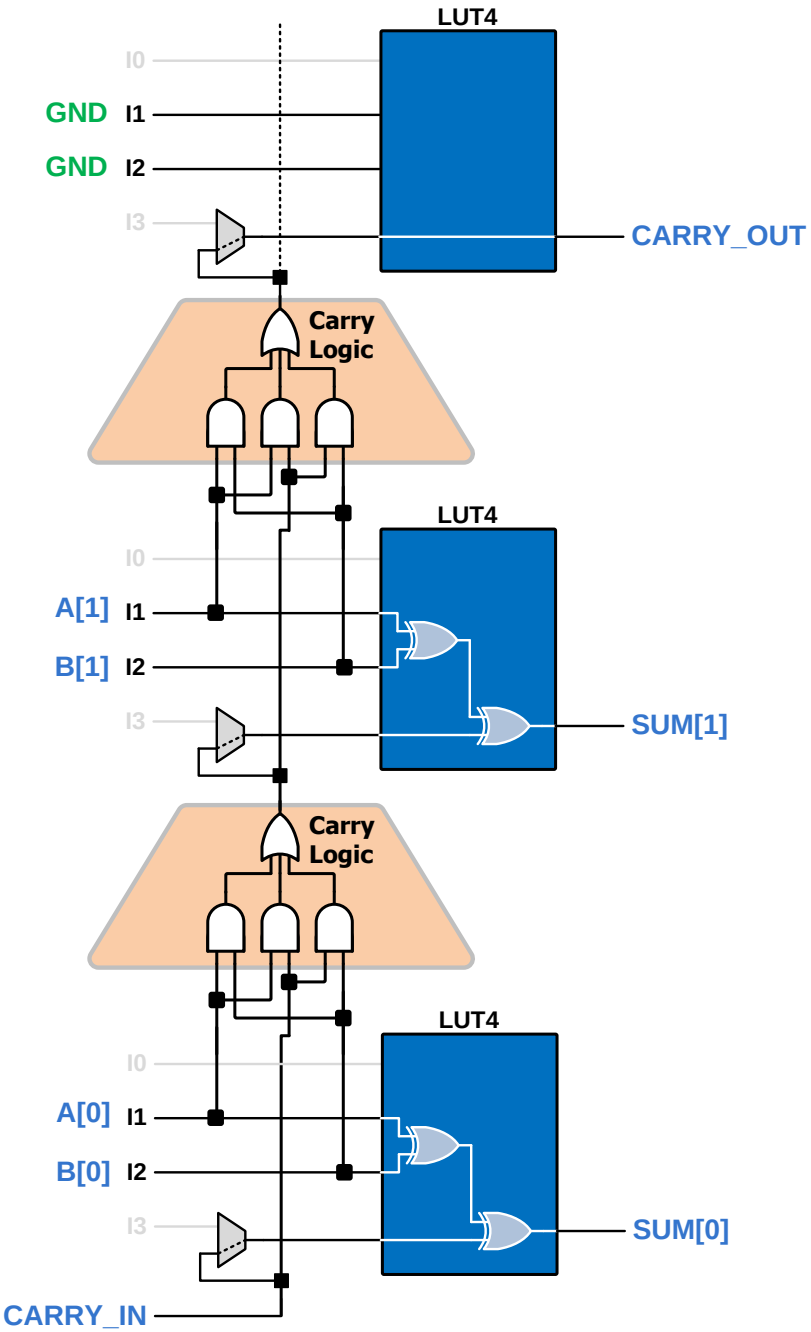
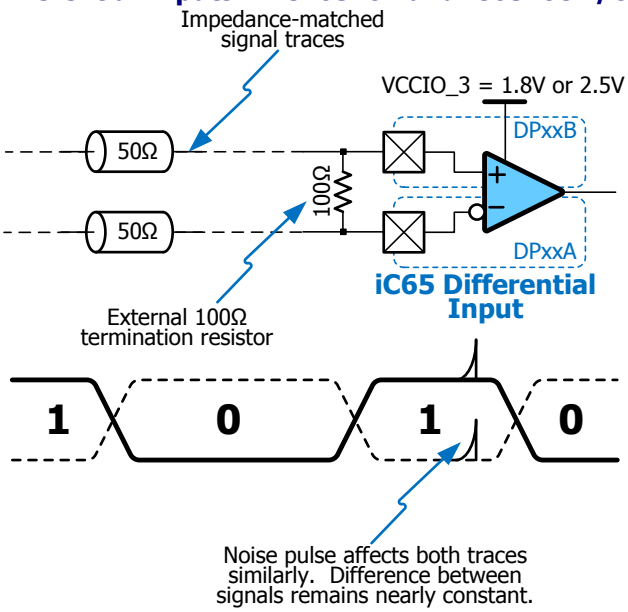


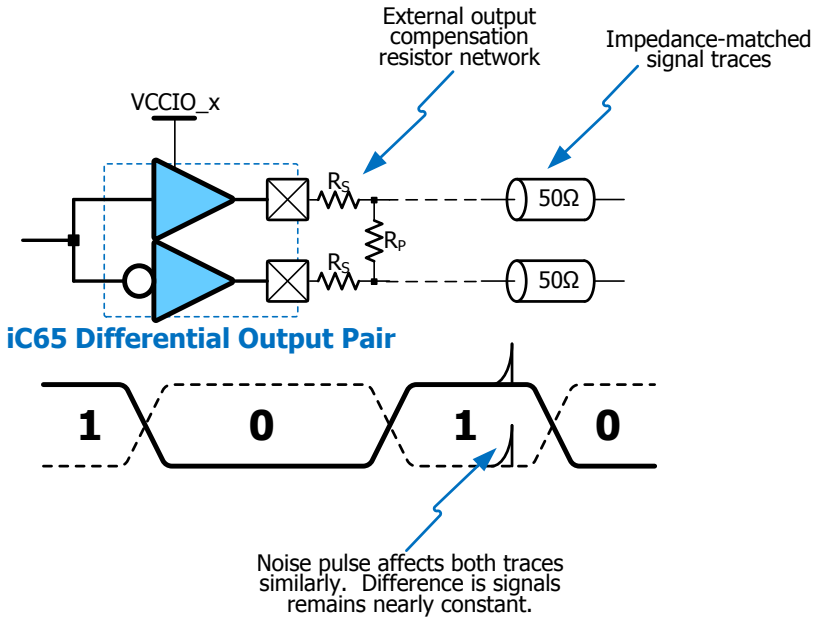
***Figure 8:*** **Differential Inputs in iCE65L04 and iC65L08 I/O Bank 3**




### *Differential Outputs in Any Bank*

Differential outputs are built using a pair of single-ended PIO pins as shown in Figure 9. Each differential I/O pair requires a three-resistor termination network to adjust output characteristic to match those for the specific differential I/O standard. The output characteristics depend on the values of the parallel resistors (RP) and series resistor (RS). Differential outputs must be located in the same I/O tile.

**Figure 9: Differential Output Pair**




For electrical characteristics, see "Differential Outputs" on page 100.

The PIO pins that make up a differential output pair are indicated with a blue bounding box in the in the tables in "Die Cross Reference" starting on page 84.

Table 12 and Table 13 list the connections between a specific global buffer and the inputs on a Programmable I/O (PIO) pair. Although there is no direct connection between a global buffer and a PIO output, such a connection is possible by first connecting through a PLB LUT4 function. Again, all global buffers optionally drive all clock inputs. However, even-numbered global buffers optionally drive the clock-enable input on a PIO pair.

The PIO clock enable connect is different between the iCE65L01/iCE65L04 and iCE65L08.

***Table 12:*** **iCE65L01 & iCE65L04: Global Buffer (GBUF) Connections to Programmable I/O (PIO) Pair**

| Global Buffer | Output Connections | Input Clock | Output Clock | Clock Enable |
|---|---|---|---|---|
| **GBUF0** | No (connect through PLB LUT) | Yes | Yes | No |
| **GBUF1** | | Yes | Yes | Yes |
| **GBUF2** | | Yes | Yes | No |
| **GBUF3** | | Yes | Yes | Yes |
| **GBUF4** | | Yes | Yes | No |
| **GBUF5** | | Yes | Yes | Yes |
| **GBUF6** | | Yes | Yes | No |
| **GBUF7** | | Yes | Yes | Yes |

***Table 13:*** **iCE64L08: Global Buffer (GBUF) Connections to Programmable I/O (PIO) Pair**

| Global Buffer | Output Connections | Input Clock | Output Clock | Clock Enable |
|---|---|---|---|---|
| **GBUF0** | No (connect through PLB LUT) | Yes | Yes | Yes |
| **GBUF1** | | Yes | Yes | No |
| **GBUF2** | | Yes | Yes | Yes |
| **GBUF3** | | Yes | Yes | No |
| **GBUF4** | | Yes | Yes | Yes |
| **GBUF5** | | Yes | Yes | No |
| **GBUF6** | | Yes | Yes | Yes |
| **GBUF7** | | Yes | Yes | No |

### *Global Buffer Inputs*

The iCE65 component has eight specialized GBIN/PIO pins that are optionally direct inputs to the global buffers, offering the best overall clock characteristics. As shown in Figure 15, each GBIN/PIO pin is a full-featured I/O pin but also provides a direct connection to its associated global buffer. The direct connection to the global buffer bypasses the iCEgate input-blocking latch and other PIO input logic. These special PIO pins are allocated two to an I/O Bank, a total of eight. These pins are labeled GBIN0 through GBIN7, as shown in Figure 14 and the pin locations for each GBIN input appear in Table 14.

***Table 14:*** **Global Buffer Input Ball/Pin Number by Package**

| Global Buffer Input (GBIN) | I/O Bank | VQ100 | CB132 | 'L04 CB196 | 'L08 CB196 | CB284 |
|---|---|---|---|---|---|---|
| **GBIN0** | 0 | 90 | A6 | A7 | A7 | E10 |
| **GBIN1** | | 89 | A7 | E7 | E7 | E11 |
| **GBIN2** | 1 | 63 | G14 | F10 | F10 | L18 |
| **GBIN3** | | 62 | F14 | G12 | G12 | K18 |
| **GBIN4** | 2 | 34 | P8 | L7 | N8 | V12 |
| **GBIN5** | | 33 | P7 | P5 | M7 | V11 |
| **GBIN6** | 3 | 15 | H1 | H1 | H1 | M5 |
| **GBIN7** | | 13 | G1 | G1 | H3 | L5 |

### Automatic Global Buffer Insertion, Manual Insertion

The iCEcube development software automatically assigns high-fanout signals to a global buffer. However, to manual insert a global buffer input/global buffer (GBIN/GBUF) combination, use the **SB_IO_GB** primitive. To insert just a global buffer (GBUF), use the **SB_GB** primitive.

### Global Hi-Z Control

The global high-impedance control signal, GHIZ, connects to all I/O pins on the iCE65 device. This GHIZ signal is automatically asserted throughout the configuration process, forcing all user-I/O pins into their high-impedance state. Similarly, the PIO pins can be forced into their high-impedance state via the JTAG controller.

### Global Reset Control

The global reset control signal connects to all PLB and PIO flip-flops on the iCE65 device. The global reset signal is automatically asserted throughout the configuration process, forcing all flip-flops to their defined wake-up state. For PLB flip-flops, the wake-up state is always reset, regardless of the PLB flip-flop primitive used in the application. See Table 3 for more information.

The PIO flip-flops are always reset during configuration, although the output flip-flop can be inverted before leaving the iCE65 device, as shown in Figure 11.

## RAM

Each iCE65 device includes multiple high-speed synchronous RAM blocks (RAM4K), each 4Kbit in size. As shown in Table 16 a single iCE65 integrates between 16 to 96 such blocks. Each RAM4K block is generically a 256-word deep by 16-bit wide, two-port register file, as illustrated in Figure 17. The input and output connections, to and from a RAM4K block, feed into the programmable interconnect resources.

**Figure 17: RAM4K Memory Block**

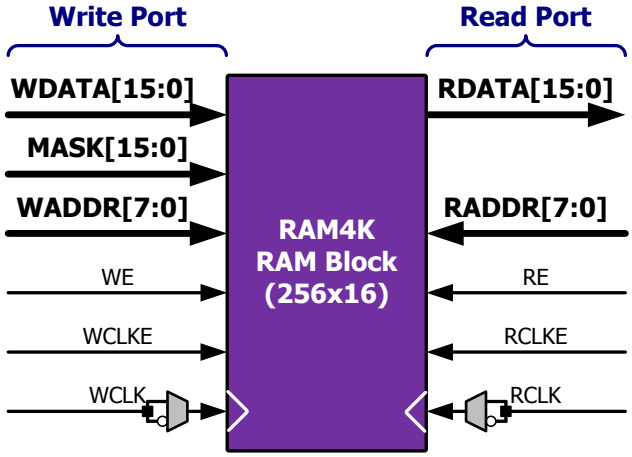



**Table 16: RAM4K Blocks per Device**

| Device | RAM4K Blocks | Default Configuration | RAM Bits per Block | Block RAM Bits |
|---|---|---|---|---|
| iCE65L01 | 16 | 256 x 16 | 4K (4,096) | 64K |
| iCE65L04 | 20 | | | 80K |
| iCE65L08 | 32 | | | 128K |

Using programmable logic resources, a RAM4K block implements a variety of logic functions, each with configurable input and output data width.

- Random-access memory (RAM)
  - Single-port RAM with a common address, enable, and clock control lines
  - Two-port RAM with separate read and write control lines, address inputs, and enable

## Device Configuration

As described in Table 20, iCE65 components are configured for a specific application by loading a binary configuration bitstream image, generated by the Lattice development system. For high-volume applications, the bitstream image is usually permanently programmed in the on-chip NVCM, However, the bitstream image can also be stored external in a standard, low-cost commodity SPI serial Flash PROM. The iCE65 component can automatically load the image using the SPI Master Configuration Interface. Similarly, the iCE65 configuration data can be downloaded from an external processor, microcontroller, or DSP processor using an SPI-like serial interface or an IEEE 1149 JTAG interface.

***Table 20:*** **iCE65 Device Configuration Modes**

| Mode | Analogy | Configuration Data Source |
|---|---|---|
| **NVCM** | ASIC | Internal, lowest-cost, secure, one-time programmable Nonvolatile Configuration Memory (NVCM) |
| **SPI Flash** | Microprocessor | External, low-cost, commodity, SPI serial Flash PROM |
| **SPI Peripheral** | Processor Peripheral | Configured by external device, such as a processor, microcontroller, or DSP using practically any data source, such as system Flash, a disk image, or over a network connection. |
| **JTAG** | JTAG | JTAG configuration requires sending a special command sequence on the SPI interface to enable JTAG configuration. Configuration is controlled by and external device. |

### Configuration Mode Selection

The iCE65 configuration mode is selected according to the following priority described below and illustrated in Figure 20.

- After exiting the Power-On Reset (POR) state or when CRESET_B returns High after being held Low for 250 ns or more, the iCE65 FPGA samples the logical value on its SPI_SS_B pin. Like other programmable I/O pins, the SPI_SS_B pin has an internal pull-up resistor (see Input Pull-Up Resistors on I/O Banks 0, 1, and 2).
- If the SPI_SS_B pin is sampled as a logic '1' (High), then …
  - Check if the iCE65 is enabled to configure from the Nonvolatile Configuration Memory (NVCM). If the iCE65 device has NVCM memory ('**F**' ordering code) but the NVCM is yet unprogrammed, then the iCE65 device is not enabled to configure from NVCM. Conversely, if the NVCM is programmed, the iCE65 device will configure from NVCM.
    - If enabled to configure from NVCM, the iCE65 device configures itself using NVCM.
    - If not enabled to configure from NVCM, then the iCE65 FPGA configures using the SPI Master Configuration Interface.
- If the SPI_SS_B pin is sampled as a logic '0' (Low), then the iCE65 device waits to be configured from an external controller or from another iCE65 device in SPI Master Configuration Mode using an SPI-like interface.

***Figure 24:*** **SPI Release from Deep Power-down Command**

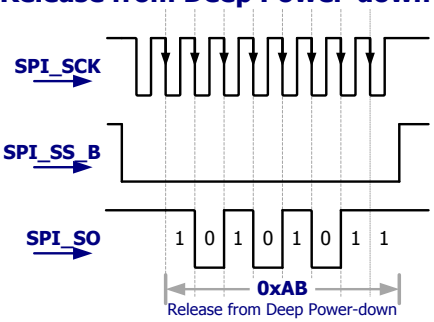
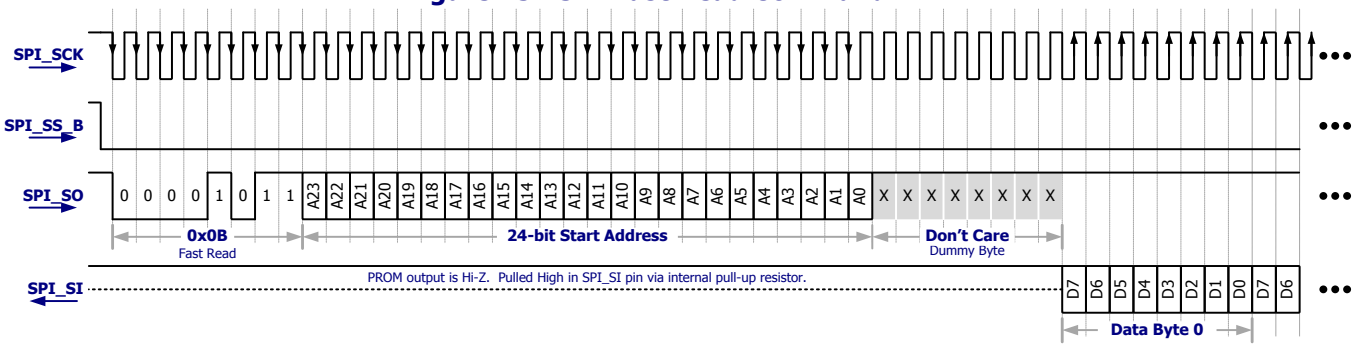



Figure 25 illustrates the next command issued by the iCE65 device. The iCE65 SPI interface again drives SPI_SS_B Low, followed by a Fast Read command, hexadecimal command code 0x0B, followed by a 24-bit start address, transmitted on the SPI_SO output. The iCE65 device provides data on the falling edge of SPI_SS_B. Upon initial power-up, the start address is always 0x00_0000. After waiting eight additional clock cycles, the iCE65 device begins reading serial data from the SPI PROM. Before presenting data, the SPI PROM's serial data output is high-impedance. The SPI_SI input pin has an internal pull-up resistor and sees high-impedance as logic '1'.

**Figure 25: SPI Fast Read Command**




The external SPI PROM supplies data on the falling edge of the iCE65 device's SPI_SCK clock output. The iCE65 device captures each PROM data value on the SPI_SI input, using the rising edge of the SPI_SCK clock signal. The SPI PROM data starts at the 24-bit address presented by the iCE65 device. PROM data is serially output, byte by byte, with most-significant bit, D7, presented first. The PROM automatically increments an internal byte counter as long as the PROM is selected and clocked.

After transferring the required number configuration data bits, the iCE65 device ends the Fast Read command by de-asserting its SPI_SS_B PROM select output, as shown in Figure 26. To conserve power, the iCE65 device then optionally issues a final Deep Power-down command, hexadecimal command code 0xB9. After de-asserting the SPI_SS_B output, the SPI PROM enters its Deep Power-down mode. The final power-down step is optional; the application may use the SPI PROM and can skip this step, controlled by a configuration option.

***Figure 26:*** **Final Configuration Data, SPI Deep Power-down Command**

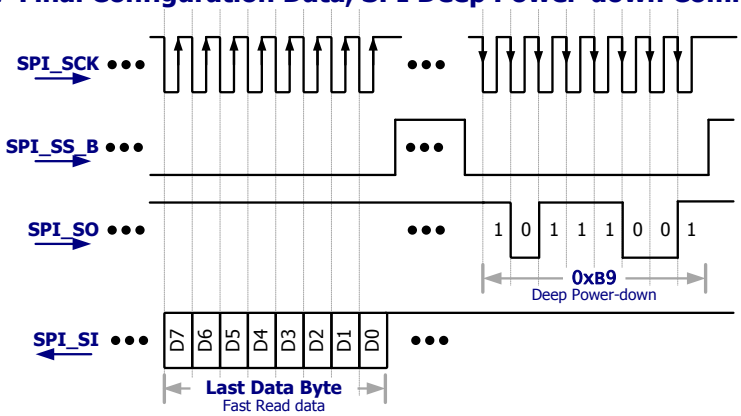
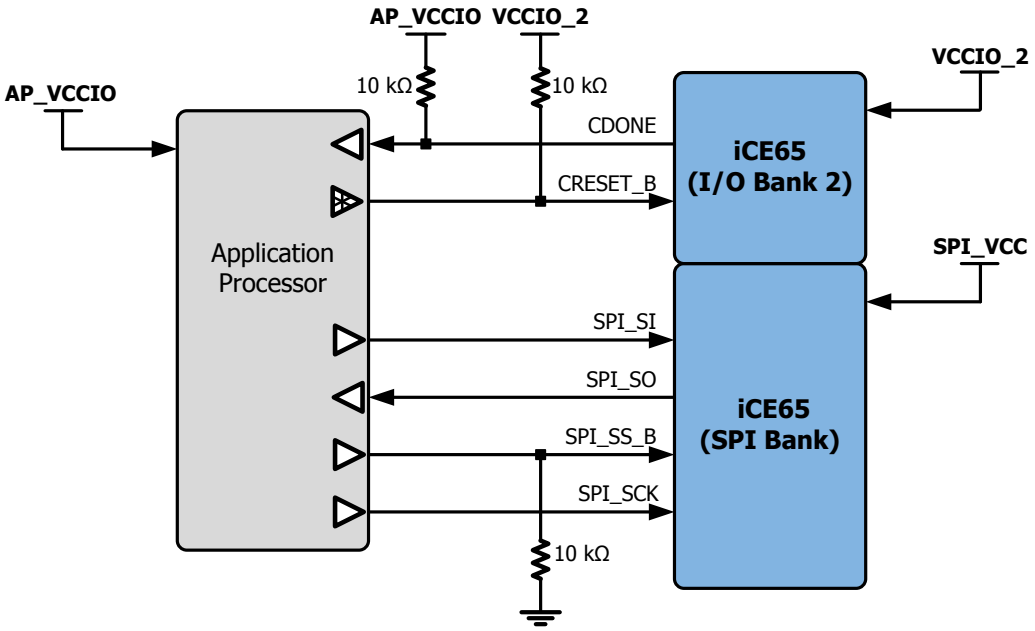


***Figure 28:*** **iCE65 SPI Peripheral Configuration Interface**




The SPI control signals are defined in Table 25.

***Table 29:*** **SPI Peripheral Configuration Interface Pins (SPI_SS_B Low when CRESET_B Released)**

| Signal Name | Direction | iCE65 I/O Supply | Description |
|---|---|---|---|
| CDONE | AP ← iCE65 | VCCIO_2 | Configuration Done output from iCE65. Connect to a 10kΩ pull-up resistor to the application processor I/O voltage, AP_VCC. |
| CRESET_B | AP → iCE65 | | Configuration Reset input on iCE65. Typically driven by AP using an open-drain driver, which also requires a 10kΩ pull-up resistor to VCCIO_2. |
| SPI_VCC | Supply | SPI_VCC | SPI Flash PROM voltage supply input. |
| SPI_SI | AP → iCE65 | | SPI Serial Input to the iCE65 FPGA, driven by the application processor. |
| SPI_SO | AP ← iCE65 | | SPI Serial Output from CE65 device to the application processor. Not actually used during SPI peripheral mode configuration but required if the SPI interface is also used to program the NVCM. |
| SPI_SS_B | AP → iCE65 | | SPI Slave Select output from the application processor. Active Low. Optionally hold Low prior to configuration using a 10kΩ pull-down resistor to ground. |
| SPI_SCK | AP → iCE65 | | SPI Slave Clock output from the application processor. |

After configuration, the SPI port pins are available to the user-application as additional PIO pins, supplied by the SPI_VCC input voltage, essentially providing a fifth "mini" I/O bank.

### *Enabling SPI Configuration Interface*

The optional 10 kΩ pull-down resistor on the SPI_SS_B signal ensures that the iCE65 FPGA powers up in the SPI peripheral mode. Optionally, the application processor drives the SPI_SS_B pin Low when CRESET_B is released, forcing the iCE65 FPGA into SPI peripheral mode.

### *SPI Peripheral Configuration Process*

Figure 29 illustrates the interface timing for the SPI peripheral mode and Figure 30 outlines the resulting configuration process. The actual timing specifications appear in Table 60. The application processor (AP) begins by driving the iCE65 CRESET_B pin Low, resetting the iCE65 FPGA. Similarly, the AP holds the iCE65's SPI_SS_B pin Low. The AP must hold the CRESET_B pin Low for at least 200 ns. Ultimately, the AP either releases the CRESET_B pin and allows it to float High via the 10 kΩ pull-up resistor to VCCIO_2 or drives CRESET_B High. The iCE65 FPGA enters SPI peripheral mode when the CRESET_B pin returns High while the SPI_SS_B pin is Low.

Table 31 describes how to maintain voltage compatibility for two interface scenarios. The easiest interface is when the Application Processor's (AP) I/O supply rail and the iCE65's SPI and VCCIO_2 bank supply rails all connect to the same voltage. The second scenario is when the AP's I/O supply voltage is greater than the iCE65's VCCIO_2 supply voltage.

***Table 31:* CRESET_B and CDONE Voltage Compatibility**

| Condition | CRESET_B | | | CDONE Pull-up | Requirement |
|---|---|---|---|---|---|
| | **Direct** | **Open-Drain** | **Pull-up** | | |
| **VCCIO_AP = VCC_SPI**<br>**VCCIO_AP = VCCIO_2** | OK | OK with pull-up | Required if using open-drain output | Recommended | AP can directly drive CRESET_B High and Low although an open-drain output recommended is if multiple devices control CRESET_B. If using an open-drain driver, the CRESET_B input must include a 10 kΩ pull-up resistor to VCCIO_2. The 10 kΩ pull-up resistor to AP_VCCIO is also recommended. |
| **AP_VCCIO > VCCIO_2** | N/A | Required, requires pull-up | Required | Required | The AP must control CRESET_B with an open-drain output, which requires a 10 kΩ pull-up resistor to VCCIO_2. The 10 kΩ pull-up resistor to AP_VCCIO is required. |

## JTAG Boundary Scan Port

### Overview

Each iCE65 device includes an IEEE 1149.1-compatible JTAG boundary-scan port. The port supports printed-circuit board (PCB) testing and debugging. It also provides an alternate means to configure the iCE65 device.

### Signal Connections

The JTAG port connections are listed in Table 32.

***Table 32:* iCE65 JTAG Boundary Scan Signals**

| Signal Name | Direction | Description |
|---|---|---|
| TDI | Input | Test Data Input. Must be tied off to GND when unused. (no pull-up resistor)* |
| TMS | Input | Test Mode Select. Must be tied off to GND when unused. (no pull-up resistor)* |
| TCK | Input | Test Clock. Must be tied off to GND when unused. (no pull-up resistor)* |
| TDO | Output | Test Data Output. |
| TRST_B | Input | Test Reset, active Low. Must be Low during normal device operation. Must be High to enable JTAG operations.* |

* Must be tied off to GND or VCCIO_1, else VCCIO_1 draws current.

Table 33 lists the ball/pin numbers for the JTAG interface by package code. The JTAG interface is available in select package types. The JTAG port is located in I/O Bank 1 along the right edge of the iCE65 device and powered by the VCCIO_1 supply inputs. Consequently, the JTAG interface uses the associated I/O standards for I/O Bank 1.

***Table 33:* JTAG Interface Ball/Pin Numbers by Package**

| JTAG Interface | VQ100 | CB132 | CB196 | CB284 |
|---|---|---|---|---|
| **TDI** | N/A | M12 | M12 | T16 |
| **TMS** | | P14 | P14 | V18 |
| **TCK** | | L12 | L12 | R16 |
| **TDO** | | N14 | N14 | U18 |
| **TRST_B** | | M14 | M14 | T18 |

| Ball Function | Ball Number | Pin Type | Bank |
|---|---|---|---|
| GND | K2 | GND | GND |
| GND | K10 | GND | GND |
| VCC | B6 | VCC | VCC |
| VCC | F1 | VCC | VCC |
| VCC | F11 | VCC | VCC |
| VCC | K6 | VCC | VCC |
| VPP_2V5 | C10 | VPP | VPP |
| VPP_FAST | A9 | VPP | VPP |

| Ball Function | Ball Number | Pin Type | Bank |
|---|---|---|---|
| **PIO2 (◆)** | ***iCE65L04:*** N8<br>***iCE65L08:*** L7 | PIO | 2 |
| **PIO2** | N9 | PIO | 2 |
| **PIO2** | N11 | PIO | 2 |
| **PIO2** | N12 | PIO | 2 |
| **PIO2** | N13 | PIO | 2 |
| **PIO2** | P1 | PIO | 2 |
| **PIO2** | P2 | PIO | 2 |
| **PIO2** | P3 | PIO | 2 |
| **PIO2** | P4 | PIO | 2 |
| **PIO2** | P7 | PIO | 2 |
| **PIO2** | P8 | PIO | 2 |
| **PIO2** | P9 | PIO | 2 |
| **PIO2/CBSEL0** | L9 | PIO | 2 |
| **PIO2/CBSEL1** | P10 | PIO | 2 |
| **VCCIO_2** | J9 | VCCIO | 2 |
| **VCCIO_2** | M5 | VCCIO | 2 |
| **VCCIO_2** | N10 | VCCIO | 2 |
| **PIO3/DP00A** | C1 | DPIO | 3 |
| **PIO3/DP00B** | B1 | DPIO | 3 |
| **PIO3/DP01A** | D3 | DPIO | 3 |
| **PIO3/DP01B** | C3 | DPIO | 3 |
| **PIO3/DP02A** | D1 | DPIO | 3 |
| **PIO3/DP02B** | D2 | DPIO | 3 |
| **PIO3/DP03A (◆)** | ***iCE65L04:*** E1<br>***iCE65L08:*** E2 | DPIO | 3 |
| **PIO3/DP03B (◆)** | ***iCE65L04:*** E2<br>***iCE65L04:*** E1 | DPIO | 3 |
| **PIO3/DP04A** | D4 | DPIO | 3 |
| **PIO3/DP04B** | E4 | DPIO | 3 |
| **PIO3/DP05A (◆)** | ***iCE65L04:*** F3<br>***iCE65L08:*** F4 | DPIO | 3 |
| **PIO3/DP05B (◆)** | ***iCE65L04:*** F4<br>***iCE65L08:*** F3 | DPIO | 3 |
| **PIO3/DP06A** | F5 | DPIO | 3 |
| **PIO3/DP06B** | E5 | DPIO | 3 |
| **PIO3/DP07A (◆)** | ***iCE65L04:*** G2<br>***iCE65L08:*** H4 | DPIO | 3 |
| **GBIN7/PIO3/DP07B (◆)** | ***iCE65L04:*** G1<br>***iCE65L08:*** H3 | GBIN | 3 |
| **GBIN6/PIO3/DP08A** | H1 | GBIN | 3 |
| **PIO3/DP08B** | H2 | DPIO | 3 |
| **PIO3/DP09A** | G3 | DPIO | 3 |
| **PIO3/DP09B** | G4 | DPIO | 3 |
| **PIO3/DP10A** | J1 | DPIO | 3 |
| **PIO3/DP10B** | J2 | DPIO | 3 |
| **PIO3/DP11A (◆)** | ***iCE65L04:*** H4<br>***iCE65L08:*** G1 | DPIO | 3 |
| **PIO3/DP11B (◆)** | ***iCE65L04:*** H3<br>***iCE65L08:*** G2 | DPIO | 3 |
| **PIO3/DP12A** | K2 | DPIO | 3 |
| **PIO3/DP12B** | J3 | DPIO | 3 |

| Ball Function | Ball Number | Pin Type | Bank |
|---|---|---|---|
| **PIO3/DP13A** | H5 | DPIO | 3 |
| **PIO3/DP13B** | G5 | DPIO | 3 |
| **PIO3/DP14A** | L1 | DPIO | 3 |
| **PIO3/DP14B** | L2 | DPIO | 3 |
| **PIO3/DP15A** | M1 | DPIO | 3 |
| **PIO3/DP15B** | M2 | DPIO | 3 |
| **PIO3/DP16A (◆)** | ***iCE65L04:*** K3<br>***iCE65L08:*** K4 | DPIO | 3 |
| **PIO3/DP16B (◆)** | ***iCE65L08:*** K4<br>***iCE65L08:*** K3 | DPIO | 3 |
| **PIO3/DP17A** | N1 | DPIO | 3 |
| **PIO3/DP17B** | N2 | DPIO | 3 |
| **VCCIO_3** | E3 | VCCIO | 3 |
| **VCCIO_3** | J6 | VCCIO | 3 |
| **VCCIO_3** | K1 | VCCIO | 3 |
| **PIOS/SPI_SO** | M11 | SPI | SPI |
| **PIOS/SPI_SI** | P11 | SPI | SPI |
| **PIOS/SPI_SCK** | P12 | SPI | SPI |
| **PIOS/SPI_SS_B** | P13 | SPI | SPI |
| **SPI_VCC** | L11 | SPI | SPI |
| **GND** | A9 | GND | GND |
| **GND** | B12 | GND | GND |
| **GND** | C2 | GND | GND |
| **GND** | F1 | GND | GND |
| **GND** | F7 | GND | GND |
| **GND** | G7 | GND | GND |
| **GND** | G8 | GND | GND |
| **GND** | G9 | GND | GND |
| **GND** | H6 | GND | GND |
| **GND** | H7 | GND | GND |
| **GND** | H8 | GND | GND |
| **GND** | J5 | GND | GND |
| **GND** | J8 | GND | GND |
| **GND** | J14 | GND | GND |
| **GND** | K10 | GND | GND |
| **GND** | L3 | GND | GND |
| **GND** | P6 | GND | GND |
| **VCC** | B7 | VCC | VCC |
| **VCC** | F2 | VCC | VCC |
| **VCC** | F8 | VCC | VCC |
| **VCC** | G6 | VCC | VCC |
| **VCC** | H9 | VCC | VCC |
| **VCC** | J4 | VCC | VCC |
| **VCC** | J7 | VCC | VCC |
| **VCC** | K13 | VCC | VCC |
| **VCC** | N7 | VCC | VCC |
| **VPP_2V5** | A14 | VPP | VPP |
| **VPP_FAST** | A13 | VPP | VPP |

### *Pinout Differences between iCE65L04 and iCE65L08 in CB196 Package*

Table 43 lists the package balls that are different between the pinouts for iCE65L04 and the iCE65L08 in the CB196 package. The table also describes the functional differences between these pins, which is critical when designing a CB196 footprint that supports both the iCE65L04 and the iCE65L08 devices. In some cases, only the differential inputs are swapped; single-ended I/Os are not affected. A swapped differential pair can be inverted internally for functional equivalence. In other cases, a global buffer input is swapped with another PIO pin in the same bank.

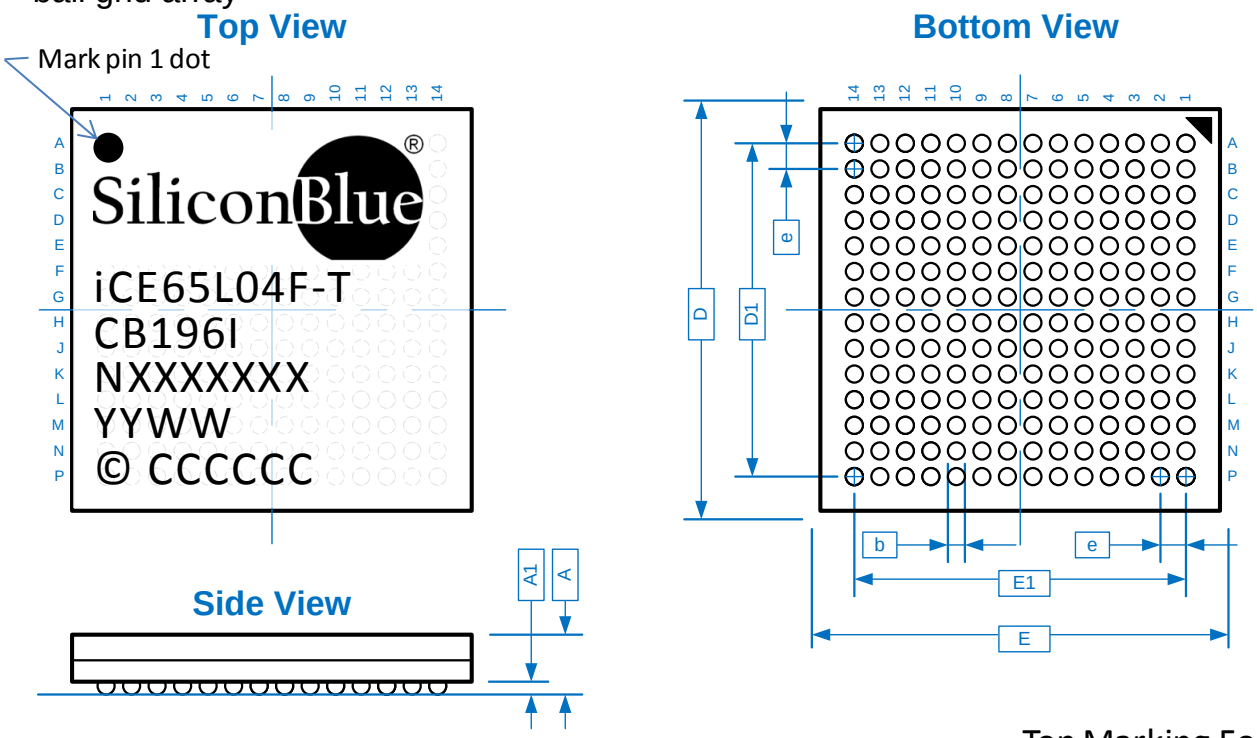
***Table 43:* Pinout Differences between iCE65L04 and iCE65L08 in CB196 Package**

| Ball Number | iCE65L04 | iCE65L08 | Functional Difference |
|---|---|---|---|
| **E1** | PIO3/DP03A | PIO3/DP03B | Differential inputs swapped, single-ended I/Os not affected |
| **E2** | PIO3/DP03B | PIO3/DP03A | |
| **F3** | PIO3/DP05A | PIO3/DP05B | Differential inputs swapped, single-ended I/Os not affected |
| **F4** | PIO3/DP05B | PIO3/DP05A | |
| **G1** | GBIN7/PIO3/DP07B | PIO3/DP11A | Global buffer input GBIN7 and its associated differential input is swapped with another differential pair in I/O Bank 3 |
| **G2** | PIO3/DP07A | PIO3/DP11B | |
| **H3** | PIO3/DP11B | GBIN7/PIO3/DP07B | |
| **H4** | PIO3/DP11A | PIO3/DP07A | |
| **K3** | PIO3/DP16A | PIO3/DP16B | Differential inputs swapped, single-ended I/Os not affected |
| **K4** | PIO3/DP16B | PIO3/DP16A | |
| **L7** | GBIN4/PIO2 | PIO2 | Global buffer input GBIN4 swapped with another PIO pin in I/O Bank 2 |
| **N8** | PIO2 | GBIN4/PIO2 | |
| **M7** | PIO2 | GBIN5/PIO2 | Global buffer input GBIN5 swapped with another PIO pin in I/O Bank 2 |
| **P5** | GBIN5/PIO2 | PIO2 | |

## *Package Mechanical Drawing*

**Figure 47:**
**(a) iCE65L04 CB196 Package Mechanical Drawing**

**CB196:** 8 x8 mm, 196-ball, 0.5 mm ball-pitch, fully-populated, chip-scale ball grid array




| Description | | Symbol | Min. | Nominal | Max. | Units |
|---|---|---|---|---|---|---|
| Number of Ball Columns | X | | | 14 | | Columns |
| Number of Ball Rows | Y | | | 14 | | Rows |
| Number of Signal Balls | | n | | 196 | | Balls |
| Body Size | X | E | 7.90 | 8.00 | 8.10 | mm |
| | Y | D | 7.90 | 8.00 | 8.10 | |
| Ball Pitch | | e | — | 0.50 | — | |
| Ball Diameter | | b | 0.27 | — | 0.37 | |
| Edge Ball Center to Center | X | E1 | — | 6.50 | — | |
| | Y | D1 | — | 6.50 | — | |
| Package Height | | A | — | — | 1.00 | |
| Stand Off | | A1 | 0.16 | — | 0.26 | |

### Top Marking Format

| Line | Content | Description |
|---|---|---|
| 1 | Logo | Logo |
| 2 | iCE65L04F | Part number |
| | -T | Power/Speed |
| 3 | CB196I | Package type |
| | ENG | Engineering |
| 4 | NXXXXXXX | Lot Number |
| 5 | YYWW | Date Code |
| 6 | © CCCCCC | Country |

### Thermal Resistance

| Junction-to-Ambient $\theta_{JA}$ (°C/W) | |
|---|---|
| 0 LFM | 200 LFM |
| 42 | 34 |

| Ball Function | Ball Number iCE65L04 iCE65L08 | Pin Type by Device iCE65L04 | iCE65L08 | Bank | CB132 Ball Equivalent |
|---|---|---|---|---|---|
| **PIO1** | L15 | PIO | PIO | 1 | G11 |
| **PIO1** | L16 | PIO | PIO | 1 | G12 |
| **PIO1 (●)** | L22 | N.C. | PIO | 1 | — |
| **PIO1** | M15 | PIO | PIO | 1 | H11 |
| **PIO1** | M16 | PIO | PIO | 1 | H12 |
| **PIO1** | M20 | PIO | PIO | 1 | — |
| **PIO1 (●)** | M22 | N.C. | PIO | 1 | — |
| **PIO1** | N15 | PIO | PIO | 1 | J11 |
| **PIO1** | N16 | PIO | PIO | 1 | J12 |
| **PIO1** | N22 | PIO | PIO | 1 | — |
| **PIO1** | P15 | PIO | PIO | 1 | K11 |
| **PIO1** | P16 | PIO | PIO | 1 | K12 |
| **PIO1** | P18 | PIO | PIO | 1 | K14 |
| **PIO1** | P20 | PIO | PIO | 1 | — |
| **PIO1** | P22 | PIO | PIO | 1 | — |
| **PIO1** | R18 | PIO | PIO | 1 | L14 |
| **PIO1** | R20 | PIO | PIO | 1 | — |
| **PIO1** | R22 | PIO | PIO | 1 | — |
| **PIO1** | T20 | PIO | PIO | 1 | — |
| **PIO1** | T22 | PIO | PIO | 1 | — |
| **PIO1** | U20 | PIO | PIO | 1 | — |
| **PIO1 (●)** | U22 | N.C. | PIO | 1 | — |
| **PIO1** | V20 | PIO | PIO | 1 | — |
| **PIO1 (●)** | V22 | N.C. | PIO | 1 | — |
| **PIO1** | W20 | PIO | PIO | 1 | — |
| **PIO1 (●)** | W22 | N.C. | PIO | 1 | — |
| **PIO1 (●)** | Y22 | N.C. | PIO | 1 | — |
| **TCK** | R16 | JTAG | JTAG | 1 | L12 |
| **TDI** | T16 | JTAG | JTAG | 1 | M12 |
| **TDO** | U18 | JTAG | JTAG | 1 | N14 |
| **TMS** | V18 | JTAG | JTAG | 1 | P14 |
| **TRST_B** | T18 | JTAG | JTAG | 1 | M14 |
| **VCCIO_1** | H22 | VCCIO | VCCIO | 1 | — |
| **VCCIO_1** | J20 | VCCIO | VCCIO | 1 | — |
| **VCCIO_1** | K13 | VCCIO | VCCIO | 1 | F9 |
| **VCCIO_1** | M18 | VCCIO | VCCIO | 1 | H14 |
| **CDONE** | T14 | CONFIG | CONFIG | 2 | M10 |
| **CRESET_B** | R14 | CONFIG | CONFIG | 2 | L10 |
| **GBIN4/PIO2** | V12 | GBIN | GBIN | 2 | P7 |
| **GBIN5/PIO2** | V11 | GBIN | GBIN | 2 | P8 |
| **PIO2** | R8 | PIO | PIO | 2 | L4 |
| **PIO2** | R9 | PIO | PIO | 2 | L5 |
| **PIO2** | R10 | PIO | PIO | 2 | L6 |
| **PIO2** | R11 | PIO | PIO | 2 | L7 |
| **PIO2** | R12 | PIO | PIO | 2 | L8 |
| **PIO2** | T7 | PIO | PIO | 2 | M3 |
| **PIO2** | T8 | PIO | PIO | 2 | M4 |
| **PIO2** | T10 | PIO | PIO | 2 | M6 |
| **PIO2** | T11 | PIO | PIO | 2 | M7 |
| **PIO2** | T12 | PIO | PIO | 2 | M8 |

| Ball Function | Ball Number iCE65L04 iCE65L08 | Pin Type by Device iCE65L04 | Pin Type by Device iCE65L08 | Bank | CB132 Ball Equivalent |
|---|---|---|---|---|---|
| **PIO2** | T13 | PIO | PIO | 2 | M9 |
| **PIO2** | V6 | PIO | PIO | 2 | P2 |
| **PIO2** | V7 | PIO | PIO | 2 | P3 |
| **PIO2** | V8 | PIO | PIO | 2 | P4 |
| **PIO2** | V9 | PIO | PIO | 2 | P5 |
| **PIO2** | V13 | PIO | PIO | 2 | P9 |
| **PIO2** | Y4 | PIO | PIO | 2 | — |
| **PIO2** | Y5 | PIO | PIO | 2 | — |
| **PIO2** | Y6 | PIO | PIO | 2 | — |
| **PIO2** | Y7 | PIO | PIO | 2 | — |
| **PIO2** | Y9 | PIO | PIO | 2 | — |
| **PIO2** | Y10 | PIO | PIO | 2 | — |
| **PIO2** | Y13 | PIO | PIO | 2 | — |
| **PIO2** | Y14 | PIO | PIO | 2 | — |
| **PIO2** | Y15 | PIO | PIO | 2 | — |
| **PIO2** | Y17 | PIO | PIO | 2 | — |
| **PIO2** | Y18 | PIO | PIO | 2 | — |
| **PIO2** | Y19 | PIO | PIO | 2 | — |
| **PIO2** | Y20 | PIO | PIO | 2 | — |
| **PIO2** | AB2 | PIO | PIO | 2 | — |
| **PIO2 (●)** | AB3 | N.C. | PIO | 2 | — |
| **PIO2 (●)** | AB4 | N.C. | PIO | 2 | — |
| **PIO2** | AB6 | PIO | PIO | 2 | — |
| **PIO2** | AB7 | PIO | PIO | 2 | — |
| **PIO2** | AB8 | PIO | PIO | 2 | — |
| **PIO2** | AB9 | PIO | PIO | 2 | — |
| **PIO2** | AB10 | PIO | PIO | 2 | — |
| **PIO2** | AB11 | PIO | PIO | 2 | — |
| **PIO2** | AB12 | PIO | PIO | 2 | — |
| **PIO2** | AB13 | PIO | PIO | 2 | — |
| **PIO2** | AB14 | PIO | PIO | 2 | — |
| **PIO2** | AB15 | PIO | PIO | 2 | — |
| **PIO2 (●)** | AB16 | N.C. | PIO | 2 | — |
| **PIO2 (●)** | AB17 | N.C. | PIO | 2 | — |
| **PIO2 (●)** | AB18 | N.C. | PIO | 2 | — |
| **PIO2 (●)** | AB19 | N.C. | PIO | 2 | — |
| **PIO2 (●)** | AB20 | N.C. | PIO | 2 | — |
| **PIO2 (●)** | AB21 | N.C. | PIO | 2 | — |
| **PIO2 (●)** | AB22 | N.C. | PIO | 2 | — |
| **PIO2/CBSEL0** | R13 | PIO | PIO | 2 | L9 |
| **PIO2/CBSEL1** | V14 | PIO | PIO | 2 | P10 |
| **VCCIO_2** | N13 | VCCIO | VCCIO | 2 | J9 |
| **VCCIO_2** | T9 | VCCIO | VCCIO | 2 | M5 |
| **VCCIO_2** | Y11 | VCCIO | VCCIO | 2 | — |
| **PIO3/DP00A** | F5 | DPIO | DPIO | 3 | B1 |
| **PIO3/DP00B** | G5 | DPIO | DPIO | 3 | C1 |
| **PIO3/DP01A** | G7 | DPIO | DPIO | 3 | C3 |
| **PIO3/DP01B** | H7 | DPIO | DPIO | 3 | D3 |
| **PIO3/DP02A** | H8 | DPIO | DPIO | 3 | D4 |
| **PIO3/DP02B** | J8 | DPIO | DPIO | 3 | E4 |

| iCE65L04 Pad Name | DiePlus VQ100 | CB132 | CB196 | CB284 | Pad | X (µm) | Y (µm) |
|---|---|---|---|---|---|---|---|
| **CRESET_B** | 44 | L10 | L10 | R14 | 121 | 2,625.00 | 139.20 |
| **PIOS_00/SPI_SO** | 45 | M11 | M11 | T15 | 122 | 2,690.00 | 37.20 |
| **PIOS_01/SPI_SI** | 46 | P11 | P11 | V15 | 123 | 2,740.00 | 139.20 |
| **GND** | 47 | — | P6 | Y16 | 124 | 2,790.00 | 37.20 |
| **PIOS_02/SPI_SCK** | 48 | P12 | P12 | V16 | 125 | 2,840.00 | 139.20 |
| **PIOS_03/SPI_SS_B** | 49 | P13 | P13 | V17 | 126 | 2,890.00 | 37.20 |
| **SPI_VCC** | 50 | L11 | L11 | R15 | 127 | 2,990.00 | 37.20 |
| **TDI** | N/A | M12 | M12 | T16 | 128 | 3,610.80 | 342.00 |
| **TMS** | N/A | P14 | P14 | V18 | 129 | 3,712.80 | 392.00 |
| **TCK** | N/A | L12 | L12 | R16 | 130 | 3,610.80 | 442.00 |
| **TDO** | N/A | N14 | N14 | U18 | 131 | 3,712.80 | 492.00 |
| **TRST_B** | N/A | M14 | M14 | T18 | 132 | 3,610.80 | 542.00 |
| **PIO1_00** | 51 | L14 | K11 | R18 | 133 | 3,712.80 | 592.00 |
| **PIO1_01** | 52 | K12 | L13 | P16 | 134 | 3,610.80 | 642.00 |
| **PIO1_02** | 53 | K11 | K12 | P15 | 135 | 3,712.80 | 692.00 |
| **PIO1_03** | 54 | K14 | M13 | P18 | 136 | 3,610.80 | 727.00 |
| **GND** | 55 | J14 | J14 | N18 | 137 | 3,712.80 | 762.00 |
| **GND** | 55 | J14 | J14 | N18 | 138 | 3,610.80 | 797.00 |
| **PIO1_04** | 56 | J12 | J10 | N16 | 139 | 3,712.80 | 832.00 |
| **PIO1_05** | 57 | J11 | L14 | N15 | 140 | 3,610.80 | 867.00 |
| **VCCIO_1** | 58 | H14 | H14 | M18 | 141 | 3,712.80 | 902.00 |
| **VCCIO_1** | — | — | — | — | 142 | 3,610.80 | 937.00 |
| **PIO1_06** | 59 | H12 | J11 | M16 | 143 | 3,712.80 | 972.00 |
| **PIO1_07** | 60 | H11 | K14 | M15 | 144 | 3,610.80 | 1,007.00 |
| **PIO1_08** | — | — | H10 | W20 | 145 | 3,712.80 | 1,042.00 |
| **PIO1_09** | — | — | J13 | V20 | 146 | 3,610.80 | 1,077.00 |
| **PIO1_10** | — | — | J12 | U20 | 147 | 3,712.80 | 1,112.00 |
| **VCC** | 61 | H9 | N7 | M13 | 148 | 3,610.80 | 1,147.00 |
| **VCC** | — | — | — | — | 149 | 3,712.80 | 1,182.00 |
| **PIO1_11** | — | — | H13 | T22 | 150 | 3,610.80 | 1,217.00 |
| **PIO1_12** | — | — | H12 | R22 | 151 | 3,712.80 | 1,252.00 |
| **PIO1_13** | — | — | — | P22 | 152 | 3,610.80 | 1,287.00 |
| **PIO1_14** | — | — | — | N22 | 153 | 3,712.80 | 1,322.00 |
| **PIO1_15** | | — | G13 | T20 | 154 | 3,610.80 | 1,357.00 |
| **PIO1_16** | — | — | H11 | R20 | 155 | 3,712.80 | 1,392.00 |
| **PIO1_17** | — | — | G14 | P20 | 156 | 3,610.80 | 1,427.00 |
| **GND** | — | — | K10 | N20 | 157 | 3,712.80 | 1,462.00 |
| **GND** | — | — | — | — | 158 | 3,610.80 | 1,497.00 |
| **PIO1_18** | — | — | G10 | M20 | 159 | 3,712.80 | 1,532.00 |
| **GBIN3/PIO1_19** | 62 | F14 | G12 | K18 | 160 | 3,610.80 | 1,567.00 |
| **GBIN2/PIO1_20** | 63 | G14 | F10 | L18 | 161 | 3,712.80 | 1,602.00 |
| **PIO1_21** | — | — | F14 | K20 | 162 | 3,610.80 | 1,637.00 |
| **VCCIO_1** | — | — | H14 | J20 | 163 | 3,712.80 | 1,672.00 |
| **VCCIO_1** | — | — | — | — | 164 | 3,610.80 | 1,707.00 |
| **PIO1_22** | — | — | F13 | H20 | 165 | 3,712.80 | 1,742.00 |
| **PIO1_23** | — | — | D13 | G20 | 166 | 3,610.80 | 1,777.00 |

## Electrical Characteristics

All parameter limits are specified under worst-case supply voltage, temperature, and processing conditions.

### Absolute Maximum Ratings

Stresses beyond those listed under Table 47 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

**Table 47: Absolute Maximum Ratings**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| **VCC** | Core supply Voltage | –0.5 | 1.42 | V |
| **VPP_2V5** | VPP_2V5 NVCM programming and operating supply | | | V |
| **VPP_FAST** | Optional fast NVCM programming supply | | | V |
| **VCCIO_0**<br>**VCCIO_1**<br>**VCCIO_2**<br>**SPI_VCC** | I/O bank supply voltage (I/O Banks 0, 1, and 2 plus SPI interface) | –0.5 | 4.00 | V |
| **VCCIO_3** | I/O Bank 3 supply voltage | –0.5 | iCE65L01: 4.00<br>iCE65L04/08: 3.6 | V |
| **VIN_0**<br>**VIN_1**<br>**VIN_2**<br>**VIN_SPI** | Voltage applied to PIO pin within a specific I/O bank (I/O Banks 0, 1, and 2 plus SPI interface) | –1.0 | 5.5 | V |
| **VIN_3**<br>**VIN_VREF** | Voltage applied to PIO pin within I/O Bank 3 | –0.5 | iCE65L01: 4.00<br>iCE65L04/08: 3.6 | V |
| **IOUT** | DC output current per pin | — | 20 | mA |
| **$T_J$** | Junction temperature | –55 | 125 | °C |
| **$T_{STG}$** | Storage temperature, no bias | –65 | 150 | °C |

### Recommended Operating Conditions

***Table 48:*** **Recommended Operating Conditions**

| Symbol | Description | | Minimum | Nominal | Maximum | Units |
|---|---|---|---|---|---|---|
| VCC | Core supply voltage | –L: Ultra-Low Power mode | 0.95 | 1.00 | 1.05 | V |
| | | –L: Low Power<br>–T: High Performance | 1.14 | 1.20 | 1.26 | V |
| VPP_2V5 | VPP_2V5 NVCM programming and operating supply | Release from Power-on Reset | 1.30 | — | 3.47 | V |
| | | Configure from NVCM | 2.30 | — | 3.47 | V |
| | | NVCM programming | 2.30 | — | 3.00 | V |
| VPP_FAST | Optional fast NVCM programming supply | | Leave unconnected in application | | | |
| SPI_VCC | SPI interface supply voltage | | 1.71 | — | 3.47 | V |
| VCCIO_0<br>VCCIO_1<br>VCCIO_2<br>VCCIO_3<br>SPI_VCC | I/O standards, all banks* | **LVCMOS33** | 3.14 | 3.30 | 3.47 | V |
| | | **Non-standard voltage:**<br>in between 2.5V and 3.3V<br>use LVCMOS25 in iCEcube2 | Nominal<br>-5% | 2.5< Nominal<br><3.3 | Nominal<br>+5% | V |
| | | **LVCMOS25, LVDS** | 2.38 | 2.50 | 2.63 | V |
| | | **LVCMOS18, SubLVDS** | 1.71 | 1.80 | 1.89 | V |
| | | **LVCMOS15** | 1.43 | 1.50 | 1.58 | V |
| VCCIO_3 | I/O standards only available in iCE65L04/08 I/O Bank 3* | **SSTL2** | 2.38 | 2.50 | 2.63 | V |
| | | **SSTL18** | 1.71 | 1.80 | 1.89 | V |
| | | **MDDR** | 1.71 | 1.80 | 1.89 | V |
| $T_A$ | Ambient temperature | Commercial (C) | 0 | — | 70 | °C |
| | | Industrial (I) | –40 | — | 85 | °C |
| **$T_{PROG}$** | NVCM programming temperature | | 10 | 25 | 30 | °C |

**NOTE:**

VPP_FAST is only used for fast production programming. Leave floating or unconnected in application. When the iCE65 device is active, VPP_2V5 must be connected to a valid voltage.

## Revision History

| Version | Date | Description |
|---|---|---|
| **2.42** | 30-MAR-2012 | Changed company name. Updated Table 1 |
| **2.41** | 1-AUG-2011 | Added VQ100 marking for NVCM programming. |
| **2.4** | 13-MAY-2011 | Added L01 CB121 package Figure 39. Added note "else VCCIO_1 draws current" to JTAG inputs TCK, TDI and TMS do not have the input pull-up resistor and must be tied off to GND when unused, Table 32. Input pin leakage current Table 49 split by bank. QN84 package drawing, Figure 35, added note "underside metal is at ground potential", increased thermal resistance. Added Marking Format and Thermal resistance to CB81 Packag Mechanical Drawing Figure 33. Added coplanarity specification to VQ100 Package Mechanical Drawing Figure 37 |
| **2.3** | 18-OCT-2010 | Added L01 CB81 and L08 CB132 packages. |
| **2.2.3** | 12-OCT-2010 | Changed Figure 29: Application Processor Waveforms for SPI Peripheral Mode Configuration Process and Table 60 from 300 µs CRESET_B to 800 µs for iCE65L01/04 and 1200 µs for iCE65L08. |
| **2.2.2** | 8-OCT-2010 | Added iCE65L04 marking specification to Figure 47 CB196 Package Mechanical Drawing. |
| **2.2.1** | 5-OCT-2010 | Changed FSPI_SCK from 0.125 MHz to 1 MHz in SPI Peripheral Configuration Interface and in Table 60. |
| **2.2** | 6-AUG-2010 | Programmable Interconnect section removed. |
| **2.1.1** | 26-MAY-2010 | Switched labels on Figure 53 LVCMOS Output High, VCCIO = 1.8V with VCCIO = 2.5V. |
| **2.1** | 15-MAR-2010 | Added JTAG unused input tie off guideline. Added marking specification and thermal characteristics to package drawings. Added production datasheet for iCE65L01 with timing update, including QN84, VQ100 and CB132. Added NVCM shut-off on SPI configuration. Added non-standard VCCIO operating conditions. Increased the minimum voltage supply specification for LVCMOS33 to 3.14V in Table 48. |
| **2.0.1** | 12-NOV-2009 | Recommended Operation Conditions, Table 47, replaced junction with ambient. |
| **2.0** | 14-SEPT-2009 | Finalized production data sheet for iCE65L04 and iCE65L08. Improved SubLVDS input specification $V_{ICM}$ in Table 52. CS63 and CC72 packages removed and placed in iCE DiCE KGD, Known Good Die datasheet. Added "IBIS Models for I/O Banks 0, 1, 2 and the SPI Bank". Added "Printed Circuit Board Layout Information". |
| **1.5.1** | 13-JUL-2009 | Updated the text in "SPI PROM Requirements" section. Minor label change in Figure 48. |
| **1.5** | 20-JUN-2009 | Updated timing information and added –T high-speed device option (affected Figure 2, Table 48, Table 54, Table 55, Table 56, and Table 61). Added support for 3.3V LVCMOS I/Os in I/O Bank 3 (affected Figure 7, Table 5, Table 7, Table 8, Table 47, Table 48, and Table 51). Added a section about the SPI Peripheral Configuration Interface and timing in Table 60. Added a warning that a Warm Boot operation can only jump to another configuration image that has Warm Boot disabled. Updated configuration image size and configuration time for the iCE65L02 in Table 27 and Table 58. Reduced the minimum voltage supply specification for LVCMOS33 to 2.7V in Table 48. Added information about which power rails can be disconnected without effecting the Power-On Reset (POR) circuit and clarified description of VPP_2V5 pin in Table 36. Added I/O characterization curves (Figure 52, Figure 53, and Figure 54). Minor changes to Figure 20 and Figure 21. Changed timing per Figures 54-58 and Tables 55-57. |
| **1.4.4** | 25-MAR-2009 | Clarified the voltage requirements for the VPP_2V5 pin in Table 36 and notes under Table 48. |
| **1.4.3** | 9-MAR-2009 | Removed volatile-only (-V) product offering from Figure 2. Corrected NC on ball V22, removed it for ball T22 on CB284 package (Figure 48). |
| **1.4.2** | 27-FEB-2009 | Updated Table 14, Table 23, Table 26, Table 30, Table 33, Table 35, and Table 46. Updated I/O Bank 3 information in Table 7 and Table 48. |
| **1.4.1** | 24-FEB-2009 | Based on characterization data, reduced 32KHz operating current by 40% in Table 1, Table 61, and Figure 1. Corrected that SSTL18 standards require VREF pin in Table 7. Correct ball numbers for GBIN4/GBIN5 for CS110 package. |
| **1.4** | 9-FEB-2009 | Added footprint and pinout information for the VQ100 Very-thin Quad Flat Package. Added footprint for iCE65L08 in CB196 (Figure 46) and added Table 43 showing the differences between the 'L04 and 'L08 in the CB196 package. Unified the package footprint nomenclature in the Package and Pinout Information section. Added note to Global Buffer Inputs that the differential clock direct input is not available on the CB132 package. Added tables showing the ball/pin number for various control functions, by package (Table 14, Table 23, Table 26, Table 30, and Table 33). Corrected the GBIN/GBUF designations. GBIN4 and GBIN5 were swapped as were GBIN6 and GBIN7. This change affected all pinout tables and footprint diagrams. Updated and corrected "Differential Global Buffer Input." Tested and corrected the clock-enable and reset connections between global buffers and various resources (Table 11, Table 12, and Table 13). Added "Automatic Global Buffer Insertion, Manual Insertion." Added "Die Cross Reference" section. Improved industrial temperature range by lowering |