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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

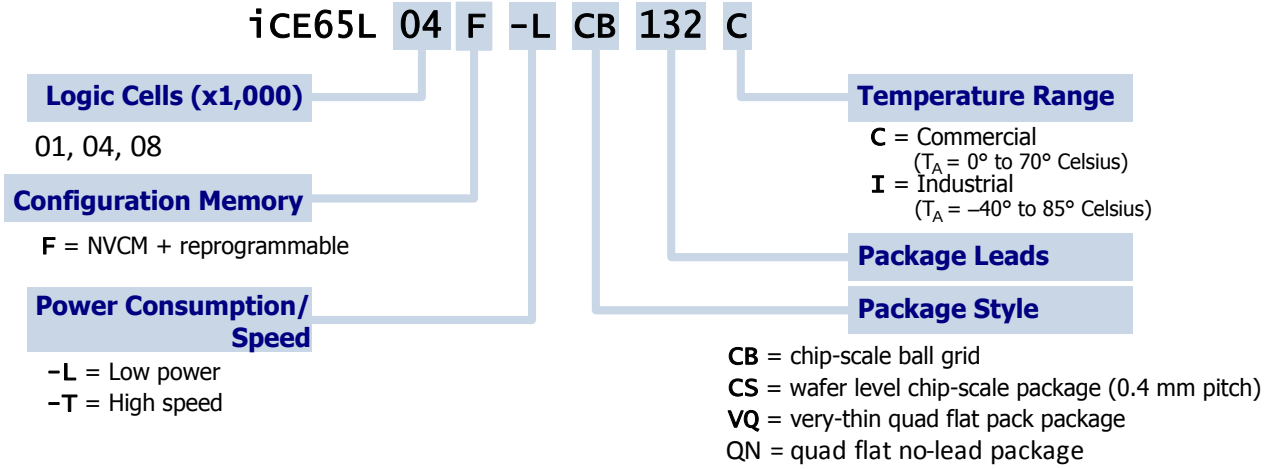
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	160
Number of Logic Elements/Cells	1280
Total RAM Bits	65536
Number of I/O	25
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	-
Supplier Device Package	36-WLCSP
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice65l01f-tcs36i

Ordering Information

Figure 2 describes the iCE65 ordering codes for all packaged, non-NVCM Programed components. See the separate DiePlus data sheets when ordering die-based products.

Figure 2: **iCE65 Ordering Codes Standard Device**

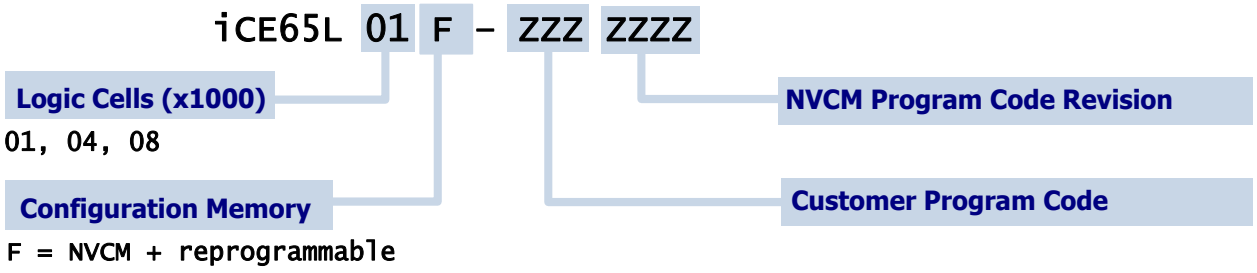


iCE65 devices offer two power consumption, speed options. Standard products ("-L" ordering code) have low standby and dynamic power consumption. The "-T" provides higher-speed logic.

Similarly, iCE65 devices are available in two operating temperature ranges, one for typical commercial applications, the other with an extended temperature range for industrial and telecommunications applications. The ordering code also specifies the device package option, as described further in Table 2.

Figure 3 describes the iCE65 ordering codes for all packaged, NVCM Programmed components.

Figure 3: **iCE65 Ordering Codes NVCM Programmed Device**



Programmable Logic Block (PLB)

Generally, a logic design for an iCE65 component is created using a high-level hardware description language such as Verilog or VHDL. The Lattice Semiconductor development software then synthesizes the high-level description into equivalent functions built using the programmable logic resources within each iCE65 device. Both sequential and combinational functions are constructed from an array of Programmable Logic Blocks (PLBs). Each PLB contains eight Logic Cells (LCs), as pictured in Figure 4, and share common control inputs, such as clocks, reset, and enable controls.

PLBs are connected to one another and other logic functions using the rich Programmable Interconnect resources.

Logic Cell (LC)

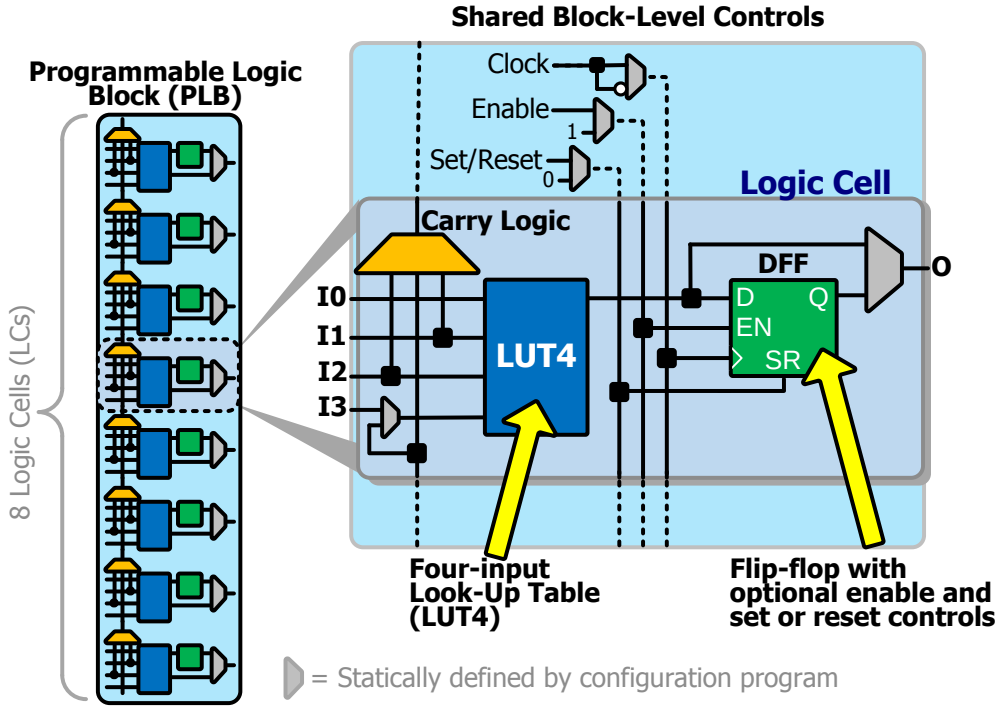
Each iCE65 device contains thousands of Logic Cells (LCs), as listed in Table 1. Each Logic Cell includes three primary logic elements, shown in Figure 4.

- A four-input Look-Up Table (LUT4) builds any combinational logic function, of any complexity, of up to four inputs. Similarly, the LUT4 element behaves as a 16x1 Read-Only Memory (ROM). Combine and cascade multiple LUT4s to create wider logic functions.

Figure 4: **Programmable Logic Block and Logic Cell**

- A 'D'-style Flip-Flop (DFF), with an optional clock-enable and reset control input, builds sequential logic functions. Each DFF also connects to a global reset signal that is automatically asserted immediately following device configuration.
- Carry Logic boosts the logic efficiency and performance of arithmetic functions, including adders, subtracters, comparators, binary counters and some wide, cascaded logic functions.

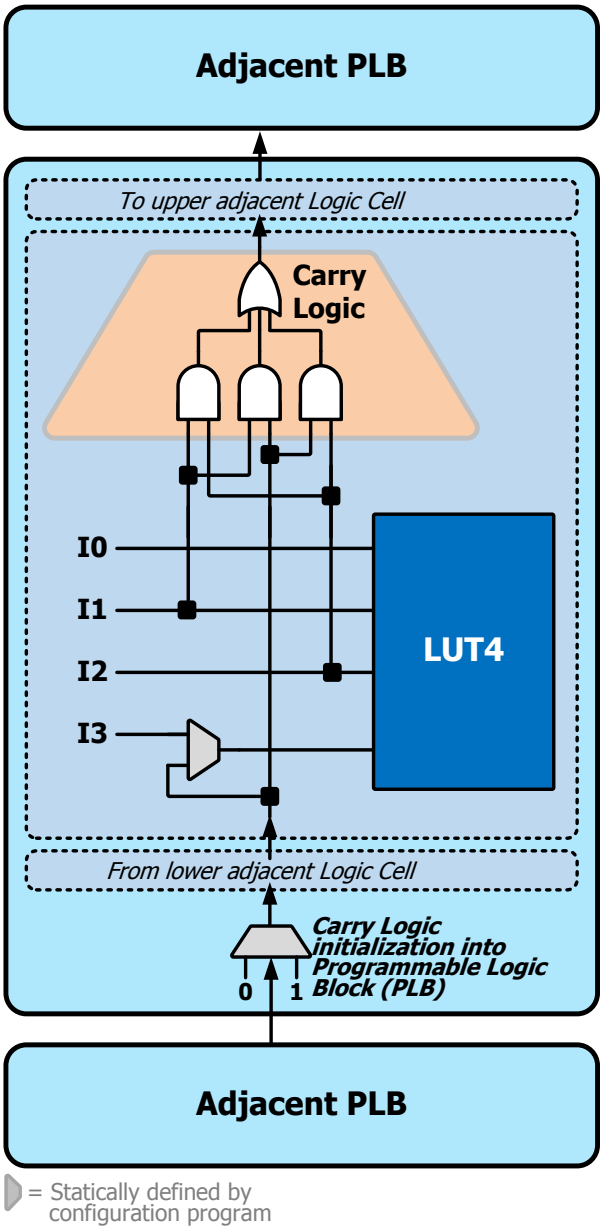
The output from a Logic Cell is available to all inputs to all eight Logic Cells within the Programmable Logic Block. Similarly, the Logic Cell output feeds into fabric to connect to other features on the iCE65 device.



The Carry Logic generates the carry value to feed the next bit in the adder. The calculated carry value replaces the I3 input to the next LUT4 in the upper Logic Cell.

If required by the application, the carry output from the final stage of the adder is available by passing it through the final LUT4.

Figure 5: **Carry Logic Structure within a Logic Cell and between PLBs**



Input and Output Register Control per PIO Pair

PIO pins are grouped into pairs for synchronous control. Registers within pairs of PIO pins share common input clock, output clock, and I/O clock enable control signals, as illustrated in Figure 11. The combinational logic paths are removed from the drawing for clarity.

The INCLK clock signal only controls the input flip-flops within the PIO pair.

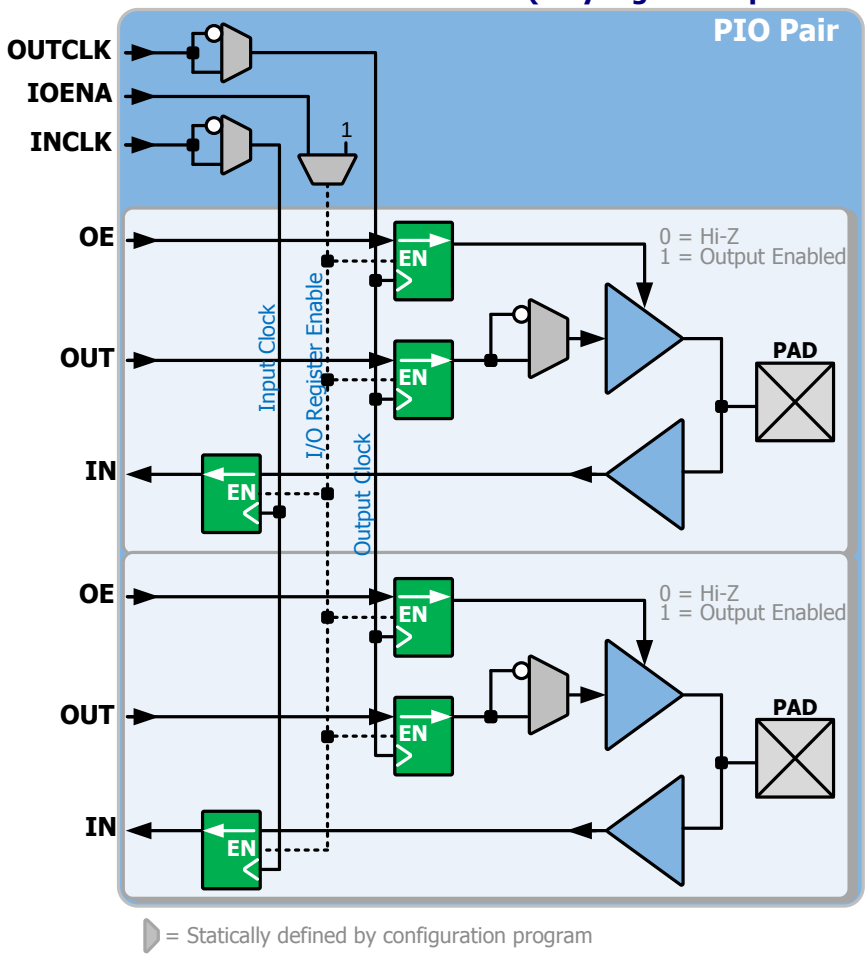
The OUTCLK clock signal controls the output flip-flops and the output-enable flip-flops within the PIO pair.

If desired in the iCE65 application, the INCLK and OUTCLK signals can be connected together.

The IOENA clock-enable input, if used, enables all registers in the PIO pair, as shown in Figure 11. By default, the registers are always enabled.

Before laying out your printed-circuit board, run the design through the iCEcube development software to verify that your selected pinout complies with these I/O register pairing requirements. See tables in "Die Cross Reference" starting on page 84.

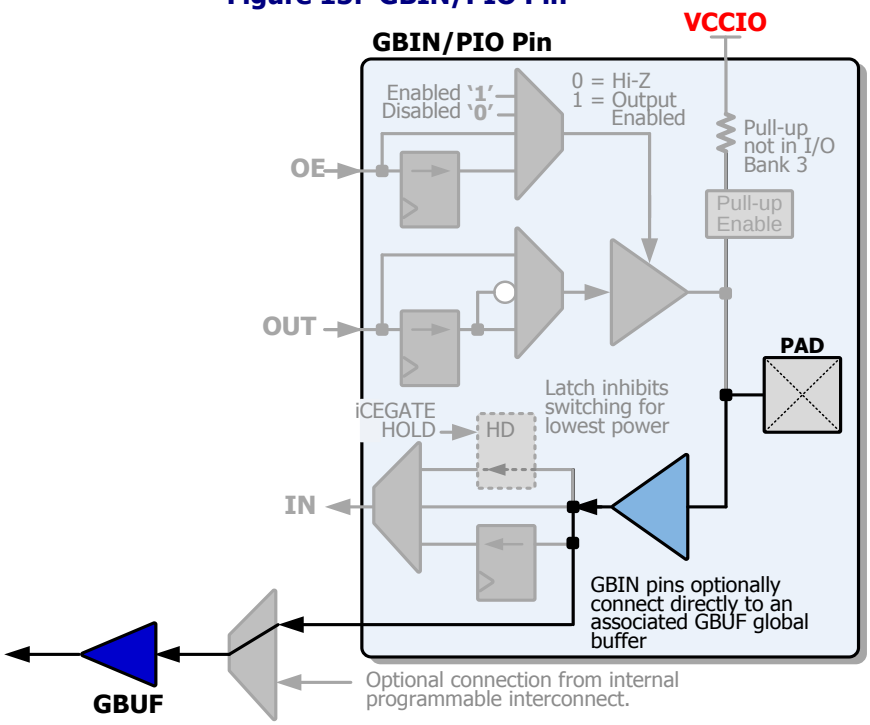
Figure 11: **PIO Pairs Share Clock and Clock Enable Controls (only registered paths shown for clarity)**



The pairing of PIO pairs is most evident in the tables in "Die Cross Reference" starting on page 84.

Note the clock differences between the iCE65L04 and iCE65L08 in the CB196 package.

Figure 15: GBIN/PIO Pin



Differential Global Buffer Input

All eight global buffer inputs support single-ended I/O standards such as LVCMOS. Global buffer GBUF7 in I/O Bank 3 also provides an optional direct SubLVDS, LVDS, or LVPECL differential clock input, as shown in Figure 16. The GBIN7 and its associated differential I/O pad accept a differential clock signal. A 100 Ω termination resistor is required across the two pads. Optionally, swap the outputs from the LVDS or LVPECL clock driver to invert the clock as it enters the iCE65 device.

Figure 16: LVDS or LVPECL Clock Input

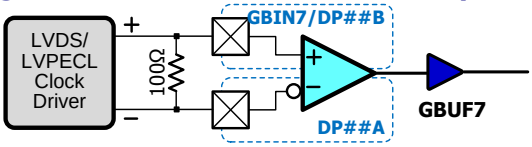


Table 15 lists the pin or ball numbers for the differential global buffer input by package style. Although this differential input is the only one that connects directly to a global buffer, other differential inputs can connect to a global buffer using general-purpose interconnect, with slightly more signal delay.

***Table 15:* Differential Global Buffer Input Ball/Pin Number by Package**

Differential Global Buffer Input (GBIN)	I/O Bank	VQ100	CB132	'L04 CB196	'L08 CB196	CB284
GBIN7/DPxxB	3	13	N/A	G1	H3	L5
DPxxA		12	N/A	G2	H4	L3

The differential global buffer input is not available for iCE65 devices in the CB132 package. This restriction is an artifact of the pin compatibility between the CB132 and CB284 package.

Note the clock differences between the iCE65L04 and iCE65L08 in the CB196 package.

- Register file and scratchpad RAM
- First-In, First-Out (FIFO) memory for data buffering applications
- Circuit buffer
- A 256-deep by 16-wide ROM with registered outputs, contents loaded during configuration
  - Sixteen different 8-input look-up tables
  - Function or waveform tables such as sine, cosine, etc.
  - Correlators or pattern matching operations
- Counters, sequencers

As pictured in Figure 17, a RAM4K block has separate write and read ports, each with independent control signals. Table 17 lists the signals for both ports. Additionally, the write port has an active-Low bit-line write-enable control; optionally mask write operations on individual bits. By default, input and output data is 16 bits wide, although the data width is configurable using programmable logic and, if needed, multiple RAM4K blocks.

The WCLK and RCLK inputs optionally connect to one of the following clock sources.

- The output from any one of the eight Global Buffers, or
- A connection from the general-purpose interconnect fabric

The data contents of the RAM4K block are optionally pre-loaded during iCE65 device configuration. If the RAM4K blocks are not pre-loaded during configuration, then the resulting configuration bitstream image is smaller. However, if an uninitialized RAM4K block is used in the application, then the application must initialize the RAM contents to guarantee the data value.

See Table 56 for detailed timing information.

Signals

Table 17 lists the signal names, direction, and function of each connection to the RAM4K block. See also Figure 17.

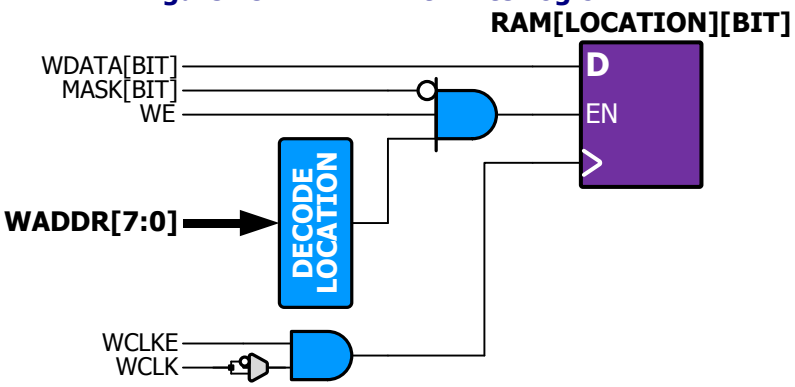
Table 17: RAM4K Block RAM Signals

Signal Name	Direction	Description
WDATA[15:0]	Input	Write Data input.
MASK[15:0]	Input	Masks write operations for individual data bit-lines. 0 = Write bit; 1 = Don't write bit
WADDR[7:0]	Input	Write Address input. Selects one of 256 possible RAM locations.
WE	Input	Write Enable input.
WCLKE	Input	Write Clock Enable input.
WCLK	Input	Write Clock input. Default rising-edge, but with falling-edge option.
RDATA[15:0]	Output	Read Data output.
RADDR[7:0]	Input	Read Address input. Selects one of 256 possible RAM locations.
RE	Input	Read Enable input.
RCLKE	Input	Read Clock Enable input.
RCLK	Input	Read Clock input. Default rising-edge, but with falling-edge option.

Write Operations

Figure 18 shows the logic involved in writing a data bit to a RAM location. Table 18 describes various write operations for a RAM4K block. By default, all RAM4K write operations are synchronized to the rising edge of WCLK although the clock is invertible as shown in Figure 18.

Figure 18: RAM4K Bit Write Logic



When the WCLKE signal is Low, the clock to the RAM4K block is disabled, keeping the RAM in its lowest power mode.

Table 18: RAM4K Write Operations

Operation	WDATA[15:0] Data	MASK[15:0] Mask Bit	WADDR[7:0] Address	WE Write Enable	WCLKE Clock Enable	WCLK Clock	RAM Location
Disabled	X	X	X	X	X	0	No change
Disabled					0	X	No change
Disabled	X	X	X	0	X	X	No change
Write Data	WDATA[i]	MASK[i] = 0	WADDR	1	1	↑	RAM[WADDR][i] = WDATA[i]
Masked Write	X	MASK[i] = 1	WADDR	1	1	↑	RAM[WADDR][i] = No change

To write data into the RAM4K block, perform the following operations.

- Supply a valid address on the WADDR[7:0] address input port
- Supply valid data on the WDATA[15:0] data input port
- To write or mask selected data bits, set the associated MASK input port accordingly. For example, write operations on data bit D[i] are controlled by the associated MASK[i] input.
  - MASK[i] = 0: Write operations are enabled for data line WDATA[i]
  - MASK[i] = 1: Mask write operations are disabled for data line WDATA[i]
- Enable the RAM4K write port (WE = 1)
- Enable the RAM4K write clock (WCLKE = 1)
- Apply a rising clock edge on WCLK (assuming that the clock is not inverted)

Read Operations

Figure 19 shows the logic involved in reading a location from RAM. Table 19 describes various read operations for a RAM4K block. By default, all RAM4K read operations are synchronized to the rising edge of RCLK although the clock is invertible as shown in Figure 19.

Figure 21: iCE65 Configuration Control Pins

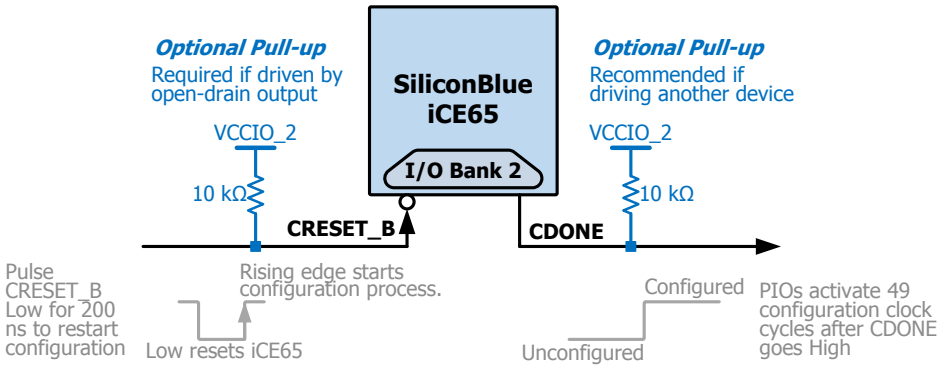


Figure 21 shows the two iCE65 configuration control pins, CRESET_B and CDONE. Table 23 lists the ball/pin numbers for the configuration control pins by package. When driven Low for at least 200 ns, the dedicated Configuration Reset input, CRESET_B, resets the iCE65 device. When CRESET_B returns High, the iCE65 FPGA restarts the configuration process from its power-on conditions (Cold Boot). The CRESET_B pin is a pure input with no internal pull-up resistor. If driven by open-drain driver or un-driven, then connect the CRESET_B pin to a 10 kΩ pull-up resistor connected to the VCCIO_2 supply.

***Table 23:* Configuration Control Ball/Pin Numbers by Package**

Configuration Control Pins	CB81	QN84	VQ100	CB132	CB196	CB284
CRESET_B	J6	A21	44	L10	L10	R14
CDONE	H6	B16	43	M10	M10	T14

The iCE65 device signals the end of the configuration process by actively turning off the internal pull-down transistor on the Configuration Done output pin, CDONE. The pin has a permanent, weak internal pull-up resistor to the VCCIO_2 rail. If the iCE65 device drives other devices, then optionally connect the CDONE pin to a 10 kΩ pull-up resistor connected to the VCCIO_2 supply.

The PIO pins activate according to their configured function after 49 configuration clock cycles. The internal oscillator is the configuration clock source for the SPI Master Configuration Interface and when configuring from

* Note: only 14 of the 16 RAM4K Memory Blocks may be pre-initialized in the iCE65L01.

Nonvolatile Configuration Memory (NVCM). When using the SPI Peripheral Configuration Interface, the configuration clock source is the SPI_SCK clock input pin.

Internal Oscillator

During SPI Master or NVCM configuration mode, the controlling clock signal is generated from an internal oscillator. The oscillator starts operating at the Default frequency. During the configuration process, however, bit settings within the configuration bitstream can specify a higher-frequency mode in order to maximize SPI bandwidth and reduce overall configuration time. See Table 57: Internal Oscillator Frequency on page 105 for the specified oscillator frequency range.

Using the SPI Master Configuration Interface, internal oscillator controls all the interface timing and clocks the SPI serial Flash PROM via the SPI_SCK clock output pin.

The oscillator output, which also supplies the SPI SCK clock output during the SPI Flash configuration process, has a 50% duty cycle.

Internal Device Reset

Figure 22 presents the various signals that internally reset the iCE65 internal logic.

- Power-On Reset (POR)
- CRESET_B Pin
- JTAG Interface

Figure 24: **SPI Release from Deep Power-down Command**

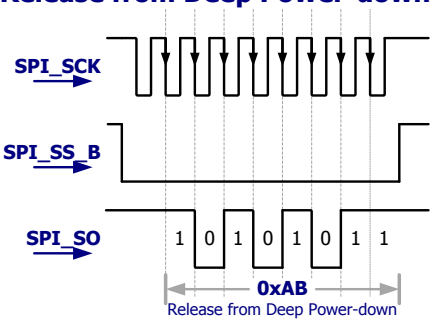
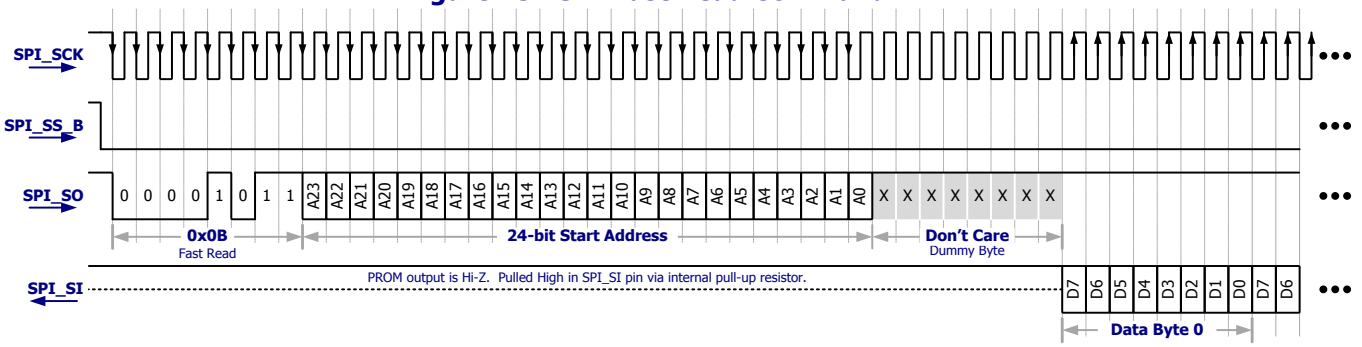


Figure 25 illustrates the next command issued by the iCE65 device. The iCE65 SPI interface again drives SPI_SS_B Low, followed by a Fast Read command, hexadecimal command code 0x0B, followed by a 24-bit start address, transmitted on the SPI_SO output. The iCE65 device provides data on the falling edge of SPI_SS_B. Upon initial power-up, the start address is always 0x00_0000. After waiting eight additional clock cycles, the iCE65 device begins reading serial data from the SPI PROM. Before presenting data, the SPI PROM's serial data output is high-impedance. The SPI_SI input pin has an internal pull-up resistor and sees high-impedance as logic '1'.

Figure 25: SPI Fast Read Command



The external SPI PROM supplies data on the falling edge of the iCE65 device's SPI_SCK clock output. The iCE65 device captures each PROM data value on the SPI_SI input, using the rising edge of the SPI_SCK clock signal. The SPI PROM data starts at the 24-bit address presented by the iCE65 device. PROM data is serially output, byte by byte, with most-significant bit, D7, presented first. The PROM automatically increments an internal byte counter as long as the PROM is selected and clocked.

After transferring the required number configuration data bits, the iCE65 device ends the Fast Read command by de-asserting its SPI_SS_B PROM select output, as shown in Figure 26. To conserve power, the iCE65 device then optionally issues a final Deep Power-down command, hexadecimal command code 0xB9. After de-asserting the SPI_SS_B output, the SPI PROM enters its Deep Power-down mode. The final power-down step is optional; the application may use the SPI PROM and can skip this step, controlled by a configuration option.

Figure 26: **Final Configuration Data, SPI Deep Power-down Command**

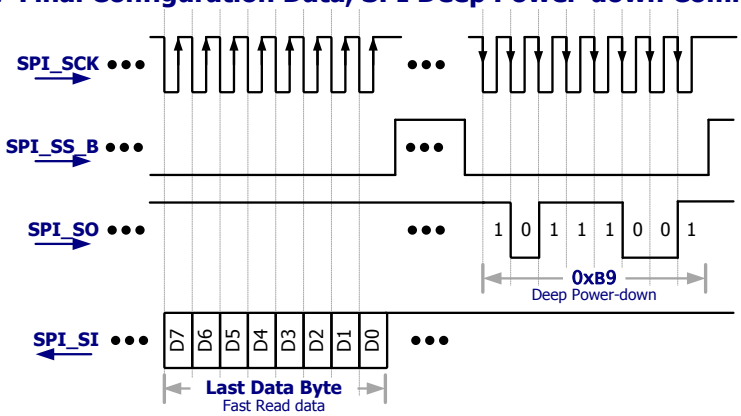
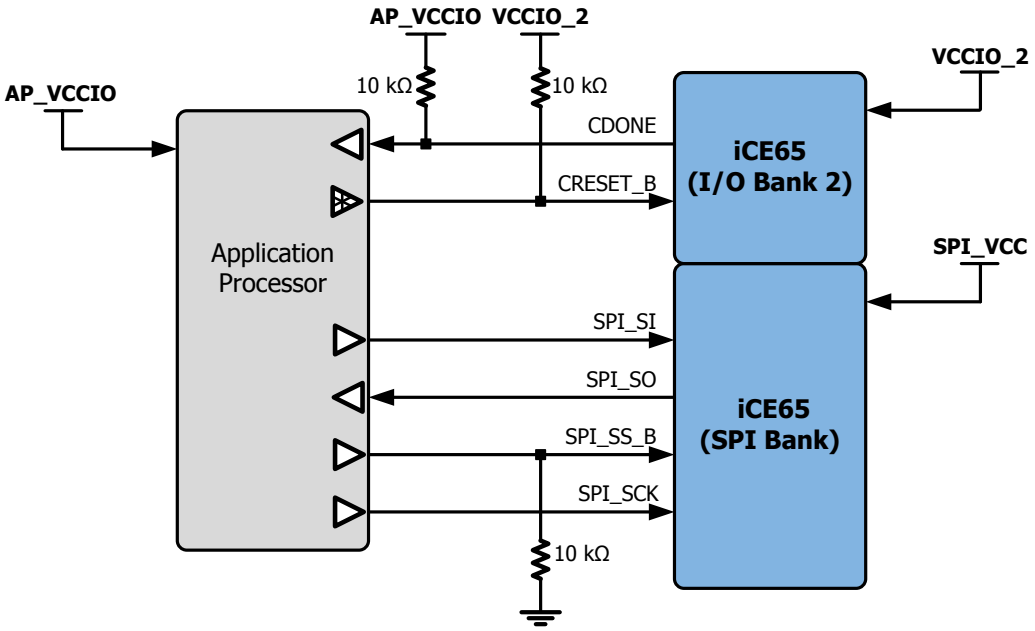


Figure 28: **iCE65 SPI Peripheral Configuration Interface**



The SPI control signals are defined in Table 25.

Table 29: **SPI Peripheral Configuration Interface Pins (SPI_SS_B Low when CRESET_B Released)**

Signal Name	Direction	iCE65 I/O Supply	Description
CDONE	AP ← iCE65	VCCIO_2	Configuration Done output from iCE65. Connect to a 10kΩ pull-up resistor to the application processor I/O voltage, AP_VCC.
CRESET_B	AP → iCE65		Configuration Reset input on iCE65. Typically driven by AP using an open-drain driver, which also requires a 10kΩ pull-up resistor to VCCIO_2.
SPI_VCC	Supply	SPI_VCC	SPI Flash PROM voltage supply input.
SPI_SI	AP → iCE65		SPI Serial Input to the iCE65 FPGA, driven by the application processor.
SPI_SO	AP ← iCE65		SPI Serial Output from CE65 device to the application processor. Not actually used during SPI peripheral mode configuration but required if the SPI interface is also used to program the NVCM.
SPI_SS_B	AP → iCE65		SPI Slave Select output from the application processor. Active Low. Optionally hold Low prior to configuration using a 10kΩ pull-down resistor to ground.
SPI_SCK	AP → iCE65		SPI Slave Clock output from the application processor.

After configuration, the SPI port pins are available to the user-application as additional PIO pins, supplied by the SPI_VCC input voltage, essentially providing a fifth "mini" I/O bank.

Enabling SPI Configuration Interface

The optional 10 kΩ pull-down resistor on the SPI_SS_B signal ensures that the iCE65 FPGA powers up in the SPI peripheral mode. Optionally, the application processor drives the SPI_SS_B pin Low when CRESET_B is released, forcing the iCE65 FPGA into SPI peripheral mode.

SPI Peripheral Configuration Process

Figure 29 illustrates the interface timing for the SPI peripheral mode and Figure 30 outlines the resulting configuration process. The actual timing specifications appear in Table 60. The application processor (AP) begins by driving the iCE65 CRESET_B pin Low, resetting the iCE65 FPGA. Similarly, the AP holds the iCE65's SPI_SS_B pin Low. The AP must hold the CRESET_B pin Low for at least 200 ns. Ultimately, the AP either releases the CRESET_B pin and allows it to float High via the 10 kΩ pull-up resistor to VCCIO_2 or drives CRESET_B High. The iCE65 FPGA enters SPI peripheral mode when the CRESET_B pin returns High while the SPI_SS_B pin is Low.

After driving CRESET_B High or allowing it to float High, the AP must wait a minimum of t_{CR_SCK} µs, (see Table 60) allowing the iCE65 FPGA to clear its internal configuration memory.

After waiting for the configuration memory to clear, the AP sends the configuration image generated by the iCEcube development system. An SPI peripheral mode configuration image must not use the ColdBoot or WarmBoot options. Send the entire configuration image, without interruption, serially to the iCE65's SPI_SI input on the falling edge of the SPI_SCK clock input. Once the AP sends the 0x7EAA997E synchronization pattern, the generated SPI_SCK clock frequency must be within the specified 1 MHz to 25 MHz range (40 ns to 1 µs clock period) while sending the configuration image. Send each byte of the configuration image with most-significant bit (msb) first. The AP sends data to the iCE65 FPGA on the falling edge of the SPI_SCK clock. The iCE65 FPGA internally captures each incoming SPI_SI data bit on the rising edge of the SPI_SCK clock. The iCE65's SPI_SO output pin is not used during SPI peripheral mode but must connect to the AP if the AP also programs the iCE65's Nonvolatile Configuration Memory (NVCM).

Prior to sending the iCE65 configuration image , an SPI NVCM shut-off sequence must be sent. See AN014 for details.
The iCE65 configuration image must be sent as one contiguous stream without interruption.
The SPI_SCK clock period must be between 40 ns to 1 µs (1 MHz to 25 MHz).

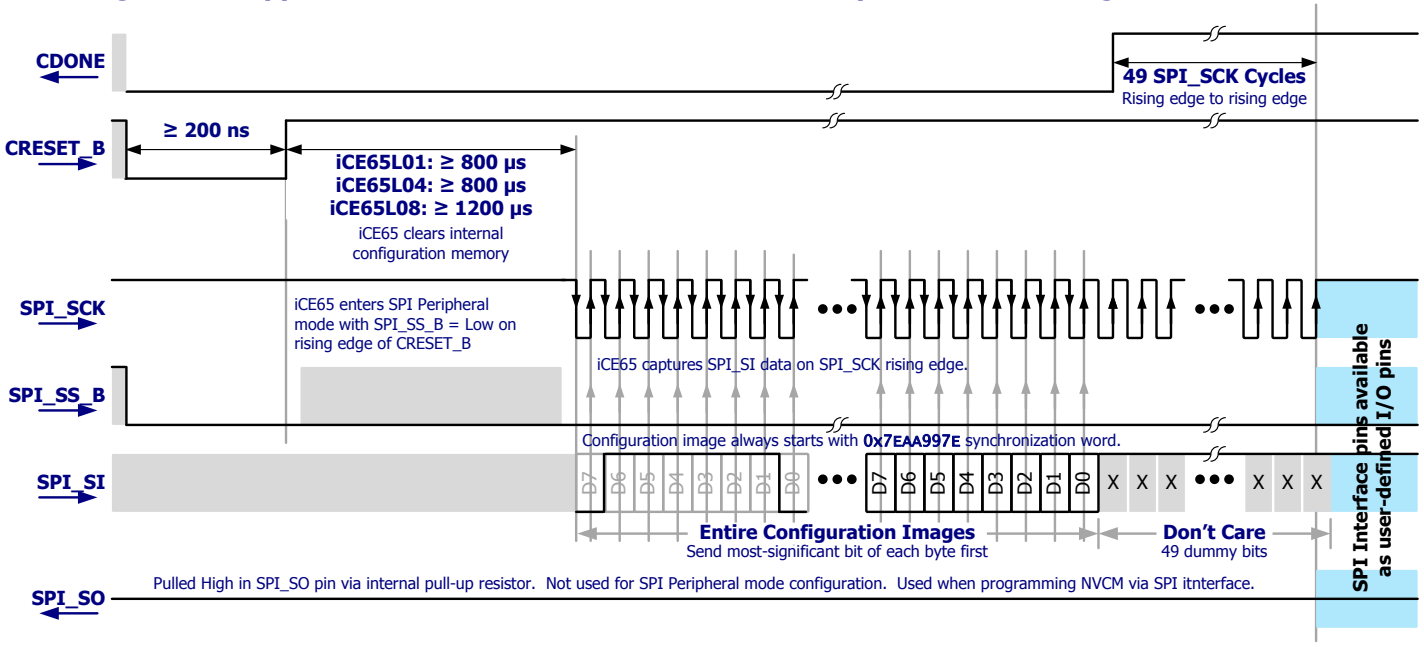
After sending the entire image, the iCE65 FPGA releases the CDONE output allowing it to float High via the 10 kΩ pull-up resistor to AP_VCC. If the CDONE pin remains Low, then an error occurred during configuration and the AP should handle the error accordingly for the application.

After the CDONE output pin goes High, send at least 49 additional dummy bits, effectively 49 additional SPI_SCK clock cycles measured from rising-edge to rising-edge.

After the additional SPI_CLK cycles, the SPI interface pins then become available to the user application loaded in FPGA.

To reconfigure the iCE65 FPGA or to load a different configuration image, merely restart the configuration process by pulsing CRESET_B Low or power-cycling the FPGA.

Figure 29: **Application Processor Waveforms for SPI Peripheral Mode Configuration Process**



The iCE65 configuration image must be sent as one contiguous stream without interruption.

The SPI_SCK clock period must be between 40 ns to 1 µs (1 MHz to 25 MHz).

Table 31 describes how to maintain voltage compatibility for two interface scenarios. The easiest interface is when the Application Processor's (AP) I/O supply rail and the iCE65's SPI and VCCIO_2 bank supply rails all connect to the same voltage. The second scenario is when the AP's I/O supply voltage is greater than the iCE65's VCCIO_2 supply voltage.

***Table 31:* CRESET_B and CDONE Voltage Compatibility**

Condition	CRESET_B			CDONE Pull-up	Requirement
	Direct	**Open-Drain**	**Pull-up**		
VCCIO_AP = VCC_SPI **VCCIO_AP = VCCIO_2**	OK	OK with pull-up	Required if using open-drain output	Recommended	AP can directly drive CRESET_B High and Low although an open-drain output recommended is if multiple devices control CRESET_B. If using an open-drain driver, the CRESET_B input must include a 10 kΩ pull-up resistor to VCCIO_2. The 10 kΩ pull-up resistor to AP_VCCIO is also recommended.
AP_VCCIO > VCCIO_2	N/A	Required, requires pull-up	Required	Required	The AP must control CRESET_B with an open-drain output, which requires a 10 kΩ pull-up resistor to VCCIO_2. The 10 kΩ pull-up resistor to AP_VCCIO is required.

JTAG Boundary Scan Port

Overview

Each iCE65 device includes an IEEE 1149.1-compatible JTAG boundary-scan port. The port supports printed-circuit board (PCB) testing and debugging. It also provides an alternate means to configure the iCE65 device.

Signal Connections

The JTAG port connections are listed in Table 32.

***Table 32:* iCE65 JTAG Boundary Scan Signals**

Signal Name	Direction	Description
TDI	Input	Test Data Input. Must be tied off to GND when unused. (no pull-up resistor)*
TMS	Input	Test Mode Select. Must be tied off to GND when unused. (no pull-up resistor)*
TCK	Input	Test Clock. Must be tied off to GND when unused. (no pull-up resistor)*
TDO	Output	Test Data Output.
TRST_B	Input	Test Reset, active Low. Must be Low during normal device operation. Must be High to enable JTAG operations.*

* Must be tied off to GND or VCCIO_1, else VCCIO_1 draws current.

Table 33 lists the ball/pin numbers for the JTAG interface by package code. The JTAG interface is available in select package types. The JTAG port is located in I/O Bank 1 along the right edge of the iCE65 device and powered by the VCCIO_1 supply inputs. Consequently, the JTAG interface uses the associated I/O standards for I/O Bank 1.

***Table 33:* JTAG Interface Ball/Pin Numbers by Package**

JTAG Interface	VQ100	CB132	CB196	CB284
TDI	N/A	M12	M12	T16
TMS		P14	P14	V18
TCK		L12	L12	R16
TDO		N14	N14	U18
TRST_B		M14	M14	T18

iCE65 Pin Descriptions

Table 36 lists the various iCE65 pins, alphabetically by name. The table indicates the directionality of the signal and the associated I/O bank. The table also indicates if the signal has an internal pull-up resistor enabled during configuration. Finally, the table describes the function of the pin.

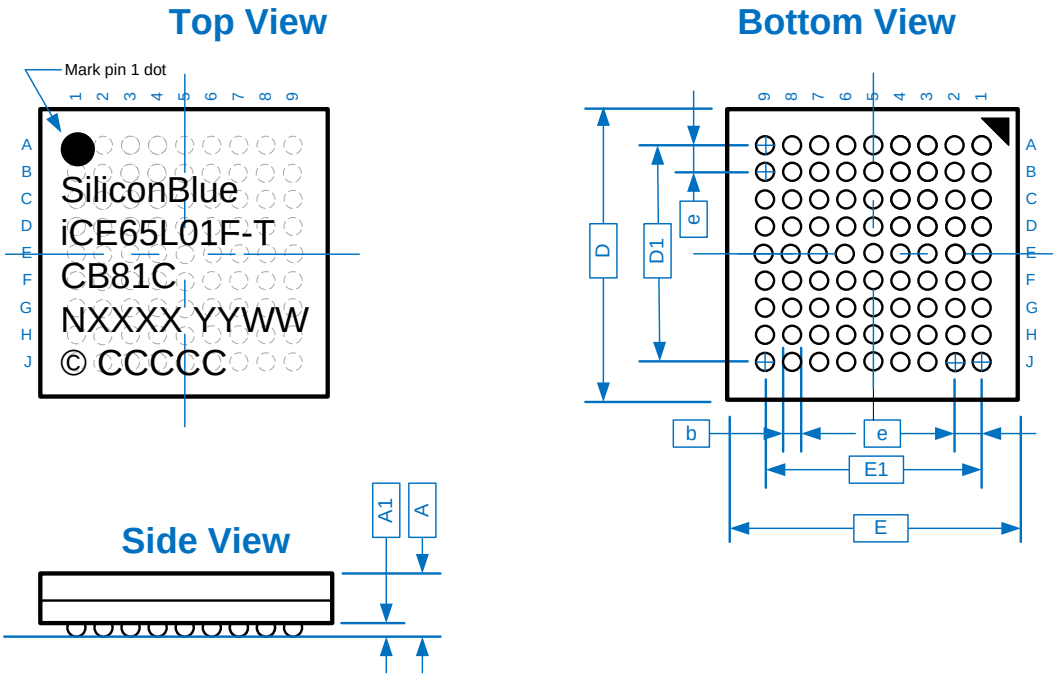
Table 36: iCE65 Pin Description

Signal Name	Direction	I/O Bank	Pull-up during Config	Description
CDONE	Output	2	Yes	Configuration Done. Dedicated output. Includes a permanent weak pull-up resistor to VCCIO_2.. If driving external devices with CDONE output, connect a 10 kΩ pull-up resistor to VCCIO_2.
CRESET_B	Input	2	No	Configuration Reset, active Low. Dedicated input. No internal pull-up resistor. Either actively drive externally or connect a 10 kΩ pull-up resistor to VCCIO_2.
GBIN0/PIO0 GBIN1/PIO0	Input/IO	0	Yes	Global buffer input from I/O Bank 0. Optionally, a full-featured PIO pin.
GBIN2/PIO1 GBIN3/PIO1	Input/IO	1	Yes	Global buffer input from I/O Bank 1. Optionally, a full-featured PIO pin.
GBIN4/PIO2 GBIN5/PIO2	Input/IO	2	Yes	Global buffer input from I/O Bank 2. Optionally, a full-featured PIO pin.
GBIN6/PIO3	Input/IO	3	No	Global buffer input from I/O Bank 3. Optionally, a full-featured PIO pin.
GBIN7/PIO3	Input/IO	3	No	Global buffer input from I/O Bank 3. Optionally, a full-featured PIO pin. Optionally, a differential clock input using the associated differential input pin.
GND	Supply	All	N/A	Ground. All must be connected.
PIOx_yy	I/O	0,1,2	Yes	Programmable I/O pin defined by the iCE65 configuration bitstream. The 'x' number specifies the I/O bank number in which the I/O pin resides. The "yy' number specifies the I/O number in that bank.
PIO2/CBSEL0	Input/IO	2	Yes	Optional ColdBoot configuration SELect input, if ColdBoot mode is enabled. A full-featured PIO pin after configuration.
PIO2/CBSEL1	Input/IO	2	Yes	Optional ColdBoot configuration SELect input, if ColdBoot mode is enabled. A full-featured PIO pin after configuration.
PIO3_yy/ DPwwz	I/O	3	No	Programmable I/O pin that is also half of a differential I/O pair. Only available in I/O Bank 3. The "yy" number specifies the I/O number in that bank. The "ww" number indicates the differential I/O pair. The 'z' indicates the polarity of the pin in the differential pair. 'A'=negative input. 'B'=positive input.
PIOS/SPI_SO	I/O	SPI	Yes	SPI Serial Output. A full-featured PIO pin after configuration.
PIOS /SPI_SI	I/O	SPI	Yes	SPI Serial Input. A full-featured PIO pin after configuration.
PIOS / SPI_SS_B	I/O	SPI	Yes	SPI Slave Select. Active Low. Includes an internal weak pull-up resistor to SPI_VCC during configuration. During configuration, the logic level sampled on this pin determines the configuration mode used by the iCE65 device, as shown in Figure 20. An input when sampled at the start of configuration. An input when in SPI Peripheral configuration mode (SPI_SS_B = Low). An output when in SPI Flash configuration mode. A full-featured PIO pin after configuration.
PIOS/ SPI_SCK	I/O	SPI	Yes	SPI Slave Clock. An input when in SPI Peripheral configuration mode (SPI_SS_B = Low). An output when in SPI Flash configuration mode. A full-featured PIO pin after configuration.
TDI	Input	1	No	JTAG Test Data Input. If using the JTAG interface, use a 10kΩ pull-up resistor to VCCIO_1. Tie off to GND when unused.

Ball Function	Ball Number	Pin Type	Bank
PIO3	B1	PIO	3
PIO3	B2	PIO	3
PIO3	B3	PIO	3
PIO3	C1	PIO	3
PIO3	C2	PIO	3
PIO3	C3	PIO	3
GBIN7/PIO3	D1	GBIN	3
PIO3	D2	PIO	3
PIO3	D3	PIO	3
GBIN6/PIO3	E1	GBIN	3
PIO3	E2	PIO	3
PIO3	E3	PIO	3
PIO3	F2	PIO	3
PIO3	F3	PIO	3
PIO3	G1	PIO	3
PIO3	G2	PIO	3
PIO3	H1	PIO	3
PIO3	H2	PIO	3
VCCIO_3	F1	VCCIO	3
PIOS/SPI_SO	H7	SPI	SPI
PIOS/SPI_SI	J7	SPI	SPI
PIOS/SPI_SCK	J8	SPI	SPI
PIOS/SPI_SS_B	H8	SPI	SPI
SPI_VCC	H9	SPI	SPI
GND	A1	GND	GND
GND	A9	GND	GND
GND	J9	GND	GND
GND	J1	GND	GND
GND	E4	GND	GND
GND	E5	GND	GND
GND	F4	GND	GND
GND	F5	GND	GND
VCC	A5	VCC	VCC
VCC	J5	VCC	VCC
VPP_2V5	B9	VPP	VPP

***Figure 33:* CB81 Package Mechanical Drawing**

CB81: 5 x 5 mm, 81-ball, 0.5 mm ball-pitch, chip-scale ball grid array



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			9		Columns
Number of Ball Rows	Y			9		Rows
Number of Signal Balls		n		81		Balls
Body Size	X	E	4.90	5.00	5.10	mm
	Y	D	4.90	5.00	5.10	
Ball Pitch		e	—	0.50	—	
Ball Diameter		b	0.2	—	0.3	
Edge Ball Center to Center	X	E1	—	4.00	—	
	Y	D1	—	4.00	—	
Package Height		A	—	—	1.00	
Stand Off		A1	0.15	—	0.25	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65P01F	Part number
	-T	Power/Speed
3	CB81C	Package type
	ENG	Engineering
4	NXXXX	Lot Number
5	YYWW	Date Code
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
67	57

QN84 Quad Flat Pack No-Lead

The QN84 is a Quad Flat Pack No-Lead package with a 0.5 mm pad pitch.

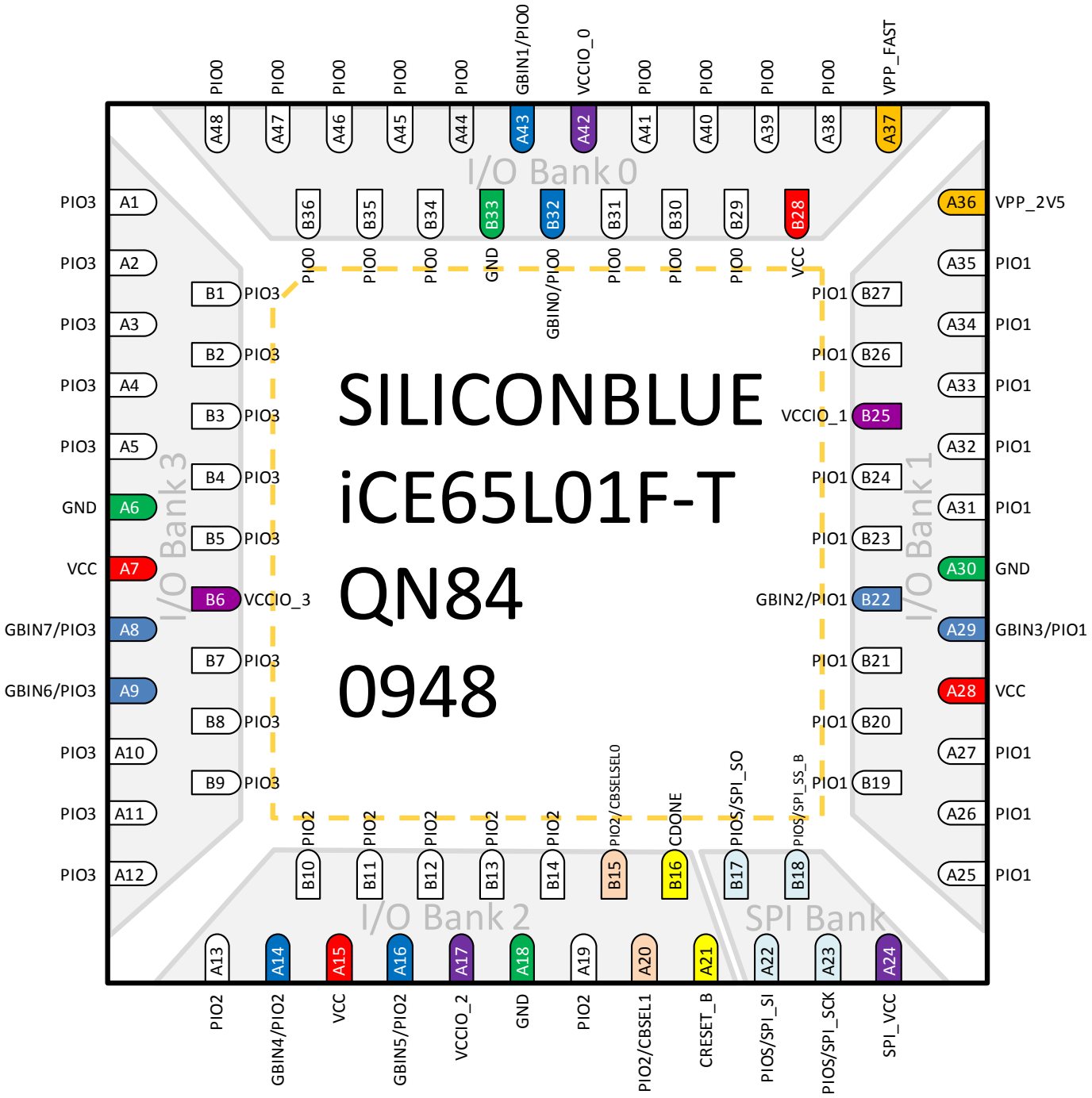
Footprint Diagram

Figure 34 shows the iCE65 footprint diagram for the QN84 package.

Also see Table 38 for a complete, detailed pinout for the QN84 package.

The signal pins are also grouped into the four I/O Banks and the SPI interface.

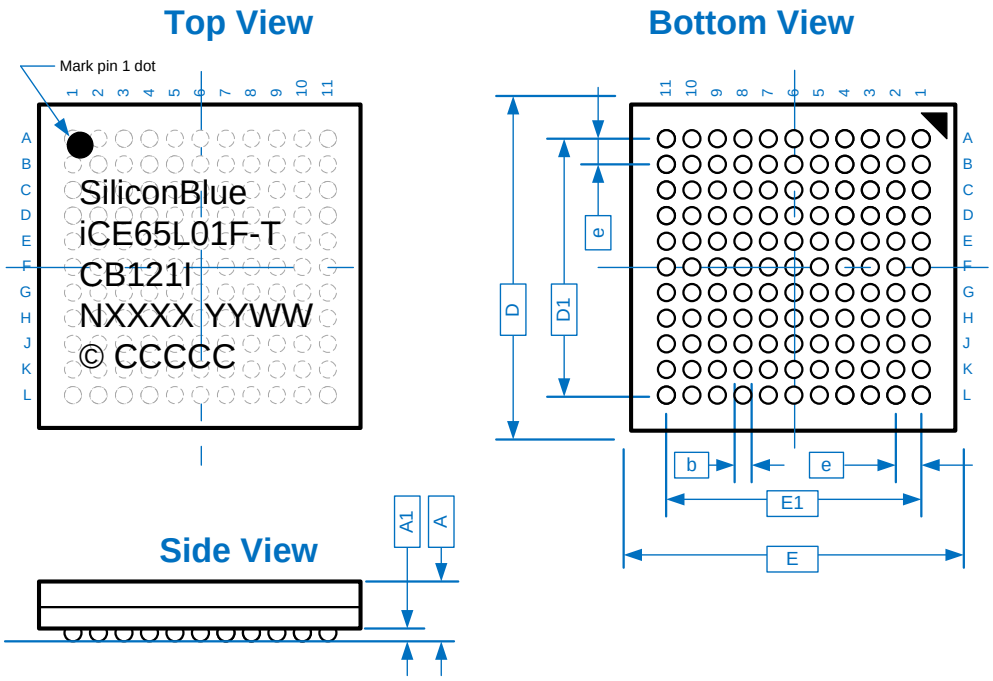
Figure 34: **iCE65 QN84 Quad Flat Pack No-Lead Footprint (Top View)**



Ball Function	Ball Number	Pin Type	Bank
GND	K2	GND	GND
GND	K10	GND	GND
VCC	B6	VCC	VCC
VCC	F1	VCC	VCC
VCC	F11	VCC	VCC
VCC	K6	VCC	VCC
VPP_2V5	C10	VPP	VPP
VPP_FAST	A9	VPP	VPP

***Figure 40:* CB121 Package Mechanical Drawing**

CB121: 6 x 6 mm, 121-ball, 0.5 mm ball-pitch, fully-populated, chip-scale ball grid array



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			11		Columns
Number of Ball Rows	Y			11		Rows
Number of Signal Balls		n		121		Balls
Body Size	X	E	5.90	6.00	6.10	mm
	Y	D	5.90	6.00	6.10	
Ball Pitch		e	—	0.50	—	
Ball Diameter		b	0.2	—	0.3	
Edge Ball Center to Center	X	E1	—	5.00	—	
	Y	D1	—	5.00	—	
Package Height		A	—	—	1.00	
Stand Off		A1	0.12	—	0.20	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65L01F	Part number
	-T	Power/Speed
3	CB121I	Package type
	ENG	Engineering
4	NXXXX	Lot Number
5	YYWW	Date Code
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
64	55

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO1_30	—	K20	222	4,572.5	2,407.115
PIO1_31	G14	F22	223	4,470.5	2,442.115
PIO1_32	—	G22	224	4,572.5	2,477.115
PIO1_33	F11	E22	225	4,470.5	2,512.115
PIO1_34	F12	L16	226	4,572.5	2,547.115
PIO1_35	G13	D22	227	4,470.5	2,582.115
GND	G8	L12	228	4,572.5	2,617.115
GND	—	—	229	4,470.5	2,652.115
PIO1_36	E10	K16	230	4,572.5	2,687.12
VCCIO_1	H14	H22	231	4,470.5	2,722.12
VCCIO_1	—	—	232	4,572.5	2,757.12
PIO1_37	F14	H20	233	4,470.5	2,792.12
PIO1_38	E11	J18	234	4,572.5	2,827.12
PIO1_39	D12	C22	235	4,470.5	2,862.12
PIO1_40	F13	J16	236	4,572.5	2,897.12
PIO1_41	E13	B22	237	4,470.5	2,932.12
PIO1_42	E12	H18	238	4,572.5	2,967.12
PIO1_43	E14	G20	239	4,470.5	3,002.12
PIO1_44	—	L15	240	4,572.5	3,037.12
PIO1_45	—	A22	241	4,470.5	3,072.12
PIO1_46	—	H16	242	4,572.5	3,107.12
VCC	K13	L20	243	4,470.5	3,142.12
VCC	—	—	244	4,572.5	3,177.12
PIO1_47	D14	F20	245	4,470.5	3,229.615
PIO1_48	D11	K15	246	4,572.5	3,279.615
VCCIO_1	H14	K13	247	4,470.5	3,329.615
VCCIO_1	—	—	248	4,572.5	3,379.615
PIO1_49	C14	E20	249	4,470.5	3,429.62
PIO1_50	D13	J15	250	4,572.5	3,479.615
GND	J14	L13	251	4,470.5	3,529.615
GND	—	—	252	4,572.5	3,579.615
PIO1_51	B14	D20	253	4,470.5	3,629.615
PIO1_52	C13	G18	254	4,572.5	3,679.595
PIO1_53	B13	C20	255	4,470.5	3,729.595
PIO1_54	C12	F18	256	4,572.5	3,779.595
VPP_2V5	A14	E18	257	4,470.5	3,879.575
VPP_FAST	A13	E17	258	3,866.975	4,054.5
VCC	F8	K12	259	3,766.98	4,156.5
VCC	—	—	260	3,716.98	4,054.5
PIO0_00	—	G16	261	3,666.98	4,156.5
PIO0_01	—	C19	262	3,616.98	4,054.5
PIO0_02	C11	H15	263	3,566.98	4,156.5
PIO0_03	—	C18	264	3,516.98	4,054.5
PIO0_04	A12	H14	265	3,466.98	4,156.5
VCCIO_0	F6	A21	266	3,416.98	4,054.5
PIO0_05	B11	C17	267	3,366.98	4,156.5
PIO0_06	D10	E16	268	3,316.98	4,054.5
PIO0_07	A11	G15	269	3,266.98	4,156.5

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO0_42	C5	A5	316	1,559.48	4,054.5
PIO0_43	B5	G9	317	1,524.48	4,156.5
PIO0_44	A4	A3	318	1,489.48	4,054.5
PIO0_45	—	A4	319	1,454.48	4,156.5
PIO0_46	—	A2	320	1,419.48	4,054.5
PIO0_47	—	C7	321	1,384.48	4,156.5
PIO0_48	—	C6	322	1,331.98	4,054.5
VCCIO_0	A8	K10	323	1,281.98	4,156.5
VCCIO_0	—	—	324	1,231.98	4,054.5
PIO0_49	—	E8	325	1,181.98	4,156.5
PIO0_50	B4	A1	326	1,131.98	4,054.5
PIO0_51	C4	E7	327	1,081.98	4,156.5
PIO0_52	A3	C5	328	1,031.98	4,054.5
PIO0_53	B3	E6	329	981.98	4,156.5
PIO0_54	D5	C3	330	931.98	4,054.5
GND	A9	L11	331	881.98	4,156.5
GND	—	—	332	831.98	4,054.5
PIO0_55	B2	G8	333	781.98	4,156.5
PIO0_56	A2	C4	334	731.98	4,054.5
PIO0_57	A1	H10	335	681.98	4,156.5
PIO0_58	—	E5	336	631.98	4,054.5
PIO0_59	—	H9	337	581.98	4,156.5