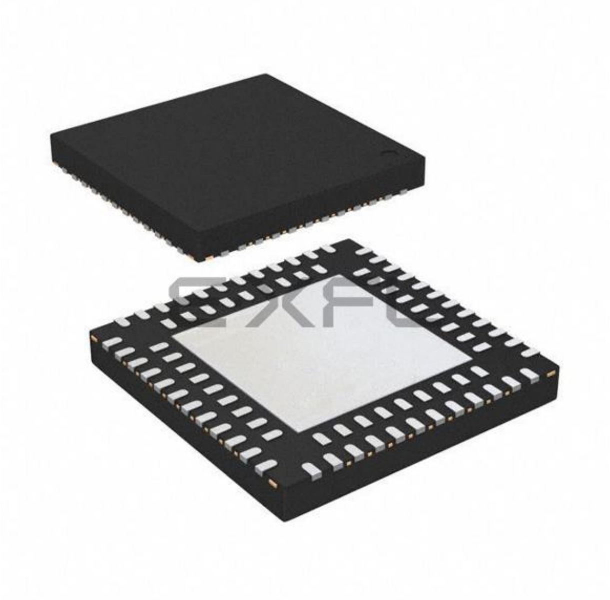

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	160
Number of Logic Elements/Cells	1280
Total RAM Bits	65536
Number of I/O	67
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	84-VFQFN Dual Rows, Exposed Pad
Supplier Device Package	84-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice65l01f-tqn84i

Look-Up Table (LUT4)

The four-input Look-Up Table (LUT4) function implements any and all combinational logic functions, regardless of complexity, of between zero and four inputs. Zero-input functions include "High" (1) and "Low" (0). The LUT4 function has four inputs, labeled I0, I1, I2, and I3. Three of the four inputs are shared with the Carry Logic function, as shown in Figure 4. The bottom-most LUT4 input connects either to the I3 input or to the Carry Logic output from the previous Logic Cell.

The output from the LUT4 function connects to the flip-flop within the same Logic Cell. The LUT4 output or the flip-flop output then connects to the programmable interconnect.

For detailed LUT4 internal timing, see Table 54.

'D'-style Flip-Flop (DFF)

The 'D'-style flip-flop (DFF) optionally stores state information for the application.

The flip-flop has a data input, 'D', and a data output, 'Q'. Additionally, each flip-flop has up to three control signals that are shared among all flip-flops in all Logic Cells within the PLB, as shown in Figure 4. Table 3 describes the behavior of the flip-flop based on inputs and upon the specific DFF design primitive used or synthesized.

Table 3: 'D'-Style Flip-Flop Behavior

DFF Primitive	Operation	Flip-Flop Mode	Inputs				Output
			D	EN	SR	CLK	Q
All	Cleared Immediately after Configuration	X	X	X	X	X	0
	Hold Present Value (Disabled)		X	0	X	X	Q
	Hold Present Value (Static Clock)		X	X	X	1 or 0	Q
	Load with Input Data		D	1*	0*	↑	D
SB_DFFR	Asynchronous Reset	Asynchronous Reset	X	X	1	X	0
SB_DFFS	Asynchronous Set	Asynchronous Set	X	X	1	X	1
SB_DFFSR	Synchronous Reset	Synchronous Reset	X	1*	1	↑	0
SB_DFFSS	Synchronous Set	Synchronous Set	X	1*	1	↑	1

X = don't care, ↑ = rising clock edge (default polarity), 1* = High or unused, 0* = Low or unused

The CLK clock signal is not optional and is shared among all flip-flops in a Programmable Logic Block. By default, flip-flops are clocked by the rising edge of the PLB clock input, although the clock polarity can be inverted for all the flip-flops in the PLB.

The CLK input optionally connects to one of the following clock sources.

- The output from any one of the eight Global Buffers, or
- A connection from the general-purpose interconnect fabric

The EN clock-enable signal is common to all Logic Cells in a Programmable Logic Block. If the enable signal is not used, then the flip-flop is always enabled. This condition is indicated as "1*" in Table 3. The asterisk indicates that this is the default state if the control signal is not connected in the application.

Similarly, the SR set/reset signal is common to all Logic Cells in a Programmable Logic Block. If not used, then the flip-flop is never set/reset, except when cleared immediately after configuration or by the Global Reset signal. This condition is indicated as "0*" in Table 3. The asterisk indicates that this is the default state if the control signal is not connected in the application.

Input Signal Path

As shown in Figure 7, a signal from a package pin optionally feeds directly into the device, or is held in an input register. The input signal connects to the programmable interconnect resources through the IN signal. Table 9 describes the input behavior, assuming that the output path is not used or if a bidirectional I/O, that the output driver is in its high-impedance state (Hi-Z). Table 9 also indicates the effect of the Power-Saving I/O Bank iCEgate Latch and the Input Pull-Up Resistors on I/O Banks 0, 1, and 2.

See Input and Output Register Control per PIO Pair for information about the registered input path.

Power-Saving I/O Bank iCEgate Latch

To save power, the optional iCEgate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Registered inputs are effectively frozen by their associated clock or clock-enable control. As shown in Figure 10, the iCEgate HOLD control signal captures the external value from the associated asynchronous input. The HOLD signal prevents switching activity on the PIO pad from affecting internal logic or programmable interconnect. Minimum power consumption occurs when there is no switching. However, individual pins within the I/O bank can bypass the iCEgate latch and directly feed into the programmable interconnect, remaining active during low-power operation. This behavior is described in Table 9. The decision on which asynchronous inputs use the iCEgate feature and which inputs bypass it is determined during system design. In other words, the iCEgate function is part of the source design used to create the iCE65 configuration image.

Figure 10: Power-Saving iCEgate Latch

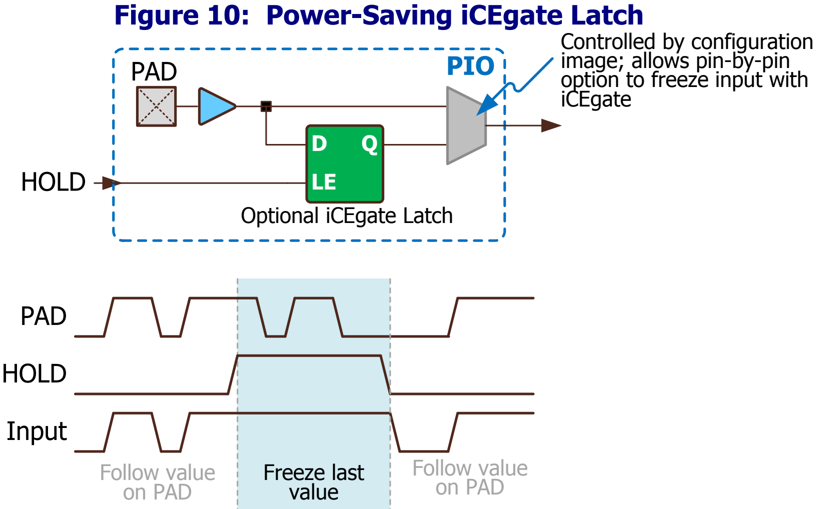


***Table 9:* PIO Non-Registered Input Operations**

Operation	HOLD iCEgate Latch	Bitstream Setting Controlled by iCEgate?	Bitstream Setting Input Pull-Up Enabled?	PAD Pin Value	IN Input Value to Interconnect
Data Input	0	X	X	PAD	PAD Value
Pad Floating, No Pull-up	0	X	No	Z	(Undefined)
Pad Floating, Pull-up	0	X	Yes	Z	1
Data Input, Latch Bypassed	X	No	X	PAD	PAD Value
Pad Floating, No Pull-up, Latch Bypassed	X	No	No	Z	(Undefined)
Pad Floating, Pull-up, Latch Bypassed	X	No	Yes	Z	1
Low Power Mode, Hold Last Value	1	Yes	X	X	Last Captured PAD Value

There are four iCEgate HOLD controls, one per each I/O bank. The iCEgate HOLD control input originates within the interconnect fabric, near the middle of the I/O edge. Consequently, the HOLD signal is optionally controlled externally through a PIO pin or from other logic within the iCE65 device.

Input and Output Register Control per PIO Pair

PIO pins are grouped into pairs for synchronous control. Registers within pairs of PIO pins share common input clock, output clock, and I/O clock enable control signals, as illustrated in Figure 11. The combinational logic paths are removed from the drawing for clarity.

The INCLK clock signal only controls the input flip-flops within the PIO pair.

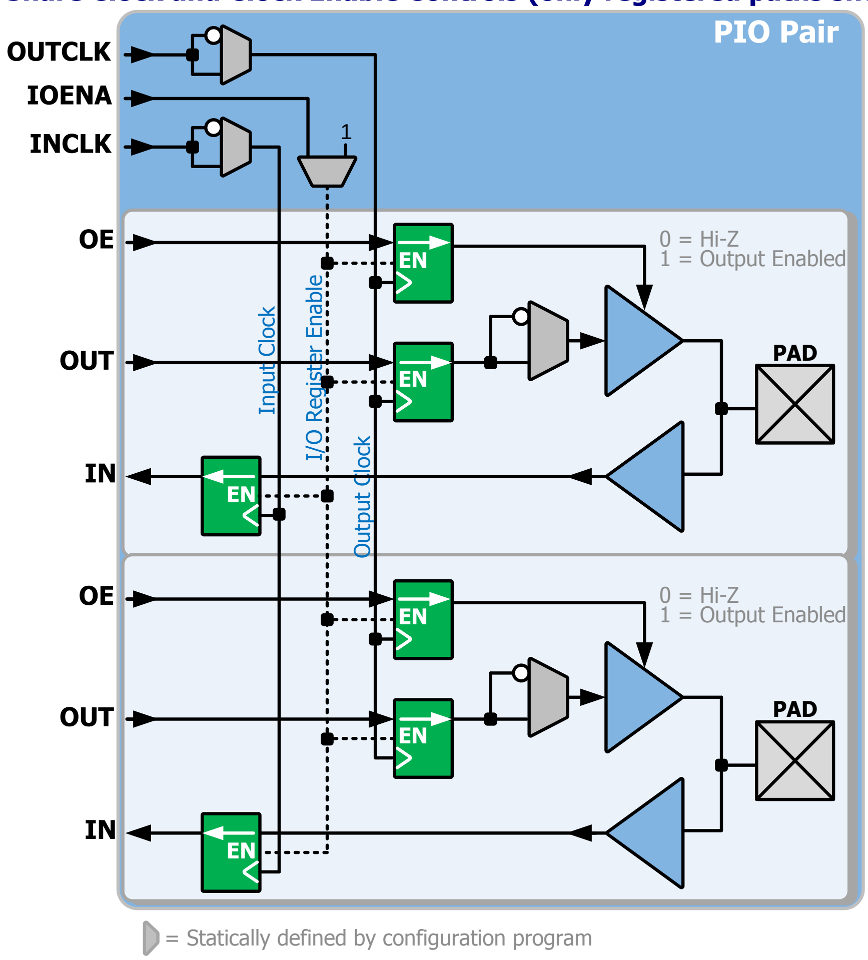
The OUTCLK clock signal controls the output flip-flops and the output-enable flip-flops within the PIO pair.

If desired in the iCE65 application, the INCLK and OUTCLK signals can be connected together.

The IOENA clock-enable input, if used, enables all registers in the PIO pair, as shown in Figure 11. By default, the registers are always enabled.

> ⚠ Before laying out your printed-circuit board, run the design through the iCEcube development software to verify that your selected pinout complies with these I/O register pairing requirements. See tables in "Die Cross Reference" starting on page 84.

Figure 11: **PIO Pairs Share Clock and Clock Enable Controls (only registered paths shown for clarity)**



The pairing of PIO pairs is most evident in the tables in "Die Cross Reference" starting on page 84.

Automatic Global Buffer Insertion, Manual Insertion

The iCEcube development software automatically assigns high-fanout signals to a global buffer. However, to manual insert a global buffer input/global buffer (GBIN/GBUF) combination, use the `SB_IO_GB` primitive. To insert just a global buffer (GBUF), use the `SB_GB` primitive.

Global Hi-Z Control

The global high-impedance control signal, GHIZ, connects to all I/O pins on the iCE65 device. This GHIZ signal is automatically asserted throughout the configuration process, forcing all user-I/O pins into their high-impedance state. Similarly, the PIO pins can be forced into their high-impedance state via the JTAG controller.

Global Reset Control

The global reset control signal connects to all PLB and PIO flip-flops on the iCE65 device. The global reset signal is automatically asserted throughout the configuration process, forcing all flip-flops to their defined wake-up state. For PLB flip-flops, the wake-up state is always reset, regardless of the PLB flip-flop primitive used in the application. See Table 3 for more information.

The PIO flip-flops are always reset during configuration, although the output flip-flop can be inverted before leaving the iCE65 device, as shown in Figure 11.

RAM

Each iCE65 device includes multiple high-speed synchronous RAM blocks (RAM4K), each 4Kbit in size. As shown in Table 16 a single iCE65 integrates between 16 to 96 such blocks. Each RAM4K block is generically a 256-word deep by 16-bit wide, two-port register file, as illustrated in Figure 17. The input and output connections, to and from a RAM4K block, feed into the programmable interconnect resources.

Figure 17: RAM4K Memory Block

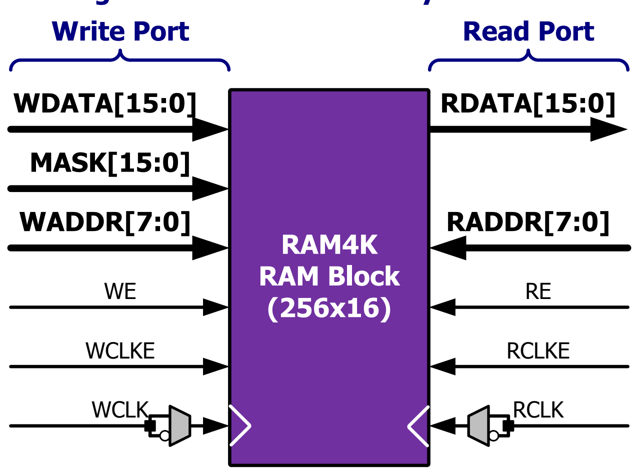


Table 16: RAM4K Blocks per Device

Device	RAM4K Blocks	Default Configuration	RAM Bits per Block	Block RAM Bits
iCE65L01	16	256 x 16	4K (4,096)	64K
iCE65L04	20			80K
iCE65L08	32			128K

Using programmable logic resources, a RAM4K block implements a variety of logic functions, each with configurable input and output data width.

- Random-access memory (RAM)
  - Single-port RAM with a common address, enable, and clock control lines
  - Two-port RAM with separate read and write control lines, address inputs, and enable

Figure 19: RAM4K Read Logic

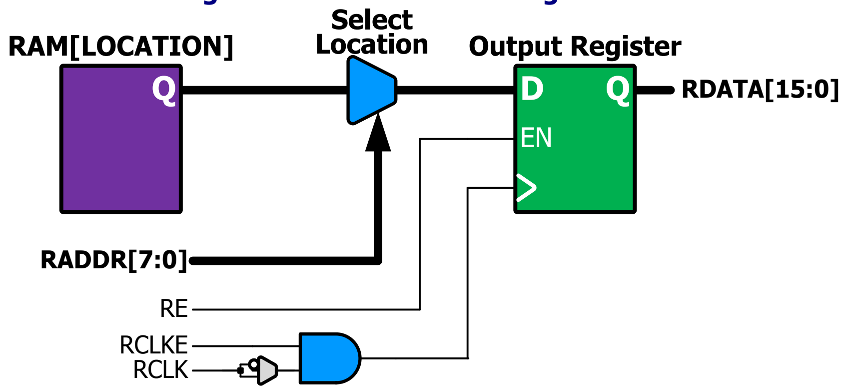


Table 19: RAM4K Read Operations

Operation	RADDR[7:0] Address	RE Read Enable	RCLKE Clock Enabe	RCLK Clock	RDATA[15:0]
After configuration, before first valid Read Data operation	X	X	X	X	Undefined
Disabled	X	X	X	0	No Change
Disabled		X	0	X	No Change
Disabled	X	0	X	X	No change
Read Data	RADDR	1	1	↑	RAM[RADDR]

To read data from the RAM4K block, perform the following operations.

- Supply a valid address on the RADDR[7:0] address input port
- Enable the RAM4K read port (RE = 1)
- Enable the RAM4K read clock (RCLKE = 1)
- Apply a rising clock edge on RCLK
- After the clock edge, the RAM contents located at the specified address (RADDR) appear on the RDATA output port

Read Data Register Undefined Immediately after Configuration

Unlike the flip-flops in the Programmable Logic Blocks and Programmable I/O pins, the RDATA[15:0] read data output register is not automatically reset after configuration. Consequently, immediately following configuration and before the first valid Read Data operation, the initial RDATA[15:0] read value is undefined.

Pre-loading RAM Data

The data contents for a RAM4K block can be optionally pre-loaded during iCE65 configuration. If not pre-loaded during configuration, then the RAM contents must be initialized by the iCE65 application before the RAM contents are valid.

Pre-loading the RAM data in the configuration bitstream increases the size of the configuration image accordingly.

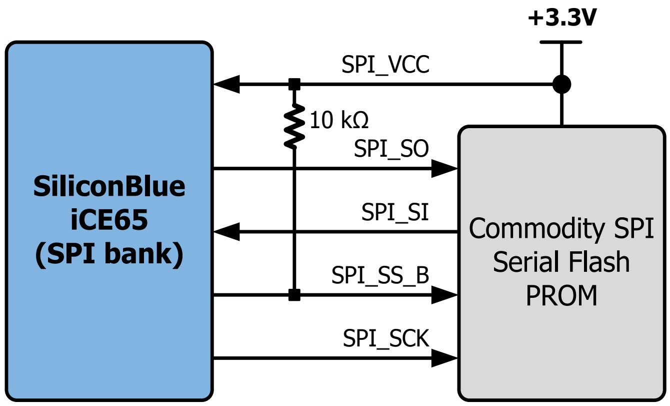
RAM Contents Preserved during Configuration

RAM contents are preserved (write protected) during configuration, assuming that voltage supplies are maintained throughout. Consequently, data can be passed between multiple iCE65 configurations by leaving it in a RAM4K block and then skipping pre-loading during the subsequent reconfiguration. See "Cold Boot Configuration Option" and "Warm Boot Configuration Option" for more information.

Low-Power Setting

To place a RAM4K block in its lowest power mode, keep WCLKE = 0 and RCLKE = 0. In other words, when not actively using a RAM4K block, disable the clock inputs.

Figure 23: **iCE65 SPI Master Configuration Interface**



The SPI configuration interface is used primarily during development before mass production, where the configuration is then permanently programmed in the NVCM configuration memory. However, the SPI interface can also be the primary configuration interface allowing easy in-system upgrades and support for multiple configuration images.

The SPI control signals are defined in Table 25. Table 26 lists the SPI interface ball or pins numbers by package.

Table 25: **SPI Master Configuration Interface Pins (SPI_SS_B High before Configuration)**

Signal Name	Direction	Description
SPI_VCC	Supply	SPI Flash PROM voltage supply input.
SPI_SO	Output	SPI Serial Output from the iCE65 device.
SPI_SI	Input	SPI Serial Input to the iCE65 device, driven by the select SPI serial Flash PROM.
SPI_SS_B	Output	SPI Slave Select output from the iCE65 device. Active Low.
SPI_SCK	Output	SPI Slave Clock output from the iCE65 device.

After configuration, the SPI port pins are available to the user-application as additional PIO pins, supplied by the SPI_VCC input voltage, essentially providing a fifth "mini" I/O bank.

Table 26: **SPI Interface Ball/Pin Numbers by Package**

SPI Interface	VQ100	CB132	CB196	CB284
SPI_VCC	50	L11	L11	R15
PIOS/SPI_SO	45	M11	M11	T15
PIOS/SPI_SI	46	P11	P11	V15
PIOS/SPI_SS_B	49	P13	P13	V17
PIOS/SPI_SCK	48	P12	P12	V16

SPI PROM Requirements

The iCE65 mobileFPGA SPI Flash configuration interface supports a variety of SPI Flash memory vendors and product families. However, Lattice Semiconductor does not specifically test, qualify, or otherwise endorse any specific SPI Flash vendor or product family. The iCE65 SPI interface supports SPI PROMs that they meet the following requirements.

- The PROM must operate at 3.3V or 2.5V in order to trigger the iCE65 FPGA's power-on reset circuit.
- The PROM must support the `0x0B` Fast Read command, using a 24-bit start address and has 8 dummy bits before the PROM provides first data (see Figure 25: SPI Fast Read Command).
- The PROM must have enough bits to program the iCE65 device (see Table 27: Smallest SPI PROM Size (bits), by Device, by Number of Images).
- The PROM must support data operations at the upper frequency range for the selected iCE65 internal oscillator frequency (see Table 57). The oscillator frequency is selectable when creating the FPGA bitstream image.

***Table 28:* ColdBoot Select Ball/Pin Numbers by Package**

ColdBoot Select	CB81	QN84	VQ100	CB132	CB196	CB284
PIO2/CBSEL0	G5	B15	41	L9	L9	R13
PIO2/CBSEL1	H5	A20	42	P10	P10	V14

When creating the initial configuration image, the Lattice development software loads the start address for up to four configuration images in the bitstream. The value on the CBSEL[1:0] pins tell the configuration controller to read a specific start address, then to load the configuration image stored at the selected address. The multiple bitstreams are stored either in the SPI Flash or in the internal NVCM.

After configuration, the CBSEL[1:0] pins become normal PIO pins available to the application.

The Cold Boot feature allows the iCE65 to be reprogrammed for special application requirements such as the following.

- A normal operating mode and a self-test or diagnostics mode.
- Different applications based on switch settings.
- Different applications based on a card-slot ID number.

Warm Boot Configuration Option

The Warm Boot configuration is similar to the Cold Boot feature, but is completely under the control of the FPGA application.

A special design primitive, SB_WARMBOOT, allows an FPGA application to choose between four configuration images using two internal signal ports, S1 and S0, as shown in Figure 27. These internal signal ports connect to programmable interconnect, which in turn can connect to PLB logic and/or PIO pins.

After selecting the desired configuration image, the application then asserts the internal signal BOOT port High to force the FPGA to restart the configuration process from the specified vector address stored in PROM.

A Warm Boot application can only jump to another configuration image that DOES NOT have Warm Boot enabled. There is no such restriction for Cold Boot applications.

Time-Out and Retry

When configuring from external SPI Flash, the iCE65 device looks for a synchronization word. If the device does not find a synchronization word within its timeout period, the device automatically attempts to restart the configuration process from the very beginning. This feature is designed to address any potential power-sequencing issues that may occur between the iCE65 device and the external PROM.

The iCE65 device attempts to reconfigure six times. If not successful after six attempts, the iCE65 FPGA automatically goes into low-power mode.

SPI Peripheral Configuration Interface

Using the SPI peripheral configuration interface, an application processor (AP) serially writes a configuration image to an iCE65 FPGA using the iCE65's SPI interface, as shown in Figure 23. The iCE65's SPI configuration interface is a separate, independent I/O bank, powered by the VCC_SPI supply input. Typically, VCC_SPI is the same voltage as the application processor's I/O. The configuration control signals, CDONE and CRESET_B, are supplied by the separate I/O Bank 2 voltage input, VCCIO_2.

This same SPI peripheral interface supports programming for the iCE65's Nonvolatile Configuration Memory (NVCM).

iCE65 Pin Descriptions

Table 36 lists the various iCE65 pins, alphabetically by name. The table indicates the directionality of the signal and the associated I/O bank. The table also indicates if the signal has an internal pull-up resistor enabled during configuration. Finally, the table describes the function of the pin.

Table 36: iCE65 Pin Description

Signal Name	Direction	I/O Bank	Pull-up during Config	Description
CDONE	Output	2	Yes	Configuration Done. Dedicated output. Includes a permanent weak pull-up resistor to VCCIO_2.. If driving external devices with CDONE output, connect a 10 kΩ pull-up resistor to VCCIO_2.
CRESET_B	Input	2	No	Configuration Reset, active Low. Dedicated input. No internal pull-up resistor. Either actively drive externally or connect a 10 kΩ pull-up resistor to VCCIO_2.
GBIN0/PIO0 **GBIN1/PIO0**	Input/IO	0	Yes	Global buffer input from I/O Bank 0. Optionally, a full-featured PIO pin.
GBIN2/PIO1 **GBIN3/PIO1**	Input/IO	1	Yes	Global buffer input from I/O Bank 1. Optionally, a full-featured PIO pin.
GBIN4/PIO2 **GBIN5/PIO2**	Input/IO	2	Yes	Global buffer input from I/O Bank 2. Optionally, a full-featured PIO pin.
GBIN6/PIO3	Input/IO	3	No	Global buffer input from I/O Bank 3. Optionally, a full-featured PIO pin.
GBIN7/PIO3	Input/IO	3	No	Global buffer input from I/O Bank 3. Optionally, a full-featured PIO pin. Optionally, a differential clock input using the associated differential input pin.
GND	Supply	All	N/A	Ground. All must be connected.
PIOx_yy	I/O	0,1,2	Yes	Programmable I/O pin defined by the iCE65 configuration bitstream. The 'x' number specifies the I/O bank number in which the I/O pin resides. The "yy' number specifies the I/O number in that bank.
PIO2/CBSEL0	Input/IO	2	Yes	Optional ColdBoot configuration SELect input, if ColdBoot mode is enabled. A full-featured PIO pin after configuration.
PIO2/CBSEL1	Input/IO	2	Yes	Optional ColdBoot configuration SELect input, if ColdBoot mode is enabled. A full-featured PIO pin after configuration.
PIO3_yy/ DPwwz	I/O	3	No	Programmable I/O pin that is also half of a differential I/O pair. Only available in I/O Bank 3. The "yy" number specifies the I/O number in that bank. The "ww" number indicates the differential I/O pair. The 'z' indicates the polarity of the pin in the differential pair. 'A'=negative input. 'B'=positive input.
PIOS/SPI_SO	I/O	SPI	Yes	SPI Serial Output. A full-featured PIO pin after configuration.
PIOS /SPI_SI	I/O	SPI	Yes	SPI Serial Input. A full-featured PIO pin after configuration.
PIOS / SPI_SS_B	I/O	SPI	Yes	SPI Slave Select. Active Low. Includes an internal weak pull-up resistor to SPI_VCC during configuration. During configuration, the logic level sampled on this pin determines the configuration mode used by the iCE65 device, as shown in Figure 20. An input when sampled at the start of configuration. An input when in SPI Peripheral configuration mode (SPI_SS_B = Low). An output when in SPI Flash configuration mode. A full-featured PIO pin after configuration.
PIOS/ SPI_SCK	I/O	SPI	Yes	SPI Slave Clock. An input when in SPI Peripheral configuration mode (SPI_SS_B = Low). An output when in SPI Flash configuration mode. A full-featured PIO pin after configuration.
TDI	Input	1	No	JTAG Test Data Input. If using the JTAG interface, use a 10kΩ pull-up resistor to VCCIO_1. Tie off to GND when unused.

CB81 Chip-Scale Ball-Grid Array

The CB81 package is a full ball grid array with 0.5 mm ball pitch. The iCE65L01 device is available in this package.

Footprint Diagram

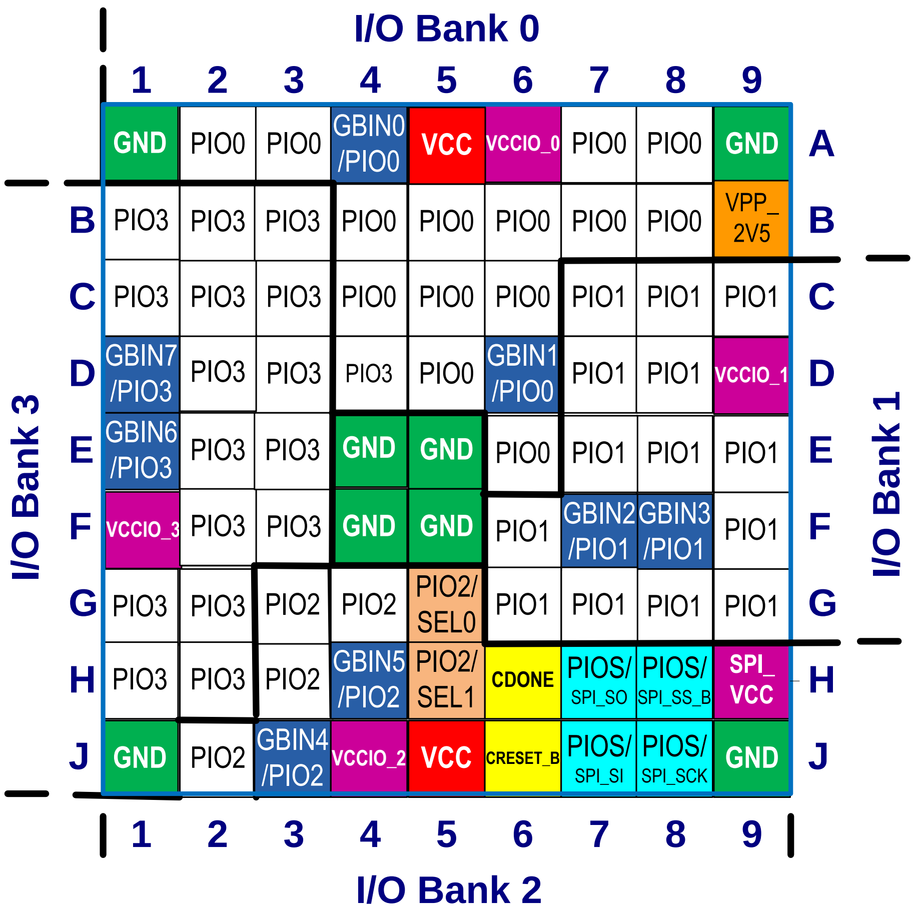
Figure 32 shows the iCE65 footprint diagram for the CB81 package.

Figure 31 shows the conventions used in the diagram.

Also see Table 37 for a complete, detailed pinout for the 81-ball BGA package.

The signal pins are also grouped into the four I/O Banks and the SPI interface.

***Figure 32*: iCE65L01 CB81 Chip-Scale BGA Footprint (Top View)**



Ball Function	Ball Number	Pin Type	Bank
PIO3	B1	PIO	3
PIO3	B2	PIO	3
PIO3	B3	PIO	3
PIO3	C1	PIO	3
PIO3	C2	PIO	3
PIO3	C3	PIO	3
GBIN7/PIO3	D1	GBIN	3
PIO3	D2	PIO	3
PIO3	D3	PIO	3
GBIN6/PIO3	E1	GBIN	3
PIO3	E2	PIO	3
PIO3	E3	PIO	3
PIO3	F2	PIO	3
PIO3	F3	PIO	3
PIO3	G1	PIO	3
PIO3	G2	PIO	3
PIO3	H1	PIO	3
PIO3	H2	PIO	3
VCCIO_3	F1	VCCIO	3
PIOS/SPI_SO	H7	SPI	SPI
PIOS/SPI_SI	J7	SPI	SPI
PIOS/SPI_SCK	J8	SPI	SPI
PIOS/SPI_SS_B	H8	SPI	SPI
SPI_VCC	H9	SPI	SPI
GND	A1	GND	GND
GND	A9	GND	GND
GND	J9	GND	GND
GND	J1	GND	GND
GND	E4	GND	GND
GND	E5	GND	GND
GND	F4	GND	GND
GND	F5	GND	GND
VCC	A5	VCC	VCC
VCC	J5	VCC	VCC
VPP_2V5	B9	VPP	VPP

Pin Function	Pin Number	Type	Bank
PIO2	28	PIO	2
PIO2	29	PIO	2
PIO2	30	PIO	2
PIO2	iCE65L01: 34 iCE65L04: 36	PIO	2
PIO2	37	PIO	2
PIO2	40	PIO	2
PIO2/CBSEL0	41	PIO	2
PIO2/CBSEL1	42	PIO	2
VCCIO_2	31	VCCIO	2
VCCIO_2	38	VCCIO	2
PIO3/DP00A	1	PIO/DPIO	3
PIO3/DP00B	2	PIO/DPIO	3
PIO3/DP01A	3	PIO/DPIO	3
PIO3/DP01B	4	PIO/DPIO	3
PIO3/DP02A	7	PIO/DPIO	3
PIO3/DP02B	8	PIO/DPIO	3
PIO3/DP03A	9	PIO/DPIO	3
PIO3/DP03B	10	PIO/DPIO	3
PIO3/DP04A	12	PIO/DPIO	3
GBIN7/PIO3/DP04B	13	GBIN/DPIO	3
GBIN6/PIO3/DP05A	15	GBIN/DPIO	3
PIO3/DP05B	16	PIO/DPIO	3
PIO3/DP06A	18	PIO/DPIO	3
PIO3/DP06B	19	PIO/DPIO	3
PIO3/DP07A	20	PIO/DPIO	3
PIO3/DP07B	21	PIO/DPIO	3
PIO3/DP08A	24	PIO/DPIO	3
PIO3/DP08B	25	PIO/DPIO	3
VCCIO_3	6	VCCIO	3
VCCIO_3	14	VCCIO	3
VCCIO_3	22	VCCIO	3
PIOS/SPI_SO	45	SPI	SPI
PIOS/SPI_SI	46	SPI	SPI
PIOS/SPI_SCK	48	SPI	SPI
PIOS/SPI_SS_B	49	SPI	SPI
SPI_VCC	50	SPI	SPI
GND	5	GND	GND
GND	17	GND	GND
GND	23	GND	GND
GND	32	GND	GND
GND	39	GND	GND
GND	47	GND	GND
GND	55	GND	GND
GND	70	GND	GND
GND	84	GND	GND
GND	98	GND	GND
VCC	11	VCC	VCC
VCC	35	VCC	VCC

Pinout Table

Table 41 provides a detailed pinout table for the CB132 package. Pins are generally arranged by I/O bank, then by ball function. The table also highlights the differential I/O pairs in I/O Bank 3.

Table 41: iCE65 CB132 Chip-scale BGA Pinout Table

Ball Function	Ball Number	Pin Type	Bank
GBIN0/PIO0	iCE65L01: A7 iCE65L04/L08: A6	GBIN	0
GBIN1/PIO0	iCE65L01: A6 iCE65L04/08: A7	GBIN	0
PIO0	A1	PIO	0
PIO0	A2	PIO	0
iCE65L01: (NC) iCE65L04/L08: PIO0	A3	iCE65L01: (NC) iCE65L04: PIO0	0
PIO0	A4	PIO	0
PIO0	A5	PIO	0
PIO0	A10	PIO	0
iCE65L01: (NC) iCE65L04/L08: PIO0	A11	iCE65L01: (NC) iCE65L04: PIO0	0
PIO0	A12	PIO	0
PIO0	C10	PIO	0
PIO0	C11	PIO	0
PIO0	C12	PIO	0
PIO0	C4	PIO	0
PIO0	C5	PIO	0
PIO0	C6	PIO	0
PIO0	C7	PIO	0
PIO0	C8	PIO	0
PIO0	C9	PIO	0
PIO0	D5	PIO	0
PIO0	D6	PIO	0
PIO0	D7	PIO	0
PIO0	D8	PIO	0
PIO0	D9	PIO	0
PIO0	D10	PIO	0
PIO0	D11	PIO	0
VCCIO_0	A8	VCCIO	0
VCCIO_0	F6	VCCIO	0
GBIN2/PIO1	G14	GBIN	1
GBIN3/PIO1	F14	GBIN	1
PIO1	B14	PIO	1
PIO1	C14	PIO	1
PIO1	D12	PIO	1
PIO1	D14	PIO	1
PIO1	E11	PIO	1
PIO1	E12	PIO	1
PIO1	E14	PIO	1
PIO1	F11	PIO	1
PIO1	F12	PIO	1
PIO1	G11	PIO	1
PIO1	G12	PIO	1
PIO1	H11	PIO	1

Ball Function	Ball Number iCE65L04 iCE65L08	Pin Type by Device iCE65L04	iCE65L08	Bank	CB132 Ball Equivalent
PIO1	L15	PIO	PIO	1	G11
PIO1	L16	PIO	PIO	1	G12
PIO1 (●)	L22	N.C.	PIO	1	—
PIO1	M15	PIO	PIO	1	H11
PIO1	M16	PIO	PIO	1	H12
PIO1	M20	PIO	PIO	1	—
PIO1 (●)	M22	N.C.	PIO	1	—
PIO1	N15	PIO	PIO	1	J11
PIO1	N16	PIO	PIO	1	J12
PIO1	N22	PIO	PIO	1	—
PIO1	P15	PIO	PIO	1	K11
PIO1	P16	PIO	PIO	1	K12
PIO1	P18	PIO	PIO	1	K14
PIO1	P20	PIO	PIO	1	—
PIO1	P22	PIO	PIO	1	—
PIO1	R18	PIO	PIO	1	L14
PIO1	R20	PIO	PIO	1	—
PIO1	R22	PIO	PIO	1	—
PIO1	T20	PIO	PIO	1	—
PIO1	T22	PIO	PIO	1	—
PIO1	U20	PIO	PIO	1	—
PIO1 (●)	U22	N.C.	PIO	1	—
PIO1	V20	PIO	PIO	1	—
PIO1 (●)	V22	N.C.	PIO	1	—
PIO1	W20	PIO	PIO	1	—
PIO1 (●)	W22	N.C.	PIO	1	—
PIO1 (●)	Y22	N.C.	PIO	1	—
TCK	R16	JTAG	JTAG	1	L12
TDI	T16	JTAG	JTAG	1	M12
TDO	U18	JTAG	JTAG	1	N14
TMS	V18	JTAG	JTAG	1	P14
TRST_B	T18	JTAG	JTAG	1	M14
VCCIO_1	H22	VCCIO	VCCIO	1	—
VCCIO_1	J20	VCCIO	VCCIO	1	—
VCCIO_1	K13	VCCIO	VCCIO	1	F9
VCCIO_1	M18	VCCIO	VCCIO	1	H14
CDONE	T14	CONFIG	CONFIG	2	M10
CRESET_B	R14	CONFIG	CONFIG	2	L10
GBIN4/PIO2	V12	GBIN	GBIN	2	P7
GBIN5/PIO2	V11	GBIN	GBIN	2	P8
PIO2	R8	PIO	PIO	2	L4
PIO2	R9	PIO	PIO	2	L5
PIO2	R10	PIO	PIO	2	L6
PIO2	R11	PIO	PIO	2	L7
PIO2	R12	PIO	PIO	2	L8
PIO2	T7	PIO	PIO	2	M3
PIO2	T8	PIO	PIO	2	M4
PIO2	T10	PIO	PIO	2	M6
PIO2	T11	PIO	PIO	2	M7
PIO2	T12	PIO	PIO	2	M8

Ball Function	Ball Number iCE65L04 iCE65L08	Pin Type by Device iCE65L04	iCE65L08	Bank	CB132 Ball Equivalent
PIO3/DP03A	H5	DPIO	DPIO	3	D1
PIO3/DP03B	J5	DPIO	DPIO	3	E1
PIO3/DP04A	K8	DPIO	DPIO	3	F4
PIO3/DP04B	K7	DPIO	DPIO	3	F3
PIO3/DP05A	E3	DPIO	DPIO	3	—
PIO3/DP05B	F3	DPIO	DPIO	3	—
PIO3/DP06A	G3	DPIO	DPIO	3	—
PIO3/DP06B	H3	DPIO	DPIO	3	—
PIO3/DP07A (●)	B1	N.C.	DPIO	3	—
PIO3/DP07B (●)	C1	N.C.	DPIO	3	—
PIO3/DP08A (●)	D1	N.C.	DPIO	3	—
PIO3/DP08B (●)	E1	N.C.	DPIO	3	—
PIO3/DP09A	H1	DPIO	DPIO	3	—
PIO3/DP09B	J1	DPIO	DPIO	3	—
PIO3/DP10A	K1	DPIO	DPIO	3	—
PIO3/DP10B	L1	DPIO	DPIO	3	—
PIO3/DP11A	L3	DPIO	DPIO	3	—
GBIN7/PIO3/DP11B	L5	GBIN	GBIN	3	G1
PIO3/DP12A (●)	T1	N.C.	DPIO	3	—
PIO3/DP12B (●)	U1	N.C.	DPIO	3	—
PIO3/DP13A (●)	W1	N.C.	DPIO	3	—
PIO3/DP13B (●)	Y1	N.C.	DPIO	3	—
PIO3/DP14A (●)	AA1	N.C.	DPIO	3	—
PIO3/DP14B (●)	AB1	N.C.	DPIO	3	—
GBIN6/PIO3/DP15A	M5	GBIN	GBIN	3	H1
PIO3/DP15B	M3	DPIO	DPIO	3	—
PIO3/DP16A	N3	DPIO	DPIO	3	—
PIO3/DP16B	P3	DPIO	DPIO	3	—
PIO3/DP17A	U3	DPIO	DPIO	3	—
PIO3/DP17B	V3	DPIO	DPIO	3	—
PIO3/DP18A	W3	DPIO	DPIO	3	—
PIO3/DP18B	Y3	DPIO	DPIO	3	—
PIO3/DP19A	L7	DPIO	DPIO	3	G3
PIO3/DP19B	L8	DPIO	DPIO	3	G4
PIO3/DP20A	M7	DPIO	DPIO	3	H3
PIO3/DP20B	M8	DPIO	DPIO	3	H4
PIO3/DP21A	N7	DPIO	DPIO	3	J3
PIO3/DP21B	N5	DPIO	DPIO	3	J1
PIO3/DP22A	P7	DPIO	DPIO	3	K3
PIO3/DP22B	P8	DPIO	DPIO	3	K4
PIO3/DP23A	R5	DPIO	DPIO	3	L1
PIO3/DP23B	T5	DPIO	DPIO	3	M1
PIO3/DP24A	U5	DPIO	DPIO	3	N1
PIO3/DP24B	V5	DPIO	DPIO	3	P1
VCCIO_3	F1	VCCIO	VCCIO	3	—
VCCIO_3	P1	VCCIO	VCCIO	3	—

iCE65L04 Pad Name	DiePlus						
	VQ100	CB132	CB196	CB284	Pad	X (µm)	Y (µm)
PIO2_08	—	L6	P3	R10	74	965.00	37.20
VCCIO_2	31	M5	M5	T9	75	1,000.00	139.20
PIO2_09	—	P5	K5	V9	76	1,035.00	37.20
PIO2_10	—	M6	N4	T10	77	1,070.00	139.20
GND	32	P6	H7	V10	78	1,105.00	37.20
PIO2_11	—	—	P4	Y4	79	1,140.00	139.20
PIO2_12	—	—	L6	Y5	80	1,175.00	37.20
PIO2_13	—	—	—	AB6	81	1,210.00	139.20
PIO2_14	—	—	—	AB7	82	1,245.00	37.20
PIO2_15	—	—	—	AB8	83	1,280.00	139.20
PIO2_16	—	—	—	AB9	84	1,315.00	37.20
PIO2_17	—	—	—	AB10	85	1,350.00	139.20
PIO2_18	—	—	—	AB11	86	1,385.00	37.20
GND	—	J8	H8	N12	87	1,420.00	139.20
PIO2_19	—	—	K6	Y6	88	1,455.00	37.20
PIO2_20	—	—	N5	Y7	89	1,490.00	139.20
VCC	—	—	J4	Y8	90	1,525.00	37.20
PIO2_21	—	—	M6	Y9	91	1,560.00	139.20
PIO2_22	—	—	N6	Y10	92	1,595.00	37.20
GBIN5/PIO2_23	33	P7	P5	V11	93	1,630.00	139.20
GBIN4/PIO2_24	34	P8	L7	V12	94	1,665.00	37.20
PIO2_25	—	—	—	AB12	95	1,700.00	139.20
VCCIO_2	—	—	J9	Y11	96	1,735.00	37.20
PIO2_26	—	—	—	AB13	97	1,770.00	139.20
PIO2_27	—	—	K7	AB14	98	1,805.00	37.20
GND	—	—	J5	Y12	99	1,840.00	139.20
PIO2_28	—	—	K9	AB15	100	1,875.00	37.20
PIO2_29	—	—	M7	Y13	101	1,910.00	139.20
PIO2_30	—	—	K8	Y14	102	1,945.00	37.20
PIO2_31	—	—	P7	Y15	103	1,980.00	139.20
PIO2_32	—	—	L8	Y17	104	2,015.00	37.20
PIO2_33	—	—	P8	Y18	105	2,050.00	139.20
PIO2_34	—	—	N8	Y19	106	2,085.00	37.20
PIO2_35	—	—	M8	Y20	107	2,120.00	139.20
VCC	35	J7	J7	N11	108	2,155.00	37.20
VCC	—	—	—	—	109	2,190.00	139.20
PIO2_36	36	P9	P9	V13	110	2,225.00	37.20
PIO2_37	37	M7	N9	T11	111	2,260.00	139.20
VCCIO_2	38	J9	N10	N13	112	2,295.00	37.20
PIO2_38	—	L7	M9	R11	113	2,330.00	139.20
GND	39	H8	J8	M12	114	2,365.00	37.20
PIO2_39	—	M8	N12	T12	115	2,400.00	139.20
PIO2_40	—	L8	N11	R12	116	2,435.00	37.20
PIO2_41	40	M9	N13	T13	117	2,470.00	139.20
PIO2_42/CBSEL0	41	L9	L9	R13	118	2,505.00	37.20
PIO2_43/CBSEL1	42	P10	P10	V14	119	2,540.00	139.20
CDONE	43	M10	M10	T14	120	2,575.00	37.20

iCE65L08

Table 46 lists all the pads on the iCE65L08 die and how these pads connect to the balls or pins in the supported package styles. Most VCC, VCCIO, and GND pads are double-bonded inside the package although the table shows only a single connection.

For additional information on the iCE65L08 DiePlus product, please refer to the following data sheet.

- DiePlusAdvantage FPGA Known Good Die

Table 46: iCE65L08 Die Cross Reference

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO3_00/DP00A	—	B1	1	129.735	3,882.665
PIO3_01/DP00B	—	C1	2	231.735	3,837.665
PIO3_02/DP01A	C1	F5	3	129.735	3,792.665
PIO3_03/DP01B	B1	G5	4	231.735	3,747.665
GND	C2	K5	5	129.735	3,702.665
GND	—	—	6	231.735	3,657.665
VCCIO_3	E3	J7	7	129.735	3,612.665
VCCIO_3	—	—	8	231.735	3,567.665
PIO3_04/DP02A	D3	E3	9	129.735	3,512.665
PIO3_05/DP02B	C3	F3	10	231.735	3,477.665
PIO3_06/DP03A	D1	G3	11	129.735	3,442.665
PIO3_07/DP03B	D2	H3	12	231.735	3,407.665
VCC	F2	D3	13	129.735	3,372.665
VCC	—	—	14	231.735	3,337.665
PIO3_08/DP04A	D4	D1	15	129.735	3,302.665
PIO3_09/DP04B	E4	E1	16	231.735	3,267.665
PIO3_10/DP05A	—	H1	17	129.735	3,232.665
PIO3_11/DP05B	—	J1	18	231.735	3,197.665
GND	F1	M10	19	129.735	3,162.665
GND	—	—	20	231.735	3,127.665
PIO3_12/DP06A	E2	H5	21	129.735	3,092.665
PIO3_13/DP06B	E1	J5	22	231.735	3,057.665
GND	L3	J3	23	129.735	3,022.665
GND	—	—	24	231.735	2,987.665
PIO3_14/DP07A	F5	K1	25	129.735	2,952.665
PIO3_15/DP07B	E5	L1	26	231.735	2,917.665
VCCIO_3	E3	K3	27	129.735	2,882.665
VCCIO_3	—	—	28	231.735	2,847.665
VCC	G6	L10	29	129.735	2,812.665
VCC	—	—	30	231.735	2,777.665
PIO3_16/DP08A	F4	G7	31	129.735	2,742.665
PIO3_17/DP08B	F3	H7	32	231.735	2,707.665
VCCIO_3	K1	F1	33	129.735	2,672.665
VCCIO_3	—	—	34	231.735	2,637.665
GND	—	G1	35	129.735	2,602.665
GND	—	—	36	231.735	2,567.665
PIO3_18/DP09A	G3	K8	37	129.735	2,532.665
PIO3_19/DP09B	G4	K7	38	231.735	2,497.665

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO3_20/DP10A	—	H8	39	129.735	2,462.665
PIO3_21/DP10B	—	J8	40	231.735	2,427.665
PIO3_22/DP11A	G1	T1	41	129.735	2,392.665
PIO3_23/DP11B	G2	U1	42	231.735	2,357.665
VCCIO_3	K1	N10	43	129.735	2,322.665
VCCIO_3	—	—	44	231.735	2,287.665
VREF	N/A	M1	45	129.735	2,252.665
VREF	N/A	—	46	231.735	2,217.665
GND	J5	N1	47	129.735	2,182.665
GND	—	—	48	231.735	2,147.665
VCCIO_3	J6	P1	49	129.735	2,112.665
VCCIO_3	—	—	50	231.735	2,077.665
GND	H6	R1	51	129.735	2,042.665
GND	—	—	52	231.735	2,007.665
PIO3_24/DP12A	H4	L3	53	129.735	1,972.665
GBIN7/PIO3_25/DP12B	H3	L5	54	231.735	1,937.665
GND	H7	V1	55	129.735	1,902.665
GBIN6/PIO3_26/DP13A	H1	M5	56	231.735	1,867.665
PIO3_27/DP13B	H2	M3	57	129.735	1,832.665
PIO3_28/DP14A	—	N7	58	231.735	1,798.665
PIO3_29/DP14B	—	N5	59	129.735	1,762.665
PIO3_30/DP15A	J1	N3	60	231.735	1,727.665
PIO3_31/DP15B	J2	P3	61	129.735	1,692.665
GND	J5	M11	62	231.735	1,657.665
GND	—	—	63	129.735	1,622.665
PIO3_32/DP16A	H5	W1	64	231.735	1,587.665
PIO3_33/DP16B	G5	Y1	65	129.735	1,552.665
VCCIO_3	J6	R3	66	231.735	1,517.665
VCCIO_3	—	—	67	129.735	1,482.665
GND	J5	T3	68	231.735	1,447.665
GND	—	—	69	129.735	1,412.665
PIO3_34/DP17A	K2	AA1	70	231.735	1,377.665
PIO3_35/DP17B	J3	AB1	71	129.735	1,342.665
PIO3_36/DP18A	—	L7	72	231.735	1,307.665
PIO3_37/DP18B	—	L8	73	129.735	1,272.665
PIO3_38/DP19A	—	M7	74	231.735	1,237.665
PIO3_39/DP19B	—	M8	75	129.735	1,202.665
PIO3_40/DP20A	L1	P7	76	231.735	1,167.665
PIO3_41/DP20B	L2	P8	77	129.735	1,132.665
VCC	J4	N8	78	231.735	1,097.665
VCC	—	—	79	129.735	1,062.665
PIO3_42/DP21A	K4	R5	80	231.735	1,027.665
PIO3_43/DP21B	K3	T5	81	129.735	992.665
VCCIO_3	K1	P5	82	231.735	957.665
VCCIO_3	—	—	83	129.735	912.665
GND	L3	R7	84	231.735	867.665
GND	—	—	85	129.735	822.67

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO2_28	—	Y13	132	2,062.5	139.5
GBIN5/PIO2_29	M7	V11	133	2,097.5	37.5
GBIN4/PIO2_30	N8	V12	134	2,132.5	139.5
GND	J8	Y12	135	2,167.5	37.5
GND	—	—	136	2,202.5	139.5
PIO2_31	P8	Y14	137	2,237.5	37.5
PIO2_32	—	AB15	138	2,272.5	139.5
PIO2_33	M8	V13	139	2,307.5	37.5
PIO2_34	—	AB16	140	2,342.5	139.5
PIO2_35	L8	Y15	141	2,377.5	37.5
PIO2_36	—	AB17	142	2,412.5	139.5
PIO2_37	N9	AB18	143	2,447.5	37.5
PIO2_38	—	AB19	144	2,482.5	139.5
PIO2_39	—	AB20	145	2,517.5	37.5
PIO2_40	—	AB21	146	2,552.5	139.5
PIO2_41	—	Y17	147	2,587.5	37.5
PIO2_42	—	AB22	148	2,622.5	139.5
PIO2_43	—	Y18	149	2,657.5	37.5
PIO2_44	P9	Y19	150	2,692.5	139.5
VCC	N7	N11	151	2,727.5	37.5
VCC	—	—	152	2,762.5	139.5
PIO2_45	M9	Y20	153	2,797.5	37.5
PIO2_46	K8	T11	154	2,832.5	139.5
VCCIO_2	J9	N13	155	2,867.5	37.5
VCCIO_2	—	—	156	2,902.5	139.5
PIO2_47	N11	R11	157	2,937.5	37.5
GND	J8	M12	158	2,972.5	139.5
GND	—	—	159	3,007.5	37.5
PIO2_48	N12	T12	160	3,042.5	139.5
PIO2_49	K9	R12	161	3,077.5	37.5
PIO2_50	N13	T13	162	3,112.5	139.5
PIO2_51/CBSEL0	L9	R13	163	3,147.5	37.5
PIO2_52/CBSEL1	P10	V14	164	3,182.5	139.5
CDONE	M10	T14	165	3,217.5	37.5
CRESET_B	L10	R14	166	3,260.0	139.5
PIOS_00/SPI_SO	M11	T15	167	3,320.0	37.5
PIOS_01/SPI_SI	P11	V15	168	3,370.0	139.5
GND	J8	Y16	169	3,420.0	37.5
GND	—	—	170	3,470.0	139.5
PIOS_02/SPI_SCK	P12	V16	171	3,520.0	37.5
PIOS_03/SPI_SS_B	P13	V17	172	3,570.0	139.5
VCC	—	—	173	3,620.0	37.5
VCC	—	—	174	3,670.0	139.5
SPI_VCC	L11	R15	175	3,720.0	37.5
SPI_VCC	—	—	176	3,770.0	139.5

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO0_42	C5	A5	316	1,559.48	4,054.5
PIO0_43	B5	G9	317	1,524.48	4,156.5
PIO0_44	A4	A3	318	1,489.48	4,054.5
PIO0_45	—	A4	319	1,454.48	4,156.5
PIO0_46	—	A2	320	1,419.48	4,054.5
PIO0_47	—	C7	321	1,384.48	4,156.5
PIO0_48	—	C6	322	1,331.98	4,054.5
VCCIO_0	A8	K10	323	1,281.98	4,156.5
VCCIO_0	—	—	324	1,231.98	4,054.5
PIO0_49	—	E8	325	1,181.98	4,156.5
PIO0_50	B4	A1	326	1,131.98	4,054.5
PIO0_51	C4	E7	327	1,081.98	4,156.5
PIO0_52	A3	C5	328	1,031.98	4,054.5
PIO0_53	B3	E6	329	981.98	4,156.5
PIO0_54	D5	C3	330	931.98	4,054.5
GND	A9	L11	331	881.98	4,156.5
GND	—	—	332	831.98	4,054.5
PIO0_55	B2	G8	333	781.98	4,156.5
PIO0_56	A2	C4	334	731.98	4,054.5
PIO0_57	A1	H10	335	681.98	4,156.5
PIO0_58	—	E5	336	631.98	4,054.5
PIO0_59	—	H9	337	581.98	4,156.5

Programmable Input/Output (PIO) Block

Table 55 provides timing information for the logic in a Programmable Logic Block (PLB), which includes the paths shown in Figure 57 and Figure 58. The timing shown is for the LVCMOS25 I/O standard in all I/O banks. The iCEcube development software reports timing adjustments for other I/O standards.

Figure 57: Programmable I/O (PIO) Pad-to-Pad Timing Circuit

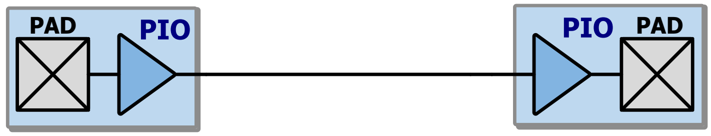


Figure 58: Programmable I/O (PIO) Sequential Timing Circuit

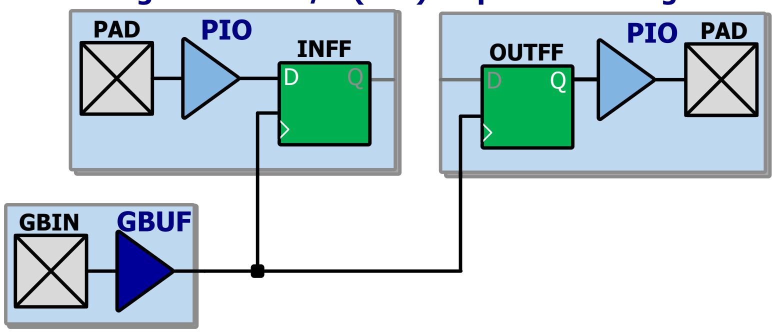


Table 55: Typical Programmable Input/Output (PIO) Timing (LVCMOS25)

			Device: iCE65	L01	L04, L08			
			Power/Speed Grad	–T	–L		–T	
			Nominal VCC	1.2 V	1.0 V	1.2 V	1.2 V	
Symbol	From	To	Description	Typ.	Typ.	Typ.	Typ.	Units
		Synchronous Output Paths						
t_{OCKO}	OUTFF clock input	PIO output	Delay from clock input on OUTFF output flip-flop to PIO output pad.	4.7	13.8	7.3	5.6	ns
t_{GBCKIO}	GBIN input	OUTFF clock input	Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to clock input on the PIO OUTFF output flip-flop.	2.1	7.3	3.8	2.6	ns
		Synchronous Input Paths						
t_{SUPDIN}	PIO input	GBIN input	Setup time on PIO input pin to INFF input flip-flop before active clock edge on GBIN input, including interconnect delay.	0	0	0	0	ns
t_{HDPDIN}	GBIN input	PIO input	Hold time on PIO input to INFF input flip-flop after active clock edge on the GBIN input, including interconnect delay.	2.7	7.1	3.6	2.8	ns
		Pad to Pad						
t_{PADIN}	PIO input	Inter-connect	Asynchronous delay from PIO input pad to adjacent interconnect.	2.5	9.5	5.0	3.2	ns
t_{PADO}	Inter-connect	PIO output	Asynchronous delay from adjacent interconnect to PIO output pad including interconnect delay.	4.5	14.6	7.7	6.2	ns