Lattice Semiconductor Corporation - ICE65L04F-LCB196C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	440
Number of Logic Elements/Cells	3520
Total RAM Bits	81920
Number of I/O	150
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	196-VFBGA, CSPBGA
Supplier Device Package	196-CSPBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice65l04f-lcb196c

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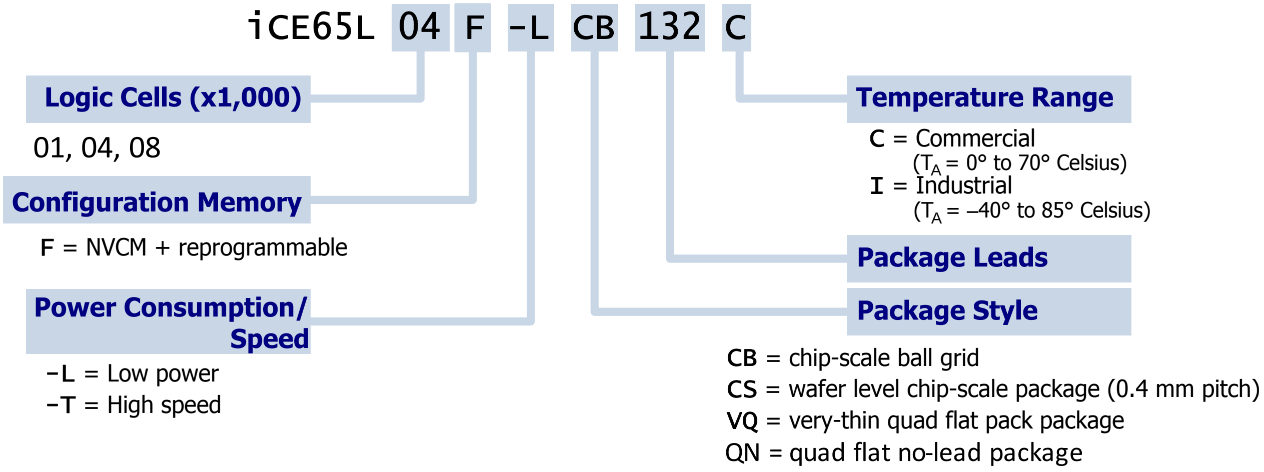
Ordering Information

Figure 2 describes the iCE65 ordering codes for all packaged, non-NVCM Programed components. See the separate DiePlus data sheets when ordering die-based products.

Figure 2: **iCE65 Ordering Codes Standard Device**

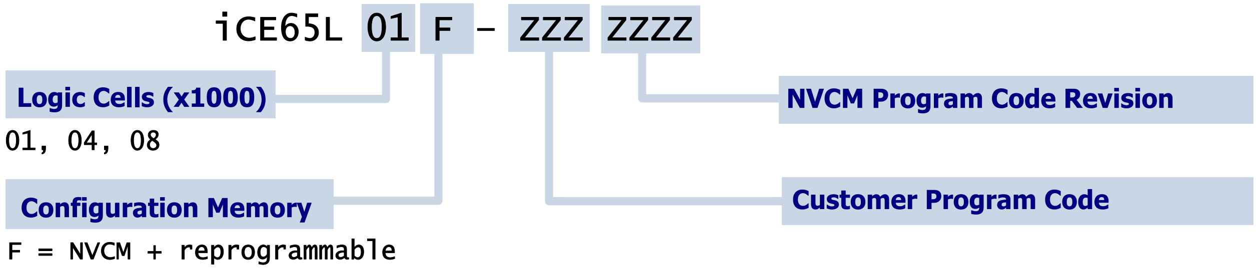


iCE65 devices offer two power consumption, speed options. Standard products (“`-L`” ordering code) have low standby and dynamic power consumption. The “`-T`” provides higher-speed logic.

Similarly, iCE65 devices are available in two operating temperature ranges, one for typical commercial applications, the other with an extended temperature range for industrial and telecommunications applications. The ordering code also specifies the device package option, as described further in Table 2.

Figure 3 describes the iCE65 ordering codes for all packaged, NVCM Programmed components.

Figure 3: **iCE65 Ordering Codes NVCM Programmed Device**



Look-Up Table (LUT4)

The four-input Look-Up Table (LUT4) function implements any and all combinational logic functions, regardless of complexity, of between zero and four inputs. Zero-input functions include "High" (1) and "Low" (0). The LUT4 function has four inputs, labeled I0, I1, I2, and I3. Three of the four inputs are shared with the Carry Logic function, as shown in Figure 4. The bottom-most LUT4 input connects either to the I3 input or to the Carry Logic output from the previous Logic Cell.

The output from the LUT4 function connects to the flip-flop within the same Logic Cell. The LUT4 output or the flip-flop output then connects to the programmable interconnect.

For detailed LUT4 internal timing, see Table 54.

'D'-style Flip-Flop (DFF)

The 'D'-style flip-flop (DFF) optionally stores state information for the application.

The flip-flop has a data input, 'D', and a data output, 'Q'. Additionally, each flip-flop has up to three control signals that are shared among all flip-flops in all Logic Cells within the PLB, as shown in Figure 4. Table 3 describes the behavior of the flip-flop based on inputs and upon the specific DFF design primitive used or synthesized.

Table 3: 'D'-Style Flip-Flop Behavior

DFF Primitive	Operation	Flip-Flop Mode	Inputs				Output
			D	**EN**	**SR**	**CLK**	**Q**
All	Cleared Immediately after Configuration	X	X	X	X	X	0
	Hold Present Value (Disabled)		X	0	X	X	Q
	Hold Present Value (Static Clock)		X	X	X	1 or 0	Q
	Load with Input Data		D	1*	0*	↑	D
SB_DFFR	Asynchronous Reset	Asynchronous Reset	X	X	1	X	0
SB_DFFS	Asynchronous Set	Asynchronous Set	X	X	1	X	1
SB_DFFSR	Synchronous Reset	Synchronous Reset	X	1*	1	↑	0
SB_DFFSS	Synchronous Set	Synchronous Set	X	1*	1	↑	1

X = don't care, ↑ = rising clock edge (default polarity), 1* = High or unused, 0* = Low or unused

The CLK clock signal is not optional and is shared among all flip-flops in a Programmable Logic Block. By default, flip-flops are clocked by the rising edge of the PLB clock input, although the clock polarity can be inverted for all the flip-flops in the PLB.

The CLK input optionally connects to one of the following clock sources.

- The output from any one of the eight Global Buffers, or
- A connection from the general-purpose interconnect fabric

The EN clock-enable signal is common to all Logic Cells in a Programmable Logic Block. If the enable signal is not used, then the flip-flop is always enabled. This condition is indicated as "1*" in Table 3. The asterisk indicates that this is the default state if the control signal is not connected in the application.

Similarly, the SR set/reset signal is common to all Logic Cells in a Programmable Logic Block. If not used, then the flip-flop is never set/reset, except when cleared immediately after configuration or by the Global Reset signal. This condition is indicated as "0*" in Table 3. The asterisk indicates that this is the default state if the control signal is not connected in the application.

Table 12 and Table 13 list the connections between a specific global buffer and the inputs on a Programmable I/O (PIO) pair. Although there is no direct connection between a global buffer and a PIO output, such a connection is possible by first connecting through a PLB LUT4 function. Again, all global buffers optionally drive all clock inputs. However, even-numbered global buffers optionally drive the clock-enable input on a PIO pair.

⚠ The PIO clock enable connect is different between the iCE65L01/iCE65L04 and iCE65L08.

Table 12: iCE65L01 & iCE65L04: Global Buffer (GBUF) Connections to Programmable I/O (PIO) Pair

Global Buffer	Output Connections	Input Clock	Output Clock	Clock Enable
GBUF0	No (connect through PLB LUT)	Yes	Yes	No
GBUF1		Yes	Yes	Yes
GBUF2		Yes	Yes	No
GBUF3		Yes	Yes	Yes
GBUF4		Yes	Yes	No
GBUF5		Yes	Yes	Yes
GBUF6		Yes	Yes	No
GBUF7		Yes	Yes	Yes

Table 13: iCE64L08: Global Buffer (GBUF) Connections to Programmable I/O (PIO) Pair

Global Buffer	Output Connections	Input Clock	Output Clock	Clock Enable
GBUF0	No (connect through PLB LUT)	Yes	Yes	Yes
GBUF1		Yes	Yes	No
GBUF2		Yes	Yes	Yes
GBUF3		Yes	Yes	No
GBUF4		Yes	Yes	Yes
GBUF5		Yes	Yes	No
GBUF6		Yes	Yes	Yes
GBUF7		Yes	Yes	No

Global Buffer Inputs

The iCE65 component has eight specialized GBIN/PIO pins that are optionally direct inputs to the global buffers, offering the best overall clock characteristics. As shown in Figure 15, each GBIN/PIO pin is a full-featured I/O pin but also provides a direct connection to its associated global buffer. The direct connection to the global buffer bypasses the iCEgate input-blocking latch and other PIO input logic. These special PIO pins are allocated two to an I/O Bank, a total of eight. These pins are labeled GBIN0 through GBIN7, as shown in Figure 14 and the pin locations for each GBIN input appear in Table 14.

Table 14: Global Buffer Input Ball/Pin Number by Package

Global Buffer Input (GBIN)	I/O Bank	**VQ100**	**CB132**	**‘L04 CB196**	**‘L08 CB196**	**CB284**
GBIN0	0	90	A6	A7	A7	E10
GBIN1		89	A7	E7	E7	E11
GBIN2	1	63	G14	F10	F10	L18
GBIN3		62	F14	G12	G12	K18
GBIN4	2	34	P8	L7	N8	V12
GBIN5		33	P7	P5	M7	V11
GBIN6	3	15	H1	H1	H1	M5
GBIN7		13	G1	G1	H3	L5

Figure 19: RAM4K Read Logic

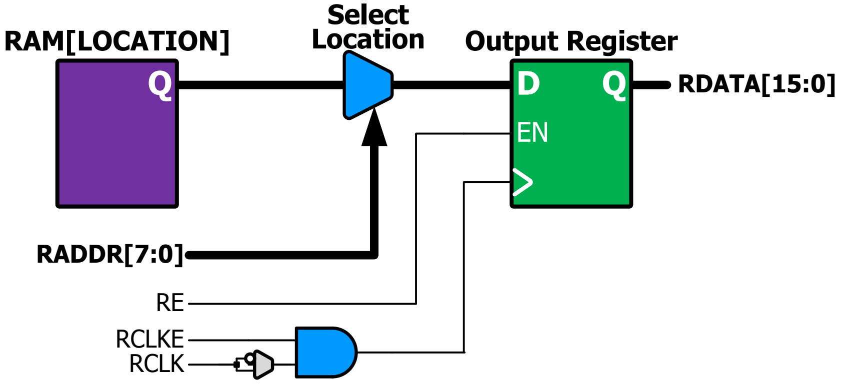


Table 19: RAM4K Read Operations

Operation	RADDR[7:0]	RE	RCLKE	RCLK	RDATA[15:0]
	Address	Read Enable	Clock Enabe	Clock	
After configuration, before first valid Read Data operation	X	X	X	X	Undefined
Disabled	X	X	X	0	No Change
Disabled		X	0	X	No Change
Disabled	X	0	X	X	No change
Read Data	RADDR	1	1	↑	RAM[RADDR]

To read data from the RAM4K block, perform the following operations.

- Supply a valid address on the RADDR[7:0] address input port
- Enable the RAM4K read port (RE = 1)
- Enable the RAM4K read clock (RCLKE = 1)
- Apply a rising clock edge on RCLK
- After the clock edge, the RAM contents located at the specified address (RADDR) appear on the RDATA output port

Read Data Register Undefined Immediately after Configuration

Unlike the flip-flops in the Programmable Logic Blocks and Programmable I/O pins, the RDATA[15:0] read data output register is not automatically reset after configuration. Consequently, immediately following configuration and before the first valid Read Data operation, the initial RDATA[15:0] read value is undefined.

Pre-loading RAM Data

The data contents for a RAM4K block can be optionally pre-loaded during iCE65 configuration. If not pre-loaded during configuration, then the RAM contents must be initialized by the iCE65 application before the RAM contents are valid.

Pre-loading the RAM data in the configuration bitstream increases the size of the configuration image accordingly.

RAM Contents Preserved during Configuration

RAM contents are preserved (write protected) during configuration, assuming that voltage supplies are maintained throughout. Consequently, data can be passed between multiple iCE65 configurations by leaving it in a RAM4K block and then skipping pre-loading during the subsequent reconfiguration. See "Cold Boot Configuration Option" and "Warm Boot Configuration Option" for more information.

Low-Power Setting

To place a RAM4K block in its lowest power mode, keep WCLKE = 0 and RCLKE = 0. In other words, when not actively using a RAM4K block, disable the clock inputs.

Device Configuration

As described in Table 20, iCE65 components are configured for a specific application by loading a binary configuration bitstream image, generated by the Lattice development system. For high-volume applications, the bitstream image is usually permanently programmed in the on-chip NVCM, However, the bitstream image can also be stored external in a standard, low-cost commodity SPI serial Flash PROM. The iCE65 component can automatically load the image using the SPI Master Configuration Interface. Similarly, the iCE65 configuration data can be downloaded from an external processor, microcontroller, or DSP processor using an SPI-like serial interface or an IEEE 1149 JTAG interface.

***Table 20:* iCE65 Device Configuration Modes**

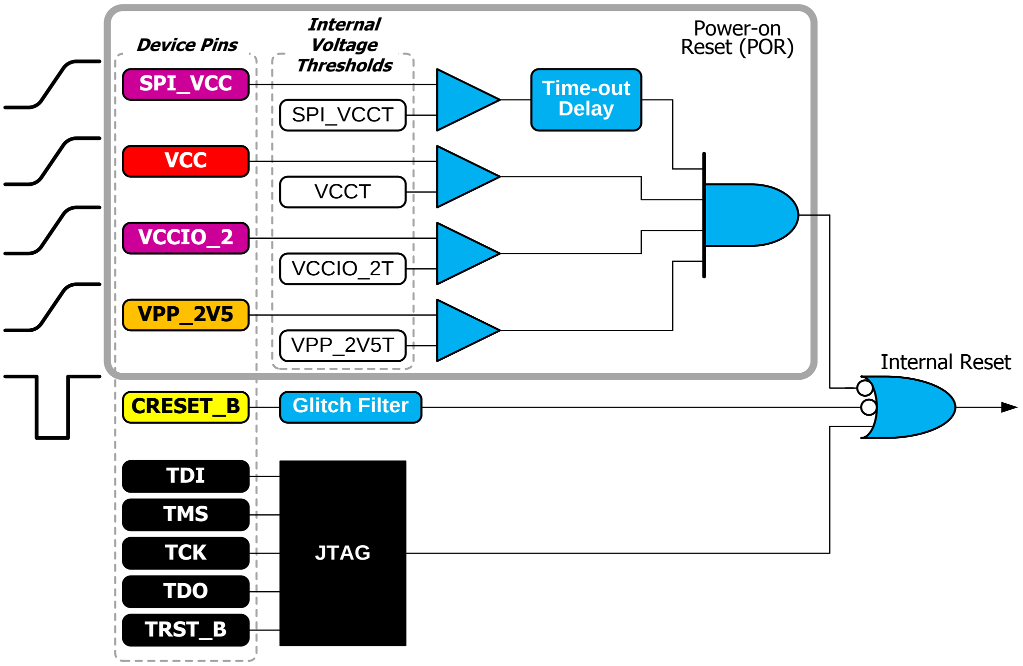
Mode	Analogy	Configuration Data Source
NVCM	ASIC	Internal, lowest-cost, secure, one-time programmable Nonvolatile Configuration Memory (NVCM)
SPI Flash	Microprocessor	External, low-cost, commodity, SPI serial Flash PROM
SPI Peripheral	Processor Peripheral	Configured by external device, such as a processor, microcontroller, or DSP using practically any data source, such as system Flash, a disk image, or over a network connection.
JTAG	JTAG	JTAG configuration requires sending a special command sequence on the SPI interface to enable JTAG configuration. Configuration is controlled by and external device.

Configuration Mode Selection

The iCE65 configuration mode is selected according to the following priority described below and illustrated in Figure 20.

- After exiting the Power-On Reset (POR) state or when CRESET_B returns High after being held Low for 250 ns or more, the iCE65 FPGA samples the logical value on its SPI_SS_B pin. Like other programmable I/O pins, the SPI_SS_B pin has an internal pull-up resistor (see Input Pull-Up Resistors on I/O Banks 0, 1, and 2).
- If the SPI_SS_B pin is sampled as a logic '1' (High), then …
  - Check if the iCE65 is enabled to configure from the Nonvolatile Configuration Memory (NVCM). If the iCE65 device has NVCM memory ('**F**' ordering code) but the NVCM is yet unprogrammed, then the iCE65 device is not enabled to configure from NVCM. Conversely, if the NVCM is programmed, the iCE65 device will configure from NVCM.
    - If enabled to configure from NVCM, the iCE65 device configures itself using NVCM.
    - If not enabled to configure from NVCM, then the iCE65 FPGA configures using the SPI Master Configuration Interface.
- If the SPI_SS_B pin is sampled as a logic '0' (Low), then the iCE65 device waits to be configured from an external controller or from another iCE65 device in SPI Master Configuration Mode using an SPI-like interface.

Figure 22: iCE65 Internal Reset Circuitry



Power-On Reset (POR)

The Power-on Reset (POR) circuit monitors specific voltage supply inputs and holds the device in reset until all the relevant supplies exceed the internal voltage thresholds. The SPI_VCC supply also has an additional time-out delay to allow an attached SPI serial PROM to power up properly. Table 24 shows the POR supply inputs. The Nonvolatile Configuration Memory (NVCM) requires that the VPP_2V5 supply be connected, even if the application does not use the NVCM.

Table 24: Power-on Reset (POR) Voltage Resources

Supply Rail	iCE65 Production Devices
VCC	Yes
SPI_VCC	Yes
VCCIO_1	No
VCCIO_2	Yes
VPP_2V5	Yes

CRESET_B Pin

The CRESET_B pin resets the iCE65 internal logic when Low.

JTAG Interface

Specific command sequences also reset the iCE65 internal logic.

SPI Master Configuration Interface

All iCE65 devices, including those with NVCM, can be configured from an external, commodity SPI serial Flash PROM, as shown in Figure 23. The SPI configuration interface is essentially its own independent I/O bank, powered by the VCC_SPI supply input. Presently, most commercially-available SPI serial Flash PROMs require a 3.3V supply.

Pinout Table

Table 37 provides a detailed pinout table for the CB81 package. Pins are generally arranged by I/O bank, then by ball function.

***Table 37:* iCE65 CB81 Chip-scale BGA Pinout Table**

Ball Function	Ball Number	Pin Type	Bank
PIO0	A2	PIO	0
PIO0	A3	PIO	0
GBIN0/PIO0	A4	GBIN	0
PIO0	A7	PIO	0
PIO0	A8	PIO	0
PIO0	B4	PIO	0
PIO0	B5	PIO	0
PIO0	B6	PIO	0
PIO0	B7	PIO	0
PIO0	B8	PIO	0
PIO0	C4	PIO	0
PIO0	C5	PIO	0
PIO0	C6	PIO	0
PIO0	D4	PIO	0
PIO0	D5	PIO	0
GBIN1/PIO0	D6	GBIN	0
PIO0	E6	PIO	0
VCCIO_0	A6	VCCIO	0
PIO1	C7	PIO	1
PIO1	C8	PIO	1
PIO1	C9	PIO	1
PIO1	D7	PIO	1
PIO1	D8	PIO	1
PIO1	E7	PIO	1
PIO1	E8	PIO	1
PIO1	E9	PIO	1
PIO1	F6	PIO	1
GBIN2/PIO1	F7	GBIN	1
GBIN3/PIO1	F8	GBIN	1
PIO1	F9	PIO	1
PIO1	G6	PIO	1
PIO1	G7	PIO	1
PIO1	G8	PIO	1
PIO1	G9	PIO	1
VCCIO_1	D9	VCCIO	1
CDONE	H6	CONFIG	2
CRESET_B	J6	CONFIG	2
PIO2	G3	PIO	2
PIO2	G4	PIO	2
PIO2/CBSEL0	G5	PIO	2
PIO2	H3	PIO	2
GBIN5/PIO2	H4	PIO	2
PIO2/CBSEL1	H5	PIO	2
PIO2	J2	PIO	2
GBIN4/PIO2	J3	PIO	2
VCCIO_2	J4	PIO	2

QN84 Quad Flat Pack No-Lead

The QN84 is a Quad Flat Pack No-Lead package with a 0.5 mm pad pitch.

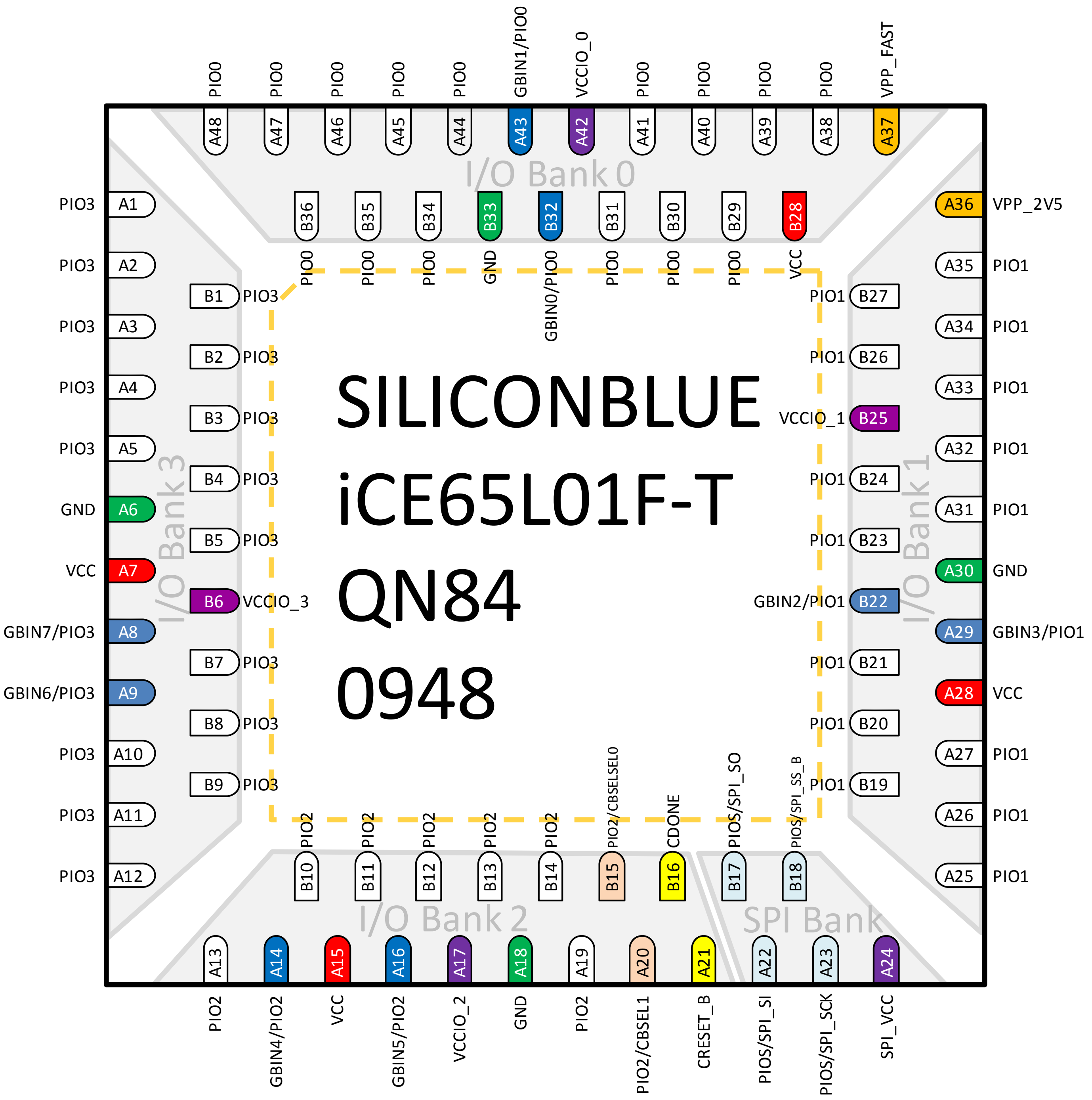
Footprint Diagram

Figure 34 shows the iCE65 footprint diagram for the QN84 package.

Also see Table 38 for a complete, detailed pinout for the QN84 package.

The signal pins are also grouped into the four I/O Banks and the SPI interface.

Figure 34: **iCE65 QN84 Quad Flat Pack No-Lead Footprint (Top View)**



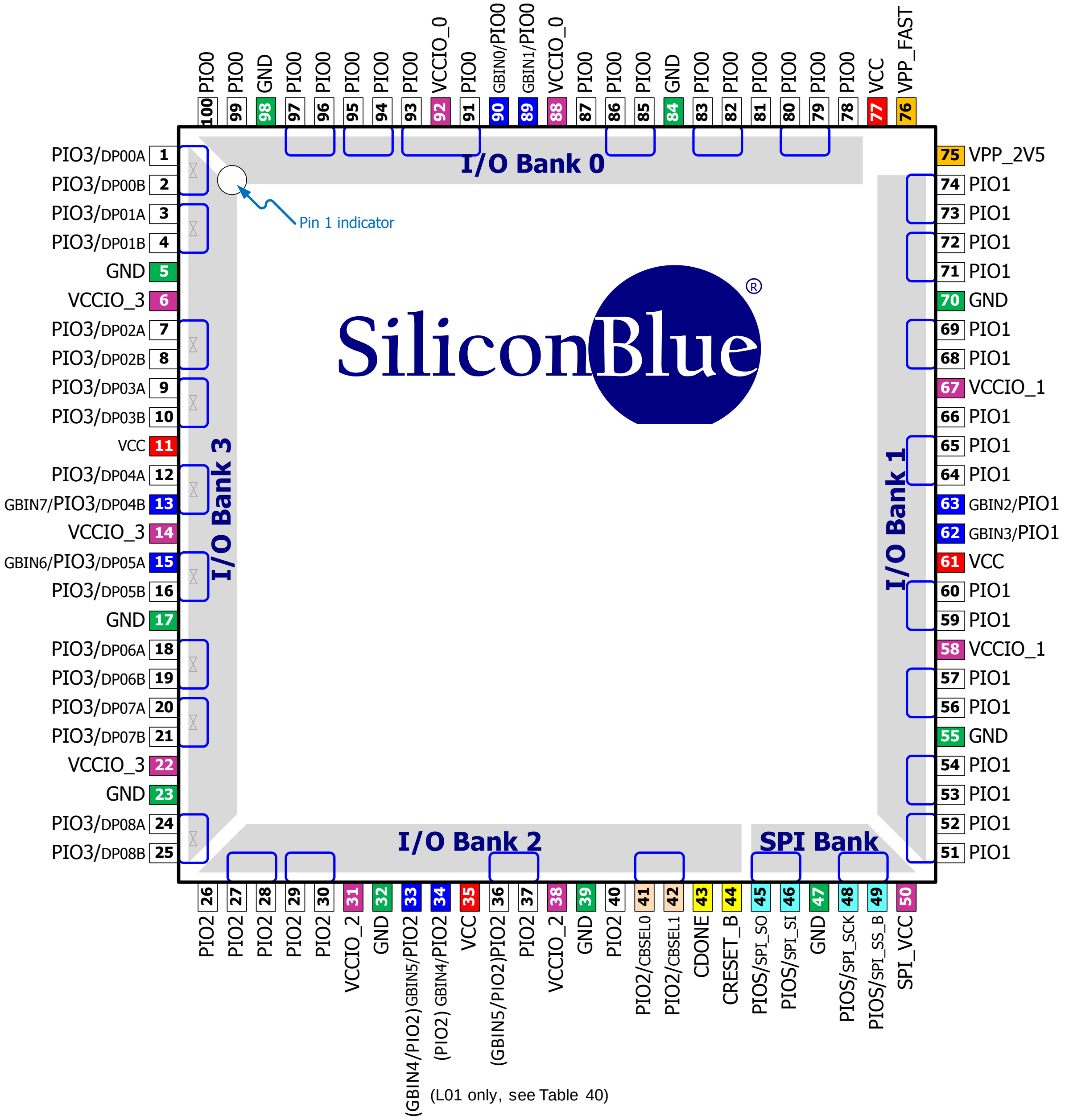
VQ100 Very-thin Quad Flat Package

The VQ100 package is a very-thin quad-flat package with 0.5 mm lead pitch. The iCE65L01 and iCE65L04 devices are available in this package.

Footprint Diagram

Figure 36 shows the footprint diagram for the 100-lead very-thin quad-flat package (VQ100). See Table 40 for a complete, detailed pinout for the 100-lead very-thin quad-flat package. The signal pins are also grouped into the four I/O Banks and the SPI interface.

Figure 36: iCE65 VQ100 Footprint (Top View)



Pinout Table

Table 39 provides a detailed pinout table for the VQ100 package. Pins are generally arranged by I/O bank, then by pin function. The table also highlights the differential I/O pairs in I/O Bank 3. The VQ100 package has no JTAG pins.

Table 39: iCE65 VQ100 Pinout Table

Pin Function	Pin Number	Type	Bank
GBIN0/PIO0	90	GBIN	0
GBIN1/PIO0	89	GBIN	0
PIO0	78	PIO	0
PIO0	79	PIO	0
PIO0	80	PIO	0
PIO0	81	PIO	0
PIO0	82	PIO	0
PIO0	83	PIO	0
PIO0	85	PIO	0
PIO0	86	PIO	0
PIO0	87	PIO	0
PIO0	91	PIO	0
PIO0	93	PIO	0
PIO0	94	PIO	0
PIO0	95	PIO	0
PIO0	96	PIO	0
PIO0	97	PIO	0
PIO0	99	PIO	0
PIO0	100	PIO	0
VCCIO_0	88	VCCIO	0
VCCIO_0	92	VCCIO	0
GBIN2/PIO1	63	GBIN	1
GBIN3/PIO1	62	GBIN	1
PIO1	51	PIO	1
PIO1	52	PIO	1
PIO1	53	PIO	1
PIO1	54	PIO	1
PIO1	56	PIO	1
PIO1	57	PIO	1
PIO1	59	PIO	1
PIO1	60	PIO	1
PIO1	64	PIO	1
PIO1	65	PIO	1
PIO1	66	PIO	1
PIO1	68	PIO	1
PIO1	69	PIO	1
PIO1	71	PIO	1
PIO1	72	PIO	1
PIO1	73	PIO	1
PIO1	74	PIO	1
VCCIO_1	58	VCCIO	1
VCCIO_1	67	VCCIO	1
CDONE	43	CONFIG	2
CRESET_B	44	CONFIG	2
GBIN4/PIO2	iCE65L01: 33 iCE65L04: 34	GBIN	2
GBIN5/PIO2	iCE65L01: 36 iCE65L04: 33	GBIN	2
PIO2	26	PIO	2
PIO2	27	PIO	2

Pin Function	Pin Number	Type	Bank
PIO2	28	PIO	2
PIO2	29	PIO	2
PIO2	30	PIO	2
PIO2	iCE65L01: 34 iCE65L04: 36	PIO	2
PIO2	37	PIO	2
PIO2	40	PIO	2
PIO2/CBSEL0	41	PIO	2
PIO2/CBSEL1	42	PIO	2
VCCIO_2	31	VCCIO	2
VCCIO_2	38	VCCIO	2
PIO3/DP00A	1	PIO/DPIO	3
PIO3/DP00B	2	PIO/DPIO	3
PIO3/DP01A	3	PIO/DPIO	3
PIO3/DP01B	4	PIO/DPIO	3
PIO3/DP02A	7	PIO/DPIO	3
PIO3/DP02B	8	PIO/DPIO	3
PIO3/DP03A	9	PIO/DPIO	3
PIO3/DP03B	10	PIO/DPIO	3
PIO3/DP04A	12	PIO/DPIO	3
GBIN7/PIO3/DP04B	13	GBIN/DPIO	3
GBIN6/PIO3/DP05A	15	GBIN/DPIO	3
PIO3/DP05B	16	PIO/DPIO	3
PIO3/DP06A	18	PIO/DPIO	3
PIO3/DP06B	19	PIO/DPIO	3
PIO3/DP07A	20	PIO/DPIO	3
PIO3/DP07B	21	PIO/DPIO	3
PIO3/DP08A	24	PIO/DPIO	3
PIO3/DP08B	25	PIO/DPIO	3
VCCIO_3	6	VCCIO	3
VCCIO_3	14	VCCIO	3
VCCIO_3	22	VCCIO	3
PIOS/SPI_SO	45	SPI	SPI
PIOS/SPI_SI	46	SPI	SPI
PIOS/SPI_SCK	48	SPI	SPI
PIOS/SPI_SS_B	49	SPI	SPI
SPI_VCC	50	SPI	SPI
GND	5	GND	GND
GND	17	GND	GND
GND	23	GND	GND
GND	32	GND	GND
GND	39	GND	GND
GND	47	GND	GND
GND	55	GND	GND
GND	70	GND	GND
GND	84	GND	GND
GND	98	GND	GND
VCC	11	VCC	VCC
VCC	35	VCC	VCC

CB196 Chip-Scale Ball-Grid Array

The CB196 package is a chip-scale, fully-populated, ball-grid array with 0.5 mm ball pitch.

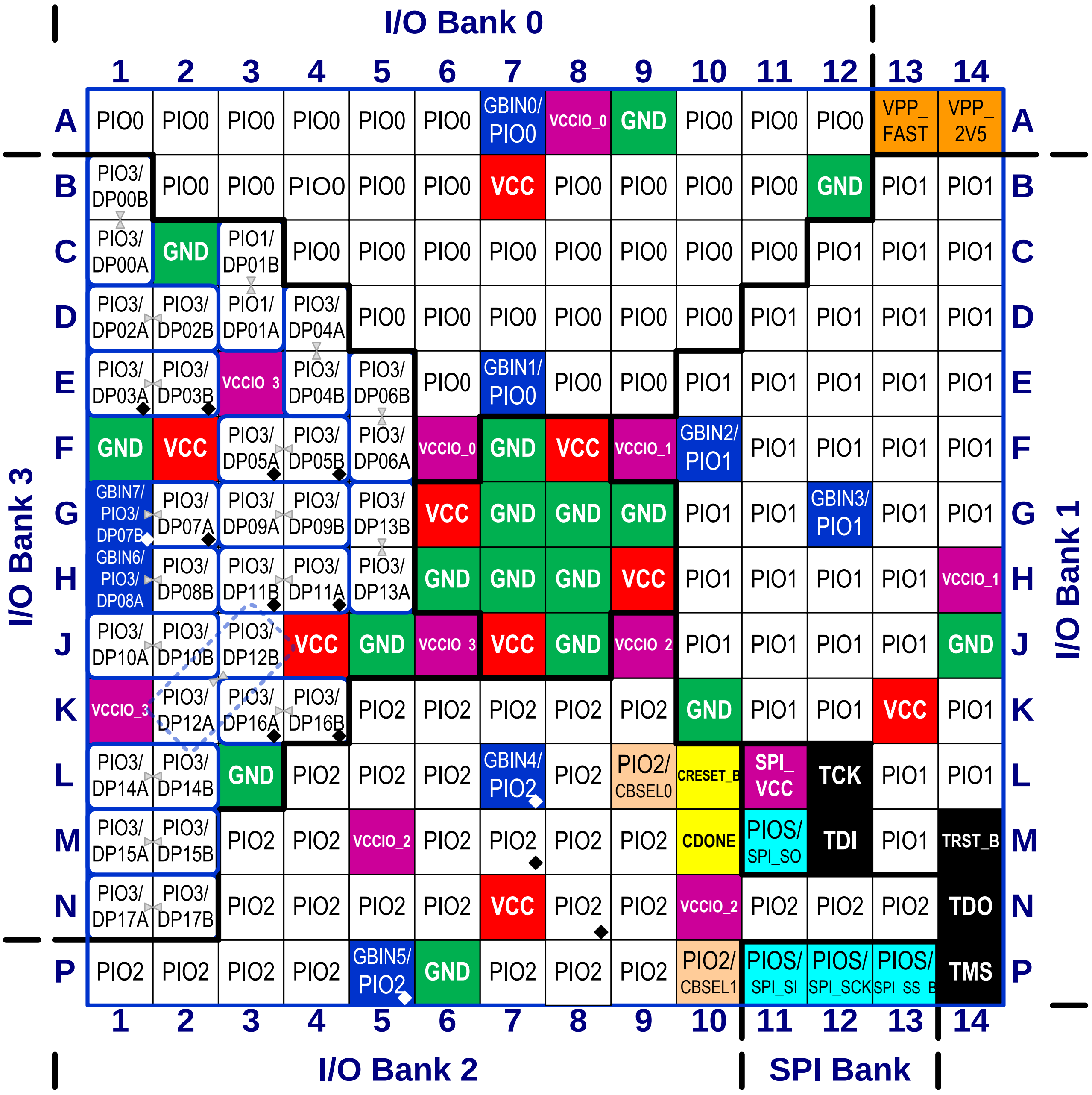
Footprint Diagram

Figure 45 shows the iCE65L04 chip-scale BGA footprint for the 8 x 8 mm CB196 package. The footprint for the iCE65L08 is different than the iCE64L04 footprint, as shown in Figure 46. The pinout differences are highlighted by warning diamonds (◆) in the footprint diagrams and summarized in Table 43.

> ⚠ Although both the iCE65L04 and iCE65L08 are both available in the CB196 package and ***almost*** completely pin compatible, there are differences as shown in Table 43.

Figure 31 shows the conventions used in the diagram. Also see Table 42 for a complete, detailed pinout for the 196-ball chip-scale BGA packages. The signal pins are also grouped into the four I/O Banks and the SPI interface.

***Figure 45:* iCE65L04 CB196 Chip-Scale BGA Footprint (Top View)**



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0	GBIN0/ PIO0	VCCIO_0	GND	PIO0	PIO0	PIO0	VPP_ FAST	VPP_ 2V5	A
B	PIO3/ DP00B	PIO0	PIO0	PIO0	PIO0	PIO0	VCC	PIO0	PIO0	PIO0	PIO0	GND	PIO1	PIO1	B
C	PIO3/ DP00A	GND	PIO1/ DP01B	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0	PIO1	PIO1	PIO1	C
D	PIO3/ DP02A	PIO3/ DP02B	PIO1/ DP01A	PIO3/ DP04A	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0	PIO1	PIO1	PIO1	PIO1	D
E	PIO3/ DP03A ◆	PIO3/ DP03B ◆	VCCIO_3	PIO3/ DP04B	PIO3/ DP06B	PIO0	GBIN1/ PIO0	PIO0	PIO0	PIO1	PIO1	PIO1	PIO1	PIO1	E
F	GND	VCC	PIO3/ DP05A ◆	PIO3/ DP05B ◆	PIO3/ DP06A	VCCIO_0	GND	VCC	VCCIO_1	GBIN2/ PIO1	PIO1	PIO1	PIO1	PIO1	F
G	GBIN7/ PIO3/ DP07B ◇	PIO3/ DP07A ◆	PIO3/ DP09A	PIO3/ DP09B	PIO3/ DP13B	VCC	GND	GND	GND	PIO1	PIO1	GBIN3/ PIO1	PIO1	PIO1	G
H	GBIN6/ PIO3/ DP08A	PIO3/ DP08B	PIO3/ DP11B ◆	PIO3/ DP11A ◆	PIO3/ DP13A	GND	GND	GND	VCC	PIO1	PIO1	PIO1	PIO1	VCCIO_1	H
J	PIO3/ DP10A	PIO3/ DP10B	PIO3/ DP12B	VCC	GND	VCCIO_3	VCC	GND	VCCIO_2	PIO1	PIO1	PIO1	PIO1	GND	J
K	VCCIO_3	PIO3/ DP12A	PIO3/ DP16A ◆	PIO3/ DP16B ◆	PIO2	PIO2	PIO2	PIO2	PIO2	GND	PIO1	PIO1	VCC	PIO1	K
L	PIO3/ DP14A	PIO3/ DP14B	GND	PIO2	PIO2	PIO2	GBIN4/ PIO2 ◇	PIO2	PIO2/ CBSEL0	CRESET_B	SPI_ VCC	TCK	PIO1	PIO1	L
M	PIO3/ DP15A	PIO3/ DP15B	PIO2	PIO2	VCCIO_2	PIO2	PIO2 ◆	PIO2	PIO2	CDONE	PIOS/ SPI_SO	TDI	PIO1	TRST_B	M
N	PIO3/ DP17A	PIO3/ DP17B	PIO2	PIO2	PIO2	PIO2	VCC	PIO2 ◆	PIO2	VCCIO_2	PIO2	PIO2	PIO2	TDO	N
P	PIO2	PIO2	PIO2	PIO2	GBIN5/ PIO2 ◇	GND	PIO2	PIO2	PIO2	PIO2/ CBSEL1	PIOS/ SPI_SI	PIOS/ SPI_SCK	PIOS/ SPI_SS_B	TMS	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Ball Function	Ball Number	Pin Type	Bank
PIO1	F14	PIO	1
PIO1	G10	PIO	1
PIO1	G11	PIO	1
PIO1	G13	PIO	1
PIO1	G14	PIO	1
PIO1	H10	PIO	1
PIO1	H11	PIO	1
PIO1	H12	PIO	1
PIO1	H13	PIO	1
PIO1	J10	PIO	1
PIO1	J11	PIO	1
PIO1	J12	PIO	1
PIO1	J13	PIO	1
PIO1	K11	PIO	1
PIO1	K12	PIO	1
PIO1	K14	PIO	1
PIO1	L13	PIO	1
PIO1	L14	PIO	1
PIO1	M13	PIO	1
TCK	L12	JTAG	1
TDI	M12	JTAG	1
TDO	N14	JTAG	1
TMS	P14	JTAG	1
TRST_B	M14	JTAG	1
VCCIO_1	F9	VCCIO	1
VCCIO_1	H14	VCCIO	1
CDONE	M10	CONFIG	2
CRESET_B	L10	CONFIG	2
GBIN4/PIO2 (◆)	***iCE65L04:*** L7 ***iCE65L08:*** N8	GBIN	2
GBIN5/PIO2 (◆)	***iCE65L04:*** P5 ***iCE65L08:*** M7	GBIN	2
PIO2	K5	PIO	2
PIO2	K6	PIO	2
PIO2	K7	PIO	2
PIO2	K8	PIO	2
PIO2	K9	PIO	2
PIO2	L4	PIO	2
PIO2	L5	PIO	2
PIO2	L6	PIO	2
PIO2	L8	PIO	2
PIO2	M3	PIO	2
PIO2	M4	PIO	2
PIO2	M6	PIO	2
PIO2 (◆)	***iCE65L04:*** M7 ***iCE65L08:*** P5	PIO	2
PIO2	M8	PIO	2
PIO2	M9	PIO	2
PIO2	N3	PIO	2
PIO2	N4	PIO	2
PIO2	N5	PIO	2
PIO2	N6	PIO	2

Pinout Table

Table 44 provides a detailed pinout table for the two chip-scale BGA packages. Pins are generally arranged by I/O bank, then by ball function. The balls with a black circle (●) are unconnected balls (N.C.) for the iCE65L04 in the CB284 package. The CB132 package fits within the CB284 package footprint as shown in Figure 48. The right-most column shows which CB132 ball corresponds to the CB284.

The table also highlights the differential I/O pairs in I/O Bank 3.

Table 44: iCE65 CB284 Chip-scale BGA Pinout Table (with CB132 cross reference)

	Ball Number	Pin Type by Device			
Ball Function	iCE65L04 iCE65L08	iCE65L04	iCE65L08	Bank	CB132 Ball Equivalent
GBIN0/PIO0	E10	GBIN	GBIN	0	A6
GBIN1/PIO0	E11	GBIN	GBIN	0	A7
PIO0 (●)	A1	N.C.	PIO	0	—
PIO0 (●)	A2	N.C.	PIO	0	—
PIO0 (●)	A3	N.C.	PIO	0	—
PIO0 (●)	A4	N.C.	PIO	0	—
PIO0	A5	PIO	PIO	0	—
PIO0	A6	PIO	PIO	0	—
PIO0	A7	PIO	PIO	0	—
PIO0 (●)	A9	N.C.	PIO	0	—
PIO0 (●)	A10	N.C.	PIO	0	—
PIO0 (●)	A11	N.C.	PIO	0	—
PIO0 (●)	A12	N.C.	PIO	0	—
PIO0 (●)	A13	N.C.	PIO	0	—
PIO0	A15	PIO	PIO	0	—
PIO0	A16	PIO	PIO	0	—
PIO0	A17	PIO	PIO	0	—
PIO0	A18	PIO	PIO	0	—
PIO0 (●)	A14	N.C.	PIO	0	—
PIO0 (●)	A19	N.C.	PIO	0	—
PIO0 (●)	A20	N.C.	PIO	0	—
PIO0	C3	PIO	PIO	0	—
PIO0	C4	PIO	PIO	0	—
PIO0	C5	PIO	PIO	0	—
PIO0	C6	PIO	PIO	0	—
PIO0	C7	PIO	PIO	0	—
PIO0	C9	PIO	PIO	0	—
PIO0	C10	PIO	PIO	0	—
PIO0	C11	PIO	PIO	0	—
PIO0	C13	PIO	PIO	0	—
PIO0	C14	PIO	PIO	0	—
PIO0	C15	PIO	PIO	0	—
PIO0	C16	PIO	PIO	0	—
PIO0	C17	PIO	PIO	0	—
PIO0	C18	PIO	PIO	0	—
PIO0	C19	PIO	PIO	0	—
PIO0	E5	PIO	PIO	0	A1
PIO0	E6	PIO	PIO	0	A2
PIO0	E7	PIO	PIO	0	A3
PIO0	E8	PIO	PIO	0	A4
PIO0	E9	PIO	PIO	0	A5
PIO0	E14	PIO	PIO	0	A10

Ball Function	Ball Number	Pin Type by Device		Bank	CB132 Ball Equivalent
	iCE65L04 iCE65L08	iCE65L04	iCE65L08		
PIO3/DP03A	H5	DPIO	DPIO	3	D1
PIO3/DP03B	J5	DPIO	DPIO	3	E1
PIO3/DP04A	K8	DPIO	DPIO	3	F4
PIO3/DP04B	K7	DPIO	DPIO	3	F3
PIO3/DP05A	E3	DPIO	DPIO	3	—
PIO3/DP05B	F3	DPIO	DPIO	3	—
PIO3/DP06A	G3	DPIO	DPIO	3	—
PIO3/DP06B	H3	DPIO	DPIO	3	—
PIO3/DP07A (●)	B1	N.C.	DPIO	3	—
PIO3/DP07B (●)	C1	N.C.	DPIO	3	—
PIO3/DP08A (●)	D1	N.C.	DPIO	3	—
PIO3/DP08B (●)	E1	N.C.	DPIO	3	—
PIO3/DP09A	H1	DPIO	DPIO	3	—
PIO3/DP09B	J1	DPIO	DPIO	3	—
PIO3/DP10A	K1	DPIO	DPIO	3	—
PIO3/DP10B	L1	DPIO	DPIO	3	—
PIO3/DP11A	L3	DPIO	DPIO	3	—
GBIN7/PIO3/DP11B	L5	GBIN	GBIN	3	G1
PIO3/DP12A (●)	T1	N.C.	DPIO	3	—
PIO3/DP12B (●)	U1	N.C.	DPIO	3	—
PIO3/DP13A (●)	W1	N.C.	DPIO	3	—
PIO3/DP13B (●)	Y1	N.C.	DPIO	3	—
PIO3/DP14A (●)	AA1	N.C.	DPIO	3	—
PIO3/DP14B (●)	AB1	N.C.	DPIO	3	—
GBIN6/PIO3/DP15A	M5	GBIN	GBIN	3	H1
PIO3/DP15B	M3	DPIO	DPIO	3	—
PIO3/DP16A	N3	DPIO	DPIO	3	—
PIO3/DP16B	P3	DPIO	DPIO	3	—
PIO3/DP17A	U3	DPIO	DPIO	3	—
PIO3/DP17B	V3	DPIO	DPIO	3	—
PIO3/DP18A	W3	DPIO	DPIO	3	—
PIO3/DP18B	Y3	DPIO	DPIO	3	—
PIO3/DP19A	L7	DPIO	DPIO	3	G3
PIO3/DP19B	L8	DPIO	DPIO	3	G4
PIO3/DP20A	M7	DPIO	DPIO	3	H3
PIO3/DP20B	M8	DPIO	DPIO	3	H4
PIO3/DP21A	N7	DPIO	DPIO	3	J3
PIO3/DP21B	N5	DPIO	DPIO	3	J1
PIO3/DP22A	P7	DPIO	DPIO	3	K3
PIO3/DP22B	P8	DPIO	DPIO	3	K4
PIO3/DP23A	R5	DPIO	DPIO	3	L1
PIO3/DP23B	T5	DPIO	DPIO	3	M1
PIO3/DP24A	U5	DPIO	DPIO	3	N1
PIO3/DP24B	V5	DPIO	DPIO	3	P1
VCCIO_3	F1	VCCIO	VCCIO	3	—
VCCIO_3	P1	VCCIO	VCCIO	3	—

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO3_44/DP22A	M1	U3	86	231.735	777.67
PIO3_45/DP22B	M2	V3	87	129.735	732.67
PIO3_46/DP23A	N1	U5	88	231.735	687.67
PIO3_47/DP23B	N2	V5	89	129.735	642.67
PIO3_48/DP24A	—	W3	90	231.735	597.67
PIO3_49/DP24B	—	Y3	91	129.735	552.665
PIO2_00	P1	AB2	92	510.0	139.5
PIO2_01	M3	R8	93	560.0	37.5
PIO2_02	P2	Y4	94	610.0	139.5
GND	P6	AB5	95	660.0	37.5
GND	—	—	96	710.0	139.5
PIO2_03	M4	T7	97	760.0	37.5
PIO2_04	N3	AB3	98	810.0	139.5
PIO2_05	—	R9	99	859.3	37.5
PIO2_06	—	Y5	100	910.0	139.5
PIO2_07	L4	T8	101	960.0	37.5
PIO2_08	P3	V6	102	1,012.5	139.5
VCCIO_2	M5	T9	103	1,047.5	37.5
VCCIO_2	—	—	104	1,082.5	139.5
PIO2_09	P4	R10	105	1,117.5	37.5
PIO2_10	N4	AB4	106	1,152.5	139.5
GND	H8	V10	107	1,187.5	37.5
GND	—	—	108	1,222.5	139.5
PIO2_11	K5	V7	109	1,257.5	37.5
PIO2_12	P5	Y7	110	1,292.5	139.5
PIO2_13	—	V9	111	1,327.5	37.5
PIO2_14	—	Y6	112	1,362.5	139.5
PIO2_15	—	AB7	113	1,397.5	37.5
PIO2_16	—	AB6	114	1,432.5	139.5
PIO2_17	L5	Y9	115	1,467.5	37.5
PIO2_18	N5	V8	116	1,502.3	139.5
GND	P6	N12	117	1,537.3	37.5
GND	—	—	118	1,572.5	139.5
PIO2_19	N6	AB8	119	1,607.5	37.5
PIO2_20	K6	AB9	120	1,642.5	139.5
VCC	J7	Y8	121	1,677.5	37.5
VCC	—	—	122	1,712.5	139.5
PIO2_21	L6	T10	123	1,747.5	37.5
PIO2_22	M6	AB10	124	1,782.5	139.5
PIO2_23	—	AB11	125	1,817.5	37.5
PIO2_24	—	AB12	126	1,852.5	139.5
PIO2_25	L7	Y10	127	1,887.5	37.5
PIO2_26	P7	AB13	128	1,922.5	139.5
PIO2_27	K7	AB14	129	1,957.5	37.5
VCCIO_2	N10	Y11	130	1,992.5	139.5
VCCIO_2	—	—	131	2,027.5	37.5

I/O Characteristics

***Table 49:* PIO Pin Electrical Characteristics**

Symbol	Description		Conditions	Minimum	Nominal	Maximum	Units
I_I	Input pin leakage current	I/O Bank 0, 1, 2	V_{IN} = $VCCIO_{max}$ to 0 V			±10	µA
		I/O Bank 3	V_{IN} = $VCCIO_{max}$				
I_{OZ}	Three-state I/O pin (Hi-Z) leakage current		V_O = $VCCIO_{max}$ to 0 V			±10	µA
C_{PIO}	PIO pin input capacitance				6		pF
C_{GBIN}	GBIN global buffer pin input capacitance				6		pF
R_{PULLUP}	Internal PIO pull-up resistance during configuration		VCCIO = 3.3V		40		kΩ
			VCCIO = 2.5V		50		kΩ
			VCCIO = 1.8V		90		kΩ
			VCCIO = 1.5V				kΩ
			VCCIO = 1.2V				kΩ
V_{HYST}	Input hysteresis		VCCIO = 1.5V to 3.3V		50		mV

NOTE: All characteristics are characterized and may or may not be tested on each pin on each device.

Single-ended I/O Characteristics

***Table 50:* I/O Characteristics (I/O Banks 0, 1, 2 and SPI only) (I/O Bank 3 iCE65L01 only)**

I/O Standard	Nominal I/O Bank Supply Voltage	Input Voltage (V)		Output Voltage (V)		Output Current at Voltage (mA)	
		V_{IL}	V_{IH}	V_{OL}	V_{OH}	I_{OL}	I_{OH}
LVCMOS33	3.3V	0.80	2.00	0.4	2.40	8	8
LVCMOS25	2.5V	0.70	1.70	0.4	2.00	6	6
LVCMOS18	1.8V	35% VCCIO	65% VCCIO	0.4	1.40	4	4
LVCMOS15	1.5V	Not supported Use I/O Bank 3		0.4	1.20	2	2

***Table 51:* I/O Characteristics (I/O Bank 3 and iCE65L04/08 only)**

I/O Standard	Supply Voltage	Input Voltage (V)		Output Voltage (V)		I/O Attribute Name	mA at Voltage
		Max. V_{IL}	Min. V_{IH}	Max. V_{OL}	Min. V_{OH}		I_{OL}, I_{OH}
LVCMOS33	3.3V	0.80	2.20	0.4	2.40	SL_LVCMOS33_8	±8
LVCMOS25	2.5V	0.70	1.70	0.4	2.00	SB_LVCMOS25_16	±16
						SB_LVCMOS25_12	±12
						SB_LVCMOS25_8 *	±8
						SB_LVCMOS25_4	±4
LVCMOS18	1.8V	35% VCCIO	65% VCCIO	0.4	VCCIO–0.45	SB_LVCMOS18_10	±10
						SB_LVCMOS18_8	±8
						SB_LVCMOS18_4 *	±4
						SB_LVCMOS18_2	±2
LVCMOS15	1.5V	35% VCCIO	65% VCCIO	25% VCCIO	75% VCCIO	SB_LVCMOS15_4	±4
						SB_LVCMOS15_2 *	±2
MDDR	1.8V	35% VCCIO	65% VCCIO	0.4	VCCIO–0.45	SB_MDDR10	±10
						SB_MDDR8	±8
						SB_MDDR4 *	±4
						SB_MDDR2	±2
SSTL2 (Class 2)	2.5V	VREF–0.180	VREF+0.180	0.35	VTT+0.430	SB_SSTL2_CLASS_2	±16.2
SSTL2 (Class 1)				0.54		SB_SSTL2_CLASS_1	±8.1
SSTL18 (Full)	1.8V	VREF–0.125	VREF+0.125	0.28	VTT+0.280	SB_SSTL18_FULL	±13.4
SSTL18 (Half)				VTT–0.475	VTT+0.475	SB_SSTL18_HALF	±6.7

NOTES:

SSTL2 and SSTL18 I/O standards require the VREF input pin, which is only available on the CB284 package and die-based products.

Programmable Input/Output (PIO) Block

Table 55 provides timing information for the logic in a Programmable Logic Block (PLB), which includes the paths shown in Figure 57 and Figure 58. The timing shown is for the LVCMOS25 I/O standard in all I/O banks. The iCEcube development software reports timing adjustments for other I/O standards.

Figure 57: Programmable I/O (PIO) Pad-to-Pad Timing Circuit

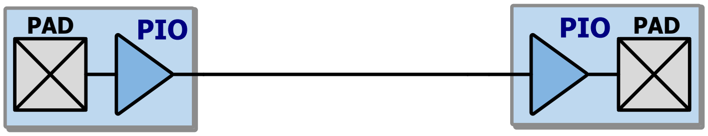


Figure 58: Programmable I/O (PIO) Sequential Timing Circuit

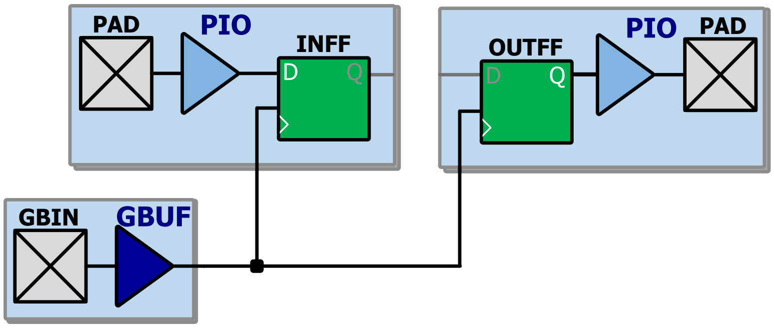


Table 55: Typical Programmable Input/Output (PIO) Timing (LVCMOS25)

			Device: iCE65	L01	L04, L08			
			Power/Speed Grad	–T	–L		–T	
			Nominal VCC	1.2 V	1.0 V	1.2 V	1.2 V	
Symbol	**From**	**To**	**Description**	**Typ.**	**Typ.**	**Typ.**	**Typ.**	**Units**
		Synchronous Output Paths						
t_{OCKO}	OUTFF clock input	PIO output	Delay from clock input on OUTFF output flip-flop to PIO output pad.	4.7	13.8	7.3	5.6	ns
t_{GBCKIO}	GBIN input	OUTFF clock input	Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to clock input on the PIO OUTFF output flip-flop.	2.1	7.3	3.8	2.6	ns
		Synchronous Input Paths						
t_{SUPDIN}	PIO input	GBIN input	Setup time on PIO input pin to INFF input flip-flop before active clock edge on GBIN input, including interconnect delay.	0	0	0	0	ns
t_{HDPDIN}	GBIN input	PIO input	Hold time on PIO input to INFF input flip-flop after active clock edge on the GBIN input, including interconnect delay.	2.7	7.1	3.6	2.8	ns
		Pad to Pad						
t_{PADIN}	PIO input	Interconnect	Asynchronous delay from PIO input pad to adjacent interconnect.	2.5	9.5	5.0	3.2	ns
t_{PADO}	Interconnect	PIO output	Asynchronous delay from adjacent interconnect to PIO output pad including interconnect delay.	4.5	14.6	7.7	6.2	ns

RAM4K Block

Table 56 provides timing information for the logic in a RAM4K block, which includes the paths shown in Figure 59.

Figure 59: RAM4K Timing Circuit

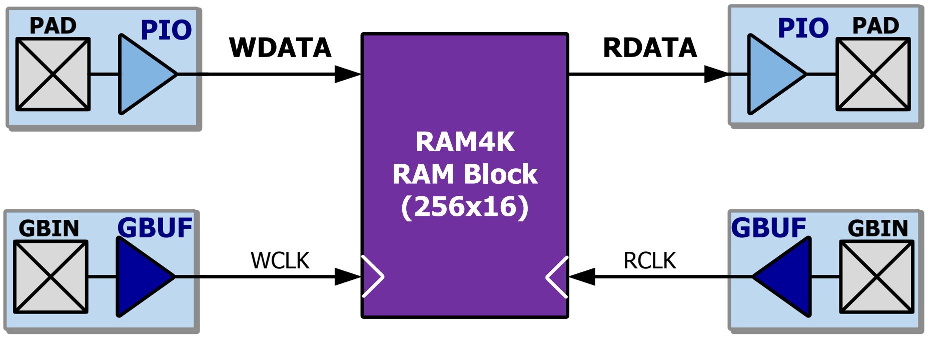


Table 56: Typical RAM4K Block Timing

			Device: iCE65	L01	L04, L08			
			Power/Speed Grade	–T	–L	–L	–T	
			Nominal VCC	1.2 V	1.0 V	1.2 V	1.2 V	
Symbol	From	To	Description	Typ.	Typ.	Typ.	Typ.	Units
Write Setup/Hold Time								
t_{SUWD}	PIO input	GBIN input	Minimum write data setup time on PIO inputs before active clock edge on GBIN input, include interconnect delay.	0.6	3.1	1.7	0.8	ns
t_{HDWD}	GBIN input	PIO input	Minimum write data hold time on PIO inputs after active clock edge on GBIN input, including interconnect delay.	0	0	0	0	ns
Read Clock-Output-Time								
t_{CKORD}	RCLK clock input	PIO output	Clock-to-output delay from RCLK input pin, through RAM4K RDATA output flip-flop to PIO output pad, including interconnect delay.	5.6	17.1	9.1	7.3	ns
t_{GBCKRM}	GBIN input	RCLK clock input	Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to the RCLK clock input.	2.1	7.3	3.8	2.6	ns
Write and Read Clock Characteristics								
t_{RMWCKH}	WCLK RCLK	WCLK RCLK	Write clock High time	0.54	1.14	0.54	0.54	ns
t_{RMWCKL}			Write clock Low time	0.63	1.32	0.63	0.63	ns
t_{RMWCYC}			Write clock cycle time	1.27	2.64	1.27	1.27	ns
F_{WMAX}			Sustained write clock frequency	256	256	256	256	MHz

Table 60 provides various timing specifications for the SPI peripheral mode interface.

Table 60: SPI Peripheral Mode Timing

Symbol	From	To	Description		All Grades		Units
					Min.	Max.	
t_{CR_SCK}	CRESET_B	SPI_SCK	Minimum time from a rising edge on CRESET_B until the first SPI write operation, first SPI_SCK. During this time, the iCE65 FPGA is clearing its internal configuration memory	iC65L01	800	—	µs
				iC65L04	800		
				iC65L08	1200		
$t_{SUSPISI}$	SPI_SI	SPI_SCK	Setup time on SPI_SI before the rising SPI_SCK clock edge		12	—	ns
$t_{HDSPISI}$	SPI_SCK	SPI_SI	Hold time on SPI_SI after the rising SPI_SCK clock edge		12	—	ns
$t_{SPISCKH}$	SPI_SCK	SPI_SCK	SPI_SCK clock High time		20	—	ns
$t_{SPISCKL}$	SPI_SCK	SPI_SCK	SPI_SCK clock Low time		20	—	ns
$t_{SPISCKCYC}$	SPI_SCK	SPI_SCK	SPI_SCK clock period*		40	1,000	ns
F_{SPI_SCK}	SPI_SCK	SPI_SCK	Sustained SPI_SCK clock frequency*		1	25	MHz

* = Applies after sending the synchronization pattern.

Power Consumption Characteristics

Core Power

Table 61 shows the power consumed on the internal VCC supply rail when the device is filled with 16-bit binary counters, measured with a 32.768 kHz and at 32.0 MHz. Low power (−L) at 1.0 V operation and high-performance (−T) version at 1.2V operation is provided.

Table 61: **VCC Power Consumption for Device Filled with 16-Bit Binary Counters**

Symbol	Description	Grade	VCC	iCE65L01		iCE65L04		iCE65L08		Units
				Typical	Max.	Typical	Max.	Typical	Max.	
I_{CC0K}	f =0,	−L	1.0V	12		26		54		µA
		−T	1.2V	19		43		90		
I_{CC32K}	f ≤ 32.768 kHz	−L	1.0V	15		31		62		µA
		−T	1.2V	23		50		100		
I_{CC32M}	f = 32.0 MHz	−L	1.0V	3		7		14		mA
		−T	1.2V	4		8		17		

I/O Power

Table 62 provides the static current by I/O bank. The typical current for I/O Banks 0, 1, 2 and the SPI bank is not measurable within the accuracy of the test environment. The PIOs in I/O Bank 3 use different circuitry and dissipate a small amount of static current.

Table 62: I/O Bank Static Current (f = 0 MHz)

Symbol	Description		Typical	Max	Units
I_{CCO_0}	I/O Bank 0	Static current consumption per I/O bank. f = 0 MHz. No PIO pull-up resistors enabled. All inputs grounded. All outputs driving Low.	« 1		µA
I_{CCO_1}	I/O Bank 1		« 1		µA
I_{CCO_2}	I/O Bank 2		« 1		µA
I_{CCO_3}	I/O Bank 3		iCE65L01: « 1 iCE65L04/08: 1.2		µA
I_{CCO_SPI}	SPI Bank		« 1		µA

NOTE: The typical static current for I/O Banks 0, 1, 2, and the SPI bank is less than the accuracy of the device tester.

Power Estimator

To estimate the power consumption for a specific application, please download and use the iCE65 Power Estimator Spreadsheet our use the power estimator built into the iCEcube software.

- iCE65 Power Estimator Spreadsheet