Lattice Semiconductor Corporation - ICE65L04F-LCB284C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

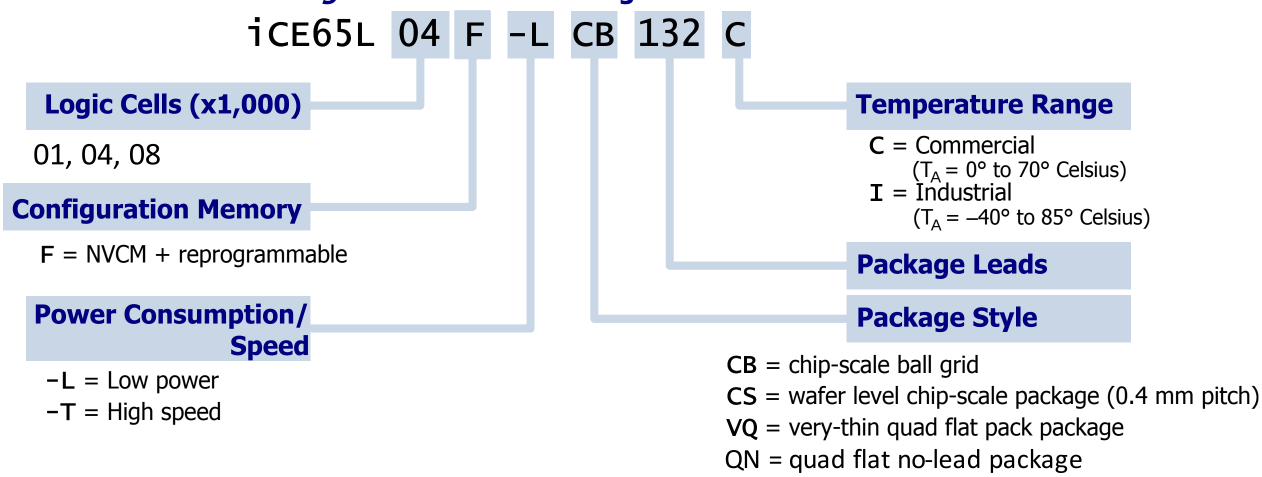
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	440
Number of Logic Elements/Cells	3520
Total RAM Bits	81920
Number of I/O	176
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	284-VFBGA, CSPBGA
Supplier Device Package	284-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice65l04f-lcb284c

Ordering Information

Figure 2 describes the iCE65 ordering codes for all packaged, non-NVCM Programed components. See the separate DiePlus data sheets when ordering die-based products.

***Figure 2:* iCE65 Ordering Codes Standard Device**

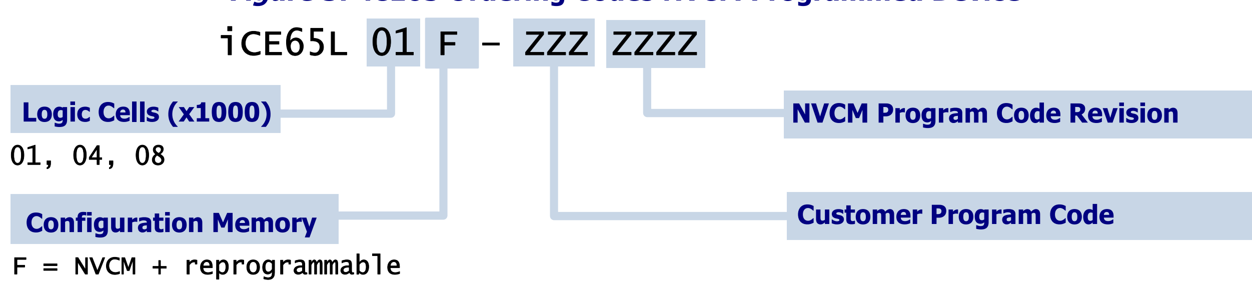


iCE65 devices offer two power consumption, speed options. Standard products ("-L" ordering code) have low standby and dynamic power consumption. The "-T" provides higher-speed logic.

Similarly, iCE65 devices are available in two operating temperature ranges, one for typical commercial applications, the other with an extended temperature range for industrial and telecommunications applications. The ordering code also specifies the device package option, as described further in Table 2.

Figure 3 describes the iCE65 ordering codes for all packaged, NVCM Programmed components.

***Figure 3:* iCE65 Ordering Codes NVCM Programmed Device**



Each flip-flop has an additional control that defines its set or reset behavior. As defined in the configuration image, the control defines whether the set or reset operation is synchronized to the active CLK clock edge or whether it is completely asynchronous.

- The SB_DFFR and SB_DFFS primitives are asynchronously controlled, solely by the SR input. If the SR input is High, then an SB_DFFR primitive is asynchronously reset and an SB_DFFS primitive is asynchronously set.
- The SB_DFFSR and SB_DFFRSS primitives are synchronously controlled by both the SR input and the clock input. If the SR input is High at a rising edge of the clock input, then an SB_DFFSR primitive is synchronously reset and an SB_DFFSS primitive is synchronously set.

The LUT4 output or the flip-flop output then connects to the programmable interconnect.

Because of the shared control signals, the design software can pack flip-flops with common control inputs into a single PLB block, as described by Table 4. There are eight total packing options.

***Table 4:* Flip-flop Packing/Sharing within a PLB**

Group	Active Clock Edge	Clock Enable	Set or Reset Control (Sync. or Async)
1	↑	None (always enabled)	None
2	↓		
3	↑		PLB set/reset control
4	↓		
5	↑	Selective (controlled by PLB clock enable)	None
6	↓		
7	↑		PLB set/reset control
8	↓		

For detailed flip-flop internal timing, see Table 54.

Carry Logic

The dedicated Carry Logic within each Logic Cell primarily accelerates and improves the efficiency of arithmetic logic such as adders, accumulators, subtracters, incrementers, decrementers, counters, ALUs, and comparators. The Carry Logic also supports wide combinational logic functions.

$$COUT = I1 \bullet I2 + CIN \bullet I1 + CIN \bullet I2 \quad \text{[Equation 1]}$$

Equation 1 and Figure 5 describe the Carry Logic structure within a Logic Cell. The Carry Logic shares inputs with the associated Look-Up Table (LUT4). The LUT4's I1 and I2 inputs directly feed the Carry Logic; inputs I0 and I3 do not. A signal cascades between Logic Cells within the Programmable Logic Block. The carry input from the previous adjacent Logic Cell optionally provides an alternate input to the LUT4 function, supplanting the I3 input.

Low-Power Disable

To save power and prevent unnecessary signal switching, the Carry Logic function within a Logic Cell is disabled if not used. The output of a Logic Cell's Carry Logic is forced High.

PLB Carry Input and Carry Output Connections

As shown in Figure 5, each Programmable Logic Block has a carry input signal that can be initialized High, Low, or come from the carry output signal from PLB immediately below.

Similarly, the Carry Logic output from the Programmable Logic Block connects to the PLB immediately above, which allows the Carry Logic to span across multiple PLBs in a column. As shown in Figure 6, the Carry Logic chain can be tapped mid-way through a chain or a PLB by feeding the value through a LUT4 function.

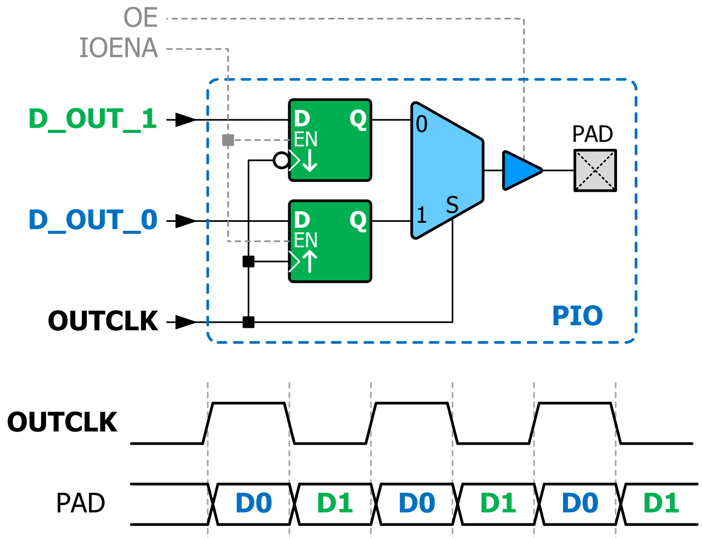
Adder Example

Figure 6 shows an example design that uses the Carry Logic. The example is a 2-bit adder, which can be expanded into an adder of arbitrary size. The LUT4 function within a Logic Cell is programmed to calculate the sum of the two input values and the carry input, `A[i] + B[i] + CARRY_IN[i-1] = SUM[i]`.

Double Data Rate (DDR) Flip-Flops

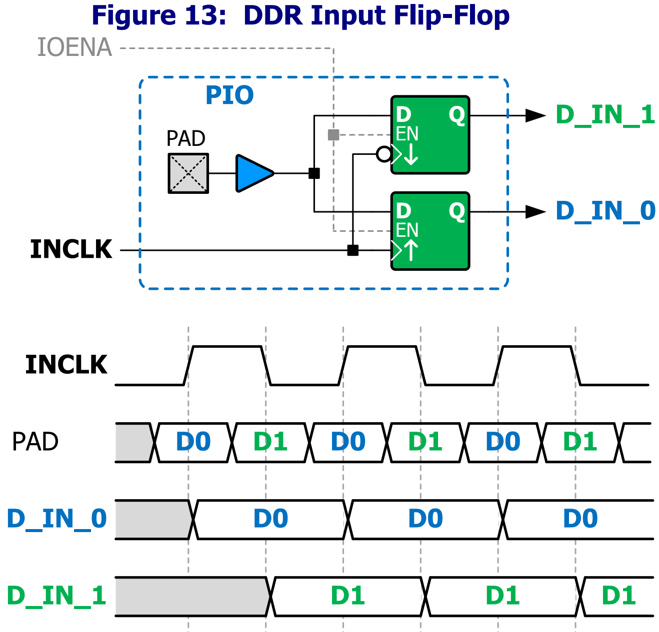
Each individual PIO pin optionally has two sets of double data rate (DDR) flip-flops; one input pair and one output pair. Figure 12 demonstrates the functionality of the output DDR flip-flop. Two signals from within the iCE65 device drive the DDR output flip-flop. The D_OUT_0 signal is clocked by the rising edge of the OUTCLK signal while the D_OUT_1 signal is clocked by the falling edge of the OUTCLK signal, assuming no optional clock polarity inversion. Internally, the two individual flip-flops are multiplexed together before the data appears at the pad, effectively doubling the output data rate.

Figure 12: DDR Output Flip-Flop



Similarly, Figure 13 demonstrates the DDR input flip-flop functionality. A double data rate (DDR) signal arrives at the pad. Internally, one value is clocked by the rising edge of the INCLK signal and another value is clocked by the falling edge of the INCLK signal. The DDR data stream is effectively de-multiplexed within the PIO pin and presented to the programmable interconnect on D_IN_0 and D_IN_1.

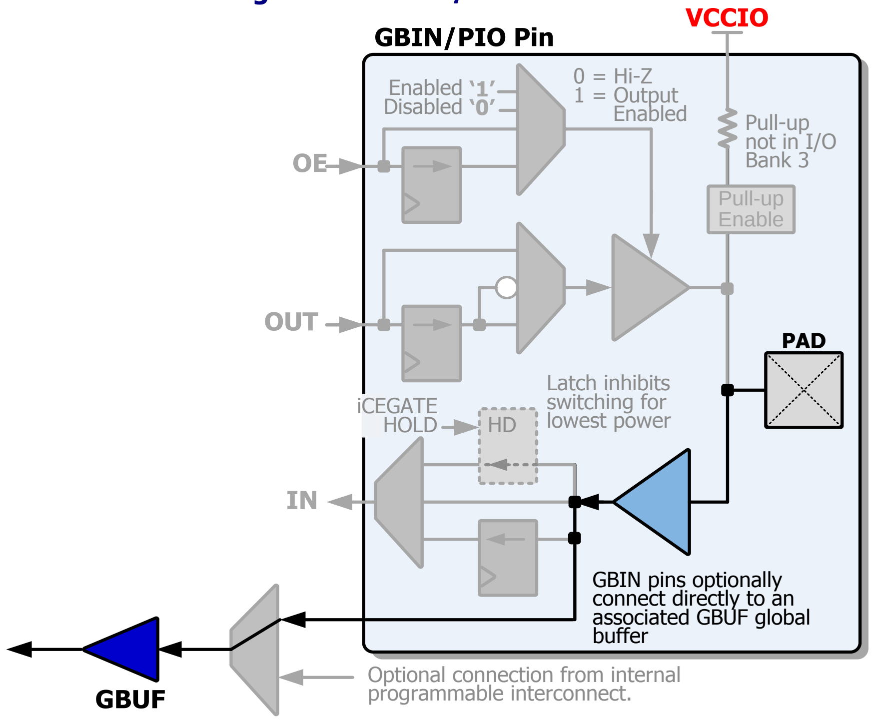
Figure 13: DDR Input Flip-Flop



The DDR flip-flops provide several design advantages. Internally within the iCE65 device, the clock frequency is half the effective external data rate. The lower clock frequency eases internal timing, doubling the clock period, and slashes the clock-related power in half.

> ⚠ Note the clock differences between the iCE65L04 and iCE65L08 in the CB196 package.

Figure 15: GBIN/PIO Pin



Differential Global Buffer Input

All eight global buffer inputs support single-ended I/O standards such as LVCMOS. Global buffer GBUF7 in I/O Bank 3 also provides an optional direct SubLVDS, LVDS, or LVPECL differential clock input, as shown in Figure 16. The GBIN7 and its associated differential I/O pad accept a differential clock signal. A 100 Ω termination resistor is required across the two pads. Optionally, swap the outputs from the LVDS or LVPECL clock driver to invert the clock as it enters the iCE65 device.

Figure 16: LVDS or LVPECL Clock Input

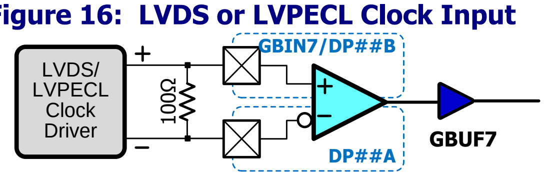


Table 15 lists the pin or ball numbers for the differential global buffer input by package style. Although this differential input is the only one that connects directly to a global buffer, other differential inputs can connect to a global buffer using general-purpose interconnect, with slightly more signal delay.

***Table 15:* Differential Global Buffer Input Ball/Pin Number by Package**

Differential Global Buffer Input (GBIN)	I/O Bank	VQ100	CB132	'L04 CB196	'L08 CB196	CB284
GBIN7/DPxxB	3	13	N/A	G1	H3	L5
DPxxA		12	N/A	G2	H4	L3

> ⚠ The differential global buffer input is not available for iCE65 devices in the CB132 package. This restriction is an artifact of the pin compatibility between the CB132 and CB284 package.
>
> Note the clock differences between the iCE65L04 and iCE65L08 in the CB196 package.

Figure 19: RAM4K Read Logic

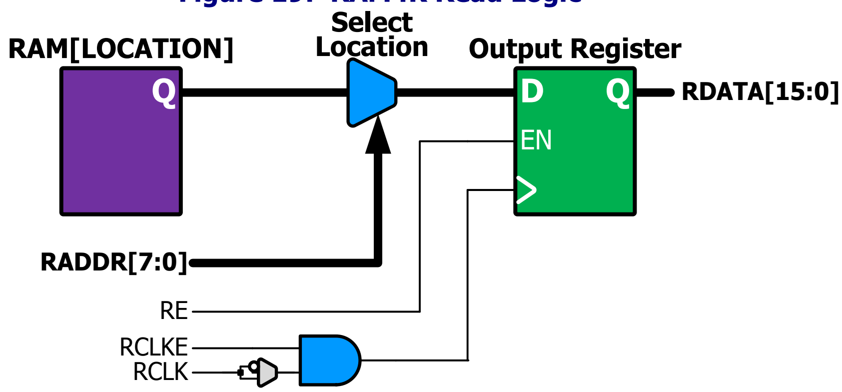


Table 19: RAM4K Read Operations

Operation	RADDR[7:0] Address	RE Read Enable	RCLKE Clock Enabe	RCLK Clock	RDATA[15:0]
After configuration, before first valid Read Data operation	X	X	X	X	Undefined
Disabled	X	X	X	0	No Change
Disabled		X	0	X	No Change
Disabled	X	0	X	X	No change
Read Data	RADDR	1	1	↑	RAM[RADDR]

To read data from the RAM4K block, perform the following operations.

- Supply a valid address on the RADDR[7:0] address input port
- Enable the RAM4K read port (RE = 1)
- Enable the RAM4K read clock (RCLKE = 1)
- Apply a rising clock edge on RCLK
- After the clock edge, the RAM contents located at the specified address (RADDR) appear on the RDATA output port

Read Data Register Undefined Immediately after Configuration

Unlike the flip-flops in the Programmable Logic Blocks and Programmable I/O pins, the RDATA[15:0] read data output register is not automatically reset after configuration. Consequently, immediately following configuration and before the first valid Read Data operation, the initial RDATA[15:0] read value is undefined.

Pre-loading RAM Data

The data contents for a RAM4K block can be optionally pre-loaded during iCE65 configuration. If not pre-loaded during configuration, then the RAM contents must be initialized by the iCE65 application before the RAM contents are valid.

Pre-loading the RAM data in the configuration bitstream increases the size of the configuration image accordingly.

RAM Contents Preserved during Configuration

RAM contents are preserved (write protected) during configuration, assuming that voltage supplies are maintained throughout. Consequently, data can be passed between multiple iCE65 configurations by leaving it in a RAM4K block and then skipping pre-loading during the subsequent reconfiguration. See “Cold Boot Configuration Option” and “Warm Boot Configuration Option” for more information.

Low-Power Setting

To place a RAM4K block in its lowest power mode, keep WCLKE = 0 and RCLKE = 0. In other words, when not actively using a RAM4K block, disable the clock inputs.

Device Configuration

As described in Table 20, iCE65 components are configured for a specific application by loading a binary configuration bitstream image, generated by the Lattice development system. For high-volume applications, the bitstream image is usually permanently programmed in the on-chip NVCM, However, the bitstream image can also be stored external in a standard, low-cost commodity SPI serial Flash PROM. The iCE65 component can automatically load the image using the SPI Master Configuration Interface. Similarly, the iCE65 configuration data can be downloaded from an external processor, microcontroller, or DSP processor using an SPI-like serial interface or an IEEE 1149 JTAG interface.

***Table 20:* iCE65 Device Configuration Modes**

Mode	Analogy	Configuration Data Source
NVCM	ASIC	Internal, lowest-cost, secure, one-time programmable Nonvolatile Configuration Memory (NVCM)
SPI Flash	Microprocessor	External, low-cost, commodity, SPI serial Flash PROM
SPI Peripheral	Processor Peripheral	Configured by external device, such as a processor, microcontroller, or DSP using practically any data source, such as system Flash, a disk image, or over a network connection.
JTAG	JTAG	JTAG configuration requires sending a special command sequence on the SPI interface to enable JTAG configuration. Configuration is controlled by and external device.

Configuration Mode Selection

The iCE65 configuration mode is selected according to the following priority described below and illustrated in Figure 20.

- After exiting the Power-On Reset (POR) state or when CRESET_B returns High after being held Low for 250 ns or more, the iCE65 FPGA samples the logical value on its SPI_SS_B pin. Like other programmable I/O pins, the SPI_SS_B pin has an internal pull-up resistor (see Input Pull-Up Resistors on I/O Banks 0, 1, and 2).
- If the SPI_SS_B pin is sampled as a logic '1' (High), then …
  - Check if the iCE65 is enabled to configure from the Nonvolatile Configuration Memory (NVCM). If the iCE65 device has NVCM memory ('**F**' ordering code) but the NVCM is yet unprogrammed, then the iCE65 device is not enabled to configure from NVCM. Conversely, if the NVCM is programmed, the iCE65 device will configure from NVCM.
    - If enabled to configure from NVCM, the iCE65 device configures itself using NVCM.
    - If not enabled to configure from NVCM, then the iCE65 FPGA configures using the SPI Master Configuration Interface.
- If the SPI_SS_B pin is sampled as a logic '0' (Low), then the iCE65 device waits to be configured from an external controller or from another iCE65 device in SPI Master Configuration Mode using an SPI-like interface.

Table 28: **ColdBoot Select Ball/Pin Numbers by Package**

ColdBoot Select	CB81	QN84	VQ100	CB132	CB196	CB284
PIO2/CBSEL0	G5	B15	41	L9	L9	R13
PIO2/CBSEL1	H5	A20	42	P10	P10	V14

When creating the initial configuration image, the Lattice development software loads the start address for up to four configuration images in the bitstream. The value on the CBSEL[1:0] pins tell the configuration controller to read a specific start address, then to load the configuration image stored at the selected address. The multiple bitstreams are stored either in the SPI Flash or in the internal NVCM.

After configuration, the CBSEL[1:0] pins become normal PIO pins available to the application.

The Cold Boot feature allows the iCE65 to be reprogrammed for special application requirements such as the following.

- A normal operating mode and a self-test or diagnostics mode.
- Different applications based on switch settings.
- Different applications based on a card-slot ID number.

Warm Boot Configuration Option

The Warm Boot configuration is similar to the Cold Boot feature, but is completely under the control of the FPGA application.

A special design primitive, SB_WARMBOOT, allows an FPGA application to choose between four configuration images using two internal signal ports, S1 and S0, as shown in Figure 27. These internal signal ports connect to programmable interconnect, which in turn can connect to PLB logic and/or PIO pins.

After selecting the desired configuration image, the application then asserts the internal signal BOOT port High to force the FPGA to restart the configuration process from the specified vector address stored in PROM.

> ! A Warm Boot application can only jump to another configuration image that DOES NOT have Warm Boot enabled. There is no such restriction for Cold Boot applications.

Time-Out and Retry

When configuring from external SPI Flash, the iCE65 device looks for a synchronization word. If the device does not find a synchronization word within its timeout period, the device automatically attempts to restart the configuration process from the very beginning. This feature is designed to address any potential power-sequencing issues that may occur between the iCE65 device and the external PROM.

The iCE65 device attempts to reconfigure six times. If not successful after six attempts, the iCE65 FPGA automatically goes into low-power mode.

SPI Peripheral Configuration Interface

Using the SPI peripheral configuration interface, an application processor (AP) serially writes a configuration image to an iCE65 FPGA using the iCE65's SPI interface, as shown in Figure 23. The iCE65's SPI configuration interface is a separate, independent I/O bank, powered by the VCC_SPI supply input. Typically, VCC_SPI is the same voltage as the application processor's I/O. The configuration control signals, CDONE and CRESET_B, are supplied by the separate I/O Bank 2 voltage input, VCCIO_2.

This same SPI peripheral interface supports programming for the iCE65's Nonvolatile Configuration Memory (NVCM).

Ball Function	Ball Number	Pin Type	Bank
PIO3	B1	PIO	3
PIO3	B2	PIO	3
PIO3	B3	PIO	3
PIO3	C1	PIO	3
PIO3	C2	PIO	3
PIO3	C3	PIO	3
GBIN7/PIO3	D1	GBIN	3
PIO3	D2	PIO	3
PIO3	D3	PIO	3
GBIN6/PIO3	E1	GBIN	3
PIO3	E2	PIO	3
PIO3	E3	PIO	3
PIO3	F2	PIO	3
PIO3	F3	PIO	3
PIO3	G1	PIO	3
PIO3	G2	PIO	3
PIO3	H1	PIO	3
PIO3	H2	PIO	3
VCCIO_3	F1	VCCIO	3
PIOS/SPI_SO	H7	SPI	SPI
PIOS/SPI_SI	J7	SPI	SPI
PIOS/SPI_SCK	J8	SPI	SPI
PIOS/SPI_SS_B	H8	SPI	SPI
SPI_VCC	H9	SPI	SPI
GND	A1	GND	GND
GND	A9	GND	GND
GND	J9	GND	GND
GND	J1	GND	GND
GND	E4	GND	GND
GND	E5	GND	GND
GND	F4	GND	GND
GND	F5	GND	GND
VCC	A5	VCC	VCC
VCC	J5	VCC	VCC
VPP_2V5	B9	VPP	VPP

Ball Function	Ball Number	Pin Type	Bank
PIO0	A5	PIO	0
PIO0	A6	PIO	0
PIO0	A8	PIO	0
PIO0	A10	PIO	0
PIO0	B3	PIO	0
PIO0	B4	PIO	0
PIO0	B5	PIO	0
PIO0	B8	PIO	0
PIO0	B9	PIO	0
PIO0	C5	PIO	0
PIO0	C7	PIO	0
PIO0	C8	PIO	0
PIO0	C9	PIO	0
PIO0	D5	PIO	0
PIO0	D7	PIO	0
PIO0	E5	PIO	0
PIO0	E6	PIO	0
PIO0	E7	PIO	0
PIO0	F7	PIO	0
VCCIO_0	B7	VCCIO	0
GBIN2/PIO1	F9	GBIN	1
GBIN3/PIO1	F8	GBIN	1
PIO1	A11	PIO	1
PIO1	B11	PIO	1
PIO1	C11	PIO	1
PIO1	D8	PIO	1
PIO1	D9	PIO	1
PIO1	D10	PIO	1
PIO1	D11	PIO	1
PIO1	E8	PIO	1
PIO1	E9	PIO	1
PIO1	E11	PIO	1
PIO1	F10	PIO	1
PIO1	G7	PIO	1
PIO1	G8	PIO	1
PIO1	G9	PIO	1
PIO1	G10	PIO	1
PIO1	H7	PIO	1
PIO1	H8	PIO	1
PIO1	H9	PIO	1
PIO1	H10	PIO	1
VCCIO_1	E10	VCCIO	1
CDONE	J7	CONFIG	2
CRESET_B	K7	CONFIG	2
GBIN4/PIO2	L8	GBIN	2
GBIN5/PIO2	L9	GBIN	2
PIO2	H4	PIO	2
PIO2	H5	PIO	2
PIO2	H11	PIO	2
PIO2	J4	PIO	2
PIO2	J5	PIO	2

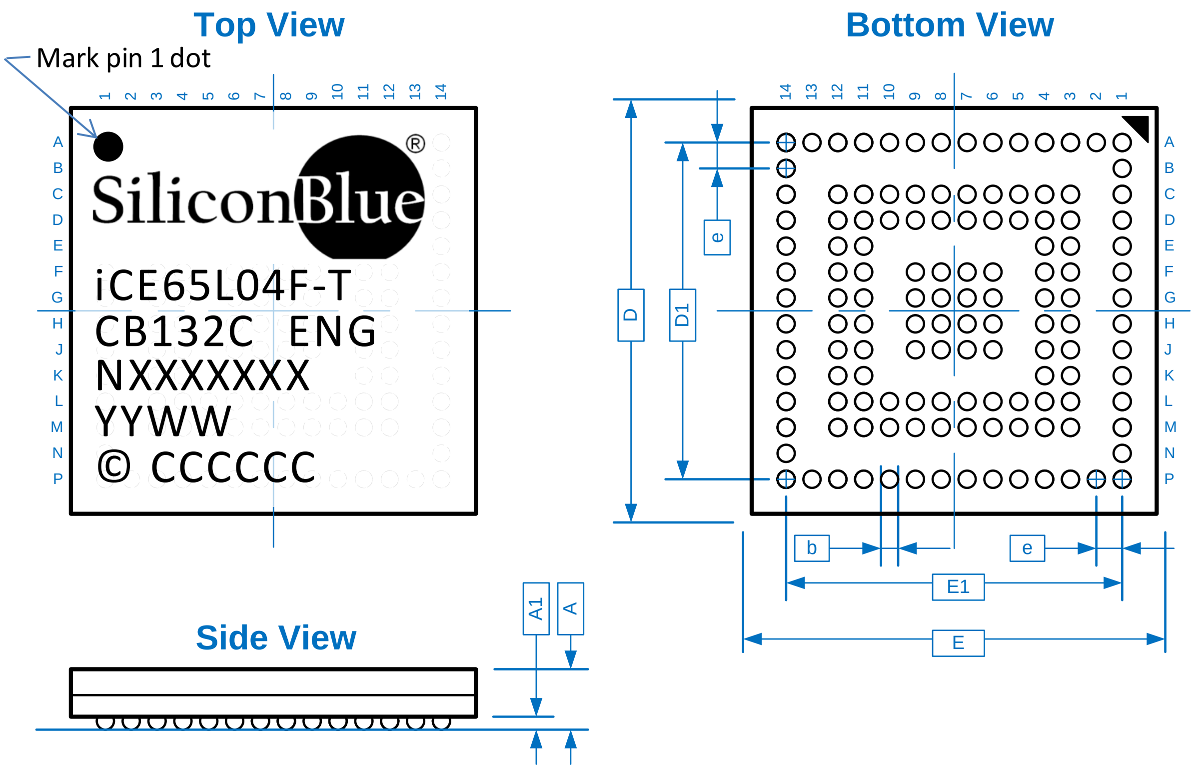
Ball Function	Ball Number	Pin Type	Bank
PIO2	J11	PIO	2
PIO2	K3	PIO	2
PIO2	K4	PIO	2
PIO2	K11	PIO	2
PIO2	L2	PIO	2
PIO2	L3	PIO	2
PIO2	L4	PIO	2
PIO2	L5	PIO	2
PIO2	L10	PIO	2
PIO2	L11	PIO	2
PIO2/CBSEL0	H6	PIO	2
PIO2/CBSEL1	J6	PIO	2
VCCIO_2	K5	VCCIO	2
PIO3	C1	PIO	3
PIO3	B1	PIO	3
PIO3	D1	PIO	3
PIO3	E2	PIO	3
PIO3	C2	PIO	3
PIO3	D2	PIO	3
PIO3	C3	PIO	3
PIO3	C4	PIO	3
PIO3	E4	PIO	3
PIO3	D4	PIO	3
PIO3	F3	PIO	3
PIO3	G3	PIO	3
PIO3	G4	PIO	3
GBIN6/PIO3	F4	GBIN	3
GBIN7/PIO3	D3	GBIN	3
PIO3	E3	PIO	3
PIO3	F2	PIO	3
PIO3	G1	PIO	3
PIO3	H1	PIO	3
PIO3	J1	PIO	3
PIO3	H2	PIO	3
PIO3	H3	PIO	3
PIO3	J3	PIO	3
PIO3	J2	PIO	3
VCCIO_3	A1	VCCIO	3
VCCIO_3	G2	VCCIO	3
PIOS/SPI_SO	J8	SPI	SPI
PIOS/SPI_SI	K8	SPI	SPI
PIOS/SPI_SCK	K9	SPI	SPI
PIOS/SPI_SS_B	J9	SPI	SPI
SPI_VCC	J10	SPI	SPI
GND	B2	GND	GND
GND	B10	GND	GND
GND	E1	GND	GND
GND	F5	GND	GND
GND	F6	GND	GND
GND	G5	GND	GND
GND	G6	GND	GND
GND	G11	GND	GND

Ball Function	Ball Number	Pin Type	Bank
PIO1	H12	PIO	1
PIO1	J11	PIO	1
PIO1	J12	PIO	1
PIO1	K11	PIO	1
PIO1	K12	PIO	1
PIO1	K14	PIO	1
PIO1	L14	PIO	1
TCK	L12	JTAG	1
TDI	M12	JTAG	1
TDO	N14	JTAG	1
TMS	P14	JTAG	1
TRST_B	M14	JTAG	1
VCCIO_1	F9	VCCIO	1
VCCIO_1	H14	VCCIO	1
CDONE	M10	CONFIG	2
CRESET_B	L10	CONFIG	2
GBIN4/PIO2	P8	GBIN	2
GBIN5/PIO2	P7	GBIN	2
PIO2	L4	PIO	2
PIO2	L5	PIO	2
PIO2	L6	PIO	2
PIO2	L7	PIO	2
PIO2	L8	PIO	2
PIO2	M3	PIO	2
PIO2	M4	PIO	2
PIO2	M6	PIO	2
PIO2	M7	PIO	2
PIO2	M8	PIO	2
PIO2	M9	PIO	2
PIO2	P2	PIO	2
PIO2	P3	PIO	2
PIO2	P4	PIO	2
PIO2	P5	PIO	2
PIO2	P9	PIO	2
PIO2/CBSEL0	L9	PIO	2
PIO2/CBSEL1	P10	PIO	2
VCCIO_2	J9	PIO	2
VCCIO_2	M5	PIO	2
PIO3/DP00A	B1	DPIO	3
PIO3/DP00B	C1	DPIO	3
PIO3/DP01A	C3	DPIO	3
PIO3/DP01B	D3	DPIO	3
PIO3/DP02A	D4	DPIO	3
PIO3/DP02B	E4	DPIO	3
PIO3/DP03A	D1	DPIO	3
PIO3/DP03B	E1	DPIO	3
PIO3/DP04A	F4	DPIO	3
PIO3/DP04B	F3	DPIO	3
L01/L04: GBIN6/PIO3 **L08: GBIN6/DP06A**	H1	GBIN	3

Package Mechanical Drawing

Figure 44: CB132 Package Mechanical Drawing

CB132: 8 x 8 mm, 132-ball, 0.5 mm ball-pitch, chip-scale ball grid array



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			14		Columns
Number of Ball Rows	Y			14		Rows
Number of Signal Balls		n		132		Balls
Body Size	X	E	7.90	8.00	8.10	mm
	Y	D	7.90	8.00	8.10	
Ball Pitch		e	—	0.50	—	
Ball Diameter		b	0.27	—	0.37	
Edge Ball Center to Center	X	E1	—	6.50	—	
	Y	D1	—	6.50	—	
Package Height		A	—	—	1.00	
Stand Off		A1	0.16	—	0.26	

Top Marking Format

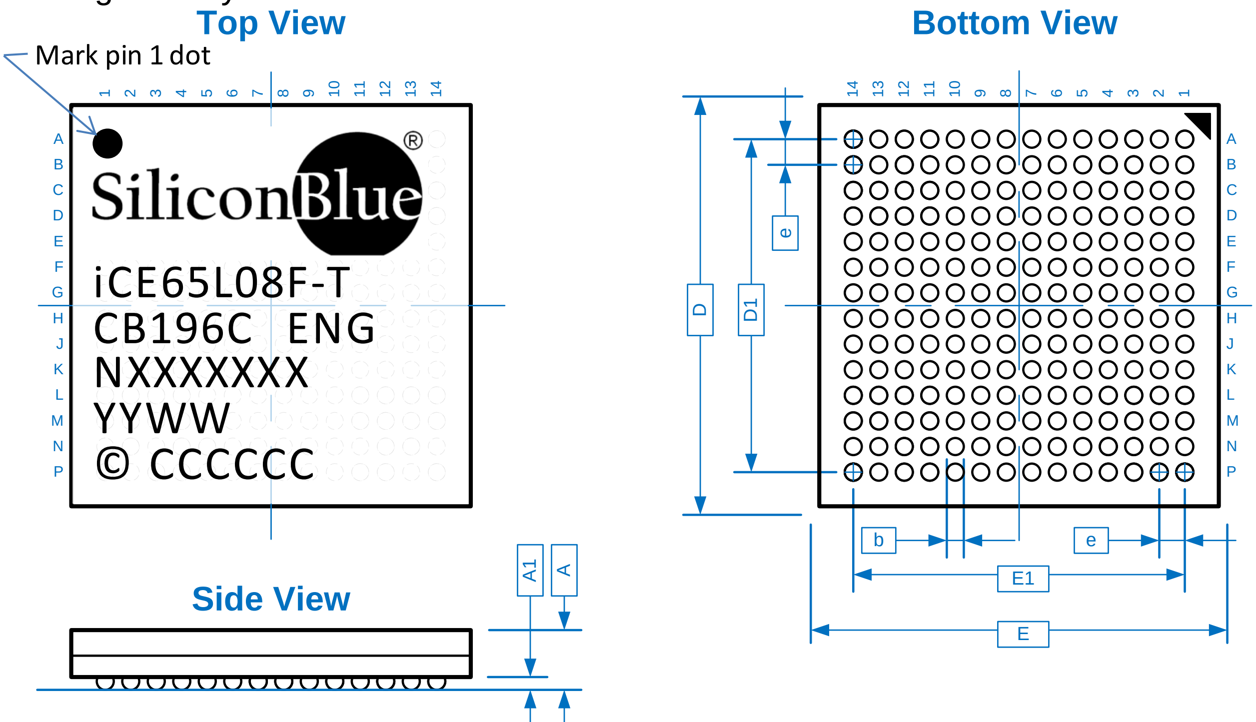
Line	Content	Description
1	Logo	Logo
2	iCE65L04F	Part number
	-T	Power/Speed
3	CB132C	Package type
	ENG	Engineering
4	NXXXXXXX	Lot Number
5	YYWW	Date Code
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
42	34

(b) iCE65L08 CB196 Package Mechanical Drawing

CB196: 8 x8 mm, 196-ball, 0.5 mm ball-pitch, fully-populated, chip-scale ball grid array



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			14		Columns
Number of Ball Rows	Y			14		Rows
Number of Signal Balls		n		196		Balls
Body Size	X	E	7.90	8.00	8.10	mm
	Y	D	7.90	8.00	8.10	
Ball Pitch		e	—	0.50	—	
Ball Diameter		b	0.27	—	0.37	
Edge Ball Center to Center	X	E1	—	6.50	—	
	Y	D1	—	6.50	—	
Package Height		A	—	—	1.00	
Stand Off		A1	0.16	—	0.26	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65L08F	Part number
	-T	Power/Speed
3	CB196C	Package type
	ENG	Engineering
4	NXXXXXXX	Lot Number
5	YYWW	Date Code
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
42	34

Ball Function	Ball Number iCE65L04 iCE65L08	Pin Type by Device iCE65L04	iCE65L08	Bank	CB132 Ball Equivalent
PIO2	T13	PIO	PIO	2	M9
PIO2	V6	PIO	PIO	2	P2
PIO2	V7	PIO	PIO	2	P3
PIO2	V8	PIO	PIO	2	P4
PIO2	V9	PIO	PIO	2	P5
PIO2	V13	PIO	PIO	2	P9
PIO2	Y4	PIO	PIO	2	—
PIO2	Y5	PIO	PIO	2	—
PIO2	Y6	PIO	PIO	2	—
PIO2	Y7	PIO	PIO	2	—
PIO2	Y9	PIO	PIO	2	—
PIO2	Y10	PIO	PIO	2	—
PIO2	Y13	PIO	PIO	2	—
PIO2	Y14	PIO	PIO	2	—
PIO2	Y15	PIO	PIO	2	—
PIO2	Y17	PIO	PIO	2	—
PIO2	Y18	PIO	PIO	2	—
PIO2	Y19	PIO	PIO	2	—
PIO2	Y20	PIO	PIO	2	—
PIO2	AB2	PIO	PIO	2	—
PIO2 (●)	AB3	N.C.	PIO	2	—
PIO2 (●)	AB4	N.C.	PIO	2	—
PIO2	AB6	PIO	PIO	2	—
PIO2	AB7	PIO	PIO	2	—
PIO2	AB8	PIO	PIO	2	—
PIO2	AB9	PIO	PIO	2	—
PIO2	AB10	PIO	PIO	2	—
PIO2	AB11	PIO	PIO	2	—
PIO2	AB12	PIO	PIO	2	—
PIO2	AB13	PIO	PIO	2	—
PIO2	AB14	PIO	PIO	2	—
PIO2	AB15	PIO	PIO	2	—
PIO2 (●)	AB16	N.C.	PIO	2	—
PIO2 (●)	AB17	N.C.	PIO	2	—
PIO2 (●)	AB18	N.C.	PIO	2	—
PIO2 (●)	AB19	N.C.	PIO	2	—
PIO2 (●)	AB20	N.C.	PIO	2	—
PIO2 (●)	AB21	N.C.	PIO	2	—
PIO2 (●)	AB22	N.C.	PIO	2	—
PIO2/CBSEL0	R13	PIO	PIO	2	L9
PIO2/CBSEL1	V14	PIO	PIO	2	P10
VCCIO_2	N13	VCCIO	VCCIO	2	J9
VCCIO_2	T9	VCCIO	VCCIO	2	M5
VCCIO_2	Y11	VCCIO	VCCIO	2	—
PIO3/DP00A	F5	DPIO	DPIO	3	B1
PIO3/DP00B	G5	DPIO	DPIO	3	C1
PIO3/DP01A	G7	DPIO	DPIO	3	C3
PIO3/DP01B	H7	DPIO	DPIO	3	D3
PIO3/DP02A	H8	DPIO	DPIO	3	D4
PIO3/DP02B	J8	DPIO	DPIO	3	E4

iCE65L08

Table 46 lists all the pads on the iCE65L08 die and how these pads connect to the balls or pins in the supported package styles. Most VCC, VCCIO, and GND pads are double-bonded inside the package although the table shows only a single connection.

For additional information on the iCE65L08 DiePlus product, please refer to the following data sheet.

- DiePlusAdvantage FPGA Known Good Die

Table 46: iCE65L08 Die Cross Reference

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO3_00/DP00A	—	B1	1	129.735	3,882.665
PIO3_01/DP00B	—	C1	2	231.735	3,837.665
PIO3_02/DP01A	C1	F5	3	129.735	3,792.665
PIO3_03/DP01B	B1	G5	4	231.735	3,747.665
GND	C2	K5	5	129.735	3,702.665
GND	—	—	6	231.735	3,657.665
VCCIO_3	E3	J7	7	129.735	3,612.665
VCCIO_3	—	—	8	231.735	3,567.665
PIO3_04/DP02A	D3	E3	9	129.735	3,512.665
PIO3_05/DP02B	C3	F3	10	231.735	3,477.665
PIO3_06/DP03A	D1	G3	11	129.735	3,442.665
PIO3_07/DP03B	D2	H3	12	231.735	3,407.665
VCC	F2	D3	13	129.735	3,372.665
VCC	—	—	14	231.735	3,337.665
PIO3_08/DP04A	D4	D1	15	129.735	3,302.665
PIO3_09/DP04B	E4	E1	16	231.735	3,267.665
PIO3_10/DP05A	—	H1	17	129.735	3,232.665
PIO3_11/DP05B	—	J1	18	231.735	3,197.665
GND	F1	M10	19	129.735	3,162.665
GND	—	—	20	231.735	3,127.665
PIO3_12/DP06A	E2	H5	21	129.735	3,092.665
PIO3_13/DP06B	E1	J5	22	231.735	3,057.665
GND	L3	J3	23	129.735	3,022.665
GND	—	—	24	231.735	2,987.665
PIO3_14/DP07A	F5	K1	25	129.735	2,952.665
PIO3_15/DP07B	E5	L1	26	231.735	2,917.665
VCCIO_3	E3	K3	27	129.735	2,882.665
VCCIO_3	—	—	28	231.735	2,847.665
VCC	G6	L10	29	129.735	2,812.665
VCC	—	—	30	231.735	2,777.665
PIO3_16/DP08A	F4	G7	31	129.735	2,742.665
PIO3_17/DP08B	F3	H7	32	231.735	2,707.665
VCCIO_3	K1	F1	33	129.735	2,672.665
VCCIO_3	—	—	34	231.735	2,637.665
GND	—	G1	35	129.735	2,602.665
GND	—	—	36	231.735	2,567.665
PIO3_18/DP09A	G3	K8	37	129.735	2,532.665
PIO3_19/DP09B	G4	K7	38	231.735	2,497.665

iCE65L08 Pad Name	Available Packages CB196	Available Packages CB284	DiePlus Pad	DiePlus X (µm)	DiePlus Y (µm)
TDI	M12	T16	177	4,470.5	634.615
TMS	P14	V18	178	4,572.5	684.615
TCK	L12	R16	179	4,470.5	734.615
TDO	N14	U18	180	4,572.5	784.615
TRST_B	M14	T18	181	4,470.5	834.615
PIO1_00	M13	R18	182	4,572.5	884.615
PIO1_01	K11	P16	183	4,470.5	934.615
PIO1_02	L13	P15	184	4,572.5	984.615
PIO1_03	L14	P18	185	4,470.5	1,034.615
GND	G9	N18	186	4,572.5	1,084.615
GND	—	—	187	4,470.5	1,134.615
PIO1_04	J11	N16	188	4,572.5	1,184.615
PIO1_05	K12	N15	189	4,470.5	1,234.62
VCCIO_1	F9	M18	190	4,572.5	1,287.115
VCCIO_1	—	—	191	4,470.5	1,322.115
PIO1_06	J12	M15	192	4,572.5	1,357.115
PIO1_07	K14	M16	193	4,470.5	1,392.115
PIO1_08	—	T20	194	4,572.5	1,427.115
PIO1_09	—	W20	195	4,470.5	1,462.115
PIO1_10	—	V20	196	4,572.5	1,497.115
VCC	H9	M13	197	4,470.5	1,532.115
VCC	—	—	198	4,572.5	1,567.115
PIO1_11	—	R20	199	4,470.5	1,602.115
PIO1_12	—	Y22	200	4,572.5	1,637.115
PIO1_13	—	AA22	201	4,470.5	1,672.115
PIO1_14	—	U20	202	4,572.5	1,707.115
PIO1_15	J13	W22	203	4,470.5	1,742.115
PIO1_16	H11	P20	204	4,572.5	1,777.115
PIO1_17	J10	V22	205	4,470.5	1,812.115
PIO1_18	H12	U22	206	4,572.5	1,847.115
GND	K10	N20	207	4,470.5	1,882.115
GND	—	—	208	4,572.5	1,917.110
PIO1_19	H13	T22	209	4,470.5	1,952.115
PIO1_20	—	M20	210	4,572.5	1,987.115
PIO1_21	H10	R22	211	4,470.5	2,022.115
PIO1_22	—	P22	212	4,572.5	2,057.115
VCCIO_1	F9	J20	213	4,470.5	2,092.115
VCCIO_1	—	—	214	4,572.5	2,127.115
PIO1_23	G10	M22	215	4,470.5	2,162.115
PIO1_24	G11	N22	216	4,572.5	2,197.115
PIO1_25	—	K22	217	4,470.5	2,232.115
PIO1_26	—	L22	218	4,572.5	2,267.115
GBIN3/PIO1_27	G12	K18	219	4,470.5	2,302.11
GBIN2/PIO1_28	F10	L18	220	4,572.5	2,337.115
PIO1_29	—	J22	221	4,470.5	2,372.115

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
GND	F7	E13	270	3,216.98	4,054.5
GND	—	—	271	3,166.98	4,156.5
PIO0_08	D9	E15	272	3,116.98	4,054.5
PIO0_09	C10	G14	273	3,064.48	4,156.5
PIO0_10	A10	A20	274	3,029.48	4,054.5
PIO0_11	B10	H13	275	2,994.48	4,156.5
PIO0_12	—	A19	276	2,959.48	4,054.5
PIO0_13	E9	G13	277	2,924.48	4,156.5
PIO0_14	—	C16	278	2,889.48	4,054.5
PIO0_15	—	E14	279	2,854.48	4,156.5
VCCIO_0	F6	E12	280	2,819.48	4,054.5
VCCIO_0	—	—	281	2,784.48	4,156.5
PIO0_16	—	A18	282	2,749.48	4,054.5
PIO0_17	—	A17	283	2,714.48	4,156.5
PIO0_18	C9	C15	284	2,679.48	4,054.5
PIO0_19	—	A16	285	2,644.48	4,156.5
PIO0_20	B9	C14	286	2,609.48	4,054.5
PIO0_21	—	H12	287	2,574.48	4,156.5
PIO0_22	D8	A15	288	2,539.48	4,054.5
PIO0_23	C8	H11	289	2,504.48	4,156.5
PIO0_24	E8	C13	290	2,469.48	4,054.5
PIO0_25	—	A14	291	2,434.48	4,156.5
GND	B12	C12	292	2,399.48	4,054.5
GND	—	—	293	2,364.48	4,156.5
PIO0_26	B8	A13	294	2,329.48	4,054.5
PIO0_27	D7	A12	295	2,294.48	4,156.5
PIO0_28	—	C11	296	2,259.48	4,054.5
GBIN1/PIO0_29	E7	E11	297	2,224.48	4,156.5
GBIN0/PIO0_30	A7	E10	298	2,189.48	4,054.5
PIO0_31	—	G12	299	2,154.48	4,156.5
VCCIO_0	A8	A8	300	2,119.48	4,054.5
VCCIO_0	—	—	301	2,084.48	4,156.5
PIO0_32	C7	A11	302	2,049.48	4,054.5
PIO0_33	—	G11	303	2,014.48	4,156.5
PIO0_34	E6	A10	304	1,979.48	4,054.5
PIO0_35	—	C10	305	1,944.48	4,156.5
VCC	B7	C8	306	1,909.48	4,054.5
VCC	—	—	307	1,874.48	4,156.5
PIO0_36	—	A9	308	1,839.48	4,054.5
PIO0_37	A6	A7	309	1,804.48	4,156.5
PIO0_38	B6	C9	310	1,769.48	4,054.5
PIO0_39	A5	A6	311	1,734.48	4,156.5
GND	G7	K11	312	1,699.48	4,054.5
GND	—	—	313	1,664.48	4,156.5
PIO0_40	D6	E9	314	1,629.48	4,054.5
PIO0_41	C6	G10	315	1,594.48	4,156.5

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO0_42	C5	A5	316	1,559.48	4,054.5
PIO0_43	B5	G9	317	1,524.48	4,156.5
PIO0_44	A4	A3	318	1,489.48	4,054.5
PIO0_45	—	A4	319	1,454.48	4,156.5
PIO0_46	—	A2	320	1,419.48	4,054.5
PIO0_47	—	C7	321	1,384.48	4,156.5
PIO0_48	—	C6	322	1,331.98	4,054.5
VCCIO_0	A8	K10	323	1,281.98	4,156.5
VCCIO_0	—	—	324	1,231.98	4,054.5
PIO0_49	—	E8	325	1,181.98	4,156.5
PIO0_50	B4	A1	326	1,131.98	4,054.5
PIO0_51	C4	E7	327	1,081.98	4,156.5
PIO0_52	A3	C5	328	1,031.98	4,054.5
PIO0_53	B3	E6	329	981.98	4,156.5
PIO0_54	D5	C3	330	931.98	4,054.5
GND	A9	L11	331	881.98	4,156.5
GND	—	—	332	831.98	4,054.5
PIO0_55	B2	G8	333	781.98	4,156.5
PIO0_56	A2	C4	334	731.98	4,054.5
PIO0_57	A1	H10	335	681.98	4,156.5
PIO0_58	—	E5	336	631.98	4,054.5
PIO0_59	—	H9	337	581.98	4,156.5

AC Timing Guidelines

The following examples provide some guidelines of device performance. The actual performance depends on the specific application and how it is physically implemented in the iCE65 FPGA using the Lattice iCEcube software. The following guidelines assume typical conditions (VCC = 1.0 V or 1.2 V as specified, temperature = 25 °C). Apply derating factors using the iCEcube timing analyzer to adjust to other operating regimes.

Programmable Logic Block (PLB) Timing

Table 54 provides timing information for the logic in a Programmable Logic Block (PLB), which includes the paths shown in Figure 55 and Figure 56.

Figure 55 PLB Sequential Timing Circuit

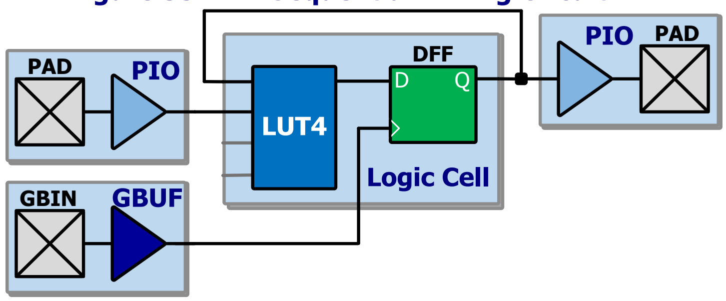


Figure 56 **PLB Combinational Timing Circuit**

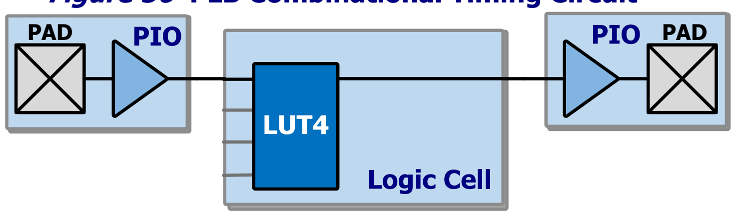


Table 54: **Typical Programmable Logic Block (PLB) Timing**

Symbol	From	To	Device: iCE65 / Power/Speed Grade / Nominal VCC / Description	L01 –T 1.2 V Typ.	L04, L08 –L 1.0 V Typ.	L04, L08 –L 1.2 V Typ.	L04, L08 –T 1.2 V Typ.	Units
		Sequential Logic Paths						
F_{TOGGLE}	GBIN input	GBIN input	Flip-flop toggle frequency. DFF flip-flop output fed back to LUT4 input with 4-input XOR, clocked on same clock edge.	256	224	256	256	MHz
t_{CKO}	DFF clock input	PIO output	Logic cell flip-flop (DFF) clock-to-output time, measured from the DFF CLK input to PIO output, including interconnect delay.	5.4	16.5	8.7	7.1	ns
t_{GBCKLC}	GBIN input	DFF clock input	Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to clock input on the logic cell DFF flip-flop.	2.2	7.3	3.8	2.7	ns
t_{SULI}	PIO input	GBIN input	Minimum setup time on PIO input, through LUT4, to DFF flip-flop D-input before active clock edge on the GBIN input, including interconnect delay.	1.0	4.0	2.1	1.2	ns
t_{HDLI}	GBIN input	PIO input	Minimum hold time on PIO input, through LUT4, to DFF flip-flop D-input after active clock edge on the GBIN input, including interconnect delay.	0	0	0	0	ns
		Combinational Logic Paths						
t_{LUT4IN}	PIO input	LUT4 input	Asynchronous delay from PIO input pad to adjacent PLB interconnect.	2.6	9.8	5.2	3.3	ns
t_{ILO}	LUT4 input	LUT4 output	Logic cell LUT4 combinational logic propagation delay, regardless of logic complexity from input to output.	0.6	1.9	1.0	0.6	ns
t_{LUT4IN}	LUT4 output	PIO output	Asynchronous delay from adjacent PLB interconnect to PIO output pad.	4.9	16.0	8.4	6.6	ns

Programmable Input/Output (PIO) Block

Table 55 provides timing information for the logic in a Programmable Logic Block (PLB), which includes the paths shown in Figure 57 and Figure 58. The timing shown is for the LVCMOS25 I/O standard in all I/O banks. The iCEcube development software reports timing adjustments for other I/O standards.

***Figure 57:* Programmable I/O (PIO) Pad-to-Pad Timing Circuit**

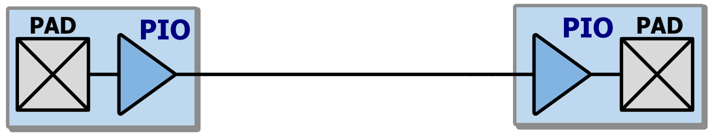


***Figure 58:* Programmable I/O (PIO) Sequential Timing Circuit**

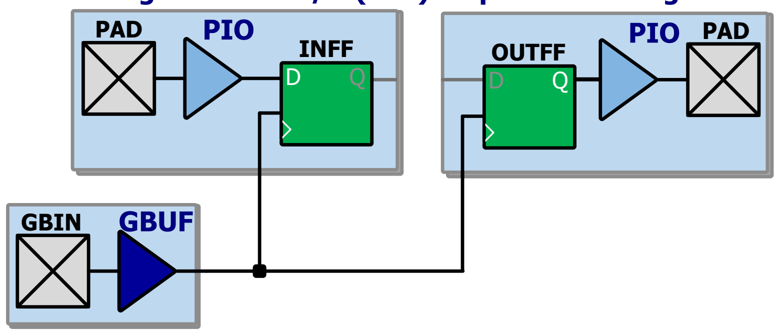


***Table 55:* Typical Programmable Input/Output (PIO) Timing (LVCMOS25)**

			Device: iCE65	L01	L04, L08			
			Power/Speed Grad	–T	–L		–T	
			Nominal VCC	1.2 V	1.0 V	1.2 V	1.2 V	
Symbol	**From**	**To**	**Description**	**Typ.**	**Typ.**	**Typ.**	**Typ.**	**Units**
		Synchronous Output Paths						
t_{OCKO}	OUTFF clock input	PIO output	Delay from clock input on OUTFF output flip-flop to PIO output pad.	4.7	13.8	7.3	5.6	ns
t_{GBCKIO}	GBIN input	OUTFF clock input	Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to clock input on the PIO OUTFF output flip-flop.	2.1	7.3	3.8	2.6	ns
		Synchronous Input Paths						
t_{SUPDIN}	PIO input	GBIN input	Setup time on PIO input pin to INFF input flip-flop before active clock edge on GBIN input, including interconnect delay.	0	0	0	0	ns
t_{HDPDIN}	GBIN input	PIO input	Hold time on PIO input to INFF input flip-flop after active clock edge on the GBIN input, including interconnect delay.	2.7	7.1	3.6	2.8	ns
		Pad to Pad						
t_{PADIN}	PIO input	Inter-connect	Asynchronous delay from PIO input pad to adjacent interconnect.	2.5	9.5	5.0	3.2	ns
t_{PADO}	Inter-connect	PIO output	Asynchronous delay from adjacent interconnect to PIO output pad including interconnect delay.	4.5	14.6	7.7	6.2	ns