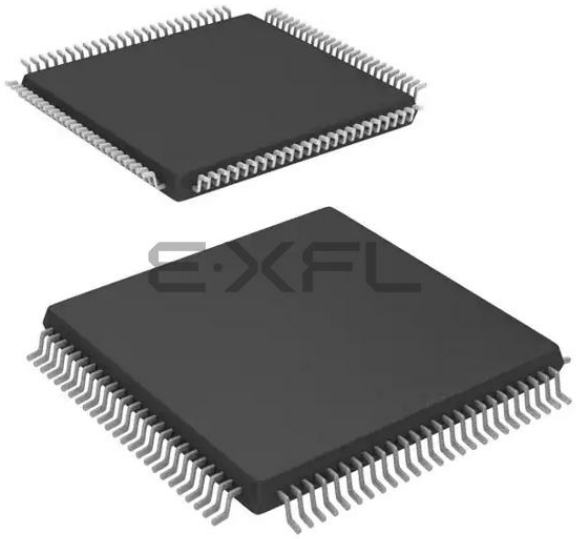
# Lattice Semiconductor Corporation - ICE65L04F-LVQ100C Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

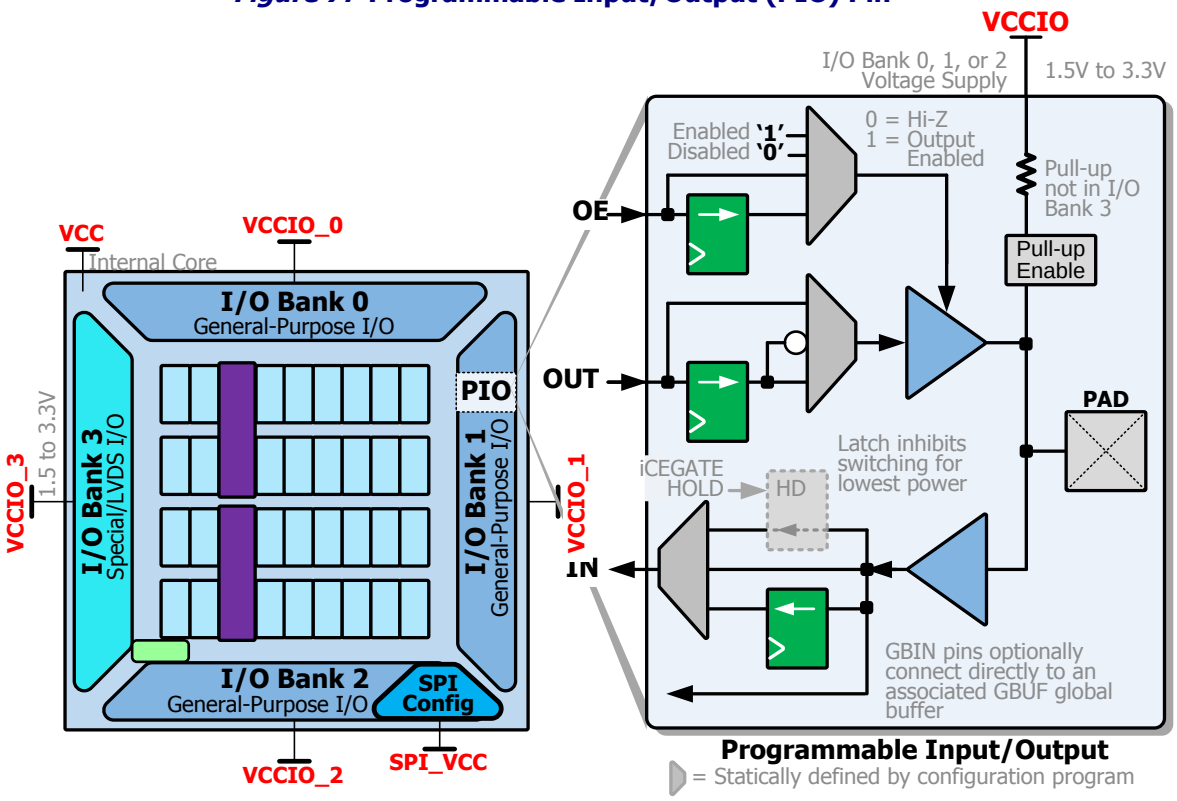
| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 440 |
| Number of Logic Elements/Cells | 3520 |
| Total RAM Bits | 81920 |
| Number of I/O | 72 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-VQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/ice65l04f-lvq100c |

## Programmable Input/Output Block (PIO)

Programmable Input/Output (PIO) blocks surround the periphery of the device and connect external components to the Programmable Logic Blocks (PLBs) and RAM4K blocks via programmable interconnect. Individual PIO pins are grouped into one of four I/O banks, as shown in Figure 7. I/O Bank 3 has additional capabilities, including LVDS differential I/O and the ability to interface to Mobile DDR memories.

Figure 7 also shows the logic within a PIO pin. When used in an application, a PIO pin becomes a signal input, an output, or a bidirectional I/O pin with a separate direction control input.

***Figure 7:*** **Programmable Input/Output (PIO) Pin**




### I/O Banks

PIO blocks are organized into four separate I/O banks, each with its own voltage supply input, as shown in Table 5. The voltage applied to the VCCIO pin on a bank defines the I/O standard used within the bank. Table 50 and Table 51 describe the I/O drive capabilities and switching thresholds by I/O standard. On iCE65L04 and iCE65L08 devices, I/O Bank 3, along the left edge of the die, is different than the others and supports specialized I/O standards.

#### *I/O Bank Voltage Supply Inputs Support Different I/O Standards*

Because each I/O bank has its own voltage supply, iCE65 components become the ideal bridging device between different interface standards. For example, the iCE65 device allows a 1.8V-only processor to interface cleanly with a 3.3V bus interface. The iCE65 device replaces external voltage translators.

**Table 5: Supported Voltages by I/O Bank**

| Bank | Device Edge | Supply Input | 3.3V | 2.5V | 1.8V | 1.5V |
|---|---|---|---|---|---|---|
| **0** | Top | VCCIO_0 | Yes | Yes | Yes | Outputs only |
| **1** | Right | VCCIO_1 | Yes | Yes | Yes | Outputs only |
| **2** | Bottom | VCCIO_2 | Yes | Yes | Yes | Outputs only |
| **3** | Left | VCCIO_3 | Yes | Yes | Yes | iCE65L01: Outputs only<br>iCE65L04/08: Yes |
| **SPI** | Bottom Right | SPI_VCC | Yes | Yes | Yes | No |

If not connected to an external SPI PROM, the four pins associated with the SPI Master Configuration Interface can be used as PIO pins, supplied by the SPI_VCC input, essentially forming a fifth "mini" I/O bank. If using an SPI Flash PROM, then connect SPI_VCC to 3.3V.

### I/O Banks 0, 1, 2, SPI and Bank 3 of iCE65L01

Table 6 highlights the available I/O standards when using an iCE65 device, indicating the drive current options, and in which bank(s) the standard is supported. I/O Banks 0, 1, 2 and SPI interface support the same standards. I/O Bank 3 has additional capabilities in iCE65L04 and iCE65L08, including support for MDDR memory standards and LVDS differential I/O.

***Table 6:* I/O Standards for I/O Banks 0, 1, 2, SPI Interface Bank, and Bank 3 of iCE65L01**

| I/O Standard | Supply Voltage | Drive Current (mA) | Attribute Name |
|---|---|---|---|
| 5V Input Tolerance | 3.3V | N/A | N/A |
| LVCMOS33 | 3.3V | ±11 | SB_LVCMOS |
| LVCMOS25 | 2.5V | ±8 | |
| LVCMOS18 | 1.8V | ±5 | |
| LVCMOS15 outputs | 1.5V | ±4 | |

#### *IBIS Models for I/O Banks 0, 1, 2 and the SPI Bank*

The IBIS (I/O Buffer Information Specification) file that describes the output buffers used in I/O Banks 0, 1, 2, SPI Bank and Bank 3 of iCE65L01 is available from the following link.

- IBIS Models for I/O Banks 0, 1, 2, SPI Bank and Bank 3 of iCE65L01

### I/O Bank 3 of iCE65L04 and iCE65L08

I/O Bank 3, located along the left edge of the die, has additional special I/O capabilities to support memory components and differential I/O signaling (LVDS). Table 7 lists the various I/O standards supported by I/O Bank 3. The SSTL2 and SSTL18 I/O standards require the VREF voltage reference input pin which is only available on the CB284 package. Also see Table 51 for electrical characteristics.

***Table 7:* I/O Standards for I/O Bank 3 Only of iCE65L04 and iCE65L08**

| I/O Standard | Supply Voltage | VREF Pin (CB284 or DiePlus) Required? | Target Drive Current (mA) | Attribute Name |
|---|---|---|---|---|
| LVCMOS33 | 3.3V | No | ±8 | SB_LVCMOS33_8 |
| LVCMOS25 | 2.5V | No | ±16 | SB_LVCMOS25_16 |
| | | | ±12 | SB_LVCMOS25_12 |
| | | | ±8 | SB_LVCMOS25_8 |
| | | | ±4 | SB_LVCMOS25_4 |
| LVCMOS18 | 1.8V | No | ±10 | SB_LVCMOS18_10 |
| | | | ±8 | SB_LVCMOS18_8 |
| | | | ±4 | SB_LVCMOS18_4 |
| | | | ±2 | SB_LVCMOS18_2 |
| LVCMOS15 | 1.5V | No | ±4 | SB_LVCMOS15_4 |
| | | | ±2 | SB_LVCMOS15_2 |
| SSTL2_II | 2.5V | Yes | ±16.2 | SB_SSTL2_CLASS_2 |
| SSTL2_I | | | ±8.1 | SB_SSTL2_CLASS_1 |
| SSTL18_II | 1.8V | Yes | ±13.4 | SB_SSTL18_FULL |
| SSTL18_I | | | ±6.7 | SB_SSTL18_HALF |
| MDDR | 1.8V | No | ±10 | SB_MDDR10 |
| | | | ±8 | SB_MDDR8 |
| | | | ±4 | SB_MDDR4 |
| | | | ±2 | SB_MDDR2 |
| LVDS | 2.5V | No | N/A | SB_LVDS_INPUT |

Table 12 and Table 13 list the connections between a specific global buffer and the inputs on a Programmable I/O (PIO) pair. Although there is no direct connection between a global buffer and a PIO output, such a connection is possible by first connecting through a PLB LUT4 function. Again, all global buffers optionally drive all clock inputs. However, even-numbered global buffers optionally drive the clock-enable input on a PIO pair.

The PIO clock enable connect is different between the iCE65L01/iCE65L04 and iCE65L08.

***Table 12:*** **iCE65L01 & iCE65L04: Global Buffer (GBUF) Connections to Programmable I/O (PIO) Pair**

| Global Buffer | Output Connections | Input Clock | Output Clock | Clock Enable |
|---|---|---|---|---|
| **GBUF0** | No (connect through PLB LUT) | Yes | Yes | No |
| **GBUF1** | | Yes | Yes | Yes |
| **GBUF2** | | Yes | Yes | No |
| **GBUF3** | | Yes | Yes | Yes |
| **GBUF4** | | Yes | Yes | No |
| **GBUF5** | | Yes | Yes | Yes |
| **GBUF6** | | Yes | Yes | No |
| **GBUF7** | | Yes | Yes | Yes |

***Table 13:*** **iCE64L08: Global Buffer (GBUF) Connections to Programmable I/O (PIO) Pair**

| Global Buffer | Output Connections | Input Clock | Output Clock | Clock Enable |
|---|---|---|---|---|
| **GBUF0** | No (connect through PLB LUT) | Yes | Yes | Yes |
| **GBUF1** | | Yes | Yes | No |
| **GBUF2** | | Yes | Yes | Yes |
| **GBUF3** | | Yes | Yes | No |
| **GBUF4** | | Yes | Yes | Yes |
| **GBUF5** | | Yes | Yes | No |
| **GBUF6** | | Yes | Yes | Yes |
| **GBUF7** | | Yes | Yes | No |

### *Global Buffer Inputs*

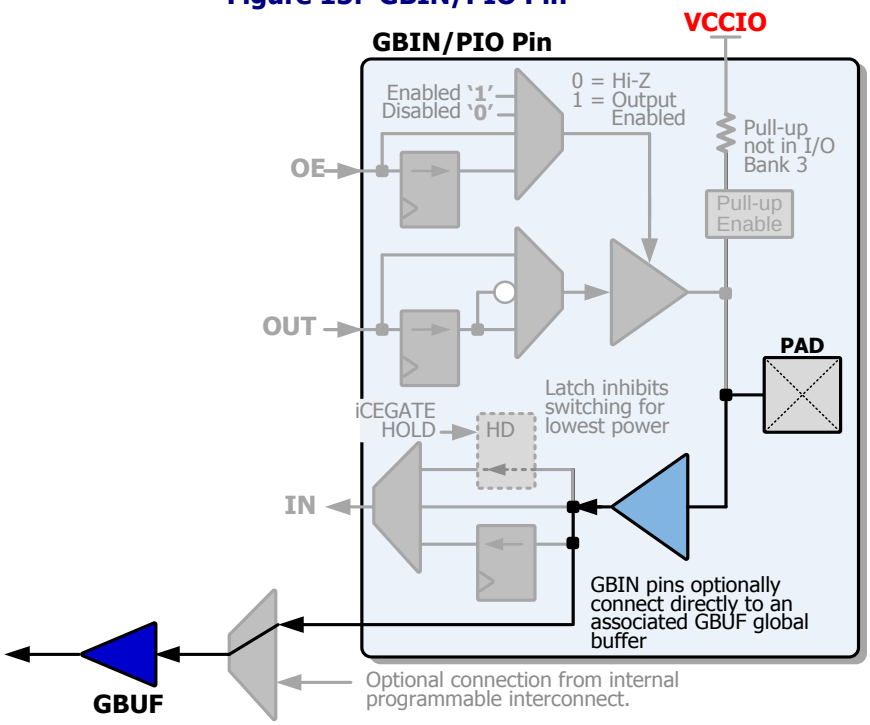
The iCE65 component has eight specialized GBIN/PIO pins that are optionally direct inputs to the global buffers, offering the best overall clock characteristics. As shown in Figure 15, each GBIN/PIO pin is a full-featured I/O pin but also provides a direct connection to its associated global buffer. The direct connection to the global buffer bypasses the iCEgate input-blocking latch and other PIO input logic. These special PIO pins are allocated two to an I/O Bank, a total of eight. These pins are labeled GBIN0 through GBIN7, as shown in Figure 14 and the pin locations for each GBIN input appear in Table 14.

***Table 14:*** **Global Buffer Input Ball/Pin Number by Package**

| Global Buffer Input (GBIN) | I/O Bank | VQ100 | CB132 | 'L04 CB196 | 'L08 CB196 | CB284 |
|---|---|---|---|---|---|---|
| **GBIN0** | 0 | 90 | A6 | A7 | A7 | E10 |
| **GBIN1** | | 89 | A7 | E7 | E7 | E11 |
| **GBIN2** | 1 | 63 | G14 | F10 | F10 | L18 |
| **GBIN3** | | 62 | F14 | G12 | G12 | K18 |
| **GBIN4** | 2 | 34 | P8 | L7 | N8 | V12 |
| **GBIN5** | | 33 | P7 | P5 | M7 | V11 |
| **GBIN6** | 3 | 15 | H1 | H1 | H1 | M5 |
| **GBIN7** | | 13 | G1 | G1 | H3 | L5 |

Note the clock differences between the iCE65L04 and iCE65L08 in the CB196 package.

**Figure 15: GBIN/PIO Pin**




### *Differential Global Buffer Input*

All eight global buffer inputs support single-ended I/O standards such as LVCMOS. Global buffer GBUF7 in I/O Bank 3 also provides an optional direct SubLVDS, LVDS, or LVPECL differential clock input, as shown in Figure 16. The GBIN7 and its associated differential I/O pad accept a differential clock signal. A 100 Ω termination resistor is required across the two pads. Optionally, swap the outputs from the LVDS or LVPECL clock driver to invert the clock as it enters the iCE65 device.

**Figure 16: LVDS or LVPECL Clock Input**

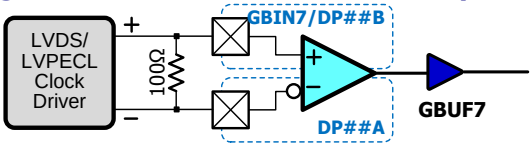



Table 15 lists the pin or ball numbers for the differential global buffer input by package style. Although this differential input is the only one that connects directly to a global buffer, other differential inputs can connect to a global buffer using general-purpose interconnect, with slightly more signal delay.

***Table 15:* Differential Global Buffer Input Ball/Pin Number by Package**

| Differential Global Buffer Input (GBIN) | I/O Bank | VQ100 | CB132 | 'L04 CB196 | 'L08 CB196 | CB284 |
|---|---|---|---|---|---|---|
| **GBIN7/DPxxB** | 3 | 13 | N/A | G1 | H3 | L5 |
| **DPxxA** | | 12 | N/A | G2 | H4 | L3 |

The differential global buffer input is not available for iCE65 devices in the CB132 package. This restriction is an artifact of the pin compatibility between the CB132 and CB284 package.

Note the clock differences between the iCE65L04 and iCE65L08 in the CB196 package.

- For lowest possible power consumption after configuration, the PROM should also support the 0xB9 Deep Power Down command and the 0xAB Release from Deep Power-down Command (see Figure 24 and Figure 26). The low-power mode is optional.
- The PROM must be ready to accept commands 10 µs after meeting its power-on conditions. In the PROM data sheet, this may be specified as $t_{VSL}$ or $t_{VCSL}$. It is possible to use slower PROMs by holding the CRESET_B input Low until the PROM is ready, then releasing CRESET_B, either under program control or using an external power-on reset circuit.

The Lattice iCEman65 development board and associated programming software uses an ST Micro/Numonyx M25Pxx SPI serial Flash PROM.

### SPI PROM Size Requirements

Table 27 lists the minimum SPI PROM size required to configure an iCE65 device. Larger PROM sizes are allowed, but not required unless the end application uses the additional space. SPI serial PROM sizes are specified in bits. For each device size, the table shows the required minimum PROM size for "Logic Only" (no BRAM initialization) and "Logic + RAM4K" (RAM4K blocks pre-initialized). Furthermore, the table shows the PROM size for varying numbers of configuration images. Most applications will use a single image. Applications that use the Cold Boot or Warm Boot features may use more than one image.

**Table 27: Smallest SPI PROM Size (bits), by Device, by Number of Images**

| Device | 1 Image | | 2 Images | | 3 Images | | 4 Images | |
|---|---|---|---|---|---|---|---|---|
| | **Logic Only** | **Logic + RAM4K** | **Logic Only** | **Logic + RAM4K** | **Logic Only** | **Logic + RAM4K** | **Logic Only** | **Logic + RAM4K** |
| **iCE65L01** | 256K | 256K | 512K | 512K | 1M | 1M | 1M | 1M |
| **iCE65L04** | 512K | 1M | 1M | 2M | 2M | 2M | 2M | 4M |
| **iCE65L08** | 1M | 2M | 2M | 4M | 4M | 4M | 4M | 8M |

### Enabling SPI Configuration Interface

To enable the SPI configuration mode, the SPI_SS_B pin must be allowed to float High. The SPI_SS_B pin has an internal pull-up resistor. If SPI_SS_B is Low, then the iCE65 component defaults to the SPI Slave configuration mode.

### SPI Master Configuration Process

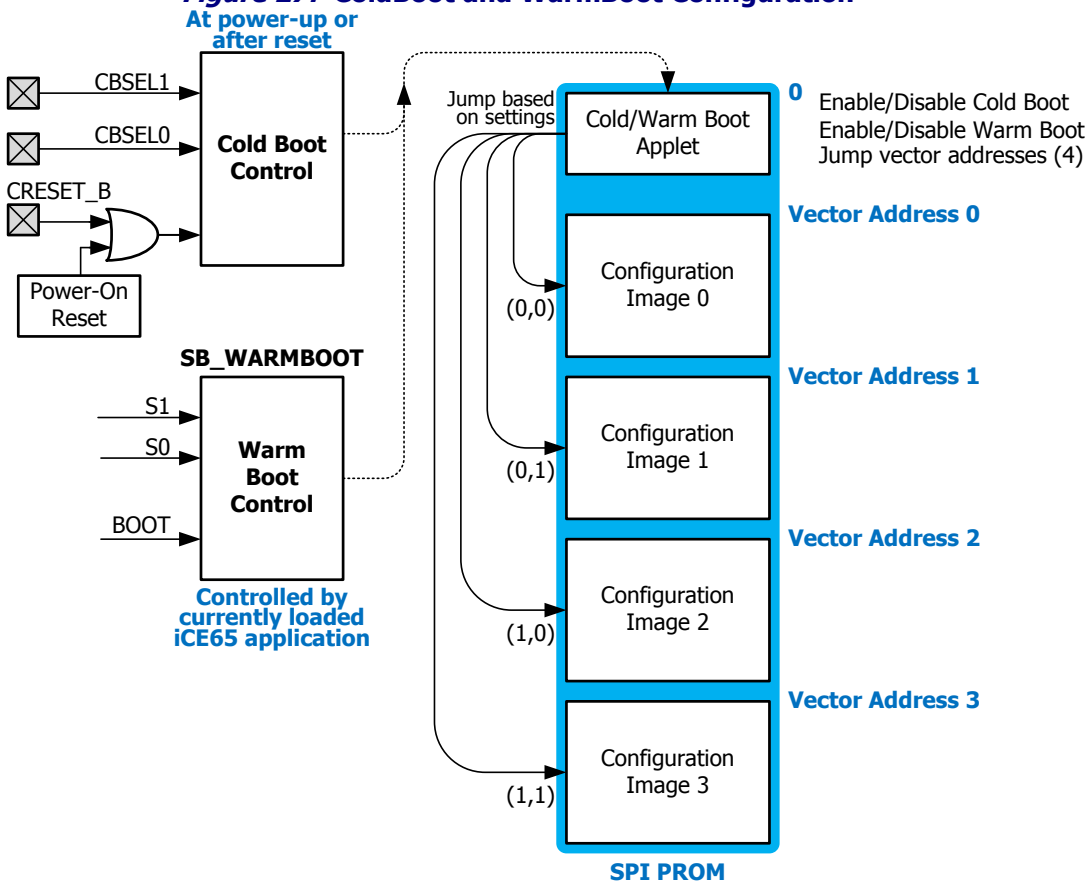
The iCE65 SPI Master Configuration Interface supports a variety of modern, high-density, low-cost SPI serial Flash PROMs. Most modern SPI PROMs include a power-saving Deep Power-down mode. The iCE65 component exploits this mode for additional system power savings.

The iCE65 SPI interface starts by driving SPI_SS_B Low, and then sends a Release from Power-down command to the SPI PROM, hexadecimal command code 0xAB. Figure 24 provides an example waveform. This initial command wakes up the SPI PROM if it is already in Deep Power-down mode. If the PROM is not in Deep Power-down mode, the extra command has no adverse affect other than that it requires a few additional microseconds during the configuration process. The iCE65 device transmits data on the SPI_SO output, on the falling edge of the SPI_SCK output. The SPI PROM does not provide any data to the iCE65 device's SPI_SI input. After sending the last command bit, the iCE65 device de-asserts SPI_SS_B High, completing the command. The iCE65 device then waits a minimum of 10 µS before sending the next SPI PROM command.

## Cold Boot Configuration Option

By default, the iCE65 FPGA is programmed with a single configuration image, either from internal NVCM memory, from an external SPI Flash PROM, or externally from a processor or microcontroller.

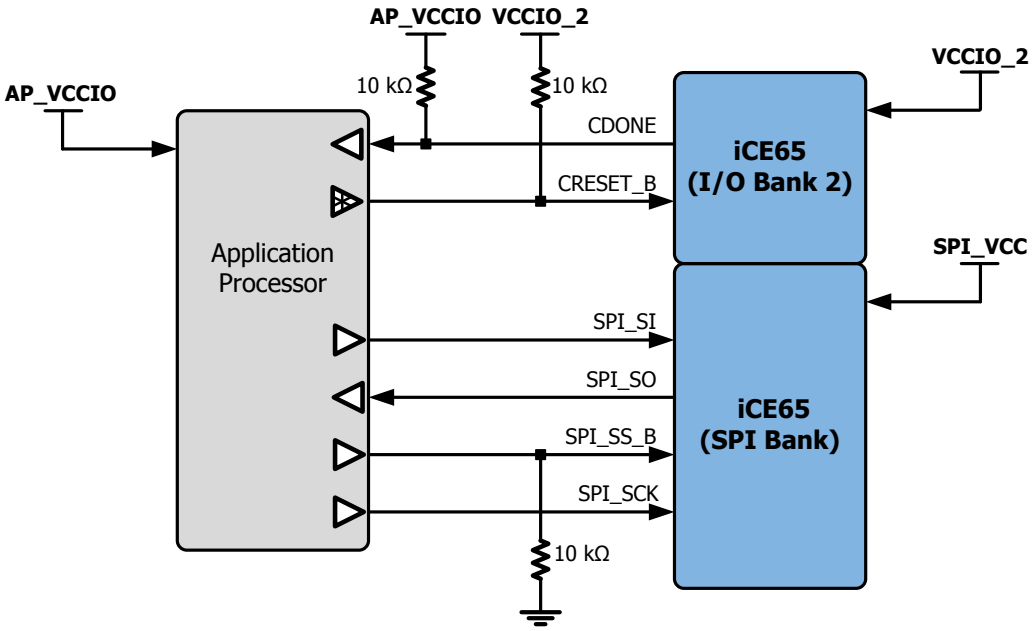
***Figure 27:*** **ColdBoot and WarmBoot Configuration**




When self loading from NVCM or from an SPI Flash PROM, there is an additional configuration option called Cold Boot mode. When this option is enabled in the configuration bitstream, the iCE65 FPGA boots normally from power-on or a master reset (CRESET_B = Low pulse), but monitors the value on two PIO pins that are borrowed during configuration, as shown in Figure 27. These pins, labeled PIO2/CBSEL0 and PIO2/CBSEL1, tell the FPGA which of the four possible SPI configurations to load into the device. Table 30 provides the pin or ball locations for these pins.

- Load from initial location, either from NVCM or from address 0 in SPI Flash PROM. For Cold Boot or Warm Boot applications, the initial configuration image contains the cold boot/warm boot applet.
- Check if Cold Boot configuration feature is enabled in the bitstream.
  - If not enabled, FPGA configures normally.
  - If Cold Boot is enabled, then the FPGA reads the logic values on pins CBSEL[1:0]. The FPGA uses the value as a vector and then reads from the indicated vector address.
  - At the selected CBSEL[1:0] vector address, there is a starting address for the selected configuration image.
    - For SPI Flash PROMs, the new address is a 24-bit start address in Flash.
    - If the selected bitstream is in NVCM, then the address points to the internal NVCM.
- Using the new start address, the FPGA restarts reading configuration memory from the new location.

***Figure 28:*** **iCE65 SPI Peripheral Configuration Interface**




The SPI control signals are defined in Table 25.

***Table 29:*** **SPI Peripheral Configuration Interface Pins (SPI_SS_B Low when CRESET_B Released)**

| Signal Name | Direction | iCE65 I/O Supply | Description |
|---|---|---|---|
| CDONE | AP ← iCE65 | VCCIO_2 | Configuration Done output from iCE65. Connect to a 10kΩ pull-up resistor to the application processor I/O voltage, AP_VCC. |
| CRESET_B | AP → iCE65 | | Configuration Reset input on iCE65. Typically driven by AP using an open-drain driver, which also requires a 10kΩ pull-up resistor to VCCIO_2. |
| SPI_VCC | Supply | SPI_VCC | SPI Flash PROM voltage supply input. |
| SPI_SI | AP → iCE65 | | SPI Serial Input to the iCE65 FPGA, driven by the application processor. |
| SPI_SO | AP ← iCE65 | | SPI Serial Output from CE65 device to the application processor. Not actually used during SPI peripheral mode configuration but required if the SPI interface is also used to program the NVCM. |
| SPI_SS_B | AP → iCE65 | | SPI Slave Select output from the application processor. Active Low. Optionally hold Low prior to configuration using a 10kΩ pull-down resistor to ground. |
| SPI_SCK | AP → iCE65 | | SPI Slave Clock output from the application processor. |

After configuration, the SPI port pins are available to the user-application as additional PIO pins, supplied by the SPI_VCC input voltage, essentially providing a fifth "mini" I/O bank.

### *Enabling SPI Configuration Interface*

The optional 10 kΩ pull-down resistor on the SPI_SS_B signal ensures that the iCE65 FPGA powers up in the SPI peripheral mode. Optionally, the application processor drives the SPI_SS_B pin Low when CRESET_B is released, forcing the iCE65 FPGA into SPI peripheral mode.

### *SPI Peripheral Configuration Process*

Figure 29 illustrates the interface timing for the SPI peripheral mode and Figure 30 outlines the resulting configuration process. The actual timing specifications appear in Table 60. The application processor (AP) begins by driving the iCE65 CRESET_B pin Low, resetting the iCE65 FPGA. Similarly, the AP holds the iCE65's SPI_SS_B pin Low. The AP must hold the CRESET_B pin Low for at least 200 ns. Ultimately, the AP either releases the CRESET_B pin and allows it to float High via the 10 kΩ pull-up resistor to VCCIO_2 or drives CRESET_B High. The iCE65 FPGA enters SPI peripheral mode when the CRESET_B pin returns High while the SPI_SS_B pin is Low.

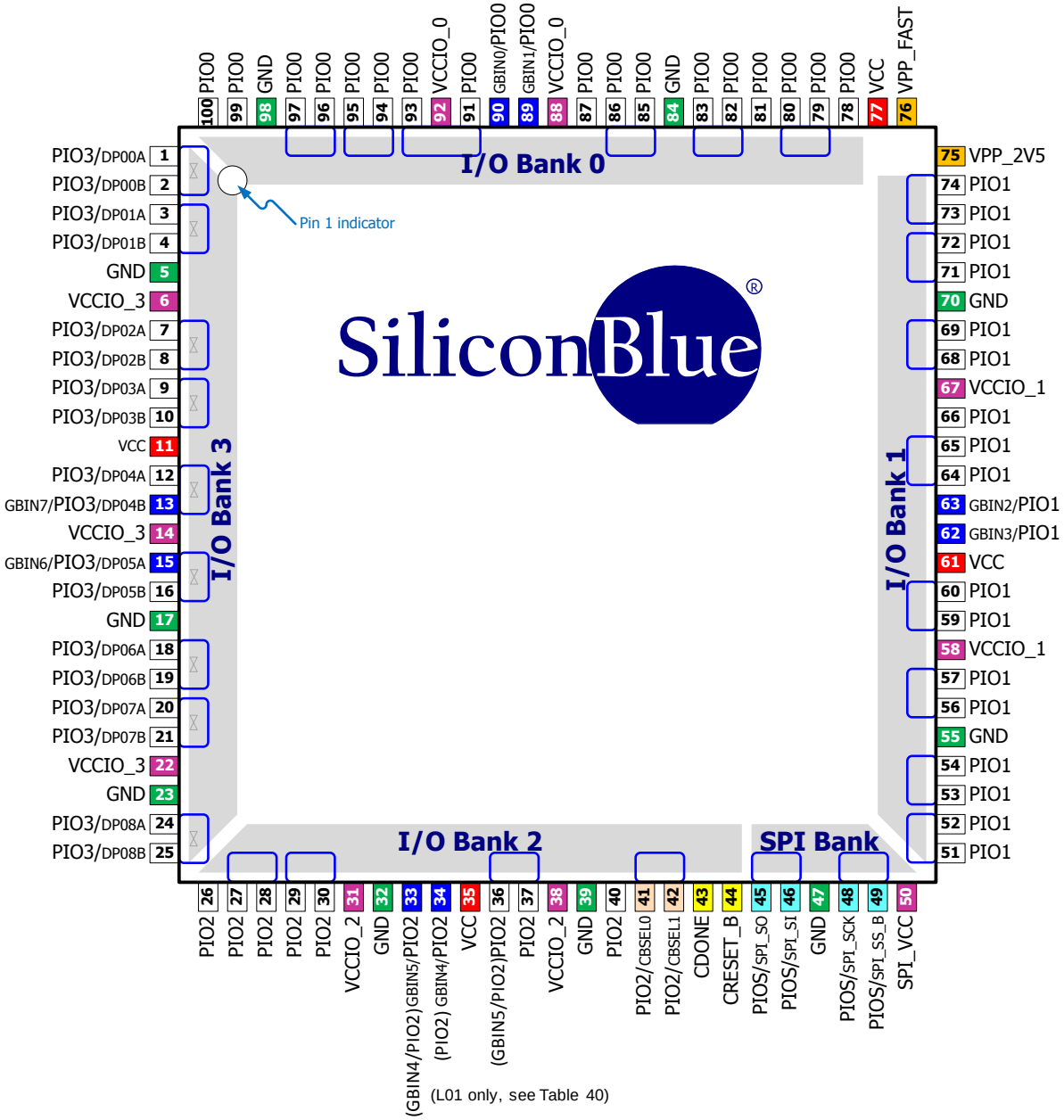
## VQ100 Very-thin Quad Flat Package

The VQ100 package is a very-thin quad-flat package with 0.5 mm lead pitch. The iCE65L01 and iCE65L04 devices are available in this package.

### *Footprint Diagram*

Figure 36 shows the footprint diagram for the 100-lead very-thin quad-flat package (VQ100). See Table 40 for a complete, detailed pinout for the 100-lead very-thin quad-flat package. The signal pins are also grouped into the four I/O Banks and the SPI interface.

**Figure 36: iCE65 VQ100 Footprint (Top View)**




### *Pinout Table*

Table 39 provides a detailed pinout table for the VQ100 package. Pins are generally arranged by I/O bank, then by pin function. The table also highlights the differential I/O pairs in I/O Bank 3. The VQ100 package has no JTAG pins.

| Pin Function | Pin Number | Type | Bank |
|---|---|---|---|
| **PIO2** | 28 | PIO | 2 |
| **PIO2** | 29 | PIO | 2 |
| **PIO2** | 30 | PIO | 2 |
| **PIO2** | iCE65L01: 34<br>iCE65L04: 36 | PIO | 2 |
| **PIO2** | 37 | PIO | 2 |
| **PIO2** | 40 | PIO | 2 |
| **PIO2/CBSEL0** | 41 | PIO | 2 |
| **PIO2/CBSEL1** | 42 | PIO | 2 |
| **VCCIO_2** | 31 | VCCIO | 2 |
| **VCCIO_2** | 38 | VCCIO | 2 |
| **PIO3/DP00A** | 1 | PIO/DPIO | 3 |
| **PIO3/DP00B** | 2 | PIO/DPIO | 3 |
| **PIO3/DP01A** | 3 | PIO/DPIO | 3 |
| **PIO3/DP01B** | 4 | PIO/DPIO | 3 |
| **PIO3/DP02A** | 7 | PIO/DPIO | 3 |
| **PIO3/DP02B** | 8 | PIO/DPIO | 3 |
| **PIO3/DP03A** | 9 | PIO/DPIO | 3 |
| **PIO3/DP03B** | 10 | PIO/DPIO | 3 |
| **PIO3/DP04A** | 12 | PIO/DPIO | 3 |
| **GBIN7/PIO3/DP04B** | 13 | GBIN/DPIO | 3 |
| **GBIN6/PIO3/DP05A** | 15 | GBIN/DPIO | 3 |
| **PIO3/DP05B** | 16 | PIO/DPIO | 3 |
| **PIO3/DP06A** | 18 | PIO/DPIO | 3 |
| **PIO3/DP06B** | 19 | PIO/DPIO | 3 |
| **PIO3/DP07A** | 20 | PIO/DPIO | 3 |
| **PIO3/DP07B** | 21 | PIO/DPIO | 3 |
| **PIO3/DP08A** | 24 | PIO/DPIO | 3 |
| **PIO3/DP08B** | 25 | PIO/DPIO | 3 |
| **VCCIO_3** | 6 | VCCIO | 3 |
| **VCCIO_3** | 14 | VCCIO | 3 |
| **VCCIO_3** | 22 | VCCIO | 3 |
| **PIOS/SPI_SO** | 45 | SPI | SPI |
| **PIOS/SPI_SI** | 46 | SPI | SPI |
| **PIOS/SPI_SCK** | 48 | SPI | SPI |
| **PIOS/SPI_SS_B** | 49 | SPI | SPI |
| **SPI_VCC** | 50 | SPI | SPI |
| **GND** | 5 | GND | GND |
| **GND** | 17 | GND | GND |
| **GND** | 23 | GND | GND |
| **GND** | 32 | GND | GND |
| **GND** | 39 | GND | GND |
| **GND** | 47 | GND | GND |
| **GND** | 55 | GND | GND |
| **GND** | 70 | GND | GND |
| **GND** | 84 | GND | GND |
| **GND** | 98 | GND | GND |
| **VCC** | 11 | VCC | VCC |
| **VCC** | 35 | VCC | VCC |

| Ball Function | Ball Number | Pin Type | Bank |
|---|---|---|---|
| GND | K2 | GND | GND |
| GND | K10 | GND | GND |
| VCC | B6 | VCC | VCC |
| VCC | F1 | VCC | VCC |
| VCC | F11 | VCC | VCC |
| VCC | K6 | VCC | VCC |
| VPP_2V5 | C10 | VPP | VPP |
| VPP_FAST | A9 | VPP | VPP |

| Ball Function | Ball Number | Pin Type | Bank |
|---|---|---|---|
| **PIO2 (◆)** | ***iCE65L04:*** N8<br>***iCE65L08:*** L7 | PIO | 2 |
| **PIO2** | N9 | PIO | 2 |
| **PIO2** | N11 | PIO | 2 |
| **PIO2** | N12 | PIO | 2 |
| **PIO2** | N13 | PIO | 2 |
| **PIO2** | P1 | PIO | 2 |
| **PIO2** | P2 | PIO | 2 |
| **PIO2** | P3 | PIO | 2 |
| **PIO2** | P4 | PIO | 2 |
| **PIO2** | P7 | PIO | 2 |
| **PIO2** | P8 | PIO | 2 |
| **PIO2** | P9 | PIO | 2 |
| **PIO2/CBSEL0** | L9 | PIO | 2 |
| **PIO2/CBSEL1** | P10 | PIO | 2 |
| **VCCIO_2** | J9 | VCCIO | 2 |
| **VCCIO_2** | M5 | VCCIO | 2 |
| **VCCIO_2** | N10 | VCCIO | 2 |
| **PIO3/DP00A** | C1 | DPIO | 3 |
| **PIO3/DP00B** | B1 | DPIO | 3 |
| **PIO3/DP01A** | D3 | DPIO | 3 |
| **PIO3/DP01B** | C3 | DPIO | 3 |
| **PIO3/DP02A** | D1 | DPIO | 3 |
| **PIO3/DP02B** | D2 | DPIO | 3 |
| **PIO3/DP03A (◆)** | ***iCE65L04:*** E1<br>***iCE65L08:*** E2 | DPIO | 3 |
| **PIO3/DP03B (◆)** | ***iCE65L04:*** E2<br>***iCE65L04:*** E1 | DPIO | 3 |
| **PIO3/DP04A** | D4 | DPIO | 3 |
| **PIO3/DP04B** | E4 | DPIO | 3 |
| **PIO3/DP05A (◆)** | ***iCE65L04:*** F3<br>***iCE65L08:*** F4 | DPIO | 3 |
| **PIO3/DP05B (◆)** | ***iCE65L04:*** F4<br>***iCE65L08:*** F3 | DPIO | 3 |
| **PIO3/DP06A** | F5 | DPIO | 3 |
| **PIO3/DP06B** | E5 | DPIO | 3 |
| **PIO3/DP07A (◆)** | ***iCE65L04:*** G2<br>***iCE65L08:*** H4 | DPIO | 3 |
| **GBIN7/PIO3/DP07B (◆)** | ***iCE65L04:*** G1<br>***iCE65L08:*** H3 | GBIN | 3 |
| **GBIN6/PIO3/DP08A** | H1 | GBIN | 3 |
| **PIO3/DP08B** | H2 | DPIO | 3 |
| **PIO3/DP09A** | G3 | DPIO | 3 |
| **PIO3/DP09B** | G4 | DPIO | 3 |
| **PIO3/DP10A** | J1 | DPIO | 3 |
| **PIO3/DP10B** | J2 | DPIO | 3 |
| **PIO3/DP11A (◆)** | ***iCE65L04:*** H4<br>***iCE65L08:*** G1 | DPIO | 3 |
| **PIO3/DP11B (◆)** | ***iCE65L04:*** H3<br>***iCE65L08:*** G2 | DPIO | 3 |
| **PIO3/DP12A** | K2 | DPIO | 3 |
| **PIO3/DP12B** | J3 | DPIO | 3 |

| Ball Function | Ball Number iCE65L04 iCE65L08 | Pin Type by Device iCE65L04 | Pin Type by Device iCE65L08 | Bank | CB132 Ball Equivalent |
|---|---|---|---|---|---|
| **VCCIO_3** | J7 | VCCIO | VCCIO | 3 | E3 |
| **VCCIO_3** | K3 | VCCIO | VCCIO | 3 | — |
| **VCCIO_3** | N10 | VCCIO | VCCIO | 3 | J6 |
| **VCCIO_3** | P5 | VCCIO | VCCIO | 3 | K1 |
| **VCCIO_3** | R3 | VCCIO | VCCIO | 3 | — |
| **VREF** | M1 | VREF | VREF | 3 | — |
| **PIOS/SPI_SO** | T15 | SPI | SPI | SPI | M11 |
| **PIOS/SPI_SI** | V15 | SPI | SPI | SPI | P11 |
| **PIOS/SPI_SCK** | V16 | SPI | SPI | SPI | P12 |
| **PIOS/SPI_SS_B** | V17 | SPI | SPI | SPI | P13 |
| **SPI_VCC** | R15 | SPI | SPI | SPI | L11 |
| **GND** | C12 | GND | GND | GND | — |
| **GND** | E13 | GND | GND | GND | A9 |
| **GND** | J3 | GND | GND | GND | — |
| **GND** | K5 | GND | GND | GND | F1 |
| **GND** | K11 | GND | GND | GND | F7 |
| **GND** | L11 | GND | GND | GND | G7 |
| **GND** | L12 | GND | GND | GND | G8 |
| **GND** | L13 | GND | GND | GND | G9 |
| **GND** | M10 | GND | GND | GND | H6 |
| **GND** | M11 | GND | GND | GND | H7 |
| **GND** | M12 | GND | GND | GND | H8 |
| **GND** | N1 | GND | GND | GND | — |
| **GND** | N12 | GND | GND | GND | J8 |
| **GND** | N18 | GND | GND | GND | J14 |
| **GND** | N20 | GND | GND | GND | — |
| **GND** | R7 | GND | GND | GND | L3 |
| **GND** | T3 | GND | GND | GND | — |
| **GND** | V1 | GND | GND | GND | — |
| **GND** | V10 | GND | GND | GND | P6 |
| **GND** | Y12 | GND | GND | GND | — |
| **GND** | Y16 | GND | GND | GND | — |
| **GND** | AB5 | GND | GND | GND | — |
| **GND** | G1 | GND | GND | GND | — |
| **GND** | R1 | GND | GND | GND | — |
| **VCC** | C8 | VCC | VCC | VCC | — |
| **VCC** | D3 | VCC | VCC | VCC | — |
| **VCC** | K12 | VCC | VCC | VCC | F8 |
| **VCC** | L10 | VCC | VCC | VCC | G6 |
| **VCC** | L20 | VCC | VCC | VCC | — |
| **VCC** | M13 | VCC | VCC | VCC | H9 |
| **VCC** | N8 | VCC | VCC | VCC | J4 |
| **VCC** | N11 | VCC | VCC | VCC | J7 |
| **VCC** | Y8 | VCC | VCC | VCC | — |
| **VPP_2V5** | E18 | VPP | VPP | VPP | A14 |
| **VPP_FAST** | E17 | VPP | VPP | VPP | A13 |

| iCE65L08 Pad Name | Available Packages | | DiePlus | | |
|---|---|---|---|---|---|
| | CB196 | CB284 | Pad | X (µm) | Y (µm) |
| TDI | M12 | T16 | 177 | 4,470.5 | 634.615 |
| TMS | P14 | V18 | 178 | 4,572.5 | 684.615 |
| TCK | L12 | R16 | 179 | 4,470.5 | 734.615 |
| TDO | N14 | U18 | 180 | 4,572.5 | 784.615 |
| TRST_B | M14 | T18 | 181 | 4,470.5 | 834.615 |
| PIO1_00 | M13 | R18 | 182 | 4,572.5 | 884.615 |
| PIO1_01 | K11 | P16 | 183 | 4,470.5 | 934.615 |
| PIO1_02 | L13 | P15 | 184 | 4,572.5 | 984.615 |
| PIO1_03 | L14 | P18 | 185 | 4,470.5 | 1,034.615 |
| GND | G9 | N18 | 186 | 4,572.5 | 1,084.615 |
| GND | — | — | 187 | 4,470.5 | 1,134.615 |
| PIO1_04 | J11 | N16 | 188 | 4,572.5 | 1,184.615 |
| PIO1_05 | K12 | N15 | 189 | 4,470.5 | 1,234.62 |
| VCCIO_1 | F9 | M18 | 190 | 4,572.5 | 1,287.115 |
| VCCIO_1 | — | — | 191 | 4,470.5 | 1,322.115 |
| PIO1_06 | J12 | M15 | 192 | 4,572.5 | 1,357.115 |
| PIO1_07 | K14 | M16 | 193 | 4,470.5 | 1,392.115 |
| PIO1_08 | — | T20 | 194 | 4,572.5 | 1,427.115 |
| PIO1_09 | — | W20 | 195 | 4,470.5 | 1,462.115 |
| PIO1_10 | — | V20 | 196 | 4,572.5 | 1,497.115 |
| VCC | H9 | M13 | 197 | 4,470.5 | 1,532.115 |
| VCC | — | — | 198 | 4,572.5 | 1,567.115 |
| PIO1_11 | — | R20 | 199 | 4,470.5 | 1,602.115 |
| PIO1_12 | — | Y22 | 200 | 4,572.5 | 1,637.115 |
| PIO1_13 | — | AA22 | 201 | 4,470.5 | 1,672.115 |
| PIO1_14 | — | U20 | 202 | 4,572.5 | 1,707.115 |
| PIO1_15 | J13 | W22 | 203 | 4,470.5 | 1,742.115 |
| PIO1_16 | H11 | P20 | 204 | 4,572.5 | 1,777.115 |
| PIO1_17 | J10 | V22 | 205 | 4,470.5 | 1,812.115 |
| PIO1_18 | H12 | U22 | 206 | 4,572.5 | 1,847.115 |
| GND | K10 | N20 | 207 | 4,470.5 | 1,882.115 |
| GND | — | — | 208 | 4,572.5 | 1,917.110 |
| PIO1_19 | H13 | T22 | 209 | 4,470.5 | 1,952.115 |
| PIO1_20 | — | M20 | 210 | 4,572.5 | 1,987.115 |
| PIO1_21 | H10 | R22 | 211 | 4,470.5 | 2,022.115 |
| PIO1_22 | — | P22 | 212 | 4,572.5 | 2,057.115 |
| VCCIO_1 | F9 | J20 | 213 | 4,470.5 | 2,092.115 |
| VCCIO_1 | — | — | 214 | 4,572.5 | 2,127.115 |
| PIO1_23 | G10 | M22 | 215 | 4,470.5 | 2,162.115 |
| PIO1_24 | G11 | N22 | 216 | 4,572.5 | 2,197.115 |
| PIO1_25 | — | K22 | 217 | 4,470.5 | 2,232.115 |
| PIO1_26 | — | L22 | 218 | 4,572.5 | 2,267.115 |
| GBIN3/PIO1_27 | G12 | K18 | 219 | 4,470.5 | 2,302.11 |
| GBIN2/PIO1_28 | F10 | L18 | 220 | 4,572.5 | 2,337.115 |
| PIO1_29 | — | J22 | 221 | 4,470.5 | 2,372.115 |

| iCE65L08 Pad Name | Available Packages | | DiePlus | | |
|---|---|---|---|---|---|
| | CB196 | CB284 | Pad | X (µm) | Y (µm) |
| GND | F7 | E13 | 270 | 3,216.98 | 4,054.5 |
| GND | — | — | 271 | 3,166.98 | 4,156.5 |
| PIO0_08 | D9 | E15 | 272 | 3,116.98 | 4,054.5 |
| PIO0_09 | C10 | G14 | 273 | 3,064.48 | 4,156.5 |
| PIO0_10 | A10 | A20 | 274 | 3,029.48 | 4,054.5 |
| PIO0_11 | B10 | H13 | 275 | 2,994.48 | 4,156.5 |
| PIO0_12 | — | A19 | 276 | 2,959.48 | 4,054.5 |
| PIO0_13 | E9 | G13 | 277 | 2,924.48 | 4,156.5 |
| PIO0_14 | — | C16 | 278 | 2,889.48 | 4,054.5 |
| PIO0_15 | — | E14 | 279 | 2,854.48 | 4,156.5 |
| VCCIO_0 | F6 | E12 | 280 | 2,819.48 | 4,054.5 |
| VCCIO_0 | — | — | 281 | 2,784.48 | 4,156.5 |
| PIO0_16 | — | A18 | 282 | 2,749.48 | 4,054.5 |
| PIO0_17 | — | A17 | 283 | 2,714.48 | 4,156.5 |
| PIO0_18 | C9 | C15 | 284 | 2,679.48 | 4,054.5 |
| PIO0_19 | — | A16 | 285 | 2,644.48 | 4,156.5 |
| PIO0_20 | B9 | C14 | 286 | 2,609.48 | 4,054.5 |
| PIO0_21 | — | H12 | 287 | 2,574.48 | 4,156.5 |
| PIO0_22 | D8 | A15 | 288 | 2,539.48 | 4,054.5 |
| PIO0_23 | C8 | H11 | 289 | 2,504.48 | 4,156.5 |
| PIO0_24 | E8 | C13 | 290 | 2,469.48 | 4,054.5 |
| PIO0_25 | — | A14 | 291 | 2,434.48 | 4,156.5 |
| GND | B12 | C12 | 292 | 2,399.48 | 4,054.5 |
| GND | — | — | 293 | 2,364.48 | 4,156.5 |
| PIO0_26 | B8 | A13 | 294 | 2,329.48 | 4,054.5 |
| PIO0_27 | D7 | A12 | 295 | 2,294.48 | 4,156.5 |
| PIO0_28 | — | C11 | 296 | 2,259.48 | 4,054.5 |
| GBIN1/PIO0_29 | E7 | E11 | 297 | 2,224.48 | 4,156.5 |
| GBIN0/PIO0_30 | A7 | E10 | 298 | 2,189.48 | 4,054.5 |
| PIO0_31 | — | G12 | 299 | 2,154.48 | 4,156.5 |
| VCCIO_0 | A8 | A8 | 300 | 2,119.48 | 4,054.5 |
| VCCIO_0 | — | — | 301 | 2,084.48 | 4,156.5 |
| PIO0_32 | C7 | A11 | 302 | 2,049.48 | 4,054.5 |
| PIO0_33 | — | G11 | 303 | 2,014.48 | 4,156.5 |
| PIO0_34 | E6 | A10 | 304 | 1,979.48 | 4,054.5 |
| PIO0_35 | — | C10 | 305 | 1,944.48 | 4,156.5 |
| VCC | B7 | C8 | 306 | 1,909.48 | 4,054.5 |
| VCC | — | — | 307 | 1,874.48 | 4,156.5 |
| PIO0_36 | — | A9 | 308 | 1,839.48 | 4,054.5 |
| PIO0_37 | A6 | A7 | 309 | 1,804.48 | 4,156.5 |
| PIO0_38 | B6 | C9 | 310 | 1,769.48 | 4,054.5 |
| PIO0_39 | A5 | A6 | 311 | 1,734.48 | 4,156.5 |
| GND | G7 | K11 | 312 | 1,699.48 | 4,054.5 |
| GND | — | — | 313 | 1,664.48 | 4,156.5 |
| PIO0_40 | D6 | E9 | 314 | 1,629.48 | 4,054.5 |
| PIO0_41 | C6 | G10 | 315 | 1,594.48 | 4,156.5 |

| iCE65L08 Pad Name | Available Packages | | DiePlus | | |
|---|---|---|---|---|---|
| | CB196 | CB284 | Pad | X (µm) | Y (µm) |
| **PIO0_42** | C5 | A5 | 316 | 1,559.48 | 4,054.5 |
| **PIO0_43** | B5 | G9 | 317 | 1,524.48 | 4,156.5 |
| **PIO0_44** | A4 | A3 | 318 | 1,489.48 | 4,054.5 |
| **PIO0_45** | — | A4 | 319 | 1,454.48 | 4,156.5 |
| **PIO0_46** | — | A2 | 320 | 1,419.48 | 4,054.5 |
| **PIO0_47** | — | C7 | 321 | 1,384.48 | 4,156.5 |
| **PIO0_48** | — | C6 | 322 | 1,331.98 | 4,054.5 |
| **VCCIO_0** | A8 | K10 | 323 | 1,281.98 | 4,156.5 |
| **VCCIO_0** | — | — | 324 | 1,231.98 | 4,054.5 |
| **PIO0_49** | — | E8 | 325 | 1,181.98 | 4,156.5 |
| **PIO0_50** | B4 | A1 | 326 | 1,131.98 | 4,054.5 |
| **PIO0_51** | C4 | E7 | 327 | 1,081.98 | 4,156.5 |
| **PIO0_52** | A3 | C5 | 328 | 1,031.98 | 4,054.5 |
| **PIO0_53** | B3 | E6 | 329 | 981.98 | 4,156.5 |
| **PIO0_54** | D5 | C3 | 330 | 931.98 | 4,054.5 |
| **GND** | A9 | L11 | 331 | 881.98 | 4,156.5 |
| **GND** | — | — | 332 | 831.98 | 4,054.5 |
| **PIO0_55** | B2 | G8 | 333 | 781.98 | 4,156.5 |
| **PIO0_56** | A2 | C4 | 334 | 731.98 | 4,054.5 |
| **PIO0_57** | A1 | H10 | 335 | 681.98 | 4,156.5 |
| **PIO0_58** | — | E5 | 336 | 631.98 | 4,054.5 |
| **PIO0_59** | — | H9 | 337 | 581.98 | 4,156.5 |

## Electrical Characteristics

All parameter limits are specified under worst-case supply voltage, temperature, and processing conditions.

### Absolute Maximum Ratings

Stresses beyond those listed under Table 47 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

**Table 47: Absolute Maximum Ratings**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| **VCC** | Core supply Voltage | –0.5 | 1.42 | V |
| **VPP_2V5** | VPP_2V5 NVCM programming and operating supply | | | V |
| **VPP_FAST** | Optional fast NVCM programming supply | | | V |
| **VCCIO_0**<br>**VCCIO_1**<br>**VCCIO_2**<br>**SPI_VCC** | I/O bank supply voltage (I/O Banks 0, 1, and 2 plus SPI interface) | –0.5 | 4.00 | V |
| **VCCIO_3** | I/O Bank 3 supply voltage | –0.5 | iCE65L01: 4.00<br>iCE65L04/08: 3.6 | V |
| **VIN_0**<br>**VIN_1**<br>**VIN_2**<br>**VIN_SPI** | Voltage applied to PIO pin within a specific I/O bank (I/O Banks 0, 1, and 2 plus SPI interface) | –1.0 | 5.5 | V |
| **VIN_3**<br>**VIN_VREF** | Voltage applied to PIO pin within I/O Bank 3 | –0.5 | iCE65L01: 4.00<br>iCE65L04/08: 3.6 | V |
| **IOUT** | DC output current per pin | — | 20 | mA |
| **$T_J$** | Junction temperature | –55 | 125 | °C |
| **$T_{STG}$** | Storage temperature, no bias | –65 | 150 | °C |

### Recommended Operating Conditions

***Table 48:*** **Recommended Operating Conditions**

| Symbol | Description | | Minimum | Nominal | Maximum | Units |
|---|---|---|---|---|---|---|
| VCC | Core supply voltage | –L: Ultra-Low Power mode | 0.95 | 1.00 | 1.05 | V |
| | | –L: Low Power<br>–T: High Performance | 1.14 | 1.20 | 1.26 | V |
| VPP_2V5 | VPP_2V5 NVCM programming and operating supply | Release from Power-on Reset | 1.30 | — | 3.47 | V |
| | | Configure from NVCM | 2.30 | — | 3.47 | V |
| | | NVCM programming | 2.30 | — | 3.00 | V |
| VPP_FAST | Optional fast NVCM programming supply | | Leave unconnected in application | | | |
| SPI_VCC | SPI interface supply voltage | | 1.71 | — | 3.47 | V |
| VCCIO_0<br>VCCIO_1<br>VCCIO_2<br>VCCIO_3<br>SPI_VCC | I/O standards, all banks* | **LVCMOS33** | 3.14 | 3.30 | 3.47 | V |
| | | **Non-standard voltage:**<br>in between 2.5V and 3.3V<br>use LVCMOS25 in iCEcube2 | Nominal<br>-5% | 2.5< Nominal<br><3.3 | Nominal<br>+5% | V |
| | | **LVCMOS25, LVDS** | 2.38 | 2.50 | 2.63 | V |
| | | **LVCMOS18, SubLVDS** | 1.71 | 1.80 | 1.89 | V |
| | | **LVCMOS15** | 1.43 | 1.50 | 1.58 | V |
| VCCIO_3 | I/O standards only available in iCE65L04/08 I/O Bank 3* | **SSTL2** | 2.38 | 2.50 | 2.63 | V |
| | | **SSTL18** | 1.71 | 1.80 | 1.89 | V |
| | | **MDDR** | 1.71 | 1.80 | 1.89 | V |
| $T_A$ | Ambient temperature | Commercial (C) | 0 | — | 70 | °C |
| | | Industrial (I) | –40 | — | 85 | °C |
| **$T_{PROG}$** | NVCM programming temperature | | 10 | 25 | 30 | °C |

**NOTE:**

VPP_FAST is only used for fast production programming. Leave floating or unconnected in application. When the iCE65 device is active, VPP_2V5 must be connected to a valid voltage.

## I/O Characteristics

### *Table 49:* PIO Pin Electrical Characteristics

| Symbol | Description | | Conditions | Minimum | Nominal | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_I$ | Input pin leakage current | I/O Bank 0, 1, 2 | $V_{IN}$ = $VCCIO_{max}$ to 0 V | | | ±10 | µA |
| | | I/O Bank 3 | $V_{IN}$ = $VCCIO_{max}$ | | | | |
| $I_{OZ}$ | Three-state I/O pin (Hi-Z) leakage current | | $V_O$ = $VCCIO_{max}$ to 0 V | | | ±10 | µA |
| $C_{PIO}$ | PIO pin input capacitance | | | | 6 | | pF |
| $C_{GBIN}$ | GBIN global buffer pin input capacitance | | | | 6 | | pF |
| $R_{PULLUP}$ | Internal PIO pull-up resistance during configuration | | VCCIO = 3.3V | | 40 | | kΩ |
| | | | VCCIO = 2.5V | | 50 | | kΩ |
| | | | VCCIO = 1.8V | | 90 | | kΩ |
| | | | VCCIO = 1.5V | | | | kΩ |
| | | | VCCIO = 1.2V | | | | kΩ |
| $V_{HYST}$ | Input hysteresis | | VCCIO = 1.5V to 3.3V | | 50 | | mV |

**NOTE:** All characteristics are characterized and may or may not be tested on each pin on each device.

### *Single-ended I/O Characteristics*

### *Table 50:* I/O Characteristics (I/O Banks 0, 1, 2 and SPI only) (I/O Bank 3 iCE65L01 only)

| I/O Standard | Nominal I/O Bank Supply Voltage | Input Voltage (V) | | Output Voltage (V) | | Output Current at Voltage (mA) | |
|---|---|---|---|---|---|---|---|
| | | $V_{IL}$ | $V_{IH}$ | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
| LVCMOS33 | 3.3V | 0.80 | 2.00 | 0.4 | 2.40 | 8 | 8 |
| LVCMOS25 | 2.5V | 0.70 | 1.70 | 0.4 | 2.00 | 6 | 6 |
| LVCMOS18 | 1.8V | 35% VCCIO | 65% VCCIO | 0.4 | 1.40 | 4 | 4 |
| LVCMOS15 | 1.5V | Not supported Use I/O Bank 3 | | 0.4 | 1.20 | 2 | 2 |

### *Table 51:* I/O Characteristics (I/O Bank 3 and iCE65L04/08 only)

| I/O Standard | Supply Voltage | Input Voltage (V) | | Output Voltage (V) | | I/O Attribute Name | mA at Voltage |
|---|---|---|---|---|---|---|---|
| | | Max. $V_{IL}$ | Min. $V_{IH}$ | Max. $V_{OL}$ | Min. $V_{OH}$ | | $I_{OL}$, $I_{OH}$ |
| LVCMOS33 | 3.3V | 0.80 | 2.20 | 0.4 | 2.40 | SL_LVCMOS33_8 | ±8 |
| LVCMOS25 | 2.5V | 0.70 | 1.70 | 0.4 | 2.00 | SB_LVCMOS25_16 | ±16 |
| | | | | | | SB_LVCMOS25_12 | ±12 |
| | | | | | | SB_LVCMOS25_8 * | ±8 |
| | | | | | | SB_LVCMOS25_4 | ±4 |
| LVCMOS18 | 1.8V | 35% VCCIO | 65% VCCIO | 0.4 | VCCIO–0.45 | SB_LVCMOS18_10 | ±10 |
| | | | | | | SB_LVCMOS18_8 | ±8 |
| | | | | | | SB_LVCMOS18_4 * | ±4 |
| | | | | | | SB_LVCMOS18_2 | ±2 |
| LVCMOS15 | 1.5V | 35% VCCIO | 65% VCCIO | 25% VCCIO | 75% VCCIO | SB_LVCMOS15_4 | ±4 |
| | | | | | | SB_LVCMOS15_2 * | ±2 |
| MDDR | 1.8V | 35% VCCIO | 65% VCCIO | 0.4 | VCCIO–0.45 | SB_MDDR10 | ±10 |
| | | | | | | SB_MDDR8 | ±8 |
| | | | | | | SB_MDDR4 * | ±4 |
| | | | | | | SB_MDDR2 | ±2 |
| SSTL2 (Class 2) | 2.5V | VREF–0.180 | VREF+0.180 | 0.35 | VTT+0.430 | SB_SSTL2_CLASS_2 | ±16.2 |
| SSTL2 (Class 1) | | | | 0.54 | | SB_SSTL2_CLASS_1 | ±8.1 |
| SSTL18 (Full) | 1.8V | VREF–0.125 | VREF+0.125 | 0.28 | VTT+0.280 | SB_SSTL18_FULL | ±13.4 |
| SSTL18 (Half) | | | | VTT–0.475 | VTT+0.475 | SB_SSTL18_HALF | ±6.7 |

**NOTES:**
SSTL2 and SSTL18 I/O standards require the VREF input pin, which is only available on the CB284 package and die-based products.

## I/O Banks 0, 1, 2 and SPI Bank Characteristic Curves

***Figure 52:*** **Typical LVCMOS Output Low Characteristics (I/O Banks 0, 1, 2, and SPI)**

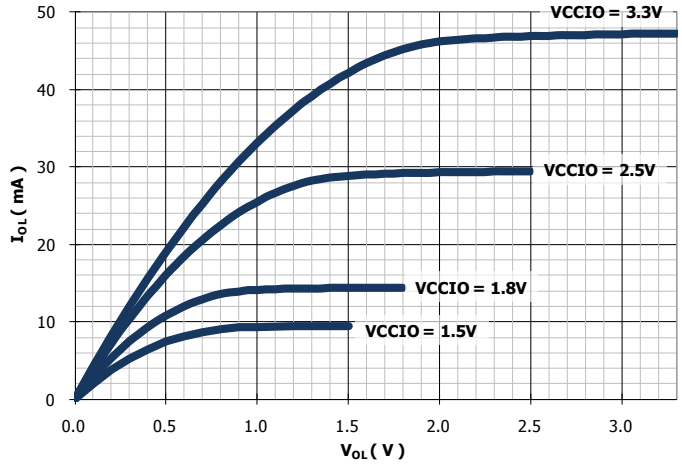



***Figure 53:*** **Typical LVCMOS Output High Characteristics (I/O Banks 0, 1, 2, and SPI)**

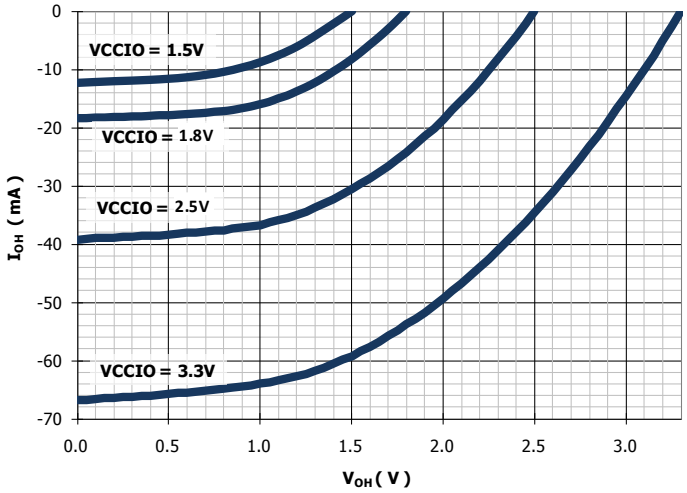
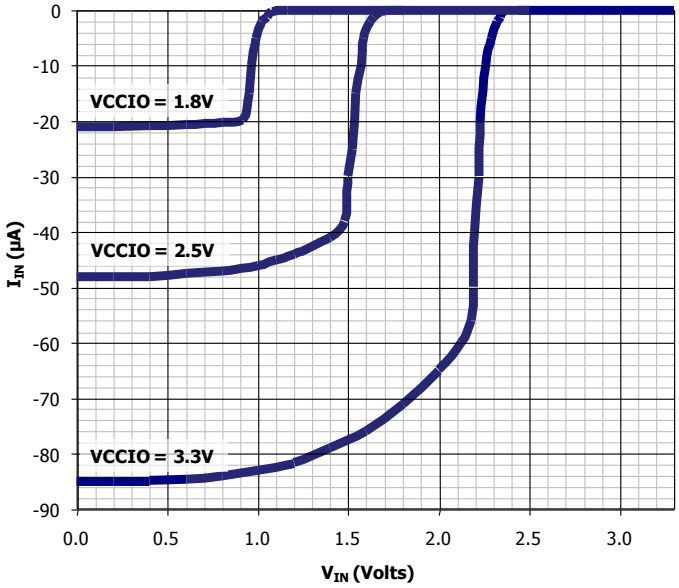



***Figure 54:*** **Input with Internal Pull-Up Resistor Enabled (I/O Banks 0, 1, 2, and SPI)**



## Programmable Input/Output (PIO) Block

Table 55 provides timing information for the logic in a Programmable Logic Block (PLB), which includes the paths shown in Figure 57 and Figure 58. The timing shown is for the LVCMOS25 I/O standard in all I/O banks. The iCEcube development software reports timing adjustments for other I/O standards.

***Figure 57:*** **Programmable I/O (PIO) Pad-to-Pad Timing Circuit**

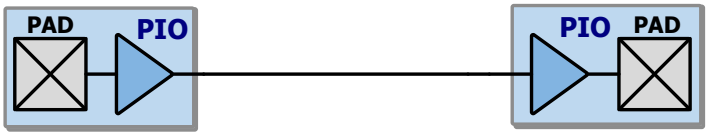



***Figure 58:*** **Programmable I/O (PIO) Sequential Timing Circuit**

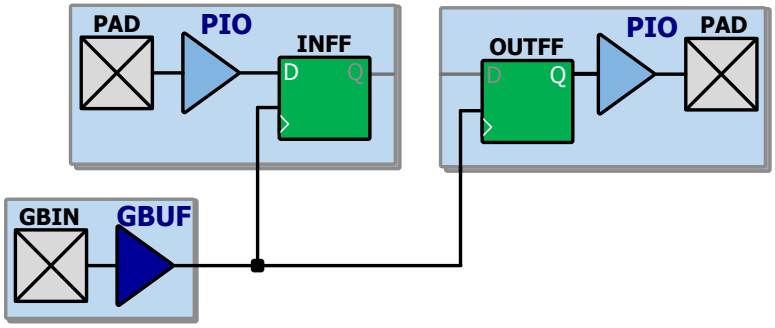



***Table 55:*** **Typical Programmable Input/Output (PIO) Timing (LVCMOS25)**

| Symbol | From | To | Device: iCE65 | L01 | L04, L08 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | Power/Speed Grad | –T | –L | | –T | |
| | | | Nominal VCC | 1.2 V | 1.0 V | 1.2 V | 1.2 V | |
| | | | Description | Typ. | Typ. | Typ. | Typ. | |
| | | **Synchronous Output Paths** | | | | | | |
| $t_{OCKO}$ | OUTFF clock input | PIO output | Delay from clock input on OUTFF output flip-flop to PIO output pad. | 4.7 | 13.8 | 7.3 | 5.6 | ns |
| $t_{GBCKIO}$ | GBIN input | OUTFF clock input | Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to clock input on the PIO OUTFF output flip-flop. | 2.1 | 7.3 | 3.8 | 2.6 | ns |
| | | **Synchronous Input Paths** | | | | | | |
| $t_{SUPDIN}$ | PIO input | GBIN input | Setup time on PIO input pin to INFF input flip-flop before active clock edge on GBIN input, including interconnect delay. | 0 | 0 | 0 | 0 | ns |
| $t_{HDPDIN}$ | GBIN input | PIO input | Hold time on PIO input to INFF input flip-flop after active clock edge on the GBIN input, including interconnect delay. | 2.7 | 7.1 | 3.6 | 2.8 | ns |
| | | **Pad to Pad** | | | | | | |
| $t_{PADIN}$ | PIO input | Inter-connect | Asynchronous delay from PIO input pad to adjacent interconnect. | 2.5 | 9.5 | 5.0 | 3.2 | ns |
| $t_{PADO}$ | Inter-connect | PIO output | Asynchronous delay from adjacent interconnect to PIO output pad including interconnect delay. | 4.5 | 14.6 | 7.7 | 6.2 | ns |

## Internal Configuration Oscillator Frequency

Table 57 shows the operating frequency for the iCE65's internal configuration oscillator.

**Table 57: Internal Oscillator Frequency**

| Symbol | Oscillator Mode | Frequency (MHz) | | Description |
|---|---|---|---|---|
| | | Min. | Max. | |
| $f_{OSCD}$ | **Default** | 4.0 | 6.8 | Default oscillator frequency. Slow enough to safely operate with any SPI serial PROM. |
| $f_{OSCL}$ | **Low Frequency** | 14 | 21 | Supported by most SPI serial Flash PROMs |
| $f_{OSCH}$ | **High Frequency** | 21 | 31 | Supported by some high-speed SPI serial Flash PROMs |
| | **Off** | 0 | 0 | Oscillator turned off by default after configuration to save power. |

## Configuration Timing

Table 58 shows the maximum time to configure an iCE65 device, by oscillator mode. The calculations use the slowest frequency for a given oscillator mode from Table 57 and the maximum configuration bitstream size from Table 1 which includes full RAM4K block initialization. The configuration bitstream selects the desired oscillator mode based on the performance of the configuration data source.

***Table 58:* Maximum SPI Master or NVCM Configuration Timing by Oscillator Mode**

| Symbol | Description | Device | Default | Low Freq. | High Freq. | Units |
|---|---|---|---|---|---|---|
| $t_{CONFIGL}$ | Time from when minimum Power-on Reset (POR) threshold is reached until user application starts. | **iCE65L01** | 53 | 25 | 11 | ms |
| | | **iCE65L04** | 115 | 55 | 25 | ms |
| | | **iCE65L08** | 230 | 110 | 50 | ms |

Table 59 provides timing for the CRESET_B and CDONE pins.

**Table 59: General Configuration Timing**

| Symbol | From | To | Description | | All Grades | | Units |
|---|---|---|---|---|---|---|---|
| | | | | | Min. | Max. | |
| **$t_{CRESET\_B}$** | CREST_B | CREST_B | Minimum CRESET_B Low pulse width required to restart configuration, from falling edge to rising edge | | 200 | — | ns |
| **$t_{DONE\_IO}$** | CDONE High | PIO pins active | Number of configuration clock cycles after CDONE goes High before the PIO pins are activated. | | — | 49 | Clock cycles |
| | | | SPI Peripheral Mode (Clock = SPI_SCK, cycles measured rising-edge to rising-edge) | | Depends on SPI_SCK frequency | | |
| | | | NVCM or SPI Master Mode by internal oscillator frequency setting (Clock = internal oscillator) | Default | 7.20 | 12.25 | µs |
| | | | | Low | 2.34 | 3.50 | µs |
| | | | | High | 1.59 | 2.33 | µs |