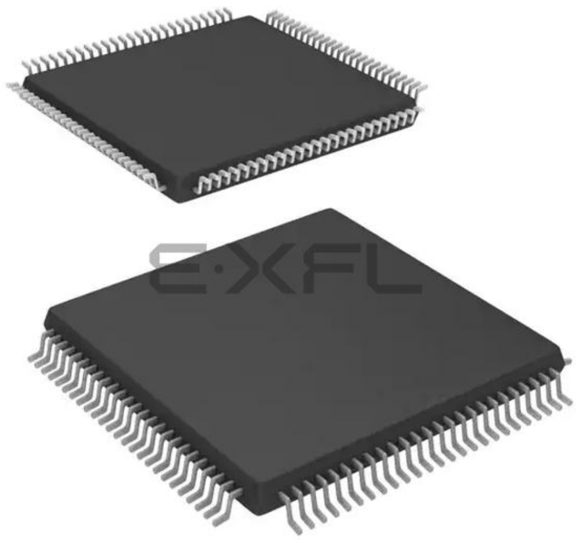
Lattice Semiconductor Corporation - ICE65L04F-LVQ100I Datasheet



Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

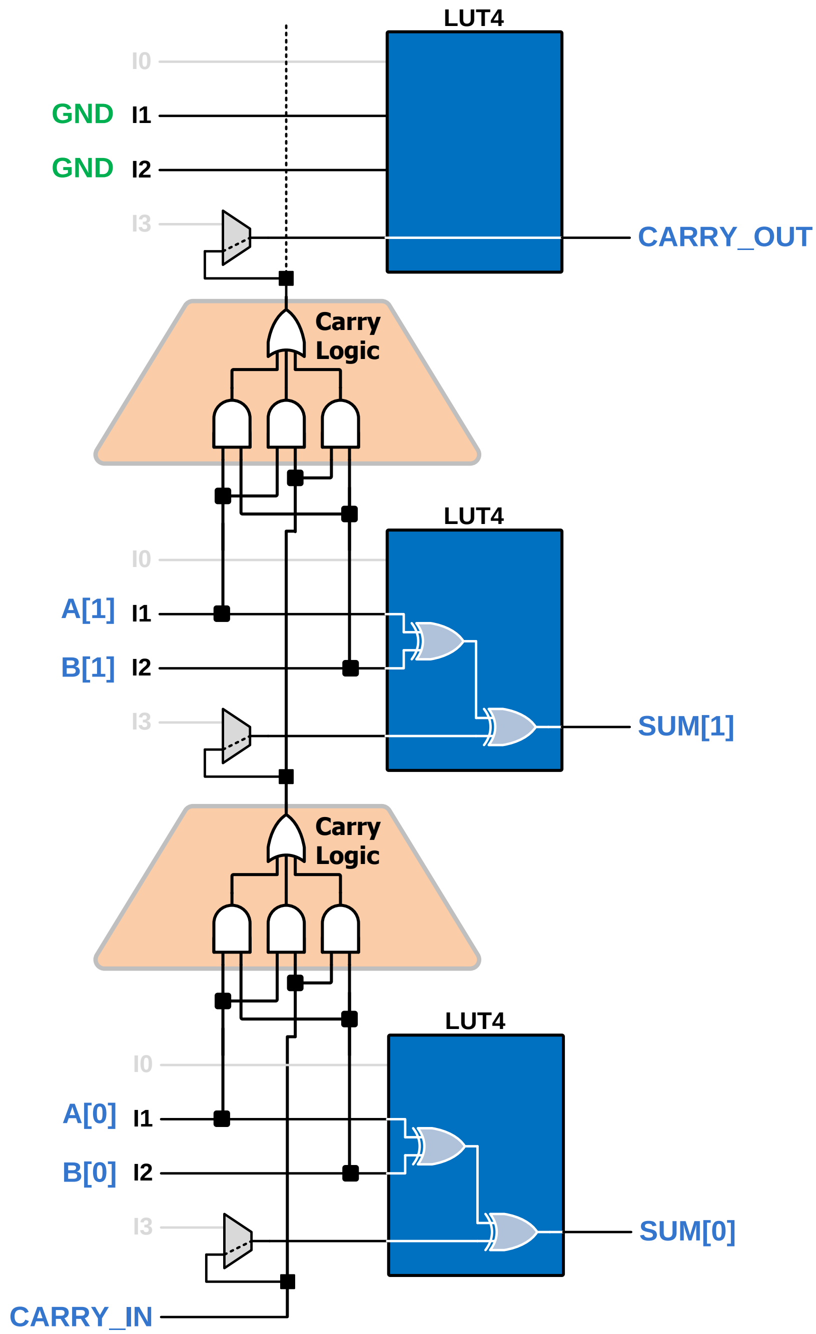
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	440
Number of Logic Elements/Cells	3520
Total RAM Bits	81920
Number of I/O	72
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice65l04f-lvq100i

Implementing Subtracters, Decrementers

As mentioned earlier, the Carry Logic generates a High output whenever the sum of `I1 + I2 + CARRY_IN` generates a carry. The Carry Logic does not specifically have a subtract mode. To implement a subtract function or decrement function, logically invert either the I1 or I2 input and invert the initial carry input. This performs a 2s complement subtract operation.

Figure 6: Two-bit Adder Example



If not connected to an external SPI PROM, the four pins associated with the SPI Master Configuration Interface can be used as PIO pins, supplied by the SPI_VCC input, essentially forming a fifth "mini" I/O bank. If using an SPI Flash PROM, then connect SPI_VCC to 3.3V.

I/O Banks 0, 1, 2, SPI and Bank 3 of iCE65L01

Table 6 highlights the available I/O standards when using an iCE65 device, indicating the drive current options, and in which bank(s) the standard is supported. I/O Banks 0, 1, 2 and SPI interface support the same standards. I/O Bank 3 has additional capabilities in iCE65L04 and iCE65L08, including support for MDDR memory standards and LVDS differential I/O.

***Table 6:* I/O Standards for I/O Banks 0, 1, 2, SPI Interface Bank, and Bank 3 of iCE65L01**

I/O Standard	Supply Voltage	Drive Current (mA)	Attribute Name
5V Input Tolerance	3.3V	N/A	N/A
LVCMOS33	3.3V	±11	SB_LVCMOS
LVCMOS25	2.5V	±8	
LVCMOS18	1.8V	±5	
LVCMOS15 outputs	1.5V	±4	

IBIS Models for I/O Banks 0, 1, 2 and the SPI Bank

The IBIS (I/O Buffer Information Specification) file that describes the output buffers used in I/O Banks 0, 1, 2, SPI Bank and Bank 3 of iCE65L01 is available from the following link.

- IBIS Models for I/O Banks 0, 1, 2, SPI Bank and Bank 3 of iCE65L01

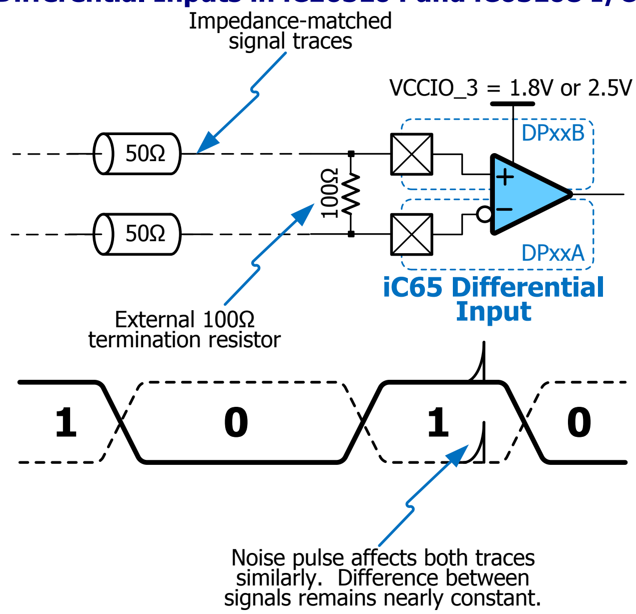
I/O Bank 3 of iCE65L04 and iCE65L08

I/O Bank 3, located along the left edge of the die, has additional special I/O capabilities to support memory components and differential I/O signaling (LVDS). Table 7 lists the various I/O standards supported by I/O Bank 3. The SSTL2 and SSTL18 I/O standards require the VREF voltage reference input pin which is only available on the CB284 package. Also see Table 51 for electrical characteristics.

***Table 7:* I/O Standards for I/O Bank 3 Only of iCE65L04 and iCE65L08**

I/O Standard	Supply Voltage	VREF Pin (CB284 or DiePlus) Required?	Target Drive Current (mA)	Attribute Name
LVCMOS33	3.3V	No	±8	SB_LVCMOS33_8
LVCMOS25	2.5V	No	±16	SB_LVCMOS25_16
			±12	SB_LVCMOS25_12
			±8	SB_LVCMOS25_8
			±4	SB_LVCMOS25_4
LVCMOS18	1.8V	No	±10	SB_LVCMOS18_10
			±8	SB_LVCMOS18_8
			±4	SB_LVCMOS18_4
			±2	SB_LVCMOS18_2
LVCMOS15	1.5V	No	±4	SB_LVCMOS15_4
			±2	SB_LVCMOS15_2
SSTL2_II	2.5V	Yes	±16.2	SB_SSTL2_CLASS_2
SSTL2_I			±8.1	SB_SSTL2_CLASS_1
SSTL18_II	1.8V	Yes	±13.4	SB_SSTL18_FULL
SSTL18_I			±6.7	SB_SSTL18_HALF
MDDR	1.8V	No	±10	SB_MDDR10
			±8	SB_MDDR8
			±4	SB_MDDR4
			±2	SB_MDDR2
LVDS	2.5V	No	N/A	SB_LVDS_INPUT

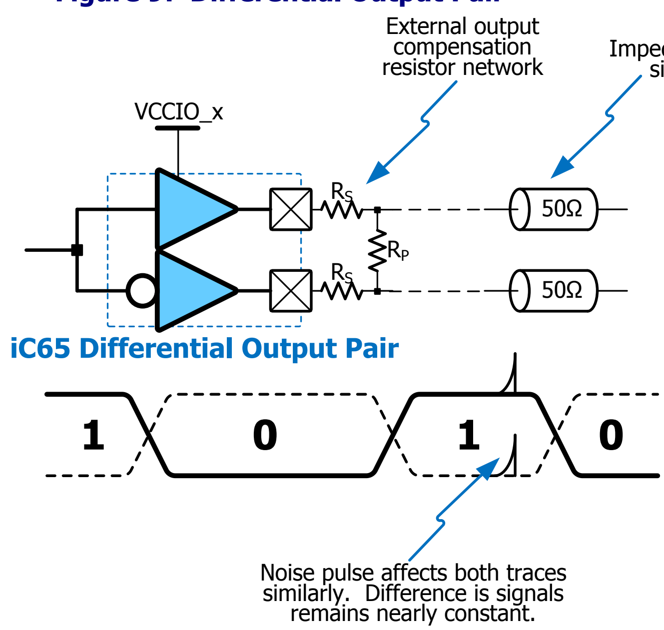
***Figure 8:* Differential Inputs in iCE65L04 and iC65L08 I/O Bank 3**



Differential Outputs in Any Bank

Differential outputs are built using a pair of single-ended PIO pins as shown in Figure 9. Each differential I/O pair requires a three-resistor termination network to adjust output characteristic to match those for the specific differential I/O standard. The output characteristics depend on the values of the parallel resistors (RP) and series resistor (RS). Differential outputs must be located in the same I/O tile.

Figure 9: Differential Output Pair

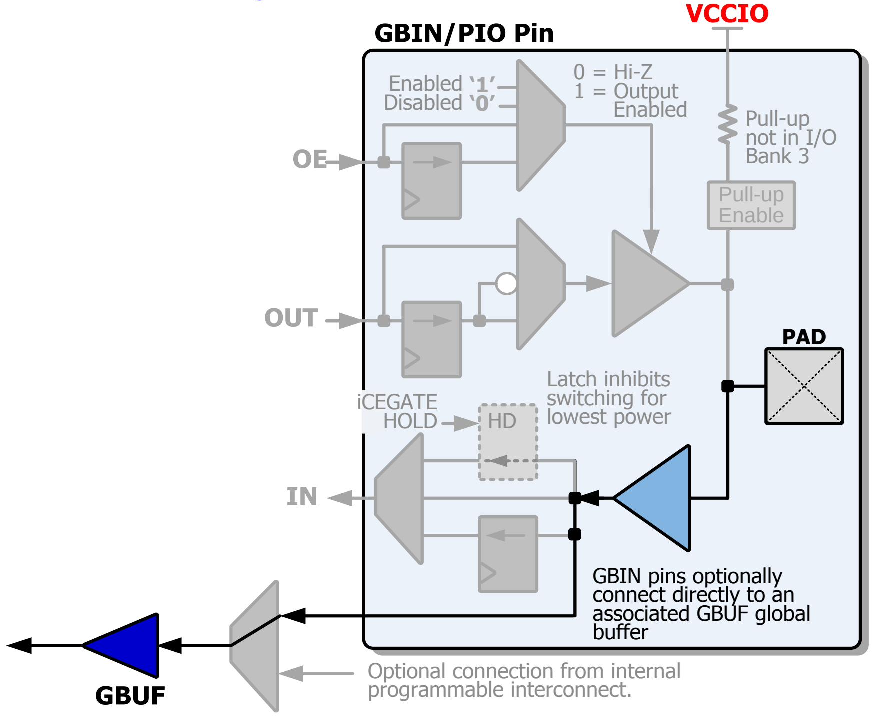


For electrical characteristics, see “Differential Outputs” on page 100.

The PIO pins that make up a differential output pair are indicated with a blue bounding box in the in the tables in “Die Cross Reference” starting on page 84.

Note the clock differences between the iCE65L04 and iCE65L08 in the CB196 package.

Figure 15: GBIN/PIO Pin



Differential Global Buffer Input

All eight global buffer inputs support single-ended I/O standards such as LVCMOS. Global buffer GBUF7 in I/O Bank 3 also provides an optional direct SubLVDS, LVDS, or LVPECL differential clock input, as shown in Figure 16. The GBIN7 and its associated differential I/O pad accept a differential clock signal. A 100 Ω termination resistor is required across the two pads. Optionally, swap the outputs from the LVDS or LVPECL clock driver to invert the clock as it enters the iCE65 device.

Figure 16: LVDS or LVPECL Clock Input

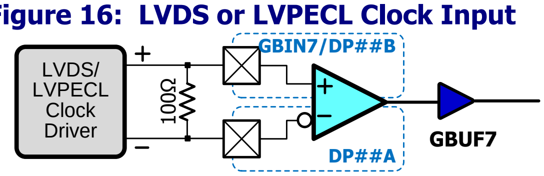


Table 15 lists the pin or ball numbers for the differential global buffer input by package style. Although this differential input is the only one that connects directly to a global buffer, other differential inputs can connect to a global buffer using general-purpose interconnect, with slightly more signal delay.

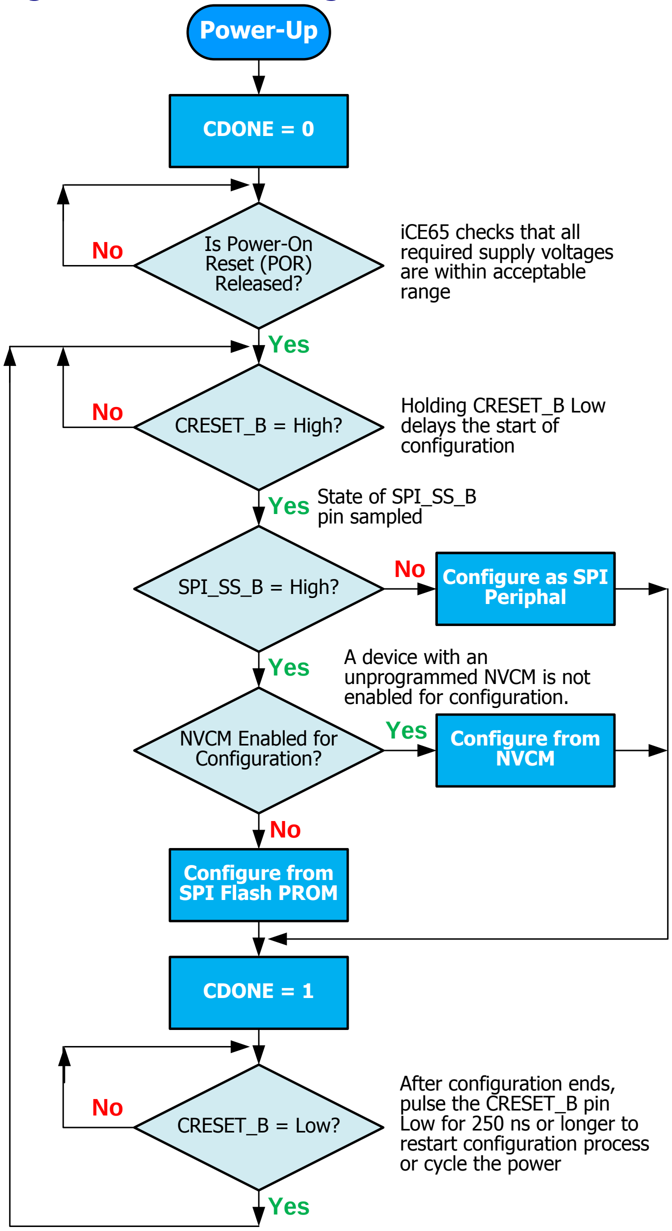
***Table 15:* Differential Global Buffer Input Ball/Pin Number by Package**

Differential Global Buffer Input (GBIN)	I/O Bank	VQ100	CB132	'L04 CB196	'L08 CB196	CB284
GBIN7/DPxxB	3	13	N/A	G1	H3	L5
DPxxA		12	N/A	G2	H4	L3

The differential global buffer input is not available for iCE65 devices in the CB132 package. This restriction is an artifact of the pin compatibility between the CB132 and CB284 package.

Note the clock differences between the iCE65L04 and iCE65L08 in the CB196 package.

Figure 20: **Device Configuration Control Flow**



Configuration Image Size

Table 23 shows the number of memory bits required to configure an iCE65 device. Two values are provided for each device. The "Logic Only" value indicates the minimum configuration size, the number of bits required to configure only the logic fabric, leaving the RAM4K blocks uninitialized. The "Logic + RAM4K" column indicates the maximum configuration size, the number of bits to configure the logic fabric and to pre-initialize all the RAM4K blocks.

Figure 21: iCE65 Configuration Control Pins

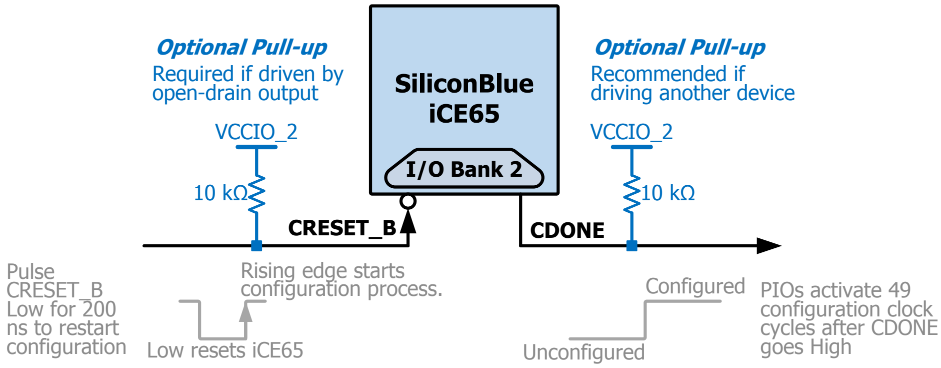


Figure 21 shows the two iCE65 configuration control pins, CRESET_B and CDONE. Table 23 lists the ball/pin numbers for the configuration control pins by package. When driven Low for at least 200 ns, the dedicated Configuration Reset input, CRESET_B, resets the iCE65 device. When CRESET_B returns High, the iCE65 FPGA restarts the configuration process from its power-on conditions (Cold Boot). The CRESET_B pin is a pure input with no internal pull-up resistor. If driven by open-drain driver or un-driven, then connect the CRESET_B pin to a 10 kΩ pull-up resistor connected to the VCCIO_2 supply.

***Table 23:* Configuration Control Ball/Pin Numbers by Package**

Configuration Control Pins	CB81	QN84	VQ100	CB132	CB196	CB284
CRESET_B	J6	A21	44	L10	L10	R14
CDONE	H6	B16	43	M10	M10	T14

The iCE65 device signals the end of the configuration process by actively turning off the internal pull-down transistor on the Configuration Done output pin, CDONE. The pin has a permanent, weak internal pull-up resistor to the VCCIO_2 rail. If the iCE65 device drives other devices, then optionally connect the CDONE pin to a 10 kΩ pull-up resistor connected to the VCCIO_2 supply.

The PIO pins activate according to their configured function after 49 configuration clock cycles. The internal oscillator is the configuration clock source for the SPI Master Configuration Interface and when configuring from

* Note: only 14 of the 16 RAM4K Memory Blocks may be pre-initialized in the iCE65L01.

Nonvolatile Configuration Memory (NVCM). When using the SPI Peripheral Configuration Interface, the configuration clock source is the SPI_SCK clock input pin.

Internal Oscillator

During SPI Master or NVCM configuration mode, the controlling clock signal is generated from an internal oscillator. The oscillator starts operating at the Default frequency. During the configuration process, however, bit settings within the configuration bitstream can specify a higher-frequency mode in order to maximize SPI bandwidth and reduce overall configuration time. See Table 57: Internal Oscillator Frequency on page 105 for the specified oscillator frequency range.

Using the SPI Master Configuration Interface, internal oscillator controls all the interface timing and clocks the SPI serial Flash PROM via the SPI_SCK clock output pin.

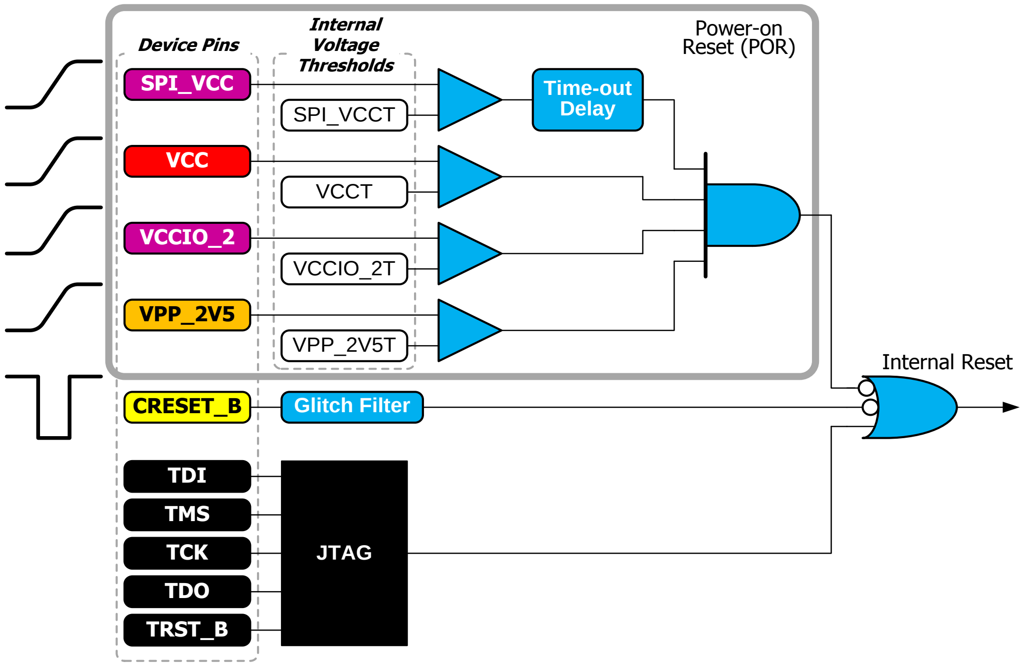
The oscillator output, which also supplies the SPI SCK clock output during the SPI Flash configuration process, has a 50% duty cycle.

Internal Device Reset

Figure 22 presents the various signals that internally reset the iCE65 internal logic.

- Power-On Reset (POR)
- CRESET_B Pin
- JTAG Interface

Figure 22: iCE65 Internal Reset Circuitry



Power-On Reset (POR)

The Power-on Reset (POR) circuit monitors specific voltage supply inputs and holds the device in reset until all the relevant supplies exceed the internal voltage thresholds. The SPI_VCC supply also has an additional time-out delay to allow an attached SPI serial PROM to power up properly. Table 24 shows the POR supply inputs. The Nonvolatile Configuration Memory (NVCM) requires that the VPP_2V5 supply be connected, even if the application does not use the NVCM.

***Table 24:* Power-on Reset (POR) Voltage Resources**

Supply Rail	iCE65 Production Devices
VCC	Yes
SPI_VCC	Yes
VCCIO_1	No
VCCIO_2	Yes
VPP_2V5	Yes

CRESET_B Pin

The CRESET_B pin resets the iCE65 internal logic when Low.

JTAG Interface

Specific command sequences also reset the iCE65 internal logic.

SPI Master Configuration Interface

All iCE65 devices, including those with NVCM, can be configured from an external, commodity SPI serial Flash PROM, as shown in Figure 23. The SPI configuration interface is essentially its own independent I/O bank, powered by the VCC_SPI supply input. Presently, most commercially-available SPI serial Flash PROMs require a 3.3V supply.

iCE65 Pin Descriptions

Table 36 lists the various iCE65 pins, alphabetically by name. The table indicates the directionality of the signal and the associated I/O bank. The table also indicates if the signal has an internal pull-up resistor enabled during configuration. Finally, the table describes the function of the pin.

Table 36: iCE65 Pin Description

Signal Name	Direction	I/O Bank	Pull-up during Config	Description
CDONE	Output	2	Yes	Configuration Done. Dedicated output. Includes a permanent weak pull-up resistor to VCCIO_2.. If driving external devices with CDONE output, connect a 10 kΩ pull-up resistor to VCCIO_2.
CRESET_B	Input	2	No	Configuration Reset, active Low. Dedicated input. No internal pull-up resistor. Either actively drive externally or connect a 10 kΩ pull-up resistor to VCCIO_2.
GBIN0/PIO0 **GBIN1/PIO0**	Input/IO	0	Yes	Global buffer input from I/O Bank 0. Optionally, a full-featured PIO pin.
GBIN2/PIO1 **GBIN3/PIO1**	Input/IO	1	Yes	Global buffer input from I/O Bank 1. Optionally, a full-featured PIO pin.
GBIN4/PIO2 **GBIN5/PIO2**	Input/IO	2	Yes	Global buffer input from I/O Bank 2. Optionally, a full-featured PIO pin.
GBIN6/PIO3	Input/IO	3	No	Global buffer input from I/O Bank 3. Optionally, a full-featured PIO pin.
GBIN7/PIO3	Input/IO	3	No	Global buffer input from I/O Bank 3. Optionally, a full-featured PIO pin. Optionally, a differential clock input using the associated differential input pin.
GND	Supply	All	N/A	Ground. All must be connected.
PIOx_yy	I/O	0,1,2	Yes	Programmable I/O pin defined by the iCE65 configuration bitstream. The 'x' number specifies the I/O bank number in which the I/O pin resides. The "yy' number specifies the I/O number in that bank.
PIO2/CBSEL0	Input/IO	2	Yes	Optional ColdBoot configuration SELect input, if ColdBoot mode is enabled. A full-featured PIO pin after configuration.
PIO2/CBSEL1	Input/IO	2	Yes	Optional ColdBoot configuration SELect input, if ColdBoot mode is enabled. A full-featured PIO pin after configuration.
PIO3_yy/ DPwwz	I/O	3	No	Programmable I/O pin that is also half of a differential I/O pair. Only available in I/O Bank 3. The "yy" number specifies the I/O number in that bank. The "ww" number indicates the differential I/O pair. The 'z' indicates the polarity of the pin in the differential pair. 'A'=negative input. 'B'=positive input.
PIOS/SPI_SO	I/O	SPI	Yes	SPI Serial Output. A full-featured PIO pin after configuration.
PIOS /SPI_SI	I/O	SPI	Yes	SPI Serial Input. A full-featured PIO pin after configuration.
PIOS / SPI_SS_B	I/O	SPI	Yes	SPI Slave Select. Active Low. Includes an internal weak pull-up resistor to SPI_VCC during configuration. During configuration, the logic level sampled on this pin determines the configuration mode used by the iCE65 device, as shown in Figure 20. An input when sampled at the start of configuration. An input when in SPI Peripheral configuration mode (SPI_SS_B = Low). An output when in SPI Flash configuration mode. A full-featured PIO pin after configuration.
PIOS/ SPI_SCK	I/O	SPI	Yes	SPI Slave Clock. An input when in SPI Peripheral configuration mode (SPI_SS_B = Low). An output when in SPI Flash configuration mode. A full-featured PIO pin after configuration.
TDI	Input	1	No	JTAG Test Data Input. If using the JTAG interface, use a 10kΩ pull-up resistor to VCCIO_1. Tie off to GND when unused.

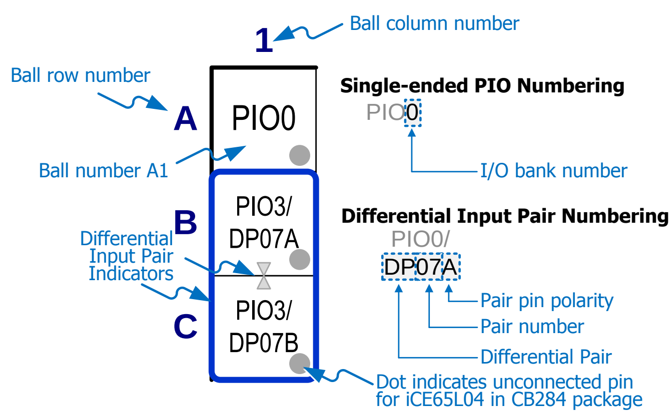
Signal Name	Direction	I/O Bank	Pull-up during Config	Description
TMS	Input	1	No	JTAG Test Mode Select. If using the JTAG interface, use a 10kΩ pull-up resistor to VCCIO_1. Tie off to GND when unused.
TCK	Input	1	No	JTAG Test Clock. If using the JTAG interface, use a 10kΩ pull-up resistor to VCCIO_1. Tie off to GND when unused.
TDO	Output	1	No	JTAG Test Data Output.
TRST_B	Input	1	No	JTAG Test Reset, active Low. Keep Low during normal operation; High for JTAG operation.
VCC	Supply	All	N/A	Internal core voltage supply. All must be connected.
VCCIO_0	Supply	0	N/A	Voltage supply to I/O Bank 0. All such pins or balls on the package must be connected. Can be disconnected or turned off without affecting the Power-On Reset (POR) circuit.
VCCIO_1	Supply	1	N/A	Voltage supply to I/O Bank 1. All such pins or balls on the package must be connected. Required to guarantee a valid input voltage on TRST_B JTAG pin.
VCCIO_2	Supply	2	N/A	Voltage supply to I/O Bank 2. All such pins or balls on the package must be connected. Required input to the Power-On Reset (POR) circuit.
VCCIO_3	Supply	3	N/A	Voltage supply to I/O Bank 3. All such pins or balls on the package must be connected. Can be disconnected or turned off without affecting the Power-On Reset (POR) circuit.
SPI_VCC	Supply	SPI	N/A	SPI interface voltage supply input. Must have a valid voltage even if configuring from NVCM. Required input to the Power-On Reset (POR) circuit.
VPP_FAST	Supply	All	N/A	Direct programming voltage supply. If unused, leave floating or unconnected during normal operation.
VPP_2V5	Supply	All	N/A	Programming supply voltage. When the iCE65 device is active, VPP_2V5 must be in the valid range between 2.3 V to 3.47 V to release the Power-On Reset circuit, even if the application is not using the NVCM.
VREF	Voltage Reference	3	N/A	Input reference voltage in I/O Bank 3 for the SSTL I/O standard. This pin only appears on the CB284 package and for die-based products.

N/A = Not Applicable

iCE65 Package Footprint Diagram Conventions

Figure 31 illustrates the naming conventions used in the following footprint diagrams. Each PIO pin is associated with an I/O Bank. PIO pins in I/O Bank 3 that support differential inputs are also numbered by differential input pair.

Figure 31: **CB Package Footprint Diagram Conventions**



Pinout Table

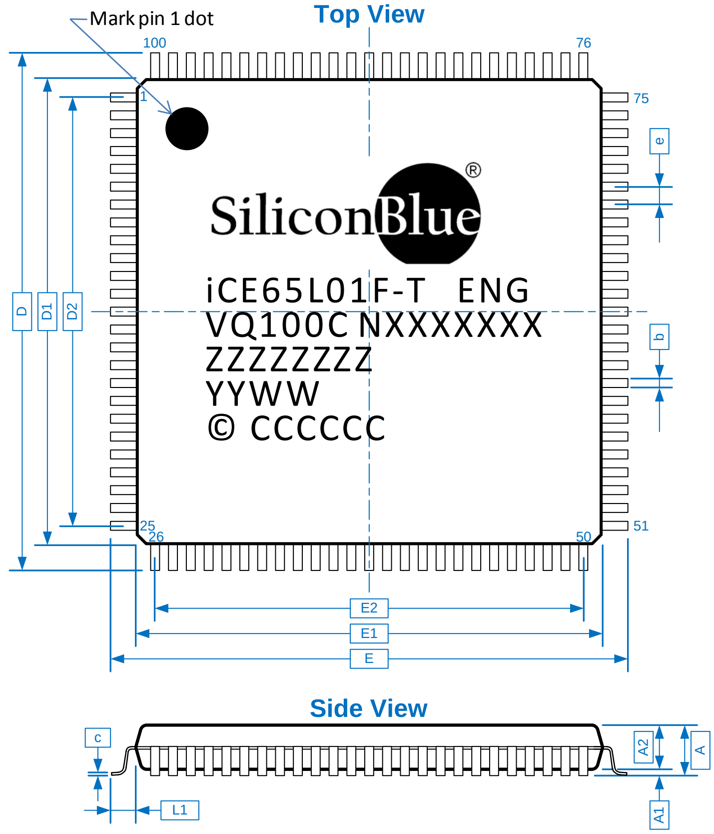
Table 38 provides a detailed pinout table for the QN84 package. Pins are generally arranged by I/O bank, then by ball function. The QN84 package has no JTAG pins.

Table 38: **iCE65 QN84 Chip-scale BGA Pinout Table**

Ball Function	Ball Number	Pin Type	Bank
GBIN0/PIO0	B32	GBIN	0
GBIN1/PIO0	A43	GBIN	0
PIO0	A38	PIO	0
PIO0	A39	PIO	0
PIO0	A40	PIO	0
PIO0	A41	PIO	0
PIO0	A44	PIO	0
PIO0	A45	PIO	0
PIO0	A46	PIO	0
PIO0	A47	PIO	0
PIO0	A48	PIO	0
PIO0	B29	PIO	0
PIO0	B30	PIO	0
PIO0	B31	PIO	0
PIO0	B34	PIO	0
PIO0	B35	PIO	0
PIO0	B36	PIO	0
VCCIO_0	A42	VCCIO	0
GBIN2/PIO1	B22	GBIN	1
GBIN3/PIO1	A29	GBIN	1
PIO1	A25	PIO	1
PIO1	A26	PIO	1
PIO1	A27	PIO	1
PIO1	A31	PIO	1
PIO1	A32	PIO	1
PIO1	A33	PIO	1
PIO1	A34	PIO	1
PIO1	A35	PIO	1
PIO1	B19	PIO	1
PIO1	B20	PIO	1
PIO1	B21	PIO	1
PIO1	B23	PIO	1
PIO1	B24	PIO	1
PIO1	B26	PIO	1
PIO1	B27	PIO	1
VCCIO_1	B25	VCCIO	1
CDONE	B16	CONFIG	2
CRESET_B	A21	CONFIG	2
GBIN4/PIO2	A14	GBIN	2
GBIN5/PIO2	A16	GBIN	2
PIO2	A13	PIO	2
PIO2	B12	PIO	2
PIO2	A19	PIO	2
PIO2	B10	PIO	2
PIO2	B11	PIO	2
PIO2	B13	PIO	2

Ball Function	Ball Number	Pin Type	Bank
PIO2	B14	PIO	2
PIO2/CBSEL0	B15	PIO	2
PIO2/CBSEL1	A20	PIO	2
VCCIO_2	A17	PIO	2
GBIN6/PIO3	A9	GBIN	3
GBIN7/PIO3	A8	GBIN	3
PIO3	A1	PIO	3
PIO3	A2	PIO	3
PIO3	A3	PIO	3
PIO3	A4	PIO	3
PIO3	A5	PIO	3
PIO3	A10	PIO	3
PIO3	A11	PIO	3
PIO3	A12	PIO	3
PIO3	B1	PIO	3
PIO3	B2	PIO	3
PIO3	B3	PIO	3
PIO3	B4	PIO	3
PIO3	B5	PIO	3
PIO3	B7	PIO	3
PIO3	B8	PIO	3
PIO3	B9	PIO	3
VCCIO_3	B6	VCCIO	3
PIOS/SPI_SO	B17	SPI	SPI
PIOS/SPI_SI	A22	SPI	SPI
PIOS/SPI_SCK	A23	SPI	SPI
PIOS/SPI_SS_B	B18	SPI	SPI
SPI_VCC	A24	SPI	SPI
GND	A6	GND	GND
GND	A18	GND	GND
GND	A30	GND	GND
GND	B33	GND	GND
VCC	A7	VCC	VCC
VCC	A15	VCC	VCC
VCC	A28	VCC	VCC
VCC	B28	VCC	VCC
VPP_2V5	A36	VPP	VPP
VPP_FAST	A37	VPP	VPP

Figure 38: VQ100 Package Mechanical Drawing: NVCM Programmed Device Marking



Description		Symbol	Min.	Nominal	Max.	Units
Leads per Edge	X			25		Leads
	Y			25		
Number of Signal Leads		n		100		
Maximum Size (lead tip to lead tip)	X	E	—	16.0	—	mm
	Y	D	—	16.0	—	
Body Size	X	E1	—	14.0	—	
	Y	D1	—	14.0	—	
Edge Pin Center to Center	X	E2	—	12.0	—	
	Y	D2	—	12.0	—	
Lead Pitch		e	—	0.50	—	
Lead Width		b	0.17	0.20	0.27	
Total Package Height		A	—	1.20	—	
Stand Off		A1	0.05	—	0.15	
Body Thickness		A2	0.95	1.00	1.05	
Lead Length		L1	—	1.00	—	
Lead Thickness		c	0.09	—	0.20	
Coplanarity			—	0.08	—	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65L01F	Part number
	-T	Power/Speed
	ENG	Engineering
3	VQ100C NXXXXXXX	Package type and Lot number
4	ZZZZZZZZ	NVCM Program. code
5	YYWW	Date Code
6	© CCCCCC	Country

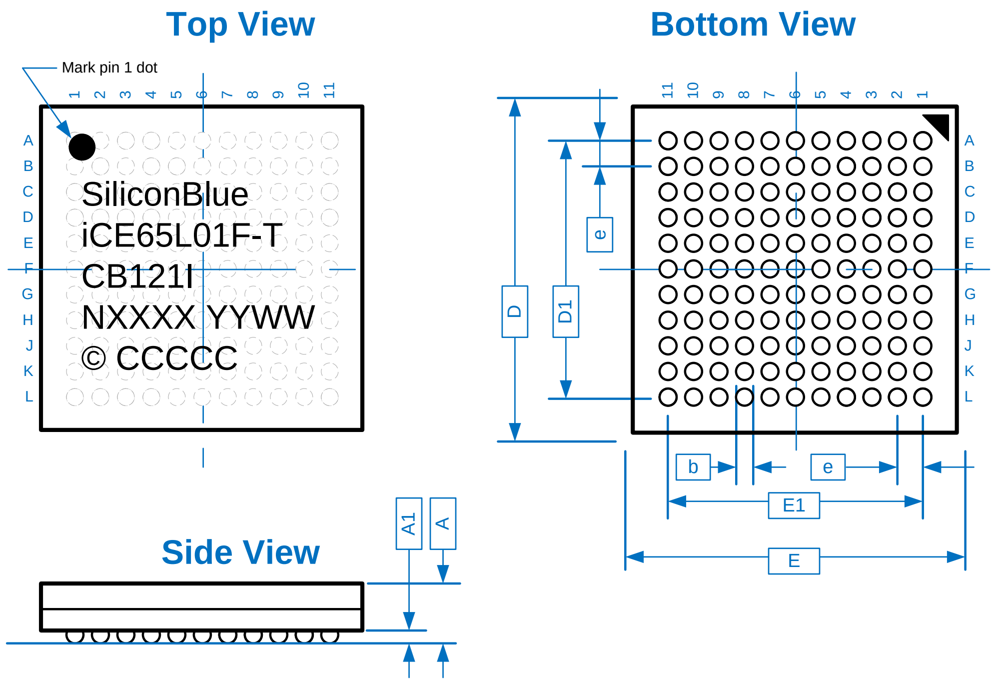
Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
38	32

Package Mechanical Drawing

Figure 40: **CB121 Package Mechanical Drawing**

CB121: 6 x 6 mm, 121-ball, 0.5 mm ball-pitch, fully-populated, chip-scale ball grid array



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			11		Columns
Number of Ball Rows	Y			11		Rows
Number of Signal Balls		n		121		Balls
Body Size	X	E	5.90	6.00	6.10	mm
	Y	D	5.90	6.00	6.10	
Ball Pitch		e	—	0.50	—	
Ball Diameter		b	0.2	—	0.3	
Edge Ball Center to Center	X	E1	—	5.00	—	
	Y	D1	—	5.00	—	
Package Height		A	—	—	1.00	
Stand Off		A1	0.12	—	0.20	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65L01F	Part number
	-T	Power/Speed
3	CB121I	Package type
	ENG	Engineering
4	NXXXX	Lot Number
5	YYWW	Date Code
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
64	55

CB196 Chip-Scale Ball-Grid Array

The CB196 package is a chip-scale, fully-populated, ball-grid array with 0.5 mm ball pitch.

Footprint Diagram

Figure 45 shows the iCE65L04 chip-scale BGA footprint for the 8 x 8 mm CB196 package. The footprint for the iCE65L08 is different than the iCE64L04 footprint, as shown in Figure 46. The pinout differences are highlighted by warning diamonds (◆) in the footprint diagrams and summarized in Table 43.

> ⚠ Although both the iCE65L04 and iCE65L08 are both available in the CB196 package and ***almost*** completely pin compatible, there are differences as shown in Table 43.

Figure 31 shows the conventions used in the diagram. Also see Table 42 for a complete, detailed pinout for the 196-ball chip-scale BGA packages. The signal pins are also grouped into the four I/O Banks and the SPI interface.

Figure 45: iCE65L04 CB196 Chip-Scale BGA Footprint (Top View)

I/O Bank 0 (top) — I/O Bank 1 (right) — I/O Bank 2 and SPI Bank (bottom) — I/O Bank 3 (left)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0	GBIN0/ PIO0	VCCIO_0	GND	PIO0	PIO0	PIO0	VPP_ FAST	VPP_ 2V5
B	PIO3/ DP00B	PIO0	PIO0	PIO0	PIO0	PIO0	VCC	PIO0	PIO0	PIO0	PIO0	GND	PIO1	PIO1
C	PIO3/ DP00A	GND	PIO1/ DP01B	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0	PIO1	PIO1	PIO1
D	PIO3/ DP02A	PIO3/ DP02B	PIO1/ DP01A	PIO3/ DP04A	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0	PIO1	PIO1	PIO1	PIO1
E	PIO3/ DP03A ◆	PIO3/ DP03B ◆	VCCIO_3	PIO3/ DP04B	PIO3/ DP06B	PIO0	GBIN1/ PIO0	PIO0	PIO0	PIO1	PIO1	PIO1	PIO1	PIO1
F	GND	VCC	PIO3/ DP05A ◆	PIO3/ DP05B ◆	PIO3/ DP06A	VCCIO_0	GND	VCC	VCCIO_1	GBIN2/ PIO1	PIO1	PIO1	PIO1	PIO1
G	GBIN7/ PIO3/ DP07B ◆	PIO3/ DP07A ◆	PIO3/ DP09A	PIO3/ DP09B	PIO3/ DP13B	VCC	GND	GND	GND	PIO1	PIO1	GBIN3/ PIO1	PIO1	PIO1
H	GBIN6/ PIO3/ DP08A	PIO3/ DP08B	PIO3/ DP11B ◆	PIO3/ DP11A ◆	PIO3/ DP13A	GND	GND	GND	VCC	PIO1	PIO1	PIO1	PIO1	VCCIO_1
J	PIO3/ DP10A	PIO3/ DP10B	PIO3/ DP12B	VCC	GND	VCCIO_3	VCC	GND	VCCIO_2	PIO1	PIO1	PIO1	PIO1	GND
K	VCCIO_3	PIO3/ DP12A	PIO3/ DP16A ◆	PIO3/ DP16B ◆	PIO2	PIO2	PIO2	PIO2	PIO2	GND	PIO1	PIO1	VCC	PIO1
L	PIO3/ DP14A	PIO3/ DP14B	GND	PIO2	PIO2	PIO2	GBIN4/ PIO2 ◆	PIO2	PIO2/ CBSEL0	CRESET_B	SPI_ VCC	TCK	PIO1	PIO1
M	PIO3/ DP15A	PIO3/ DP15B	PIO2	PIO2	VCCIO_2	PIO2	PIO2 ◆	PIO2	PIO2	CDONE	PIOS/ SPI_SO	TDI	PIO1	TRST_B
N	PIO3/ DP17A	PIO3/ DP17B	PIO2	PIO2	PIO2	PIO2	VCC	PIO2 ◆	PIO2	VCCIO_2	PIO2	PIO2	PIO2	TDO
P	PIO2	PIO2	PIO2	PIO2	GBIN5/ PIO2 ◆	GND	PIO2	PIO2	PIO2	PIO2/ CBSEL1	PIOS/ SPI_SI	PIOS/ SPI_SCK	PIOS/ SPI_SS_B	TMS

Pinout Table

Table 44 provides a detailed pinout table for the two chip-scale BGA packages. Pins are generally arranged by I/O bank, then by ball function. The balls with a black circle (●) are unconnected balls (N.C.) for the iCE65L04 in the CB284 package. The CB132 package fits within the CB284 package footprint as shown in Figure 48. The right-most column shows which CB132 ball corresponds to the CB284.

The table also highlights the differential I/O pairs in I/O Bank 3.

Table 44: iCE65 CB284 Chip-scale BGA Pinout Table (with CB132 cross reference)

Ball Function	Ball Number	Pin Type by Device		Bank	CB132 Ball Equivalent
	iCE65L04 iCE65L08	iCE65L04	iCE65L08		
GBIN0/PIO0	E10	GBIN	GBIN	0	A6
GBIN1/PIO0	E11	GBIN	GBIN	0	A7
PIO0 (●)	A1	N.C.	PIO	0	—
PIO0 (●)	A2	N.C.	PIO	0	—
PIO0 (●)	A3	N.C.	PIO	0	—
PIO0 (●)	A4	N.C.	PIO	0	—
PIO0	A5	PIO	PIO	0	—
PIO0	A6	PIO	PIO	0	—
PIO0	A7	PIO	PIO	0	—
PIO0 (●)	A9	N.C.	PIO	0	—
PIO0 (●)	A10	N.C.	PIO	0	—
PIO0 (●)	A11	N.C.	PIO	0	—
PIO0 (●)	A12	N.C.	PIO	0	—
PIO0 (●)	A13	N.C.	PIO	0	—
PIO0	A15	PIO	PIO	0	—
PIO0	A16	PIO	PIO	0	—
PIO0	A17	PIO	PIO	0	—
PIO0	A18	PIO	PIO	0	—
PIO0 (●)	A14	N.C.	PIO	0	—
PIO0 (●)	A19	N.C.	PIO	0	—
PIO0 (●)	A20	N.C.	PIO	0	—
PIO0	C3	PIO	PIO	0	—
PIO0	C4	PIO	PIO	0	—
PIO0	C5	PIO	PIO	0	—
PIO0	C6	PIO	PIO	0	—
PIO0	C7	PIO	PIO	0	—
PIO0	C9	PIO	PIO	0	—
PIO0	C10	PIO	PIO	0	—
PIO0	C11	PIO	PIO	0	—
PIO0	C13	PIO	PIO	0	—
PIO0	C14	PIO	PIO	0	—
PIO0	C15	PIO	PIO	0	—
PIO0	C16	PIO	PIO	0	—
PIO0	C17	PIO	PIO	0	—
PIO0	C18	PIO	PIO	0	—
PIO0	C19	PIO	PIO	0	—
PIO0	E5	PIO	PIO	0	A1
PIO0	E6	PIO	PIO	0	A2
PIO0	E7	PIO	PIO	0	A3
PIO0	E8	PIO	PIO	0	A4
PIO0	E9	PIO	PIO	0	A5
PIO0	E14	PIO	PIO	0	A10

Die Cross Reference

The tables in this section list all the pads on a specific die type and provide a cross reference on how a specific pad connects to a ball or pin in each of the available package offerings. Similarly, the tables provide the pad coordinates for the die-based version of the product (DiePlus). These tables also provide a way to prototype with one package option and then later move to a different package or die.

As described in "Input and Output Register Control per PIO Pair" on page 16, PIO pairs share register control inputs. Similarly, as described in "Differential Inputs and Outputs" on page 12, a PIO pair can form a differential input or output. PIO pairs in I/O Bank 3 are optionally differential inputs or differential outputs. PIO pairs in all other I/O Banks are optionally differential outputs. In the tables, differential pairs are surrounded by a heavy blue box.

iCE65L04

Table 45 lists all the pads on the iCE65L04 die and how these pads connect to the balls or pins in the supported package styles. Most VCC, VCCIO, and GND pads are double-bonded inside the package although the table shows only a single connection.

For additional information on the iCE65L04 DiePlus product, please refer to the following data sheet.

DiePlus Advantage FPGA Known Good Die

Table 45: iCE65L04 Die Cross Reference

iCE65L04 Pad Name	VQ100	CB132	CB196	CB284	DiePlus Pad	X (µm)	Y (µm)
PIO3_00/DP00A	1	B1	C1	F5	1	129.40	2,687.75
PIO3_01/DP00B	2	C1	B1	G5	2	231.40	2,642.74
PIO3_02/DP01A	3	C3	D3	G7	3	129.40	2,597.75
PIO3_03/DP01B	4	D3	C3	H7	4	231.40	2,552.74
GND	5	F1	F1	K5	5	129.40	2,507.75
GND	—	—	—	—	6	231.40	2,462.74
VCCIO_3	6	E3	E3	J7	7	129.40	2,417.75
VCCIO_3	—	—	—	—	8	231.40	2,372.74
PIO3_04/DP02A	7	D4	D1	H8	9	129.40	2,327.75
PIO3_05/DP02B	8	E4	D2	J8	10	231.40	2,292.74
PIO3_06/DP03A	—	D1	E1	H5	11	129.40	2,257.75
PIO3_07/DP03B	—	E1	E2	J5	12	231.40	2,222.74
VCC	—	—	H9	D3	13	129.40	2,187.75
PIO3_08/DP04A	9	F4	D4	K8	14	231.40	2,152.74
PIO3_09/DP04B	10	F3	E4	K7	15	129.40	2,117.75
PIO3_10/DP05A	—	—	F3	E3	16	231.40	2,082.74
PIO3_11/DP05B	—	—	F4	F3	17	129.40	2,047.75
GND	—	H6	A9	M10	18	231.40	2,012.74
PIO3_12/DP06A	—	—	F5	G3	19	129.40	1,977.75
PIO3_13/DP06B	—	—	E5	H3	20	231.40	1,942.74
GND	—	—	A9	J3	21	129.40	1,907.75
GND	—	—	—	—	22	231.40	1,872.74
PIO3_14/DP07A	—	—	—	H1	23	129.40	1,837.75
PIO3_15/DP07B	—	—	—	J1	24	231.40	1,802.74
VCCIO_3	—	—	K1	K3	25	129.40	1,767.75
VCC	11	G6	G6	L10	26	231.40	1,732.74
PIO3_16/DP08A	—	—	—	K1	27	129.40	1,697.75
PIO3_17/DP08B	—	—	—	L1	28	231.40	1,662.74

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO3_44/DP22A	M1	U3	86	231.735	777.67
PIO3_45/DP22B	M2	V3	87	129.735	732.67
PIO3_46/DP23A	N1	U5	88	231.735	687.67
PIO3_47/DP23B	N2	V5	89	129.735	642.67
PIO3_48/DP24A	—	W3	90	231.735	597.67
PIO3_49/DP24B	—	Y3	91	129.735	552.665
PIO2_00	P1	AB2	92	510.0	139.5
PIO2_01	M3	R8	93	560.0	37.5
PIO2_02	P2	Y4	94	610.0	139.5
GND	P6	AB5	95	660.0	37.5
GND	—	—	96	710.0	139.5
PIO2_03	M4	T7	97	760.0	37.5
PIO2_04	N3	AB3	98	810.0	139.5
PIO2_05	—	R9	99	859.3	37.5
PIO2_06	—	Y5	100	910.0	139.5
PIO2_07	L4	T8	101	960.0	37.5
PIO2_08	P3	V6	102	1,012.5	139.5
VCCIO_2	M5	T9	103	1,047.5	37.5
VCCIO_2	—	—	104	1,082.5	139.5
PIO2_09	P4	R10	105	1,117.5	37.5
PIO2_10	N4	AB4	106	1,152.5	139.5
GND	H8	V10	107	1,187.5	37.5
GND	—	—	108	1,222.5	139.5
PIO2_11	K5	V7	109	1,257.5	37.5
PIO2_12	P5	Y7	110	1,292.5	139.5
PIO2_13	—	V9	111	1,327.5	37.5
PIO2_14	—	Y6	112	1,362.5	139.5
PIO2_15	—	AB7	113	1,397.5	37.5
PIO2_16	—	AB6	114	1,432.5	139.5
PIO2_17	L5	Y9	115	1,467.5	37.5
PIO2_18	N5	V8	116	1,502.3	139.5
GND	P6	N12	117	1,537.3	37.5
GND	—	—	118	1,572.5	139.5
PIO2_19	N6	AB8	119	1,607.5	37.5
PIO2_20	K6	AB9	120	1,642.5	139.5
VCC	J7	Y8	121	1,677.5	37.5
VCC	—	—	122	1,712.5	139.5
PIO2_21	L6	T10	123	1,747.5	37.5
PIO2_22	M6	AB10	124	1,782.5	139.5
PIO2_23	—	AB11	125	1,817.5	37.5
PIO2_24	—	AB12	126	1,852.5	139.5
PIO2_25	L7	Y10	127	1,887.5	37.5
PIO2_26	P7	AB13	128	1,922.5	139.5
PIO2_27	K7	AB14	129	1,957.5	37.5
VCCIO_2	N10	Y11	130	1,992.5	139.5
VCCIO_2	—	—	131	2,027.5	37.5

Electrical Characteristics

All parameter limits are specified under worst-case supply voltage, temperature, and processing conditions.

Absolute Maximum Ratings

Stresses beyond those listed under Table 47 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 47: Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
VCC	Core supply Voltage	–0.5	1.42	V
VPP_2V5	VPP_2V5 NVCM programming and operating supply			V
VPP_FAST	Optional fast NVCM programming supply			V
VCCIO_0 **VCCIO_1** **VCCIO_2** **SPI_VCC**	I/O bank supply voltage (I/O Banks 0, 1, and 2 plus SPI interface)	–0.5	4.00	V
VCCIO_3	I/O Bank 3 supply voltage	–0.5	iCE65L01: 4.00 iCE65L04/08: 3.6	V
VIN_0 **VIN_1** **VIN_2** **VIN_SPI**	Voltage applied to PIO pin within a specific I/O bank (I/O Banks 0, 1, and 2 plus SPI interface)	–1.0	5.5	V
VIN_3 **VIN_VREF**	Voltage applied to PIO pin within I/O Bank 3	–0.5	iCE65L01: 4.00 iCE65L04/08: 3.6	V
IOUT	DC output current per pin	—	20	mA
T_J	Junction temperature	–55	125	°C
T_{STG}	Storage temperature, no bias	–65	150	°C

Recommended Operating Conditions

Table 48: **Recommended Operating Conditions**

Symbol	Description		Minimum	Nominal	Maximum	Units
VCC	Core supply voltage	–L: Ultra-Low Power mode	0.95	1.00	1.05	V
		–L: Low Power –T: High Performance	1.14	1.20	1.26	V
VPP_2V5	VPP_2V5 NVCM programming and operating supply	Release from Power-on Reset	1.30	—	3.47	V
		Configure from NVCM	2.30	—	3.47	V
		NVCM programming	2.30	—	3.00	V
VPP_FAST	Optional fast NVCM programming supply		Leave unconnected in application			
SPI_VCC	SPI interface supply voltage		1.71	—	3.47	V
VCCIO_0 VCCIO_1 VCCIO_2 VCCIO_3 SPI_VCC	I/O standards, all banks*	**LVCMOS33**	3.14	3.30	3.47	V
		Non-standard voltage: in between 2.5V and 3.3V use LVCMOS25 in iCEcube2	Nominal -5%	2.5< Nominal <3.3	Nominal +5%	V
		LVCMOS25, LVDS	2.38	2.50	2.63	V
		LVCMOS18, SubLVDS	1.71	1.80	1.89	V
		LVCMOS15	1.43	1.50	1.58	V
VCCIO_3	I/O standards only available in iCE65L04/08 I/O Bank 3*	**SSTL2**	2.38	2.50	2.63	V
		SSTL18	1.71	1.80	1.89	V
		MDDR	1.71	1.80	1.89	V
T_A	Ambient temperature	Commercial (C)	0	—	70	°C
		Industrial (I)	–40	—	85	°C
T_{PROG}	NVCM programming temperature		10	25	30	°C

NOTE:

VPP_FAST is only used for fast production programming. Leave floating or unconnected in application. When the iCE65 device is active, VPP_2V5 must be connected to a valid voltage.

Programmable Input/Output (PIO) Block

Table 55 provides timing information for the logic in a Programmable Logic Block (PLB), which includes the paths shown in Figure 57 and Figure 58. The timing shown is for the LVCMOS25 I/O standard in all I/O banks. The iCEcube development software reports timing adjustments for other I/O standards.

Figure 57: Programmable I/O (PIO) Pad-to-Pad Timing Circuit

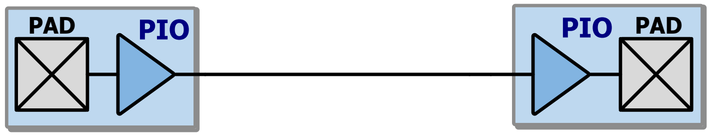


Figure 58: Programmable I/O (PIO) Sequential Timing Circuit

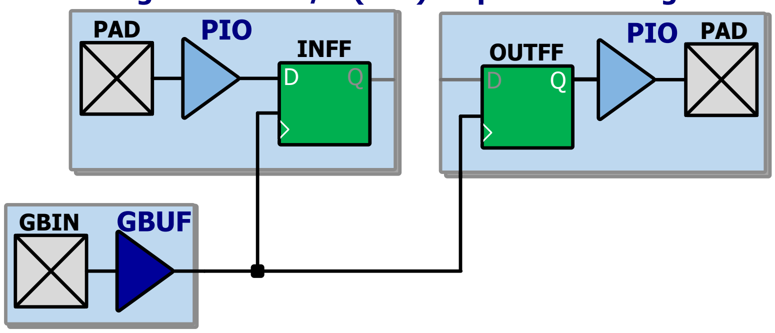


Table 55: Typical Programmable Input/Output (PIO) Timing (LVCMOS25)

Symbol	From	To	Description	L01	L04, L08			Units
			Device: iCE65	L01	L04, L08			
			Power/Speed Grad	–T	–L		–T	
			Nominal VCC	1.2 V	1.0 V	1.2 V	1.2 V	
			Description	Typ.	Typ.	Typ.	Typ.	
		Synchronous Output Paths						
t_{OCKO}	OUTFF clock input	PIO output	Delay from clock input on OUTFF output flip-flop to PIO output pad.	4.7	13.8	7.3	5.6	ns
t_{GBCKIO}	GBIN input	OUTFF clock input	Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to clock input on the PIO OUTFF output flip-flop.	2.1	7.3	3.8	2.6	ns
		Synchronous Input Paths						
t_{SUPDIN}	PIO input	GBIN input	Setup time on PIO input pin to INFF input flip-flop before active clock edge on GBIN input, including interconnect delay.	0	0	0	0	ns
t_{HDPDIN}	GBIN input	PIO input	Hold time on PIO input to INFF input flip-flop after active clock edge on the GBIN input, including interconnect delay.	2.7	7.1	3.6	2.8	ns
		Pad to Pad						
t_{PADIN}	PIO input	Inter-connect	Asynchronous delay from PIO input pad to adjacent interconnect.	2.5	9.5	5.0	3.2	ns
t_{PADO}	Inter-connect	PIO output	Asynchronous delay from adjacent interconnect to PIO output pad including interconnect delay.	4.5	14.6	7.7	6.2	ns

Revision History

Version	Date	Description
2.42	30-MAR-2012	Changed company name. Updated Table 1
2.41	1-AUG-2011	Added VQ100 marking for NVCM programming.
2.4	13-MAY-2011	Added L01 CB121 package Figure 39. Added note "else VCCIO_1 draws current" to JTAG inputs TCK, TDI and TMS do not have the input pull-up resistor and must be tied off to GND when unused, Table 32. Input pin leakage current Table 49 split by bank. QN84 package drawing, Figure 35, added note "underside metal is at ground potential", increased thermal resistance. Added Marking Format and Thermal resistance to CB81 Packag Mechanical Drawing Figure 33. Added coplanarity specification to VQ100 Package Mechanical Drawing Figure 37
2.3	18-OCT-2010	Added L01 CB81 and L08 CB132 packages.
2.2.3	12-OCT-2010	Changed Figure 29: Application Processor Waveforms for SPI Peripheral Mode Configuration Process and Table 60 from 300 µs CRESET_B to 800 µs for iCE65L01/04 and 1200 µs for iCE65L08.
2.2.2	8-OCT-2010	Added iCE65L04 marking specification to Figure 47 CB196 Package Mechanical Drawing.
2.2.1	5-OCT-2010	Changed FSPI_SCK from 0.125 MHz to 1 MHz in SPI Peripheral Configuration Interface and in Table 60.
2.2	6-AUG-2010	Programmable Interconnect section removed.
2.1.1	26-MAY-2010	Switched labels on Figure 53 LVCMOS Output High, VCCIO = 1.8V with VCCIO = 2.5V.
2.1	15-MAR-2010	Added JTAG unused input tie off guideline. Added marking specification and thermal characteristics to package drawings. Added production datasheet for iCE65L01 with timing update, including QN84, VQ100 and CB132. Added NVCM shut-off on SPI configuration. Added non-standard VCCIO operating conditions. Increased the minimum voltage supply specification for LVCMOS33 to 3.14V in Table 48.
2.0.1	12-NOV-2009	Recommended Operation Conditions, Table 47, replaced junction with ambient.
2.0	14-SEPT-2009	Finalized production data sheet for iCE65L04 and iCE65L08. Improved SubLVDS input specification V_{ICM} in Table 52. CS63 and CC72 packages removed and placed in iCE DiCE KGD, Known Good Die datasheet. Added "IBIS Models for I/O Banks 0, 1, 2 and the SPI Bank". Added "Printed Circuit Board Layout Information".
1.5.1	13-JUL-2009	Updated the text in "SPI PROM Requirements" section. Minor label change in Figure 48.
1.5	20-JUN-2009	Updated timing information and added –T high-speed device option (affected Figure 2, Table 48, Table 54, Table 55, Table 56, and Table 61). Added support for 3.3V LVCMOS I/Os in I/O Bank 3 (affected Figure 7, Table 5, Table 7, Table 8, Table 47, Table 48, and Table 51). Added a section about the SPI Peripheral Configuration Interface and timing in Table 60. Added a warning that a Warm Boot operation can only jump to another configuration image that has Warm Boot disabled. Updated configuration image size and configuration time for the iCE65L02 in Table 27 and Table 58. Reduced the minimum voltage supply specification for LVCMOS33 to 2.7V in Table 48. Added information about which power rails can be disconnected without effecting the Power-On Reset (POR) circuit and clarified description of VPP_2V5 pin in Table 36. Added I/O characterization curves (Figure 52, Figure 53, and Figure 54). Minor changes to Figure 20 and Figure 21. Changed timing per Figures 54-58 and Tables 55-57.
1.4.4	25-MAR-2009	Clarified the voltage requirements for the VPP_2V5 pin in Table 36 and notes under Table 48.
1.4.3	9-MAR-2009	Removed volatile-only (-V) product offering from Figure 2. Corrected NC on ball V22, removed it for ball T22 on CB284 package (Figure 48).
1.4.2	27-FEB-2009	Updated Table 14, Table 23, Table 26, Table 30, Table 33, Table 35, and Table 46. Updated I/O Bank 3 information in Table 7 and Table 48.
1.4.1	24-FEB-2009	Based on characterization data, reduced 32KHz operating current by 40% in Table 1, Table 61, and Figure 1. Corrected that SSTL18 standards require VREF pin in Table 7. Correct ball numbers for GBIN4/GBIN5 for CS110 package.
1.4	9-FEB-2009	Added footprint and pinout information for the VQ100 Very-thin Quad Flat Package. Added footprint for iCE65L08 in CB196 (Figure 46) and added Table 43 showing the differences between the 'L04 and 'L08 in the CB196 package. Unified the package footprint nomenclature in the Package and Pinout Information section. Added note to Global Buffer Inputs that the differential clock direct input is not available on the CB132 package. Added tables showing the ball/pin number for various control functions, by package (Table 14, Table 23, Table 26, Table 30, and Table 33). Corrected the GBIN/GBUF designations. GBIN4 and GBIN5 were swapped as were GBIN6 and GBIN7. This change affected all pinout tables and footprint diagrams. Updated and corrected "Differential Global Buffer Input." Tested and corrected the clock-enable and reset connections between global buffers and various resources (Table 11, Table 12, and Table 13). Added "Automatic Global Buffer Insertion, Manual Insertion." Added "Die Cross Reference" section. Improved industrial temperature range by lowering