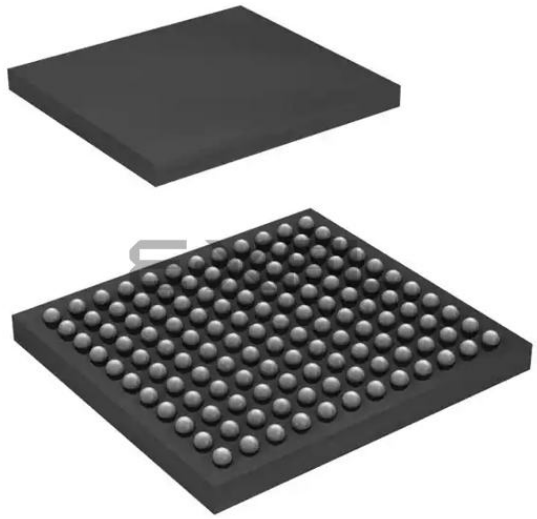
Lattice Semiconductor Corporation - ICE65L04F-TCB132C Datasheet



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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	440
Number of Logic Elements/Cells	3520
Total RAM Bits	81920
Number of I/O	95
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	132-VFBGA, CSPBGA
Supplier Device Package	132-CSBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice65l04f-tcb132c

Overview

The Lattice Semiconductor iCE65 programmable logic family is specifically designed to deliver the lowest static and dynamic power consumption of any comparable CPLD or FPGA device. iCE65 devices are designed for cost-sensitive, high-volume applications and provide on-chip, nonvolatile configuration memory (NVCM) to customize for a specific application. iCE65 devices can self-configure from a configuration image stored in an external commodity SPI serial Flash PROM or be downloaded from an external processor over an SPI-like serial port.

The three iCE65 components, highlighted in Table 1, deliver from approximately 1K to nearly 8K logic cells and flip-flops while consuming a fraction of the power of comparable programmable logic devices. Each iCE65 device includes between 16 to 32 RAM blocks, each with 4Kbits of storage, for on-chip data storage and data buffering.

As pictured in Figure 1, each iCE65 device consists of four primary architectural elements.

- An array of Programmable Logic Blocks (PLBs)
  - Each PLB contains eight Logic Cells (LCs); each Logic Cell consists of ...
    - A fast, four-input look-up table (LUT4) capable of implementing any combinational logic function of up to four inputs, regardless of complexity
    - A 'D'-type flip-flop with an optional clock-enable and set/reset control
    - Fast carry logic to accelerate arithmetic functions such as adders, subtracters, comparators, and counters.
  - Common clock input with polarity control, clock-enable input, and optional set/reset control input to the PLB is shared among all eight Logic Cells
- Two-port, 4Kbit RAM blocks (RAM4K)
  - 256x16 default configuration; selectable data width using programmable logic resources
  - Simultaneous read and write access; ideal for FIFO memory and data buffering applications
  - RAM contents pre-loadable during configuration
- Four I/O banks with independent supply voltage, each with multiple Programmable Input/Output (PIO) blocks
  - LVCMOS I/O standards and LVDS outputs supported in all banks
  - I/O Bank 3 supports additional SSTL, MDDR, LVDS, and SubLVDS I/O standards
- Programmable interconnections between the blocks
  - Flexible connections between all programmable logic functions
  - Eight dedicated low-skew, high-fanout clock distribution networks

Look-Up Table (LUT4)

The four-input Look-Up Table (LUT4) function implements any and all combinational logic functions, regardless of complexity, of between zero and four inputs. Zero-input functions include "High" (1) and "Low" (0). The LUT4 function has four inputs, labeled I0, I1, I2, and I3. Three of the four inputs are shared with the Carry Logic function, as shown in Figure 4. The bottom-most LUT4 input connects either to the I3 input or to the Carry Logic output from the previous Logic Cell.

The output from the LUT4 function connects to the flip-flop within the same Logic Cell. The LUT4 output or the flip-flop output then connects to the programmable interconnect.

For detailed LUT4 internal timing, see Table 54.

'D'-style Flip-Flop (DFF)

The 'D'-style flip-flop (DFF) optionally stores state information for the application.

The flip-flop has a data input, 'D', and a data output, 'Q'. Additionally, each flip-flop has up to three control signals that are shared among all flip-flops in all Logic Cells within the PLB, as shown in Figure 4. Table 3 describes the behavior of the flip-flop based on inputs and upon the specific DFF design primitive used or synthesized.

Table 3: 'D'-Style Flip-Flop Behavior

DFF Primitive	Operation	Flip-Flop Mode	Inputs				Output
			D	EN	SR	CLK	Q
All	Cleared Immediately after Configuration	X	X	X	X	X	0
	Hold Present Value (Disabled)		X	0	X	X	Q
	Hold Present Value (Static Clock)		X	X	X	1 or 0	Q
	Load with Input Data		D	1*	0*	↑	D
SB_DFFR	Asynchronous Reset	Asynchronous Reset	X	X	1	X	0
SB_DFFS	Asynchronous Set	Asynchronous Set	X	X	1	X	1
SB_DFFSR	Synchronous Reset	Synchronous Reset	X	1*	1	↑	0
SB_DFFSS	Synchronous Set	Synchronous Set	X	1*	1	↑	1

X = don't care, ↑ = rising clock edge (default polarity), 1* = High or unused, 0* = Low or unused

The CLK clock signal is not optional and is shared among all flip-flops in a Programmable Logic Block. By default, flip-flops are clocked by the rising edge of the PLB clock input, although the clock polarity can be inverted for all the flip-flops in the PLB.

The CLK input optionally connects to one of the following clock sources.

- The output from any one of the eight Global Buffers, or
- A connection from the general-purpose interconnect fabric

The EN clock-enable signal is common to all Logic Cells in a Programmable Logic Block. If the enable signal is not used, then the flip-flop is always enabled. This condition is indicated as "1*" in Table 3. The asterisk indicates that this is the default state if the control signal is not connected in the application.

Similarly, the SR set/reset signal is common to all Logic Cells in a Programmable Logic Block. If not used, then the flip-flop is never set/reset, except when cleared immediately after configuration or by the Global Reset signal. This condition is indicated as "0*" in Table 3. The asterisk indicates that this is the default state if the control signal is not connected in the application.

If not connected to an external SPI PROM, the four pins associated with the SPI Master Configuration Interface can be used as PIO pins, supplied by the SPI_VCC input, essentially forming a fifth "mini" I/O bank. If using an SPI Flash PROM, then connect SPI_VCC to 3.3V.

I/O Banks 0, 1, 2, SPI and Bank 3 of iCE65L01

Table 6 highlights the available I/O standards when using an iCE65 device, indicating the drive current options, and in which bank(s) the standard is supported. I/O Banks 0, 1, 2 and SPI interface support the same standards. I/O Bank 3 has additional capabilities in iCE65L04 and iCE65L08, including support for MDDR memory standards and LVDS differential I/O.

***Table 6:* I/O Standards for I/O Banks 0, 1, 2, SPI Interface Bank, and Bank 3 of iCE65L01**

I/O Standard	Supply Voltage	Drive Current (mA)	Attribute Name
5V Input Tolerance	3.3V	N/A	N/A
LVCMOS33	3.3V	±11	SB_LVCMOS
LVCMOS25	2.5V	±8	
LVCMOS18	1.8V	±5	
LVCMOS15 outputs	1.5V	±4	

IBIS Models for I/O Banks 0, 1, 2 and the SPI Bank

The IBIS (I/O Buffer Information Specification) file that describes the output buffers used in I/O Banks 0, 1, 2, SPI Bank and Bank 3 of iCE65L01 is available from the following link.

- IBIS Models for I/O Banks 0, 1, 2, SPI Bank and Bank 3 of iCE65L01

I/O Bank 3 of iCE65L04 and iCE65L08

I/O Bank 3, located along the left edge of the die, has additional special I/O capabilities to support memory components and differential I/O signaling (LVDS). Table 7 lists the various I/O standards supported by I/O Bank 3. The SSTL2 and SSTL18 I/O standards require the VREF voltage reference input pin which is only available on the CB284 package. Also see Table 51 for electrical characteristics.

***Table 7:* I/O Standards for I/O Bank 3 Only of iCE65L04 and iCE65L08**

I/O Standard	Supply Voltage	VREF Pin (CB284 or DiePlus) Required?	Target Drive Current (mA)	Attribute Name
LVCMOS33	3.3V	No	±8	SB_LVCMOS33_8
LVCMOS25	2.5V	No	±16	SB_LVCMOS25_16
			±12	SB_LVCMOS25_12
			±8	SB_LVCMOS25_8
			±4	SB_LVCMOS25_4
LVCMOS18	1.8V	No	±10	SB_LVCMOS18_10
			±8	SB_LVCMOS18_8
			±4	SB_LVCMOS18_4
			±2	SB_LVCMOS18_2
LVCMOS15	1.5V	No	±4	SB_LVCMOS15_4
			±2	SB_LVCMOS15_2
SSTL2_II	2.5V	Yes	±16.2	SB_SSTL2_CLASS_2
SSTL2_I			±8.1	SB_SSTL2_CLASS_1
SSTL18_II	1.8V	Yes	±13.4	SB_SSTL18_FULL
SSTL18_I			±6.7	SB_SSTL18_HALF
MDDR	1.8V	No	±10	SB_MDDR10
			±8	SB_MDDR8
			±4	SB_MDDR4
			±2	SB_MDDR2
LVDS	2.5V	No	N/A	SB_LVDS_INPUT

Input Signal Path

As shown in Figure 7, a signal from a package pin optionally feeds directly into the device, or is held in an input register. The input signal connects to the programmable interconnect resources through the IN signal. Table 9 describes the input behavior, assuming that the output path is not used or if a bidirectional I/O, that the output driver is in its high-impedance state (Hi-Z). Table 9 also indicates the effect of the Power-Saving I/O Bank iCEgate Latch and the Input Pull-Up Resistors on I/O Banks 0, 1, and 2.

See Input and Output Register Control per PIO Pair for information about the registered input path.

Power-Saving I/O Bank iCEgate Latch

To save power, the optional iCEgate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Registered inputs are effectively frozen by their associated clock or clock-enable control. As shown in Figure 10, the iCEgate HOLD control signal captures the external value from the associated asynchronous input. The HOLD signal prevents switching activity on the PIO pad from affecting internal logic or programmable interconnect. Minimum power consumption occurs when there is no switching. However, individual pins within the I/O bank can bypass the iCEgate latch and directly feed into the programmable interconnect, remaining active during low-power operation. This behavior is described in Table 9. The decision on which asynchronous inputs use the iCEgate feature and which inputs bypass it is determined during system design. In other words, the iCEgate function is part of the source design used to create the iCE65 configuration image.

Figure 10: Power-Saving iCEgate Latch

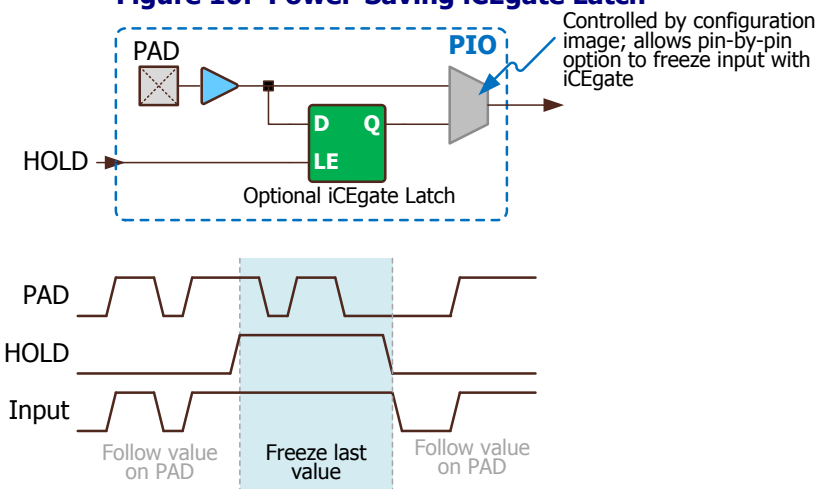


***Table 9:* PIO Non-Registered Input Operations**

Operation	HOLD	Bitstream Setting		PAD	IN
	iCEgate Latch	Controlled by iCEgate?	Input Pull-Up Enabled?	Pin Value	Input Value to Interconnect
Data Input	0	X	X	PAD	PAD Value
Pad Floating, No Pull-up	0	X	No	Z	(Undefined)
Pad Floating, Pull-up	0	X	Yes	Z	1
Data Input, Latch Bypassed	X	No	X	PAD	PAD Value
Pad Floating, No Pull-up, Latch Bypassed	X	No	No	Z	(Undefined)
Pad Floating, Pull-up, Latch Bypassed	X	No	Yes	Z	1
Low Power Mode, Hold Last Value	1	Yes	X	X	Last Captured PAD Value

There are four iCEgate HOLD controls, one per each I/O bank. The iCEgate HOLD control input originates within the interconnect fabric, near the middle of the I/O edge. Consequently, the HOLD signal is optionally controlled externally through a PIO pin or from other logic within the iCE65 device.

For best possible performance, the global buffer inputs (GBIN[7:0]) connect directly to the their associated global buffers (GBUF[7:0]), bypassing the PIO logic and iCEgate circuitry as shown in Figure 7. Consequently, the direct GBIN-to-GBUF connection cannot be blocked by the iCEgate circuitry. However, it is possible to use iCEgate to block PIO-to-GBUF clock connections.

For additional information on using the iCEgate feature, please refer to the following application note.

AN002: Using iCEgate Blocking for Ultra-Low Power

Input Pull-Up Resistors on I/O Banks 0, 1, and 2

The PIO pins in I/O Banks 0, 1, and 2 have an optional input pull-up resistor. Pull-up resistors are not provided in iCE65L04 and iCE65L08 I/O Bank 3. During the iCE65 configuration process, the input pull-up resistor is unconditionally enabled and pulls the input to within a diode drop of the associated I/O bank supply voltage (VCCIO_#). This prevents any signals from floating on the circuit board during configuration.

After iCE65 configuration is complete, the input pull-up resistor is optional, defined by a configuration bit. The pull-up resistor is also useful to tie off unused PIO pins. The Lattice iCEcube development software defines all unused PIO pins in I/O Banks 0, 1 and 2 as inputs with the pull-up resistor turned on. The pull-up resistor value depends on the VCCIO voltage applied to the bank, as shown in Table 49.

Note: JTAG inputs TCK, TDI and TMS do not have the input pull-up resistor and must be tied off to GND when unused, else VCCIO_1 draws current.

No Input Pull-up Resistors on I/O Bank 3 of iCE65L04 and iCE65L08

The PIO pins in I/O Bank 3 do not have an internal pull-up resistor. To minimize power consumption, tie unused PIO pins in Bank 3 to a known logic level or drive them as a disabled high-impedance output.

Input Hysteresis

Inputs typically have about 50 mV of hysteresis, as indicated in Table 49.

Output and Output Enable Signal Path

As shown in Figure 7, a signal from programmable interconnect feeds the OUT signal on a Programmable I/O pad. This output connects either directly to the associated package pin or is held in an optional output flip-flop. Because all flip-flops are automatically reset after configuration, the output from the output flip-flop can be optionally inverted so that an active-Low output signal is held in the disabled (High) state immediately after configuration.

Similarly, each Programmable I/O pin has an output enable or three-state control called OE. When OE = High, the OUT output signal drives the associated pad, as described in Table 10. When OE = Low, the output driver is in the high-impedance (Hi-Z) state. The OE output enable control signal itself connects either directly to the output buffer or is held in an optional register. The output buffer is optionally permanently enabled or permanently disabled, either to unconditionally drive output signals, or to allow input-only signals.

Table 10: **PIO Output Operations (non-registered operation, no inversions)**

Operation	OUT Data Output	OE Enable	PAD
Three-State	X	0	Hi-Z
Drive Output Data	OUT	1*	OUT

X = don't care, 1* = High or unused, Hi-Z = high-impedance, three-stated, floating.

See Input and Output Register Control per PIO Pair for information about the registered input path.

Global Routing Resources

Global Buffers

Each iCE65 component has eight global buffer routing connections, illustrated in Figure 14. There are eight high-drive buffers, connected to the eight low-skew, global lines. These lines are designed primarily for clock distribution but are also useful for other high-fanout signals such as set/reset and enable signals. The global buffers originate either from the Global Buffer Inputs (GBINx) or from programmable interconnect. The associated GBINx pin represents the best pin to drive a global buffer from an external source. However, the application with an iCE65 FPGA can also drive a global buffer via any other PIO pin or from internal logic using the programmable interconnect.

If not used in an application, individual global buffers are turned off to save power.

Figure 14: **High-drive, Low-skew, High-fanout Global Buffer Routing Resources**

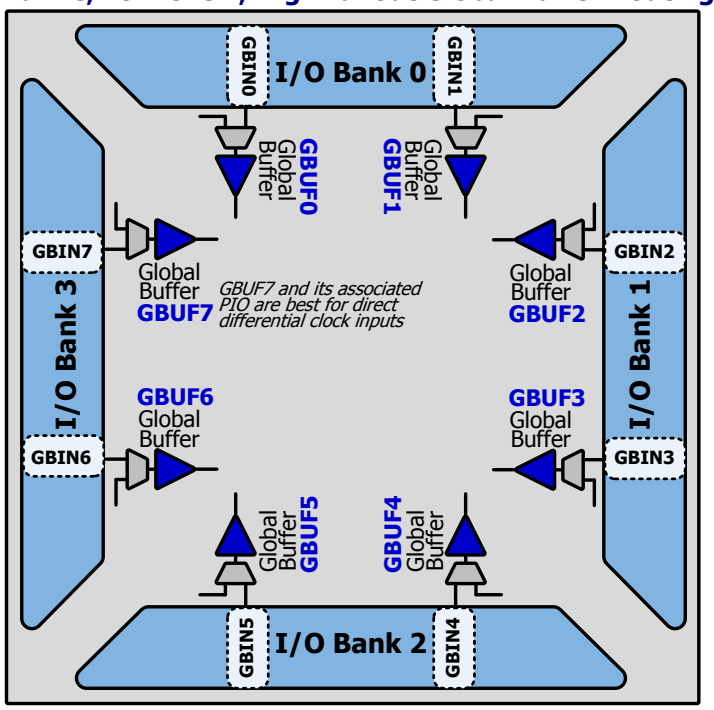
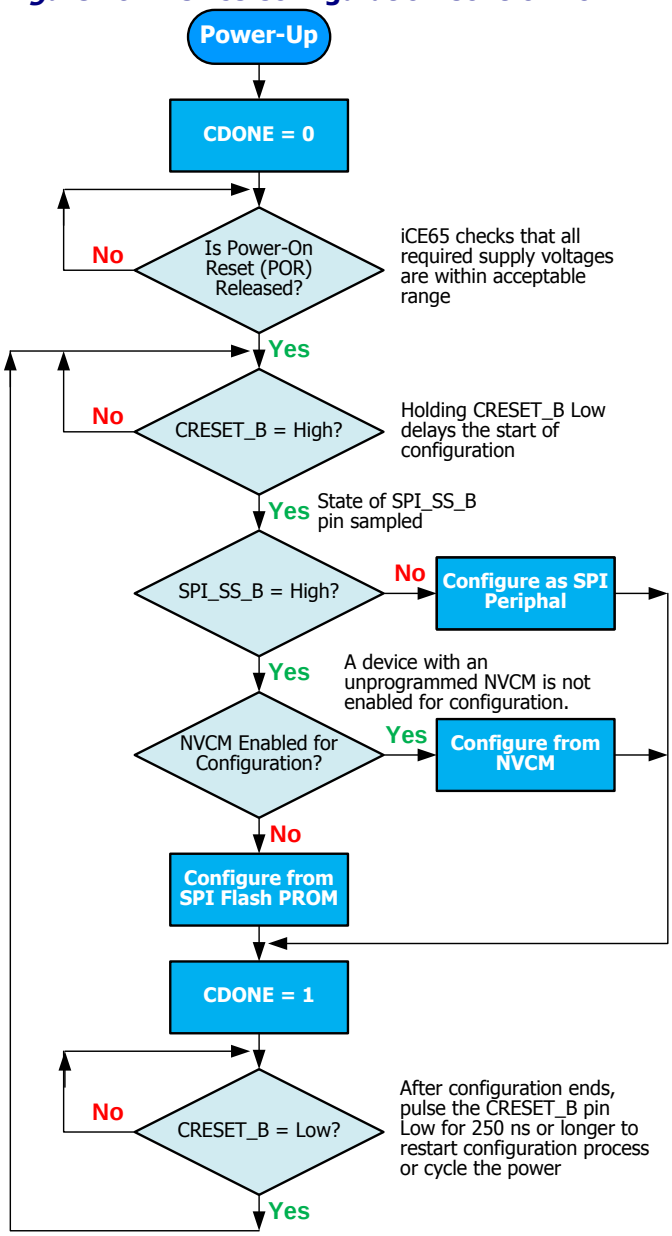


Table 11 lists the connections between a specific global buffer and the inputs on a Programmable Logic Block (PLB). All global buffers optionally connect to all clock inputs. Any four of the eight global buffers can drive logic inputs to a PLB. Even-numbered global buffers optionally drive the Reset input to a PLB. Similarly, odd-numbered buffers optionally drive the PLB clock-enable input.

Table 11: **Global Buffer (GBUF) Connections to Programmable Logic Block (PLB)**

Global Buffer	LUT Inputs	Clock	Clock Enable	Reset
GBUF0	Yes, any 4 of 8 GBUF buffers	Yes	Yes	No
GBUF1		Yes	No	Yes
GBUF2		Yes	Yes	No
GBUF3		Yes	No	Yes
GBUF4		Yes	Yes	No
GBUF5		Yes	No	Yes
GBUF6		Yes	Yes	No
GBUF7		Yes	No	Yes

Figure 20: **Device Configuration Control Flow**



Configuration Image Size

Table 23 shows the number of memory bits required to configure an iCE65 device. Two values are provided for each device. The "Logic Only" value indicates the minimum configuration size, the number of bits required to configure only the logic fabric, leaving the RAM4K blocks uninitialized. The "Logic + RAM4K" column indicates the maximum configuration size, the number of bits to configure the logic fabric and to pre-initialize all the RAM4K blocks.

- For lowest possible power consumption after configuration, the PROM should also support the 0xB9 Deep Power Down command and the 0xAB Release from Deep Power-down Command (see Figure 24 and Figure 26). The low-power mode is optional.
- The PROM must be ready to accept commands 10 µs after meeting its power-on conditions. In the PROM data sheet, this may be specified as t_{VSL} or t_{VCSL}. It is possible to use slower PROMs by holding the CRESET_B input Low until the PROM is ready, then releasing CRESET_B, either under program control or using an external power-on reset circuit.

The Lattice iCEman65 development board and associated programming software uses an ST Micro/Numonyx M25Pxx SPI serial Flash PROM.

SPI PROM Size Requirements

Table 27 lists the minimum SPI PROM size required to configure an iCE65 device. Larger PROM sizes are allowed, but not required unless the end application uses the additional space. SPI serial PROM sizes are specified in bits. For each device size, the table shows the required minimum PROM size for "Logic Only" (no BRAM initialization) and "Logic + RAM4K" (RAM4K blocks pre-initialized). Furthermore, the table shows the PROM size for varying numbers of configuration images. Most applications will use a single image. Applications that use the Cold Boot or Warm Boot features may use more than one image.

Table 27: Smallest SPI PROM Size (bits), by Device, by Number of Images

Device	1 Image		2 Images		3 Images		4 Images	
	Logic Only	**Logic + RAM4K**	**Logic Only**	**Logic + RAM4K**	**Logic Only**	**Logic + RAM4K**	**Logic Only**	**Logic + RAM4K**
iCE65L01	256K	256K	512K	512K	1M	1M	1M	1M
iCE65L04	512K	1M	1M	2M	2M	2M	2M	4M
iCE65L08	1M	2M	2M	4M	4M	4M	4M	8M

Enabling SPI Configuration Interface

To enable the SPI configuration mode, the SPI_SS_B pin must be allowed to float High. The SPI_SS_B pin has an internal pull-up resistor. If SPI_SS_B is Low, then the iCE65 component defaults to the SPI Slave configuration mode.

SPI Master Configuration Process

The iCE65 SPI Master Configuration Interface supports a variety of modern, high-density, low-cost SPI serial Flash PROMs. Most modern SPI PROMs include a power-saving Deep Power-down mode. The iCE65 component exploits this mode for additional system power savings.

The iCE65 SPI interface starts by driving SPI_SS_B Low, and then sends a Release from Power-down command to the SPI PROM, hexadecimal command code 0xAB. Figure 24 provides an example waveform. This initial command wakes up the SPI PROM if it is already in Deep Power-down mode. If the PROM is not in Deep Power-down mode, the extra command has no adverse affect other than that it requires a few additional microseconds during the configuration process. The iCE65 device transmits data on the SPI_SO output, on the falling edge of the SPI_SCK output. The SPI PROM does not provide any data to the iCE65 device's SPI_SI input. After sending the last command bit, the iCE65 device de-asserts SPI_SS_B High, completing the command. The iCE65 device then waits a minimum of 10 µS before sending the next SPI PROM command.

Table 28: **ColdBoot Select Ball/Pin Numbers by Package**

ColdBoot Select	CB81	QN84	VQ100	CB132	CB196	CB284
PIO2/CBSEL0	G5	B15	41	L9	L9	R13
PIO2/CBSEL1	H5	A20	42	P10	P10	V14

When creating the initial configuration image, the Lattice development software loads the start address for up to four configuration images in the bitstream. The value on the CBSEL[1:0] pins tell the configuration controller to read a specific start address, then to load the configuration image stored at the selected address. The multiple bitstreams are stored either in the SPI Flash or in the internal NVCM.

After configuration, the CBSEL[1:0] pins become normal PIO pins available to the application.

The Cold Boot feature allows the iCE65 to be reprogrammed for special application requirements such as the following.

- A normal operating mode and a self-test or diagnostics mode.
- Different applications based on switch settings.
- Different applications based on a card-slot ID number.

Warm Boot Configuration Option

The Warm Boot configuration is similar to the Cold Boot feature, but is completely under the control of the FPGA application.

A special design primitive, SB_WARMBOOT, allows an FPGA application to choose between four configuration images using two internal signal ports, S1 and S0, as shown in Figure 27. These internal signal ports connect to programmable interconnect, which in turn can connect to PLB logic and/or PIO pins.

After selecting the desired configuration image, the application then asserts the internal signal BOOT port High to force the FPGA to restart the configuration process from the specified vector address stored in PROM.

A Warm Boot application can only jump to another configuration image that DOES NOT have Warm Boot enabled. There is no such restriction for Cold Boot applications.

Time-Out and Retry

When configuring from external SPI Flash, the iCE65 device looks for a synchronization word. If the device does not find a synchronization word within its timeout period, the device automatically attempts to restart the configuration process from the very beginning. This feature is designed to address any potential power-sequencing issues that may occur between the iCE65 device and the external PROM.

The iCE65 device attempts to reconfigure six times. If not successful after six attempts, the iCE65 FPGA automatically goes into low-power mode.

SPI Peripheral Configuration Interface

Using the SPI peripheral configuration interface, an application processor (AP) serially writes a configuration image to an iCE65 FPGA using the iCE65's SPI interface, as shown in Figure 23. The iCE65's SPI configuration interface is a separate, independent I/O bank, powered by the VCC_SPI supply input. Typically, VCC_SPI is the same voltage as the application processor's I/O. The configuration control signals, CDONE and CRESET_B, are supplied by the separate I/O Bank 2 voltage input, VCCIO_2.

This same SPI peripheral interface supports programming for the iCE65's Nonvolatile Configuration Memory (NVCM).

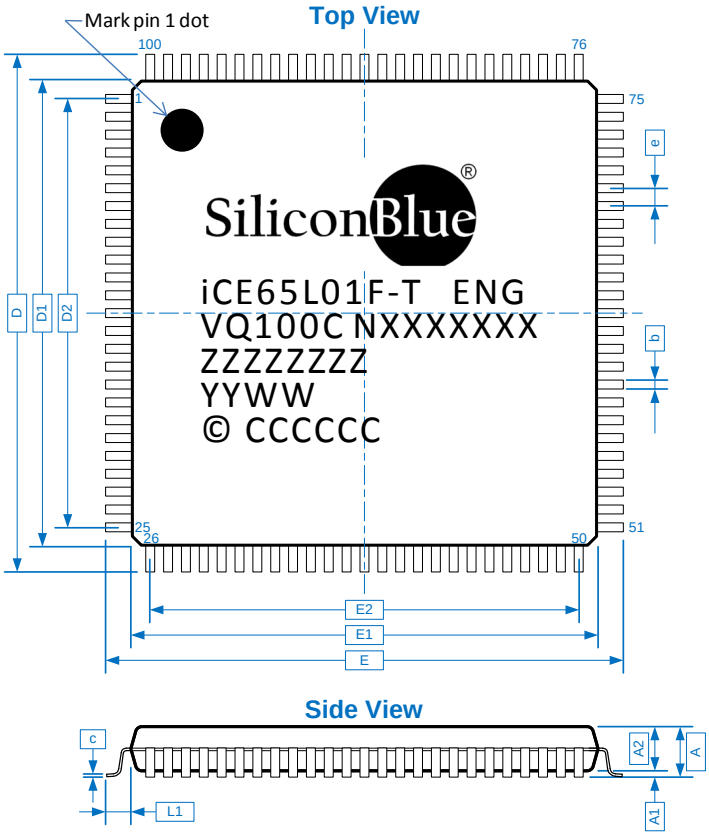
iCE65 Pin Descriptions

Table 36 lists the various iCE65 pins, alphabetically by name. The table indicates the directionality of the signal and the associated I/O bank. The table also indicates if the signal has an internal pull-up resistor enabled during configuration. Finally, the table describes the function of the pin.

Table 36: iCE65 Pin Description

Signal Name	Direction	I/O Bank	Pull-up during Config	Description
CDONE	Output	2	Yes	Configuration Done. Dedicated output. Includes a permanent weak pull-up resistor to VCCIO_2.. If driving external devices with CDONE output, connect a 10 kΩ pull-up resistor to VCCIO_2.
CRESET_B	Input	2	No	Configuration Reset, active Low. Dedicated input. No internal pull-up resistor. Either actively drive externally or connect a 10 kΩ pull-up resistor to VCCIO_2.
GBIN0/PIO0 GBIN1/PIO0	Input/IO	0	Yes	Global buffer input from I/O Bank 0. Optionally, a full-featured PIO pin.
GBIN2/PIO1 GBIN3/PIO1	Input/IO	1	Yes	Global buffer input from I/O Bank 1. Optionally, a full-featured PIO pin.
GBIN4/PIO2 GBIN5/PIO2	Input/IO	2	Yes	Global buffer input from I/O Bank 2. Optionally, a full-featured PIO pin.
GBIN6/PIO3	Input/IO	3	No	Global buffer input from I/O Bank 3. Optionally, a full-featured PIO pin.
GBIN7/PIO3	Input/IO	3	No	Global buffer input from I/O Bank 3. Optionally, a full-featured PIO pin. Optionally, a differential clock input using the associated differential input pin.
GND	Supply	All	N/A	Ground. All must be connected.
PIOx_yy	I/O	0,1,2	Yes	Programmable I/O pin defined by the iCE65 configuration bitstream. The 'x' number specifies the I/O bank number in which the I/O pin resides. The "yy' number specifies the I/O number in that bank.
PIO2/CBSEL0	Input/IO	2	Yes	Optional ColdBoot configuration SELect input, if ColdBoot mode is enabled. A full-featured PIO pin after configuration.
PIO2/CBSEL1	Input/IO	2	Yes	Optional ColdBoot configuration SELect input, if ColdBoot mode is enabled. A full-featured PIO pin after configuration.
PIO3_yy/ DPwwz	I/O	3	No	Programmable I/O pin that is also half of a differential I/O pair. Only available in I/O Bank 3. The "yy" number specifies the I/O number in that bank. The "ww" number indicates the differential I/O pair. The 'z' indicates the polarity of the pin in the differential pair. 'A'=negative input. 'B'=positive input.
PIOS/SPI_SO	I/O	SPI	Yes	SPI Serial Output. A full-featured PIO pin after configuration.
PIOS /SPI_SI	I/O	SPI	Yes	SPI Serial Input. A full-featured PIO pin after configuration.
PIOS / SPI_SS_B	I/O	SPI	Yes	SPI Slave Select. Active Low. Includes an internal weak pull-up resistor to SPI_VCC during configuration. During configuration, the logic level sampled on this pin determines the configuration mode used by the iCE65 device, as shown in Figure 20. An input when sampled at the start of configuration. An input when in SPI Peripheral configuration mode (SPI_SS_B = Low). An output when in SPI Flash configuration mode. A full-featured PIO pin after configuration.
PIOS/ SPI_SCK	I/O	SPI	Yes	SPI Slave Clock. An input when in SPI Peripheral configuration mode (SPI_SS_B = Low). An output when in SPI Flash configuration mode. A full-featured PIO pin after configuration.
TDI	Input	1	No	JTAG Test Data Input. If using the JTAG interface, use a 10kΩ pull-up resistor to VCCIO_1. Tie off to GND when unused.

Figure 38: VQ100 Package Mechanical Drawing: NVCM Programmed Device Marking



Description		Symbol	Min.	Nominal	Max.	Units
Leads per Edge	X			25		Leads
	Y			25		
Number of Signal Leads		n		100		
Maximum Size (lead tip to lead tip)	X	E	—	16.0	—	mm
	Y	D	—	16.0	—	
Body Size	X	E1	—	14.0	—	
	Y	D1	—	14.0	—	
Edge Pin Center to Center	X	E2	—	12.0	—	
	Y	D2	—	12.0	—	
Lead Pitch		e	—	0.50	—	
Lead Width		b	0.17	0.20	0.27	
Total Package Height		A	—	1.20	—	
Stand Off		A1	0.05	—	0.15	
Body Thickness		A2	0.95	1.00	1.05	
Lead Length		L1	—	1.00	—	
Lead Thickness		c	0.09	—	0.20	
Coplanarity			—	0.08	—	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65L01F	Part number
	-T	Power/Speed
	ENG	Engineering
3	VQ100C NXXXXXXX	Package type and Lot number
4	ZZZZZZZZ	NVCM Program. code
5	YYWW	Date Code
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
38	32

Ball Function	Ball Number	Pin Type	Bank
PIO2	J11	PIO	2
PIO2	K3	PIO	2
PIO2	K4	PIO	2
PIO2	K11	PIO	2
PIO2	L2	PIO	2
PIO2	L3	PIO	2
PIO2	L4	PIO	2
PIO2	L5	PIO	2
PIO2	L10	PIO	2
PIO2	L11	PIO	2
PIO2/CBSEL0	H6	PIO	2
PIO2/CBSEL1	J6	PIO	2
VCCIO_2	K5	VCCIO	2
PIO3	C1	PIO	3
PIO3	B1	PIO	3
PIO3	D1	PIO	3
PIO3	E2	PIO	3
PIO3	C2	PIO	3
PIO3	D2	PIO	3
PIO3	C3	PIO	3
PIO3	C4	PIO	3
PIO3	E4	PIO	3
PIO3	D4	PIO	3
PIO3	F3	PIO	3
PIO3	G3	PIO	3
PIO3	G4	PIO	3
GBIN6/PIO3	F4	GBIN	3
GBIN7/PIO3	D3	GBIN	3
PIO3	E3	PIO	3
PIO3	F2	PIO	3
PIO3	G1	PIO	3
PIO3	H1	PIO	3
PIO3	J1	PIO	3
PIO3	H2	PIO	3
PIO3	H3	PIO	3
PIO3	J3	PIO	3
PIO3	J2	PIO	3
VCCIO_3	A1	VCCIO	3
VCCIO_3	G2	VCCIO	3
PIOS/SPI_SO	J8	SPI	SPI
PIOS/SPI_SI	K8	SPI	SPI
PIOS/SPI_SCK	K9	SPI	SPI
PIOS/SPI_SS_B	J9	SPI	SPI
SPI_VCC	J10	SPI	SPI
GND	B2	GND	GND
GND	B10	GND	GND
GND	E1	GND	GND
GND	F5	GND	GND
GND	F6	GND	GND
GND	G5	GND	GND
GND	G6	GND	GND
GND	G11	GND	GND

Ball Function	Ball Number	Pin Type	Bank
PIO0	A5	PIO	0
PIO0	A6	PIO	0
PIO0	A10	PIO	0
PIO0	A11	PIO	0
PIO0	A12	PIO	0
PIO0	B2	PIO	0
PIO0	B3	PIO	0
PIO0	B4	PIO	0
PIO0	B5	PIO	0
PIO0	B6	PIO	0
PIO0	B8	PIO	0
PIO0	B9	PIO	0
PIO0	B10	PIO	0
PIO0	B11	PIO	0
PIO0	C4	PIO	0
PIO0	C5	PIO	0
PIO0	C6	PIO	0
PIO0	C7	PIO	0
PIO0	C8	PIO	0
PIO0	C9	PIO	0
PIO0	C10	PIO	0
PIO0	C11	PIO	0
PIO0	D5	PIO	0
PIO0	D6	PIO	0
PIO0	D7	PIO	0
PIO0	D8	PIO	0
PIO0	D9	PIO	0
PIO0	D10	PIO	0
PIO0	E6	PIO	0
PIO0	E8	PIO	0
PIO0	E9	PIO	0
VCCIO_0	A8	VCCIO	0
VCCIO_0	F6	VCCIO	0
GBIN2/PIO1	F10	GBIN	1
GBIN3/PIO1	G12	GBIN	1
PIO1	B13	PIO	1
PIO1	B14	PIO	1
PIO1	C12	PIO	1
PIO1	C13	PIO	1
PIO1	C14	PIO	1
PIO1	D11	PIO	1
PIO1	D12	PIO	1
PIO1	D13	PIO	1
PIO1	D14	PIO	1
PIO1	E10	PIO	1
PIO1	E11	PIO	1
PIO1	E12	PIO	1
PIO1	E13	PIO	1
PIO1	E14	PIO	1
PIO1	F11	PIO	1
PIO1	F12	PIO	1
PIO1	F13	PIO	1

Pinout Table

Table 44 provides a detailed pinout table for the two chip-scale BGA packages. Pins are generally arranged by I/O bank, then by ball function. The balls with a black circle (●) are unconnected balls (N.C.) for the iCE65L04 in the CB284 package. The CB132 package fits within the CB284 package footprint as shown in Figure 48. The right-most column shows which CB132 ball corresponds to the CB284.

The table also highlights the differential I/O pairs in I/O Bank 3.

Table 44: iCE65 CB284 Chip-scale BGA Pinout Table (with CB132 cross reference)

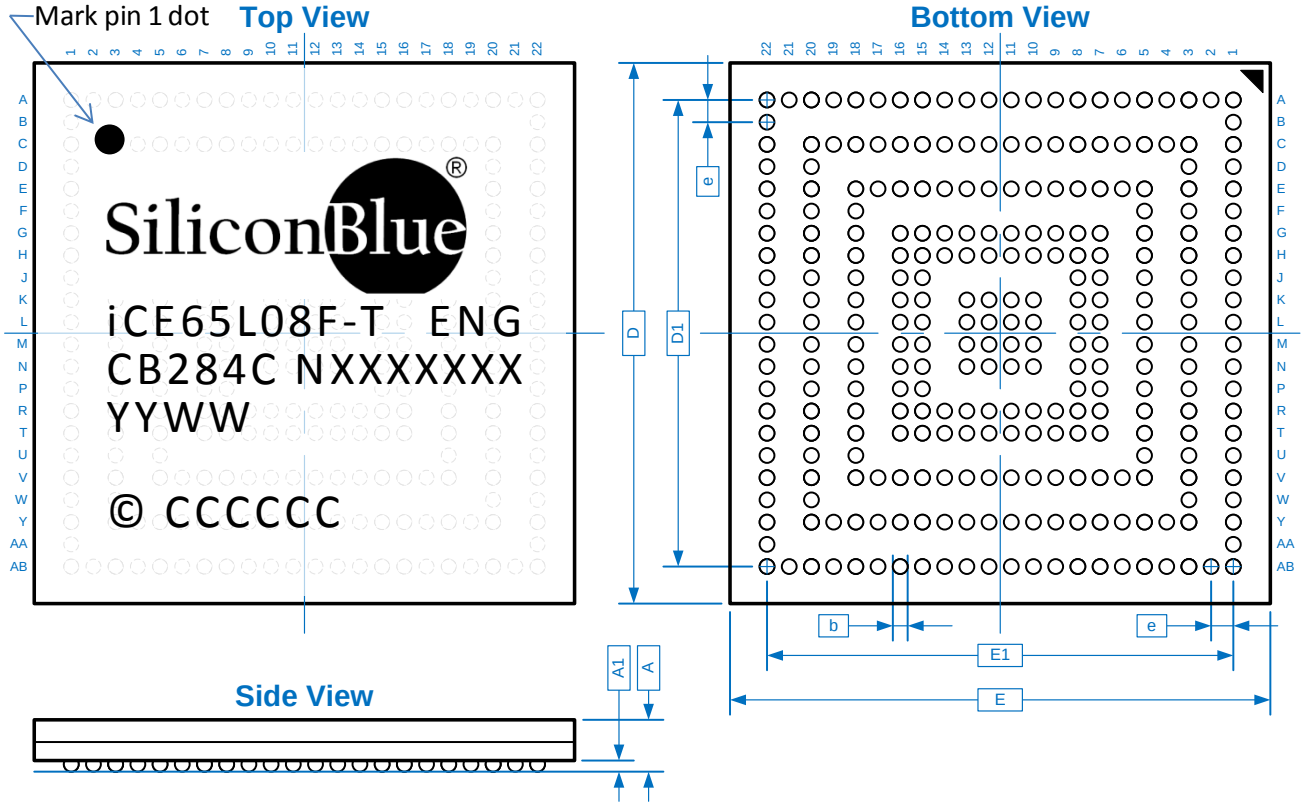
Ball Function	Ball Number	Pin Type by Device		Bank	CB132 Ball Equivalent
	iCE65L04 iCE65L08	iCE65L04	iCE65L08		
GBIN0/PIO0	E10	GBIN	GBIN	0	A6
GBIN1/PIO0	E11	GBIN	GBIN	0	A7
PIO0 (●)	A1	N.C.	PIO	0	—
PIO0 (●)	A2	N.C.	PIO	0	—
PIO0 (●)	A3	N.C.	PIO	0	—
PIO0 (●)	A4	N.C.	PIO	0	—
PIO0	A5	PIO	PIO	0	—
PIO0	A6	PIO	PIO	0	—
PIO0	A7	PIO	PIO	0	—
PIO0 (●)	A9	N.C.	PIO	0	—
PIO0 (●)	A10	N.C.	PIO	0	—
PIO0 (●)	A11	N.C.	PIO	0	—
PIO0 (●)	A12	N.C.	PIO	0	—
PIO0 (●)	A13	N.C.	PIO	0	—
PIO0	A15	PIO	PIO	0	—
PIO0	A16	PIO	PIO	0	—
PIO0	A17	PIO	PIO	0	—
PIO0	A18	PIO	PIO	0	—
PIO0 (●)	A14	N.C.	PIO	0	—
PIO0 (●)	A19	N.C.	PIO	0	—
PIO0 (●)	A20	N.C.	PIO	0	—
PIO0	C3	PIO	PIO	0	—
PIO0	C4	PIO	PIO	0	—
PIO0	C5	PIO	PIO	0	—
PIO0	C6	PIO	PIO	0	—
PIO0	C7	PIO	PIO	0	—
PIO0	C9	PIO	PIO	0	—
PIO0	C10	PIO	PIO	0	—
PIO0	C11	PIO	PIO	0	—
PIO0	C13	PIO	PIO	0	—
PIO0	C14	PIO	PIO	0	—
PIO0	C15	PIO	PIO	0	—
PIO0	C16	PIO	PIO	0	—
PIO0	C17	PIO	PIO	0	—
PIO0	C18	PIO	PIO	0	—
PIO0	C19	PIO	PIO	0	—
PIO0	E5	PIO	PIO	0	A1
PIO0	E6	PIO	PIO	0	A2
PIO0	E7	PIO	PIO	0	A3
PIO0	E8	PIO	PIO	0	A4
PIO0	E9	PIO	PIO	0	A5
PIO0	E14	PIO	PIO	0	A10

Ball Function	Ball Number iCE65L04 iCE65L08	Pin Type by Device iCE65L04	Pin Type by Device iCE65L08	Bank	CB132 Ball Equivalent
PIO2	T13	PIO	PIO	2	M9
PIO2	V6	PIO	PIO	2	P2
PIO2	V7	PIO	PIO	2	P3
PIO2	V8	PIO	PIO	2	P4
PIO2	V9	PIO	PIO	2	P5
PIO2	V13	PIO	PIO	2	P9
PIO2	Y4	PIO	PIO	2	—
PIO2	Y5	PIO	PIO	2	—
PIO2	Y6	PIO	PIO	2	—
PIO2	Y7	PIO	PIO	2	—
PIO2	Y9	PIO	PIO	2	—
PIO2	Y10	PIO	PIO	2	—
PIO2	Y13	PIO	PIO	2	—
PIO2	Y14	PIO	PIO	2	—
PIO2	Y15	PIO	PIO	2	—
PIO2	Y17	PIO	PIO	2	—
PIO2	Y18	PIO	PIO	2	—
PIO2	Y19	PIO	PIO	2	—
PIO2	Y20	PIO	PIO	2	—
PIO2	AB2	PIO	PIO	2	—
PIO2 (●)	AB3	N.C.	PIO	2	—
PIO2 (●)	AB4	N.C.	PIO	2	—
PIO2	AB6	PIO	PIO	2	—
PIO2	AB7	PIO	PIO	2	—
PIO2	AB8	PIO	PIO	2	—
PIO2	AB9	PIO	PIO	2	—
PIO2	AB10	PIO	PIO	2	—
PIO2	AB11	PIO	PIO	2	—
PIO2	AB12	PIO	PIO	2	—
PIO2	AB13	PIO	PIO	2	—
PIO2	AB14	PIO	PIO	2	—
PIO2	AB15	PIO	PIO	2	—
PIO2 (●)	AB16	N.C.	PIO	2	—
PIO2 (●)	AB17	N.C.	PIO	2	—
PIO2 (●)	AB18	N.C.	PIO	2	—
PIO2 (●)	AB19	N.C.	PIO	2	—
PIO2 (●)	AB20	N.C.	PIO	2	—
PIO2 (●)	AB21	N.C.	PIO	2	—
PIO2 (●)	AB22	N.C.	PIO	2	—
PIO2/CBSEL0	R13	PIO	PIO	2	L9
PIO2/CBSEL1	V14	PIO	PIO	2	P10
VCCIO_2	N13	VCCIO	VCCIO	2	J9
VCCIO_2	T9	VCCIO	VCCIO	2	M5
VCCIO_2	Y11	VCCIO	VCCIO	2	—
PIO3/DP00A	F5	DPIO	DPIO	3	B1
PIO3/DP00B	G5	DPIO	DPIO	3	C1
PIO3/DP01A	G7	DPIO	DPIO	3	C3
PIO3/DP01B	H7	DPIO	DPIO	3	D3
PIO3/DP02A	H8	DPIO	DPIO	3	D4
PIO3/DP02B	J8	DPIO	DPIO	3	E4

Package Mechanical Drawing

Figure 49: CB284 Package Mechanical Drawing

CB284: 12 x 12 mm, 284-ball, 0.5 mm ball-pitch, chip-scale ball grid array



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			22		Columns
Number of Ball Rows	Y			22		Rows
Number of Signal Balls		n		284		Balls
Body Size	X	E	11.90	12.00	12.10	mm
	Y	D	11.90	12.00	12.10	
Ball Pitch		e	—	0.50	—	
Ball Diameter		b	0.27	—	0.37	
Edge Ball Center to Center	X	E1	—	10.50	—	
	Y	D1	—	10.50	—	
Package Height		A	—	—	1.00	
Stand Off		A1	0.16	—	0.26	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65L08F	Part number
	-T	Power/Speed
	ENG	Engineering
3	CB284C NXXXXXXX	Package type and Lot number
4	YYWW	Date Code
5	N/A	Blank
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
35	28

Die Cross Reference

The tables in this section list all the pads on a specific die type and provide a cross reference on how a specific pad connects to a ball or pin in each of the available package offerings. Similarly, the tables provide the pad coordinates for the die-based version of the product (DiePlus). These tables also provide a way to prototype with one package option and then later move to a different package or die.

As described in "Input and Output Register Control per PIO Pair" on page 16, PIO pairs share register control inputs. Similarly, as described in "Differential Inputs and Outputs" on page 12, a PIO pair can form a differential input or output. PIO pairs in I/O Bank 3 are optionally differential inputs or differential outputs. PIO pairs in all other I/O Banks are optionally differential outputs. In the tables, differential pairs are surrounded by a heavy blue box.

iCE65L04

Table 45 lists all the pads on the iCE65L04 die and how these pads connect to the balls or pins in the supported package styles. Most VCC, VCCIO, and GND pads are double-bonded inside the package although the table shows only a single connection.

For additional information on the iCE65L04 DiePlus product, please refer to the following data sheet.

DiePlus Advantage FPGA Known Good Die

Table 45: iCE65L04 Die Cross Reference

iCE65L04	DiePlus						
Pad Name	VQ100	CB132	CB196	CB284	Pad	X (µm)	Y (µm)
PIO3_00/DP00A	1	B1	C1	F5	1	129.40	2,687.75
PIO3_01/DP00B	2	C1	B1	G5	2	231.40	2,642.74
PIO3_02/DP01A	3	C3	D3	G7	3	129.40	2,597.75
PIO3_03/DP01B	4	D3	C3	H7	4	231.40	2,552.74
GND	5	F1	F1	K5	5	129.40	2,507.75
GND	—	—	—	—	6	231.40	2,462.74
VCCIO_3	6	E3	E3	J7	7	129.40	2,417.75
VCCIO_3	—	—	—	—	8	231.40	2,372.74
PIO3_04/DP02A	7	D4	D1	H8	9	129.40	2,327.75
PIO3_05/DP02B	8	E4	D2	J8	10	231.40	2,292.74
PIO3_06/DP03A	—	D1	E1	H5	11	129.40	2,257.75
PIO3_07/DP03B	—	E1	E2	J5	12	231.40	2,222.74
VCC	—	—	H9	D3	13	129.40	2,187.75
PIO3_08/DP04A	9	F4	D4	K8	14	231.40	2,152.74
PIO3_09/DP04B	10	F3	E4	K7	15	129.40	2,117.75
PIO3_10/DP05A	—	—	F3	E3	16	231.40	2,082.74
PIO3_11/DP05B	—	—	F4	F3	17	129.40	2,047.75
GND	—	H6	A9	M10	18	231.40	2,012.74
PIO3_12/DP06A	—	—	F5	G3	19	129.40	1,977.75
PIO3_13/DP06B	—	—	E5	H3	20	231.40	1,942.74
GND	—	—	A9	J3	21	129.40	1,907.75
GND	—	—	—	—	22	231.40	1,872.74
PIO3_14/DP07A	—	—	—	H1	23	129.40	1,837.75
PIO3_15/DP07B	—	—	—	J1	24	231.40	1,802.74
VCCIO_3	—	—	K1	K3	25	129.40	1,767.75
VCC	11	G6	G6	L10	26	231.40	1,732.74
PIO3_16/DP08A	—	—	—	K1	27	129.40	1,697.75
PIO3_17/DP08B	—	—	—	L1	28	231.40	1,662.74

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
TDI	M12	T16	177	4,470.5	634.615
TMS	P14	V18	178	4,572.5	684.615
TCK	L12	R16	179	4,470.5	734.615
TDO	N14	U18	180	4,572.5	784.615
TRST_B	M14	T18	181	4,470.5	834.615
PIO1_00	M13	R18	182	4,572.5	884.615
PIO1_01	K11	P16	183	4,470.5	934.615
PIO1_02	L13	P15	184	4,572.5	984.615
PIO1_03	L14	P18	185	4,470.5	1,034.615
GND	G9	N18	186	4,572.5	1,084.615
GND	—	—	187	4,470.5	1,134.615
PIO1_04	J11	N16	188	4,572.5	1,184.615
PIO1_05	K12	N15	189	4,470.5	1,234.62
VCCIO_1	F9	M18	190	4,572.5	1,287.115
VCCIO_1	—	—	191	4,470.5	1,322.115
PIO1_06	J12	M15	192	4,572.5	1,357.115
PIO1_07	K14	M16	193	4,470.5	1,392.115
PIO1_08	—	T20	194	4,572.5	1,427.115
PIO1_09	—	W20	195	4,470.5	1,462.115
PIO1_10	—	V20	196	4,572.5	1,497.115
VCC	H9	M13	197	4,470.5	1,532.115
VCC	—	—	198	4,572.5	1,567.115
PIO1_11	—	R20	199	4,470.5	1,602.115
PIO1_12	—	Y22	200	4,572.5	1,637.115
PIO1_13	—	AA22	201	4,470.5	1,672.115
PIO1_14	—	U20	202	4,572.5	1,707.115
PIO1_15	J13	W22	203	4,470.5	1,742.115
PIO1_16	H11	P20	204	4,572.5	1,777.115
PIO1_17	J10	V22	205	4,470.5	1,812.115
PIO1_18	H12	U22	206	4,572.5	1,847.115
GND	K10	N20	207	4,470.5	1,882.115
GND	—	—	208	4,572.5	1,917.110
PIO1_19	H13	T22	209	4,470.5	1,952.115
PIO1_20	—	M20	210	4,572.5	1,987.115
PIO1_21	H10	R22	211	4,470.5	2,022.115
PIO1_22	—	P22	212	4,572.5	2,057.115
VCCIO_1	F9	J20	213	4,470.5	2,092.115
VCCIO_1	—	—	214	4,572.5	2,127.115
PIO1_23	G10	M22	215	4,470.5	2,162.115
PIO1_24	G11	N22	216	4,572.5	2,197.115
PIO1_25	—	K22	217	4,470.5	2,232.115
PIO1_26	—	L22	218	4,572.5	2,267.115
GBIN3/PIO1_27	G12	K18	219	4,470.5	2,302.11
GBIN2/PIO1_28	F10	L18	220	4,572.5	2,337.115
PIO1_29	—	J22	221	4,470.5	2,372.115

Internal Configuration Oscillator Frequency

Table 57 shows the operating frequency for the iCE65's internal configuration oscillator.

Table 57: Internal Oscillator Frequency

Symbol	Oscillator Mode	Frequency (MHz)		Description
		Min.	Max.	
f_{OSCD}	**Default**	4.0	6.8	Default oscillator frequency. Slow enough to safely operate with any SPI serial PROM.
f_{OSCL}	**Low Frequency**	14	21	Supported by most SPI serial Flash PROMs
f_{OSCH}	**High Frequency**	21	31	Supported by some high-speed SPI serial Flash PROMs
	Off	0	0	Oscillator turned off by default after configuration to save power.

Configuration Timing

Table 58 shows the maximum time to configure an iCE65 device, by oscillator mode. The calculations use the slowest frequency for a given oscillator mode from Table 57 and the maximum configuration bitstream size from Table 1 which includes full RAM4K block initialization. The configuration bitstream selects the desired oscillator mode based on the performance of the configuration data source.

***Table 58:* Maximum SPI Master or NVCM Configuration Timing by Oscillator Mode**

Symbol	Description	Device	Default	Low Freq.	High Freq.	Units
$t_{CONFIGL}$	Time from when minimum Power-on Reset (POR) threshold is reached until user application starts.	**iCE65L01**	53	25	11	ms
		iCE65L04	115	55	25	ms
		iCE65L08	230	110	50	ms

Table 59 provides timing for the CRESET_B and CDONE pins.

Table 59: General Configuration Timing

Symbol	From	To	Description		All Grades		Units
					Min.	Max.	
t_{CRESET_B}	CREST_B	CREST_B	Minimum CRESET_B Low pulse width required to restart configuration, from falling edge to rising edge		200	—	ns
t_{DONE_IO}	CDONE High	PIO pins active	Number of configuration clock cycles after CDONE goes High before the PIO pins are activated.		—	49	Clock cycles
			SPI Peripheral Mode (Clock = SPI_SCK, cycles measured rising-edge to rising-edge)		Depends on SPI_SCK frequency		
			NVCM or SPI Master Mode by internal oscillator frequency setting (Clock = internal oscillator)	Default	7.20	12.25	µs
				Low	2.34	3.50	µs
				High	1.59	2.33	µs

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