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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

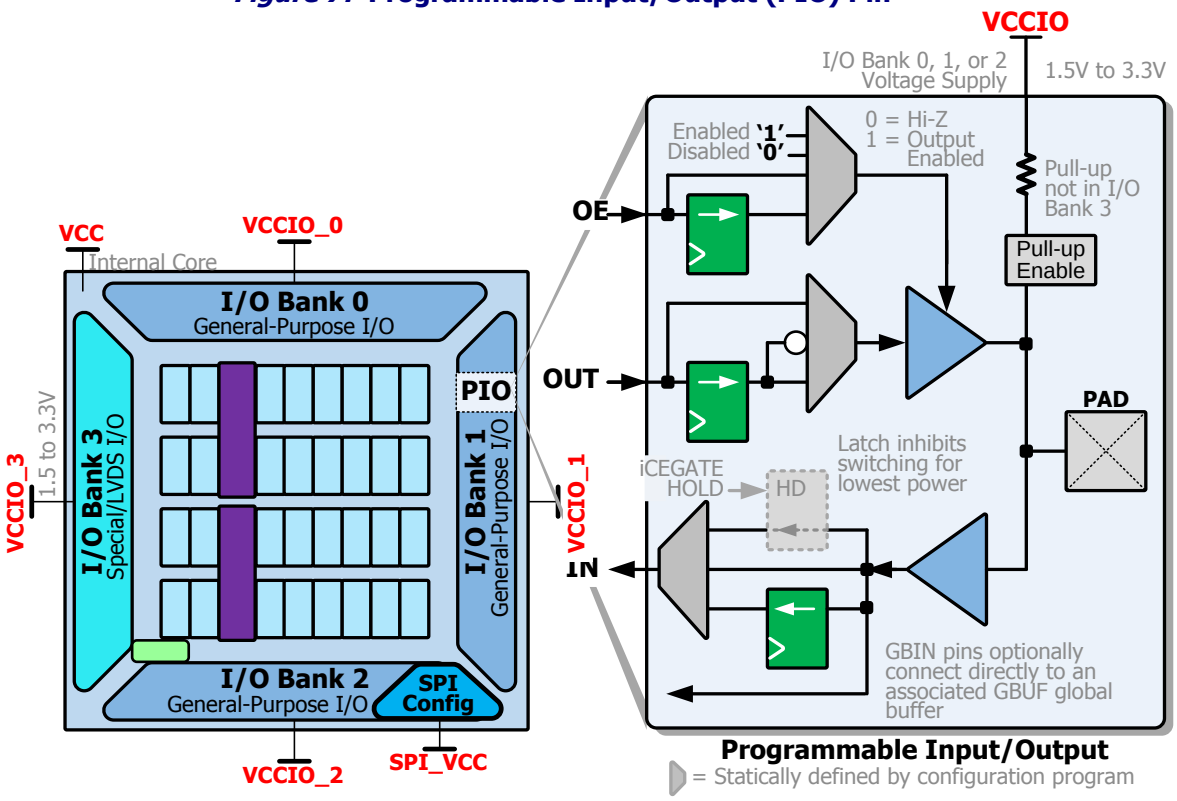
Details	
Product Status	Obsolete
Number of LABs/CLBs	440
Number of Logic Elements/Cells	3520
Total RAM Bits	81920
Number of I/O	176
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	284-VFBGA, CSPBGA
Supplier Device Package	284-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice65l04f-tcb284c

Programmable Input/Output Block (PIO)

Programmable Input/Output (PIO) blocks surround the periphery of the device and connect external components to the Programmable Logic Blocks (PLBs) and RAM4K blocks via programmable interconnect. Individual PIO pins are grouped into one of four I/O banks, as shown in Figure 7. I/O Bank 3 has additional capabilities, including LVDS differential I/O and the ability to interface to Mobile DDR memories.

Figure 7 also shows the logic within a PIO pin. When used in an application, a PIO pin becomes a signal input, an output, or a bidirectional I/O pin with a separate direction control input.

Figure 7: **Programmable Input/Output (PIO) Pin**



I/O Banks

PIO blocks are organized into four separate I/O banks, each with its own voltage supply input, as shown in Table 5. The voltage applied to the VCCIO pin on a bank defines the I/O standard used within the bank. Table 50 and Table 51 describe the I/O drive capabilities and switching thresholds by I/O standard. On iCE65L04 and iCE65L08 devices, I/O Bank 3, along the left edge of the die, is different than the others and supports specialized I/O standards.

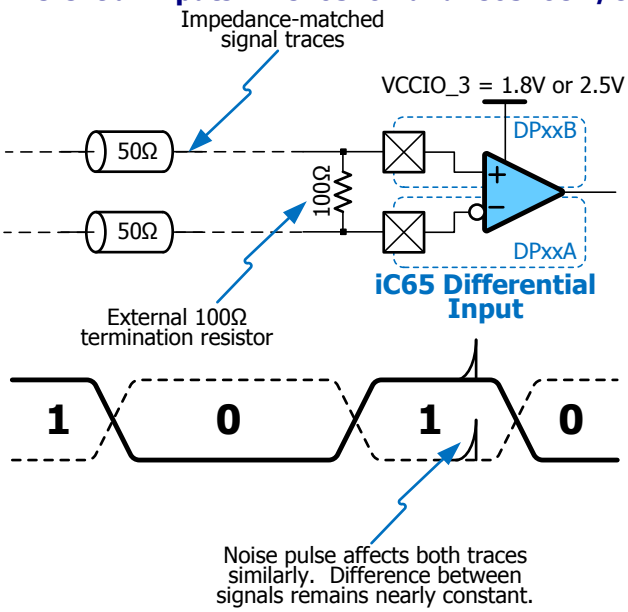
I/O Bank Voltage Supply Inputs Support Different I/O Standards

Because each I/O bank has its own voltage supply, iCE65 components become the ideal bridging device between different interface standards. For example, the iCE65 device allows a 1.8V-only processor to interface cleanly with a 3.3V bus interface. The iCE65 device replaces external voltage translators.

Table 5: Supported Voltages by I/O Bank

Bank	Device Edge	Supply Input	3.3V	2.5V	1.8V	1.5V
0	Top	VCCIO_0	Yes	Yes	Yes	Outputs only
1	Right	VCCIO_1	Yes	Yes	Yes	Outputs only
2	Bottom	VCCIO_2	Yes	Yes	Yes	Outputs only
3	Left	VCCIO_3	Yes	Yes	Yes	iCE65L01: Outputs only iCE65L04/08: Yes
SPI	Bottom Right	SPI_VCC	Yes	Yes	Yes	No

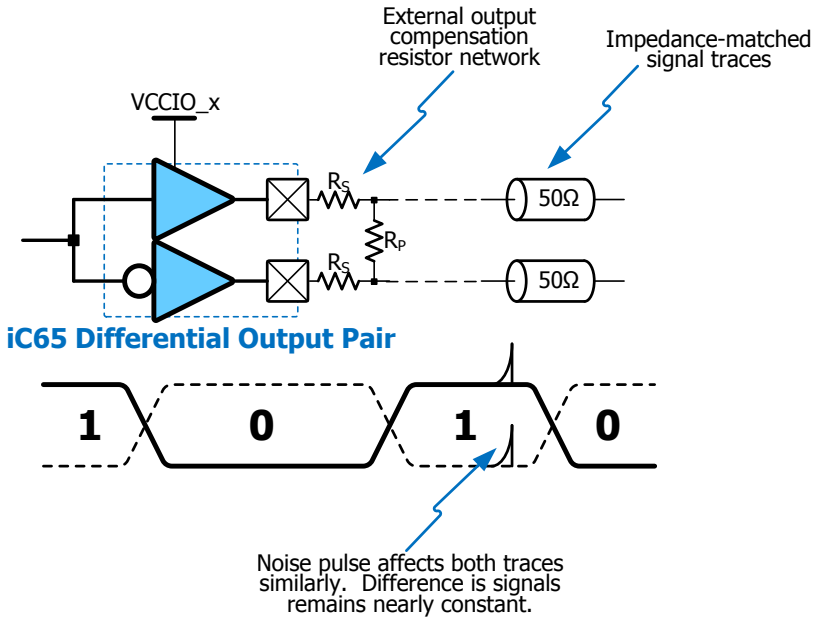
Figure 8: **Differential Inputs in iCE65L04 and iC65L08 I/O Bank 3**



Differential Outputs in Any Bank

Differential outputs are built using a pair of single-ended PIO pins as shown in Figure 9. Each differential I/O pair requires a three-resistor termination network to adjust output characteristic to match those for the specific differential I/O standard. The output characteristics depend on the values of the parallel resistors (RP) and series resistor (RS). Differential outputs must be located in the same I/O tile.

Figure 9: Differential Output Pair



For electrical characteristics, see "Differential Outputs" on page 100.

The PIO pins that make up a differential output pair are indicated with a blue bounding box in the in the tables in "Die Cross Reference" starting on page 84.

Input and Output Register Control per PIO Pair

PIO pins are grouped into pairs for synchronous control. Registers within pairs of PIO pins share common input clock, output clock, and I/O clock enable control signals, as illustrated in Figure 11. The combinational logic paths are removed from the drawing for clarity.

The INCLK clock signal only controls the input flip-flops within the PIO pair.

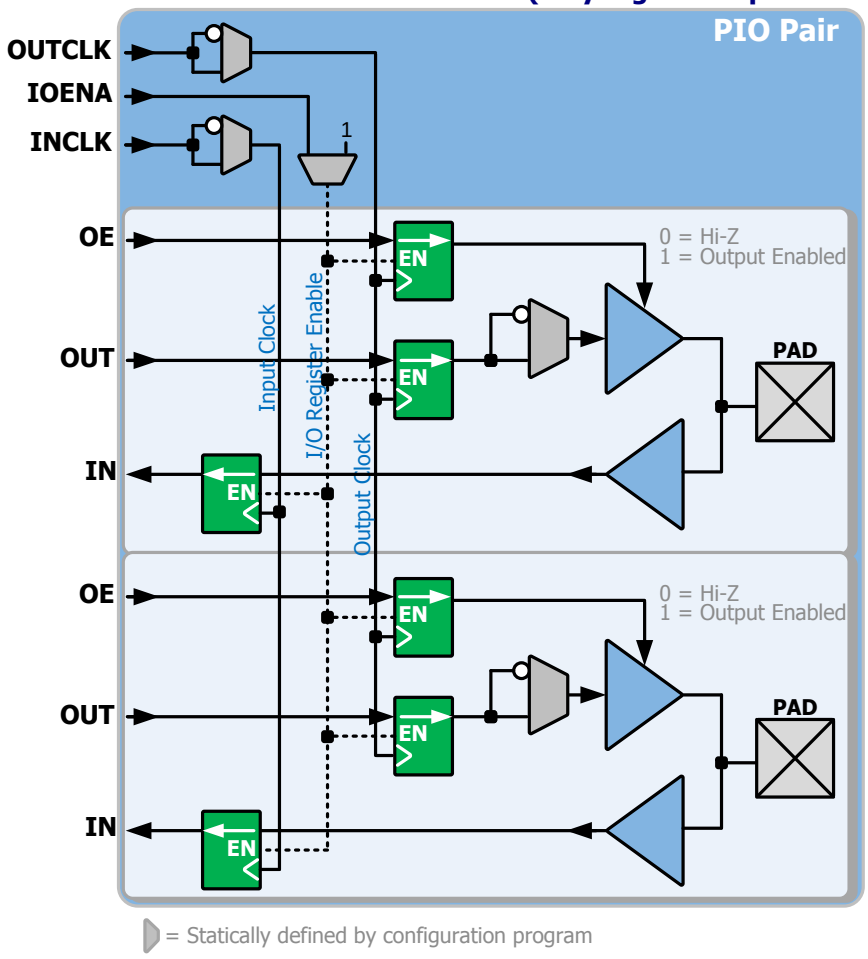
The OUTCLK clock signal controls the output flip-flops and the output-enable flip-flops within the PIO pair.

If desired in the iCE65 application, the INCLK and OUTCLK signals can be connected together.

The IOENA clock-enable input, if used, enables all registers in the PIO pair, as shown in Figure 11. By default, the registers are always enabled.

Before laying out your printed-circuit board, run the design through the iCEcube development software to verify that your selected pinout complies with these I/O register pairing requirements. See tables in "Die Cross Reference" starting on page 84.

Figure 11: **PIO Pairs Share Clock and Clock Enable Controls (only registered paths shown for clarity)**



The pairing of PIO pairs is most evident in the tables in "Die Cross Reference" starting on page 84.

Table 21: **iCE65 Configuration Image Size (Kbits)**

Device	MINIMUM Logic Only (RAM4K not initialized)	MAXIUM Logic + RAM4K (RAM4K pre-initialized)
iCE65L01	181 Kbits	245 Kbits*
iCE65L04	453 Kbits	533 Kbits
iCE65L08	929 Kbits	1,057 Kbits

* Note: only 14 of the 16 RAM4K Memory Blocks may be pre-initialized in the iCE65L01.

Nonvolatile Configuration Memory (NVCM)

All standard iCE65 devices have an internal, nonvolatile configuration memory (NVCM). The NVCM is large enough to program a complete iCE65 device, including initializing all RAM4K block locations (MAXIMUM column in Table 23. The NVCM memory also has very high programming yield due to extensive error checking and correction (ECC) circuitry.

The NVCM is ideal for cost-sensitive, high-volume production applications, saving the cost and board space associated with an external configuration PROM. Furthermore, the NVCM provides exceptional design security, protecting critical intellectual property (IP). The NVCM contents are entirely contained within the iCE65 device and are not readable once protected by the one-time programmable Security bits. Furthermore, there is no observable difference between a programmed or un-programmed memory cell using optical or electron microscopy.

The NVCM memory has a programming interface similar to a 25-series SPI serial Flash PROM. Consequently, it can be programmed using standard device programmers before or after circuit board assembly or programmed in-system from a microprocessor or other intelligent controller. NVCM programming requires VCCIO_1, Bank 1 voltage to be applied on power-up, at the same time as other voltage supplies.

Configuration Control Signals

The iCE65 configuration process is self-timed and controlled by a few internal signals and device I/O pins, as described in Table 22.

Table 22: **iCE65 Configuration Control Signals**

Signal Name	Direction	Description
POR	Internal control	Internal Power-On Reset (POR) circuit.
OSC	Internal control	Internal configuration oscillator.
CRESET_B	Input	Configuration Reset input. Active-Low. No internal pull-up resistor.
CDONE	Open-drain Output	Configuration Done output. Permanent, weak pull-up resistor to VCCIO_2.

The Power-On Reset circuit, POR, automatically resets the iCE65 component to a known state during power-up (cold boot). The POR circuit monitors the relevant voltage supply inputs, as shown in Figure 22. Once all supplies exceed their minimum thresholds, the configuration controller can start the configuration process.

The configuration controller begins configuring the iCE65 device, clocked by the Internal Oscillator, OSC. The OSC oscillator continues controlling configuration unless the iCE65 device is configured using the SPI Peripheral Configuration Interface.

iCE65 Pin Descriptions

Table 36 lists the various iCE65 pins, alphabetically by name. The table indicates the directionality of the signal and the associated I/O bank. The table also indicates if the signal has an internal pull-up resistor enabled during configuration. Finally, the table describes the function of the pin.

Table 36: iCE65 Pin Description

Signal Name	Direction	I/O Bank	Pull-up during Config	Description
CDONE	Output	2	Yes	Configuration Done. Dedicated output. Includes a permanent weak pull-up resistor to VCCIO_2.. If driving external devices with CDONE output, connect a 10 kΩ pull-up resistor to VCCIO_2.
CRESET_B	Input	2	No	Configuration Reset, active Low. Dedicated input. No internal pull-up resistor. Either actively drive externally or connect a 10 kΩ pull-up resistor to VCCIO_2.
GBIN0/PIO0 GBIN1/PIO0	Input/IO	0	Yes	Global buffer input from I/O Bank 0. Optionally, a full-featured PIO pin.
GBIN2/PIO1 GBIN3/PIO1	Input/IO	1	Yes	Global buffer input from I/O Bank 1. Optionally, a full-featured PIO pin.
GBIN4/PIO2 GBIN5/PIO2	Input/IO	2	Yes	Global buffer input from I/O Bank 2. Optionally, a full-featured PIO pin.
GBIN6/PIO3	Input/IO	3	No	Global buffer input from I/O Bank 3. Optionally, a full-featured PIO pin.
GBIN7/PIO3	Input/IO	3	No	Global buffer input from I/O Bank 3. Optionally, a full-featured PIO pin. Optionally, a differential clock input using the associated differential input pin.
GND	Supply	All	N/A	Ground. All must be connected.
PIOx_yy	I/O	0,1,2	Yes	Programmable I/O pin defined by the iCE65 configuration bitstream. The 'x' number specifies the I/O bank number in which the I/O pin resides. The "yy' number specifies the I/O number in that bank.
PIO2/CBSEL0	Input/IO	2	Yes	Optional ColdBoot configuration SELect input, if ColdBoot mode is enabled. A full-featured PIO pin after configuration.
PIO2/CBSEL1	Input/IO	2	Yes	Optional ColdBoot configuration SELect input, if ColdBoot mode is enabled. A full-featured PIO pin after configuration.
PIO3_yy/ DPwwz	I/O	3	No	Programmable I/O pin that is also half of a differential I/O pair. Only available in I/O Bank 3. The "yy" number specifies the I/O number in that bank. The "ww" number indicates the differential I/O pair. The 'z' indicates the polarity of the pin in the differential pair. 'A'=negative input. 'B'=positive input.
PIOS/SPI_SO	I/O	SPI	Yes	SPI Serial Output. A full-featured PIO pin after configuration.
PIOS /SPI_SI	I/O	SPI	Yes	SPI Serial Input. A full-featured PIO pin after configuration.
PIOS / SPI_SS_B	I/O	SPI	Yes	SPI Slave Select. Active Low. Includes an internal weak pull-up resistor to SPI_VCC during configuration. During configuration, the logic level sampled on this pin determines the configuration mode used by the iCE65 device, as shown in Figure 20. An input when sampled at the start of configuration. An input when in SPI Peripheral configuration mode (SPI_SS_B = Low). An output when in SPI Flash configuration mode. A full-featured PIO pin after configuration.
PIOS/ SPI_SCK	I/O	SPI	Yes	SPI Slave Clock. An input when in SPI Peripheral configuration mode (SPI_SS_B = Low). An output when in SPI Flash configuration mode. A full-featured PIO pin after configuration.
TDI	Input	1	No	JTAG Test Data Input. If using the JTAG interface, use a 10kΩ pull-up resistor to VCCIO_1. Tie off to GND when unused.

Ball Function	Ball Number	Pin Type	Bank
PIO3	B1	PIO	3
PIO3	B2	PIO	3
PIO3	B3	PIO	3
PIO3	C1	PIO	3
PIO3	C2	PIO	3
PIO3	C3	PIO	3
GBIN7/PIO3	D1	GBIN	3
PIO3	D2	PIO	3
PIO3	D3	PIO	3
GBIN6/PIO3	E1	GBIN	3
PIO3	E2	PIO	3
PIO3	E3	PIO	3
PIO3	F2	PIO	3
PIO3	F3	PIO	3
PIO3	G1	PIO	3
PIO3	G2	PIO	3
PIO3	H1	PIO	3
PIO3	H2	PIO	3
VCCIO_3	F1	VCCIO	3
PIOS/SPI_SO	H7	SPI	SPI
PIOS/SPI_SI	J7	SPI	SPI
PIOS/SPI_SCK	J8	SPI	SPI
PIOS/SPI_SS_B	H8	SPI	SPI
SPI_VCC	H9	SPI	SPI
GND	A1	GND	GND
GND	A9	GND	GND
GND	J9	GND	GND
GND	J1	GND	GND
GND	E4	GND	GND
GND	E5	GND	GND
GND	F4	GND	GND
GND	F5	GND	GND
VCC	A5	VCC	VCC
VCC	J5	VCC	VCC
VPP_2V5	B9	VPP	VPP

Table 39: iCE65 VQ100 Pinout Table

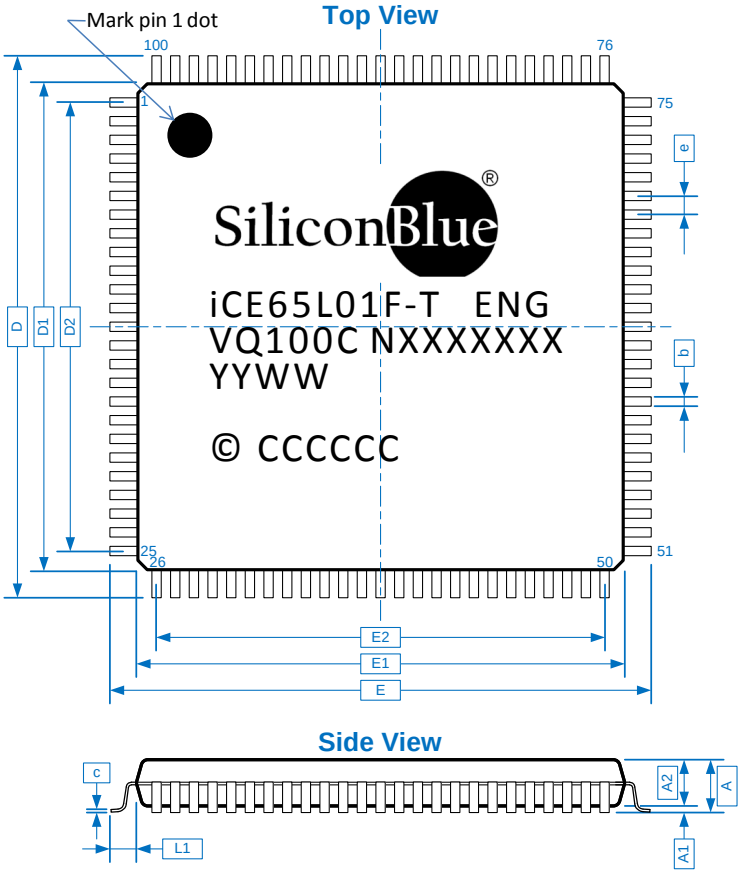
Pin Function	Pin Number	Type	Bank
GBIN0/PIO0	90	GBIN	0
GBIN1/PIO0	89	GBIN	0
PIO0	78	PIO	0
PIO0	79	PIO	0
PIO0	80	PIO	0
PIO0	81	PIO	0
PIO0	82	PIO	0
PIO0	83	PIO	0
PIO0	85	PIO	0
PIO0	86	PIO	0
PIO0	87	PIO	0
PIO0	91	PIO	0
PIO0	93	PIO	0
PIO0	94	PIO	0
PIO0	95	PIO	0
PIO0	96	PIO	0
PIO0	97	PIO	0
PIO0	99	PIO	0
PIO0	100	PIO	0
VCCIO_0	88	VCCIO	0
VCCIO_0	92	VCCIO	0
GBIN2/PIO1	63	GBIN	1
GBIN3/PIO1	62	GBIN	1
PIO1	51	PIO	1
PIO1	52	PIO	1
PIO1	53	PIO	1
PIO1	54	PIO	1
PIO1	56	PIO	1
PIO1	57	PIO	1
PIO1	59	PIO	1
PIO1	60	PIO	1
PIO1	64	PIO	1
PIO1	65	PIO	1
PIO1	66	PIO	1
PIO1	68	PIO	1
PIO1	69	PIO	1
PIO1	71	PIO	1
PIO1	72	PIO	1
PIO1	73	PIO	1
PIO1	74	PIO	1
VCCIO_1	58	VCCIO	1
VCCIO_1	67	VCCIO	1
CDONE	43	CONFIG	2
CRESET_B	44	CONFIG	2
GBIN4/PIO2	iCE65L01: 33 iCE65L04: 34	GBIN	2
GBIN5/PIO2	iCE65L01: 36 iCE65L04: 33	GBIN	2
PIO2	26	PIO	2
PIO2	27	PIO	2

Pin Function	Pin Number	Type	Bank
PIO2	28	PIO	2
PIO2	29	PIO	2
PIO2	30	PIO	2
PIO2	iCE65L01: 34 iCE65L04: 36	PIO	2
PIO2	37	PIO	2
PIO2	40	PIO	2
PIO2/CBSEL0	41	PIO	2
PIO2/CBSEL1	42	PIO	2
VCCIO_2	31	VCCIO	2
VCCIO_2	38	VCCIO	2
PIO3/DP00A	1	PIO/DPIO	3
PIO3/DP00B	2	PIO/DPIO	3
PIO3/DP01A	3	PIO/DPIO	3
PIO3/DP01B	4	PIO/DPIO	3
PIO3/DP02A	7	PIO/DPIO	3
PIO3/DP02B	8	PIO/DPIO	3
PIO3/DP03A	9	PIO/DPIO	3
PIO3/DP03B	10	PIO/DPIO	3
PIO3/DP04A	12	PIO/DPIO	3
GBIN7/PIO3/DP04B	13	GBIN/DPIO	3
GBIN6/PIO3/DP05A	15	GBIN/DPIO	3
PIO3/DP05B	16	PIO/DPIO	3
PIO3/DP06A	18	PIO/DPIO	3
PIO3/DP06B	19	PIO/DPIO	3
PIO3/DP07A	20	PIO/DPIO	3
PIO3/DP07B	21	PIO/DPIO	3
PIO3/DP08A	24	PIO/DPIO	3
PIO3/DP08B	25	PIO/DPIO	3
VCCIO_3	6	VCCIO	3
VCCIO_3	14	VCCIO	3
VCCIO_3	22	VCCIO	3
PIOS/SPI_SO	45	SPI	SPI
PIOS/SPI_SI	46	SPI	SPI
PIOS/SPI_SCK	48	SPI	SPI
PIOS/SPI_SS_B	49	SPI	SPI
SPI_VCC	50	SPI	SPI
GND	5	GND	GND
GND	17	GND	GND
GND	23	GND	GND
GND	32	GND	GND
GND	39	GND	GND
GND	47	GND	GND
GND	55	GND	GND
GND	70	GND	GND
GND	84	GND	GND
GND	98	GND	GND
VCC	11	VCC	VCC
VCC	35	VCC	VCC

Pin Function	Pin Number	Type	Bank
VCC	61	VCC	VCC
VCC	77	VCC	VCC
VPP_2V5	75	VPP	VPP
VPP_FAST	76	VPP	VPP

Package Mechanical Drawing

Figure 37: VQ100 Package Mechanical Drawing: Standard Device Marking



Description		Symbol	Min.	Nominal	Max.	Units
Leads per Edge	X			25		Leads
	Y			25		
Number of Signal Leads		n		100		
Maximum Size (lead tip to lead tip)	X	E	—	16.0	—	mm
	Y	D	—	16.0	—	
Body Size	X	E1	—	14.0	—	
	Y	D1	—	14.0	—	
Edge Pin Center to Center	X	E2	—	12.0	—	
	Y	D2	—	12.0	—	
Lead Pitch		e	—	0.50	—	
Lead Width		b	0.17	0.20	0.27	
Total Package Height		A	—	1.20	—	
Stand Off		A1	0.05	—	0.15	
Body Thickness		A2	0.95	1.00	1.05	
Lead Length		L1	—	1.00	—	
Lead Thickness		c	0.09	—	0.20	
Coplanarity			—	0.08	—	

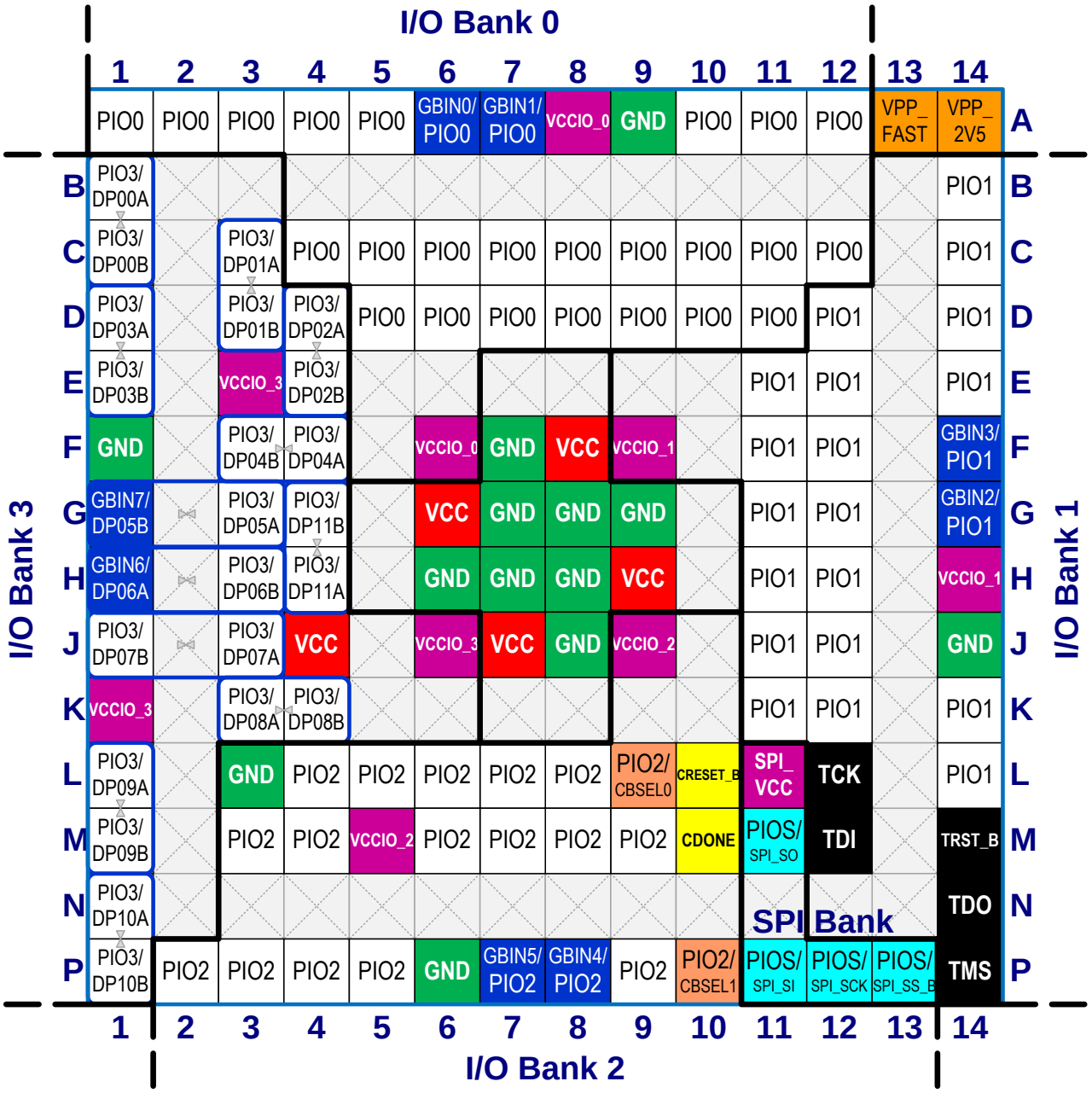
Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65L01F	Part number
	-T	Power/Speed
	ENG	Engineering
3	VQ100C NXXXXXXX	Package type and Lot number
4	YYWW	Date Code
5	N/A	Blank
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θJA (°C/W)	
0 LFM	200 LFM
38	32

Figure 43: **iCE65L08 CB132 Chip-Scale BGA Footprint (Top View)**



Pinout Table

Table 41 provides a detailed pinout table for the CB132 package. Pins are generally arranged by I/O bank, then by ball function. The table also highlights the differential I/O pairs in I/O Bank 3.

Table 41: iCE65 CB132 Chip-scale BGA Pinout Table

Ball Function	Ball Number	Pin Type	Bank
GBIN0/PIO0	iCE65L01: A7 iCE65L04/L08: A6	GBIN	0
GBIN1/PIO0	iCE65L01: A6 iCE65L04/08: A7	GBIN	0
PIO0	A1	PIO	0
PIO0	A2	PIO	0
iCE65L01: (NC) iCE65L04/L08: PIO0	A3	iCE65L01: (NC) iCE65L04: PIO0	0
PIO0	A4	PIO	0
PIO0	A5	PIO	0
PIO0	A10	PIO	0
iCE65L01: (NC) iCE65L04/L08: PIO0	A11	iCE65L01: (NC) iCE65L04: PIO0	0
PIO0	A12	PIO	0
PIO0	C10	PIO	0
PIO0	C11	PIO	0
PIO0	C12	PIO	0
PIO0	C4	PIO	0
PIO0	C5	PIO	0
PIO0	C6	PIO	0
PIO0	C7	PIO	0
PIO0	C8	PIO	0
PIO0	C9	PIO	0
PIO0	D5	PIO	0
PIO0	D6	PIO	0
PIO0	D7	PIO	0
PIO0	D8	PIO	0
PIO0	D9	PIO	0
PIO0	D10	PIO	0
PIO0	D11	PIO	0
VCCIO_0	A8	VCCIO	0
VCCIO_0	F6	VCCIO	0
GBIN2/PIO1	G14	GBIN	1
GBIN3/PIO1	F14	GBIN	1
PIO1	B14	PIO	1
PIO1	C14	PIO	1
PIO1	D12	PIO	1
PIO1	D14	PIO	1
PIO1	E11	PIO	1
PIO1	E12	PIO	1
PIO1	E14	PIO	1
PIO1	F11	PIO	1
PIO1	F12	PIO	1
PIO1	G11	PIO	1
PIO1	G12	PIO	1
PIO1	H11	PIO	1

Ball Function	Ball Number	Pin Type	Bank
PIO1	F14	PIO	1
PIO1	G10	PIO	1
PIO1	G11	PIO	1
PIO1	G13	PIO	1
PIO1	G14	PIO	1
PIO1	H10	PIO	1
PIO1	H11	PIO	1
PIO1	H12	PIO	1
PIO1	H13	PIO	1
PIO1	J10	PIO	1
PIO1	J11	PIO	1
PIO1	J12	PIO	1
PIO1	J13	PIO	1
PIO1	K11	PIO	1
PIO1	K12	PIO	1
PIO1	K14	PIO	1
PIO1	L13	PIO	1
PIO1	L14	PIO	1
PIO1	M13	PIO	1
TCK	L12	JTAG	1
TDI	M12	JTAG	1
TDO	N14	JTAG	1
TMS	P14	JTAG	1
TRST_B	M14	JTAG	1
VCCIO_1	F9	VCCIO	1
VCCIO_1	H14	VCCIO	1
CDONE	M10	CONFIG	2
CRESET_B	L10	CONFIG	2
GBIN4/PIO2 (◆)	***iCE65L04:*** L7 ***iCE65L08:*** N8	GBIN	2
GBIN5/PIO2 (◆)	***iCE65L04:*** P5 ***iCE65L08:*** M7	GBIN	2
PIO2	K5	PIO	2
PIO2	K6	PIO	2
PIO2	K7	PIO	2
PIO2	K8	PIO	2
PIO2	K9	PIO	2
PIO2	L4	PIO	2
PIO2	L5	PIO	2
PIO2	L6	PIO	2
PIO2	L8	PIO	2
PIO2	M3	PIO	2
PIO2	M4	PIO	2
PIO2	M6	PIO	2
PIO2 (◆)	***iCE65L04:*** M7 ***iCE65L08:*** P5	PIO	2
PIO2	M8	PIO	2
PIO2	M9	PIO	2
PIO2	N3	PIO	2
PIO2	N4	PIO	2
PIO2	N5	PIO	2
PIO2	N6	PIO	2

Ball Function	Ball Number	Pin Type	Bank
PIO3/DP13A	H5	DPIO	3
PIO3/DP13B	G5	DPIO	3
PIO3/DP14A	L1	DPIO	3
PIO3/DP14B	L2	DPIO	3
PIO3/DP15A	M1	DPIO	3
PIO3/DP15B	M2	DPIO	3
PIO3/DP16A (◆)	***iCE65L04:*** K3 ***iCE65L08:*** K4	DPIO	3
PIO3/DP16B (◆)	***iCE65L08:*** K4 ***iCE65L08:*** K3	DPIO	3
PIO3/DP17A	N1	DPIO	3
PIO3/DP17B	N2	DPIO	3
VCCIO_3	E3	VCCIO	3
VCCIO_3	J6	VCCIO	3
VCCIO_3	K1	VCCIO	3
PIOS/SPI_SO	M11	SPI	SPI
PIOS/SPI_SI	P11	SPI	SPI
PIOS/SPI_SCK	P12	SPI	SPI
PIOS/SPI_SS_B	P13	SPI	SPI
SPI_VCC	L11	SPI	SPI
GND	A9	GND	GND
GND	B12	GND	GND
GND	C2	GND	GND
GND	F1	GND	GND
GND	F7	GND	GND
GND	G7	GND	GND
GND	G8	GND	GND
GND	G9	GND	GND
GND	H6	GND	GND
GND	H7	GND	GND
GND	H8	GND	GND
GND	J5	GND	GND
GND	J8	GND	GND
GND	J14	GND	GND
GND	K10	GND	GND
GND	L3	GND	GND
GND	P6	GND	GND
VCC	B7	VCC	VCC
VCC	F2	VCC	VCC
VCC	F8	VCC	VCC
VCC	G6	VCC	VCC
VCC	H9	VCC	VCC
VCC	J4	VCC	VCC
VCC	J7	VCC	VCC
VCC	K13	VCC	VCC
VCC	N7	VCC	VCC
VPP_2V5	A14	VPP	VPP
VPP_FAST	A13	VPP	VPP

Pinout Differences between iCE65L04 and iCE65L08 in CB196 Package

Table 43 lists the package balls that are different between the pinouts for iCE65L04 and the iCE65L08 in the CB196 package. The table also describes the functional differences between these pins, which is critical when designing a CB196 footprint that supports both the iCE65L04 and the iCE65L08 devices. In some cases, only the differential inputs are swapped; single-ended I/Os are not affected. A swapped differential pair can be inverted internally for functional equivalence. In other cases, a global buffer input is swapped with another PIO pin in the same bank.

***Table 43:* Pinout Differences between iCE65L04 and iCE65L08 in CB196 Package**

Ball Number	iCE65L04	iCE65L08	Functional Difference
E1	PIO3/DP03A	PIO3/DP03B	Differential inputs swapped, single-ended I/Os not affected
E2	PIO3/DP03B	PIO3/DP03A	
F3	PIO3/DP05A	PIO3/DP05B	Differential inputs swapped, single-ended I/Os not affected
F4	PIO3/DP05B	PIO3/DP05A	
G1	GBIN7/PIO3/DP07B	PIO3/DP11A	Global buffer input GBIN7 and its associated differential input is swapped with another differential pair in I/O Bank 3
G2	PIO3/DP07A	PIO3/DP11B	
H3	PIO3/DP11B	GBIN7/PIO3/DP07B	
H4	PIO3/DP11A	PIO3/DP07A	
K3	PIO3/DP16A	PIO3/DP16B	Differential inputs swapped, single-ended I/Os not affected
K4	PIO3/DP16B	PIO3/DP16A	
L7	GBIN4/PIO2	PIO2	Global buffer input GBIN4 swapped with another PIO pin in I/O Bank 2
N8	PIO2	GBIN4/PIO2	
M7	PIO2	GBIN5/PIO2	Global buffer input GBIN5 swapped with another PIO pin in I/O Bank 2
P5	GBIN5/PIO2	PIO2	

iCE65L04 Pad Name	DiePlus VQ100	CB132	CB196	CB284	Pad	X (µm)	Y (µm)
PIO0_16	—	—	—	C19	214	2,122.00	2,860.80
PIO0_17	—	—	C9	C18	215	2,087.00	2,962.80
PIO0_18	—	—	B9	C17	216	2,052.00	2,860.80
PIO0_19	—	—	D8	C16	217	2,017.00	2,962.80
PIO0_20	—	—	C8	C15	218	1,982.00	2,860.80
PIO0_21	—	—	E8	C14	219	1,947.00	2,962.80
PIO0_22	—	—	B8	C13	220	1,912.00	2,860.80
GBIN1/PIO0_23	89	A7	E7	E11	221	1,877.00	2,962.80
GND	—	—	B12	C12	222	1,842.00	2,860.80
GND	—	—	—	—	223	1,807.00	2,962.80
GBIN0/PIO0_24	90	A6	A7	E10	224	1,772.00	2,860.80
PIO0_25	—	—	D7	C11	225	1,737.00	2,962.80
PIO0_26	—	—	C7	C10	226	1,702.00	2,860.80
PIO0_27	—	—	E6	C9	227	1,667.00	2,962.80
VCC	—	—	B7	C8	228	1,632.00	2,860.80
VCC	—	—	—	—	229	1,597.00	2,962.80
PIO0_28	—	—	A6	C7	230	1,562.00	2,860.80
PIO0_29	—	—	B6	C6	231	1,527.00	2,962.80
PIO0_30	—	—	A5	C5	232	1,492.00	2,860.80
PIO0_31	—	—	D6	C4	233	1,457.00	2,962.80
GND	—	F7	F7	K11	234	1,422.00	2,860.80
GND	—	—	—	—	235	1,387.00	2,962.80
PIO0_32	—	—	—	C3	236	1,352.00	2,860.80
PIO0_33	—	—	—	A7	237	1,317.00	2,962.80
PIO0_34	—	—	—	A6	238	1,282.00	2,860.80
PIO0_35	—	—	—	A5	239	1,247.00	2,962.80
PIO0_36	91	C7	C6	G11	240	1,212.00	2,860.80
VCCIO_0	92	F6	F6	K10	241	1,177.00	2,962.80
VCCIO_0	92	F6	F6	K10	242	1,142.00	2,860.80
PIO0_37	93	D7	C5	H11	243	1,107.00	2,962.80
PIO0_38	94	C6	B5	G10	244	1,072.00	2,860.80
PIO0_39	95	A5	A4	E9	245	1,037.00	2,962.80
PIO0_40	96	D6	B4	H10	246	1,002.00	2,860.80
PIO0_41	97	C5	D5	G9	247	967.00	2,962.80
PIO0_42	—	A4	A3	E8	248	917.00	2,860.80
GND	98	G7	G7	L11	249	867.00	2,962.80
PIO0_43	99	D5	B3	H9	250	817.00	2,860.80
PIO0_44	—	C4	C4	G8	251	767.00	2,962.80
PIO0_45	100	A3	A2	E7	252	717.00	2,860.80
PIO0_46	—	A2	A1	E6	253	667.00	2,962.80
PIO0_47	—	A1	B2	E5	254	617.00	2,860.80

I/O Banks 0, 1, 2 and SPI Bank Characteristic Curves

Figure 52: **Typical LVCMOS Output Low Characteristics (I/O Banks 0, 1, 2, and SPI)**

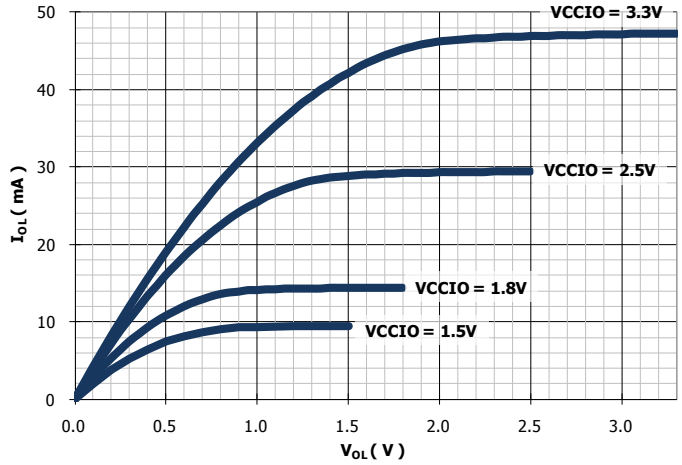


Figure 53: **Typical LVCMOS Output High Characteristics (I/O Banks 0, 1, 2, and SPI)**

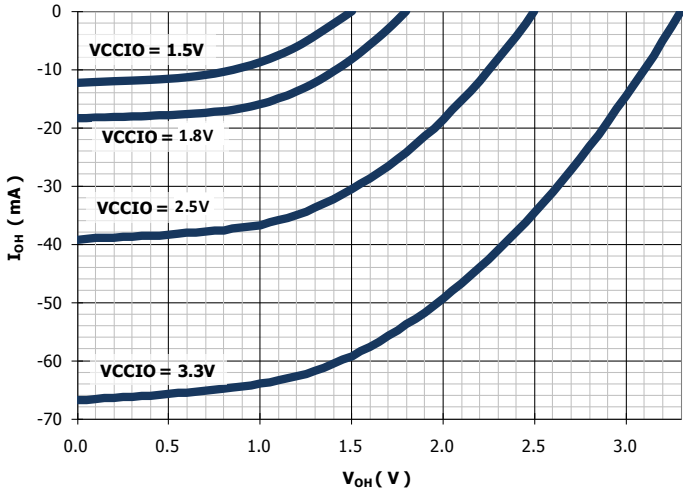


Figure 54: **Input with Internal Pull-Up Resistor Enabled (I/O Banks 0, 1, 2, and SPI)**

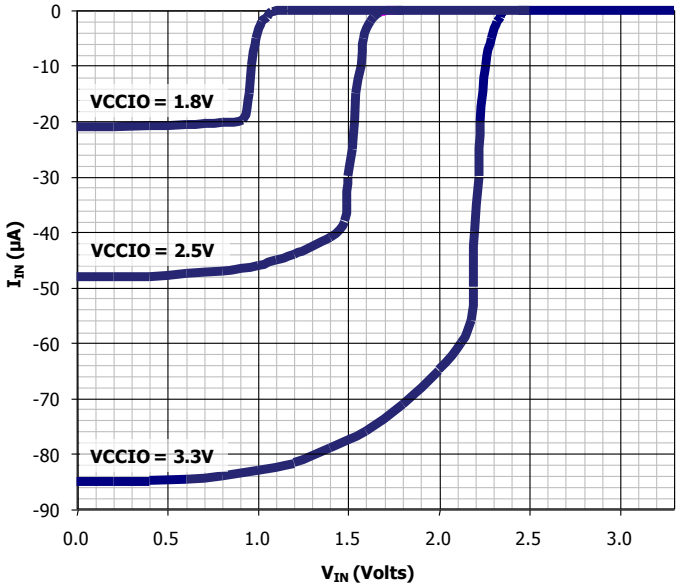


Table 60 provides various timing specifications for the SPI peripheral mode interface.

Table 60: SPI Peripheral Mode Timing

Symbol	From	To	Description		All Grades Min.	All Grades Max.	Units
t_{CR_SCK}	CRESET_B	SPI_SCK	Minimum time from a rising edge on CRESET_B until the first SPI write operation, first SPI_SCK. During this time, the iCE65 FPGA is clearing its internal configuration memory	iC65L01	800	—	µs
				iC65L04	800		
				iC65L08	1200		
$t_{SUSPISI}$	SPI_SI	SPI_SCK	Setup time on SPI_SI before the rising SPI_SCK clock edge		12	—	ns
$t_{HDSPISI}$	SPI_SCK	SPI_SI	Hold time on SPI_SI after the rising SPI_SCK clock edge		12	—	ns
$t_{SPISCKH}$	SPI_SCK	SPI_SCK	SPI_SCK clock High time		20	—	ns
$t_{SPISCKL}$	SPI_SCK	SPI_SCK	SPI_SCK clock Low time		20	—	ns
$t_{SPISCKCYC}$	SPI_SCK	SPI_SCK	SPI_SCK clock period*		40	1,000	ns
F_{SPI_SCK}	SPI_SCK	SPI_SCK	Sustained SPI_SCK clock frequency*		1	25	MHz

* = Applies after sending the synchronization pattern.

Power Consumption Characteristics

Core Power

Table 61 shows the power consumed on the internal VCC supply rail when the device is filled with 16-bit binary counters, measured with a 32.768 kHz and at 32.0 MHz. Low power (-L) at 1.0 V operation and high-performance (-T) version at 1.2V operation is provided.

***Table 61:* VCC Power Consumption for Device Filled with 16-Bit Binary Counters**

Symbol	Description	Grade	VCC	iCE65L01 Typical	iCE65L01 Max.	iCE65L04 Typical	iCE65L04 Max.	iCE65L08 Typical	iCE65L08 Max.	Units
I_{CC0K}	f =0,	-L	1.0V	12		26		54		µA
		-T	1.2V	19		43		90		
I_{CC32K}	f ≤ 32.768 kHz	-L	1.0V	15		31		62		µA
		-T	1.2V	23		50		100		
I_{CC32M}	f = 32.0 MHz	-L	1.0V	3		7		14		mA
		-T	1.2V	4		8		17		

I/O Power

Table 62 provides the static current by I/O bank. The typical current for I/O Banks 0, 1, 2 and the SPI bank is not measurable within the accuracy of the test environment. The PIOs in I/O Bank 3 use different circuitry and dissipate a small amount of static current.

Table 62: I/O Bank Static Current (f = 0 MHz)

Symbol	Description		Typical	Max	Units
I_{CCO_0}	I/O Bank 0	Static current consumption per I/O bank. f = 0 MHz. No PIO pull-up resistors enabled. All inputs grounded. All outputs driving Low.	« 1		µA
I_{CCO_1}	I/O Bank 1		« 1		µA
I_{CCO_2}	I/O Bank 2		« 1		µA
I_{CCO_3}	I/O Bank 3		iCE65L01: « 1 iCE65L04/08: 1.2		µA
I_{CCO_SPI}	SPI Bank		« 1		µA

NOTE: The typical static current for I/O Banks 0, 1, 2, and the SPI bank is less than the accuracy of the device tester.

Power Estimator

To estimate the power consumption for a specific application, please download and use the iCE65 Power Estimator Spreadsheet our use the power estimator built into the iCEcube software.

- iCE65 Power Estimator Spreadsheet

Notes

Revision History

Version	Date	Description
2.42	30-MAR-2012	Changed company name. Updated Table 1
2.41	1-AUG-2011	Added VQ100 marking for NVCM programming.
2.4	13-MAY-2011	Added L01 CB121 package Figure 39. Added note "else VCCIO_1 draws current" to JTAG inputs TCK, TDI and TMS do not have the input pull-up resistor and must be tied off to GND when unused, Table 32. Input pin leakage current Table 49 split by bank. QN84 package drawing, Figure 35, added note "underside metal is at ground potential", increased thermal resistance. Added Marking Format and Thermal resistance to CB81 Packag Mechanical Drawing Figure 33. Added coplanarity specification to VQ100 Package Mechanical Drawing Figure 37
2.3	18-OCT-2010	Added L01 CB81 and L08 CB132 packages.
2.2.3	12-OCT-2010	Changed Figure 29: Application Processor Waveforms for SPI Peripheral Mode Configuration Process and Table 60 from 300 µs CRESET_B to 800 µs for iCE65L01/04 and 1200 µs for iCE65L08.
2.2.2	8-OCT-2010	Added iCE65L04 marking specification to Figure 47 CB196 Package Mechanical Drawing.
2.2.1	5-OCT-2010	Changed FSPI_SCK from 0.125 MHz to 1 MHz in SPI Peripheral Configuration Interface and in Table 60.
2.2	6-AUG-2010	Programmable Interconnect section removed.
2.1.1	26-MAY-2010	Switched labels on Figure 53 LVCMOS Output High, VCCIO = 1.8V with VCCIO = 2.5V.
2.1	15-MAR-2010	Added JTAG unused input tie off guideline. Added marking specification and thermal characteristics to package drawings. Added production datasheet for iCE65L01 with timing update, including QN84, VQ100 and CB132. Added NVCM shut-off on SPI configuration. Added non-standard VCCIO operating conditions. Increased the minimum voltage supply specification for LVCMOS33 to 3.14V in Table 48.
2.0.1	12-NOV-2009	Recommended Operation Conditions, Table 47, replaced junction with ambient.
2.0	14-SEPT-2009	Finalized production data sheet for iCE65L04 and iCE65L08. Improved SubLVDS input specification V_{ICM} in Table 52. CS63 and CC72 packages removed and placed in iCE DiCE KGD, Known Good Die datasheet. Added "IBIS Models for I/O Banks 0, 1, 2 and the SPI Bank". Added "Printed Circuit Board Layout Information".
1.5.1	13-JUL-2009	Updated the text in "SPI PROM Requirements" section. Minor label change in Figure 48.
1.5	20-JUN-2009	Updated timing information and added –T high-speed device option (affected Figure 2, Table 48, Table 54, Table 55, Table 56, and Table 61). Added support for 3.3V LVCMOS I/Os in I/O Bank 3 (affected Figure 7, Table 5, Table 7, Table 8, Table 47, Table 48, and Table 51). Added a section about the SPI Peripheral Configuration Interface and timing in Table 60. Added a warning that a Warm Boot operation can only jump to another configuration image that has Warm Boot disabled. Updated configuration image size and configuration time for the iCE65L02 in Table 27 and Table 58. Reduced the minimum voltage supply specification for LVCMOS33 to 2.7V in Table 48. Added information about which power rails can be disconnected without effecting the Power-On Reset (POR) circuit and clarified description of VPP_2V5 pin in Table 36. Added I/O characterization curves (Figure 52, Figure 53, and Figure 54). Minor changes to Figure 20 and Figure 21. Changed timing per Figures 54-58 and Tables 55-57.
1.4.4	25-MAR-2009	Clarified the voltage requirements for the VPP_2V5 pin in Table 36 and notes under Table 48.
1.4.3	9-MAR-2009	Removed volatile-only (-V) product offering from Figure 2. Corrected NC on ball V22, removed it for ball T22 on CB284 package (Figure 48).
1.4.2	27-FEB-2009	Updated Table 14, Table 23, Table 26, Table 30, Table 33, Table 35, and Table 46. Updated I/O Bank 3 information in Table 7 and Table 48.
1.4.1	24-FEB-2009	Based on characterization data, reduced 32KHz operating current by 40% in Table 1, Table 61, and Figure 1. Corrected that SSTL18 standards require VREF pin in Table 7. Correct ball numbers for GBIN4/GBIN5 for CS110 package.
1.4	9-FEB-2009	Added footprint and pinout information for the VQ100 Very-thin Quad Flat Package. Added footprint for iCE65L08 in CB196 (Figure 46) and added Table 43 showing the differences between the 'L04 and 'L08 in the CB196 package. Unified the package footprint nomenclature in the Package and Pinout Information section. Added note to Global Buffer Inputs that the differential clock direct input is not available on the CB132 package. Added tables showing the ball/pin number for various control functions, by package (Table 14, Table 23, Table 26, Table 30, and Table 33). Corrected the GBIN/GBUF designations. GBIN4 and GBIN5 were swapped as were GBIN6 and GBIN7. This change affected all pinout tables and footprint diagrams. Updated and corrected "Differential Global Buffer Input." Tested and corrected the clock-enable and reset connections between global buffers and various resources (Table 11, Table 12, and Table 13). Added "Automatic Global Buffer Insertion, Manual Insertion." Added "Die Cross Reference" section. Improved industrial temperature range by lowering

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