Lattice Semiconductor Corporation - ICE65L04F-TCB284I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	440
Number of Logic Elements/Cells	3520
Total RAM Bits	81920
Number of I/O	176
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	284-VFBGA, CSPBGA
Supplier Device Package	284-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice65l04f-tcb284i

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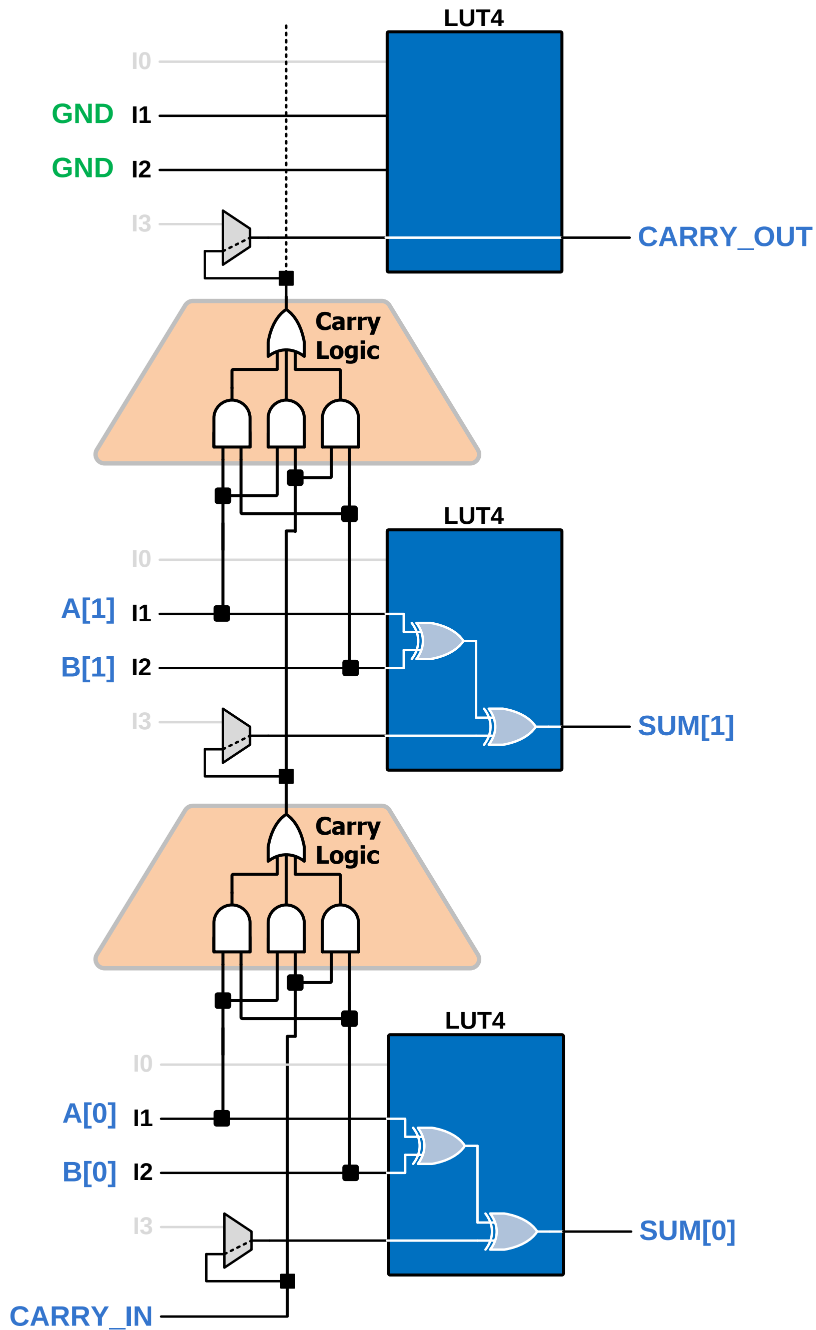
Implementing Subtracters, Decrementers

As mentioned earlier, the Carry Logic generates a High output whenever the sum of `I1 + I2 + CARRY_IN` generates a carry. The Carry Logic does not specifically have a subtract mode. To implement a subtract function or decrement function, logically invert either the I1 or I2 input and invert the initial carry input. This performs a 2s complement subtract operation.

Figure 6: Two-bit Adder Example



If not connected to an external SPI PROM, the four pins associated with the SPI Master Configuration Interface can be used as PIO pins, supplied by the SPI_VCC input, essentially forming a fifth "mini" I/O bank. If using an SPI Flash PROM, then connect SPI_VCC to 3.3V.

I/O Banks 0, 1, 2, SPI and Bank 3 of iCE65L01

Table 6 highlights the available I/O standards when using an iCE65 device, indicating the drive current options, and in which bank(s) the standard is supported. I/O Banks 0, 1, 2 and SPI interface support the same standards. I/O Bank 3 has additional capabilities in iCE65L04 and iCE65L08, including support for MDDR memory standards and LVDS differential I/O.

***Table 6:* I/O Standards for I/O Banks 0, 1, 2, SPI Interface Bank, and Bank 3 of iCE65L01**

I/O Standard	Supply Voltage	Drive Current (mA)	Attribute Name
5V Input Tolerance	3.3V	N/A	N/A
LVCMOS33	3.3V	±11	SB_LVCMOS
LVCMOS25	2.5V	±8	
LVCMOS18	1.8V	±5	
LVCMOS15 outputs	1.5V	±4	

IBIS Models for I/O Banks 0, 1, 2 and the SPI Bank

The IBIS (I/O Buffer Information Specification) file that describes the output buffers used in I/O Banks 0, 1, 2, SPI Bank and Bank 3 of iCE65L01 is available from the following link.

- IBIS Models for I/O Banks 0, 1, 2, SPI Bank and Bank 3 of iCE65L01

I/O Bank 3 of iCE65L04 and iCE65L08

I/O Bank 3, located along the left edge of the die, has additional special I/O capabilities to support memory components and differential I/O signaling (LVDS). Table 7 lists the various I/O standards supported by I/O Bank 3. The SSTL2 and SSTL18 I/O standards require the VREF voltage reference input pin which is only available on the CB284 package. Also see Table 51 for electrical characteristics.

***Table 7:* I/O Standards for I/O Bank 3 Only of iCE65L04 and iCE65L08**

I/O Standard	Supply Voltage	VREF Pin (CB284 or DiePlus) Required?	Target Drive Current (mA)	Attribute Name
LVCMOS33	3.3V	No	±8	SB_LVCMOS33_8
LVCMOS25	2.5V	No	±16	SB_LVCMOS25_16
			±12	SB_LVCMOS25_12
			±8	SB_LVCMOS25_8
			±4	SB_LVCMOS25_4
LVCMOS18	1.8V	No	±10	SB_LVCMOS18_10
			±8	SB_LVCMOS18_8
			±4	SB_LVCMOS18_4
			±2	SB_LVCMOS18_2
LVCMOS15	1.5V	No	±4	SB_LVCMOS15_4
			±2	SB_LVCMOS15_2
SSTL2_II	2.5V	Yes	±16.2	SB_SSTL2_CLASS_2
SSTL2_I			±8.1	SB_SSTL2_CLASS_1
SSTL18_II	1.8V	Yes	±13.4	SB_SSTL18_FULL
SSTL18_I			±6.7	SB_SSTL18_HALF
MDDR	1.8V	No	±10	SB_MDDR10
			±8	SB_MDDR8
			±4	SB_MDDR4
			±2	SB_MDDR2
LVDS	2.5V	No	N/A	SB_LVDS_INPUT

Table 8 lists the I/O standards that can co-exist in I/O Bank 3, depending on the VCCIO_3 voltage.

***Table 8:* Compatible I/O Standards in I/O Bank 3 of iCE65L04 and iCE65L08**

VCCIO_3 Voltage	3.3V	2.5V	1.8V	1.5V
Compatible I/O Standards	SB_LVCMOS33_8	Any SB_LVCMOS25 SB_SSTL2_Class_2 SB_SSTL2_Class_1 SB_LVDS_INPUT	Any SB_LVCMOS18 SB_SSTL18_FULL SB_SSTL18_HALF SB_MDDR10 SB_MDDR8 SB_MDDR4 SB_MDDR2 SB_LVDS_INPUT	Any SB_LVCMOS15

Programmable Output Drive Strength

Each PIO in I/O Bank 3 offers programmable output drive strength, as listed in Table 8. For the LVCMOS and MDDR I/O standards, the output driver has settings for static drive currents ranging from 2 mA to 16 mA output drive current, depending on the I/O standard and supply voltage.

The SSTL18 and SSTL2 I/O standards offer full- and half-strength drive current options

Differential Inputs and Outputs

All PIO pins support "single-ended" I/O standards, such as LVCMOS. However, iCE65 FPGAs also support differential I/O standards where a single data value is represented by two complementary signals transmitted or received using a pair of PIO pins. The PIO pins in I/O Bank 3 of iCE65L04 and iCE65L08L08 support Low-Voltage Differential Swing (LVDS) and SubLVDS inputs as shown in Figure 8. Differential outputs are available in all four I/O banks.

Differential Inputs Only on I/O Bank 3 of iCE65L04 and iCE65L08

Differential receivers are required for popular applications such as LVDS and LVPECL clock inputs, camera interfaces, and for various telecommunications standards.

Specific pairs of PIO pins in I/O Bank 3 form a differential input. Each pair consists of a DPxxA and DPxxB pin, where "xx" represents the pair number. The DPxxB receives the true version of the signal while the DPxxA receives the complement of the signal. Typically, the resulting signal pair is routed on the printed circuit board (PCB) with matched 50Ω signal impedance. The differential signaling, the low voltage swing, and the matched signal routing are ideal for communicating very-high frequency signals. Differential signals are generally also more tolerant of system noise and generate little EMI themselves.

The LVDS input circuitry requires 2.5V on the VCCIO_3 voltage supply. Similarly, the SubLVDS input circuitry requires 1.8V on the VCCIO_3 voltage supply. For electrical specifications, see "Differential Inputs" on page 100.

Each differential input pair requires an external 100 Ω termination resistor, as shown in Figure 8.

The PIO pins that make up a differential input pair are indicated with a blue bounding box in the footprint diagrams and in the pinout tables.

Input and Output Register Control per PIO Pair

PIO pins are grouped into pairs for synchronous control. Registers within pairs of PIO pins share common input clock, output clock, and I/O clock enable control signals, as illustrated in Figure 11. The combinational logic paths are removed from the drawing for clarity.

The INCLK clock signal only controls the input flip-flops within the PIO pair.

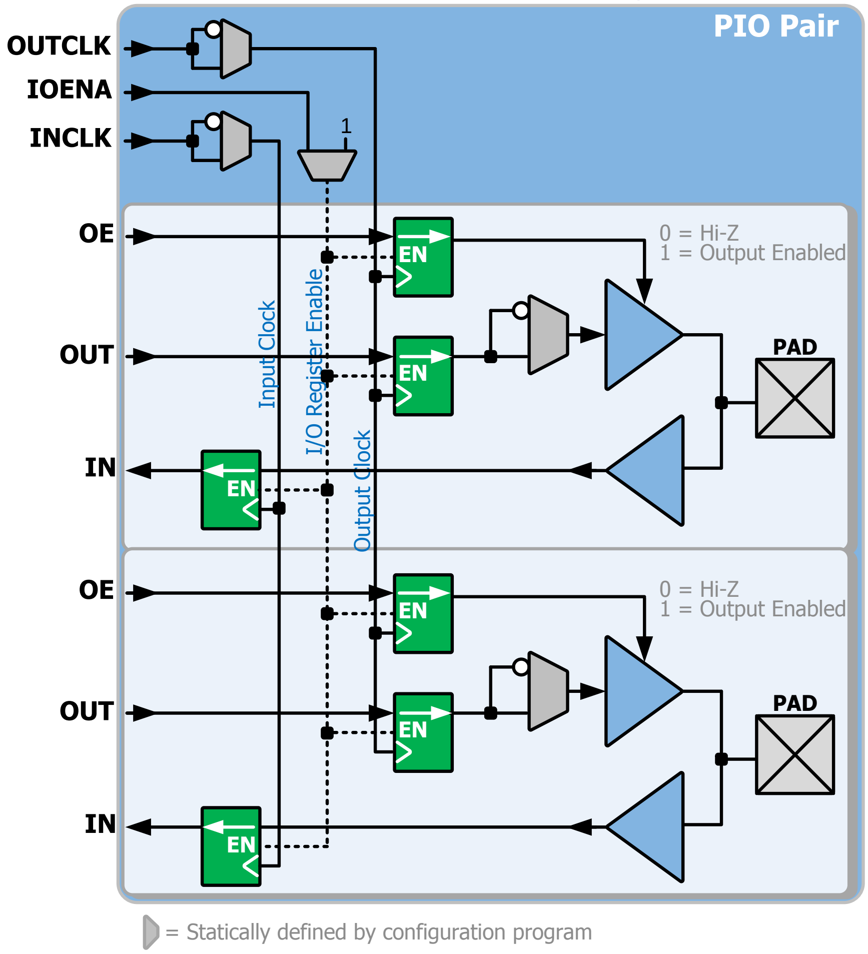
The OUTCLK clock signal controls the output flip-flops and the output-enable flip-flops within the PIO pair.

If desired in the iCE65 application, the INCLK and OUTCLK signals can be connected together.

The IOENA clock-enable input, if used, enables all registers in the PIO pair, as shown in Figure 11. By default, the registers are always enabled.

> ⚠ Before laying out your printed-circuit board, run the design through the iCEcube development software to verify that your selected pinout complies with these I/O register pairing requirements. See tables in "Die Cross Reference" starting on page 84.

Figure 11: **PIO Pairs Share Clock and Clock Enable Controls (only registered paths shown for clarity)**



The pairing of PIO pairs is most evident in the tables in "Die Cross Reference" starting on page 84.

Table 12 and Table 13 list the connections between a specific global buffer and the inputs on a Programmable I/O (PIO) pair. Although there is no direct connection between a global buffer and a PIO output, such a connection is possible by first connecting through a PLB LUT4 function. Again, all global buffers optionally drive all clock inputs. However, even-numbered global buffers optionally drive the clock-enable input on a PIO pair.

> ⚠ The PIO clock enable connect is different between the iCE65L01/iCE65L04 and iCE65L08.

***Table 12:* iCE65L01 & iCE65L04: Global Buffer (GBUF) Connections to Programmable I/O (PIO) Pair**

Global Buffer	Output Connections	Input Clock	Output Clock	Clock Enable
GBUF0	No (connect through PLB LUT)	Yes	Yes	No
GBUF1		Yes	Yes	Yes
GBUF2		Yes	Yes	No
GBUF3		Yes	Yes	Yes
GBUF4		Yes	Yes	No
GBUF5		Yes	Yes	Yes
GBUF6		Yes	Yes	No
GBUF7		Yes	Yes	Yes

***Table 13:* iCE64L08: Global Buffer (GBUF) Connections to Programmable I/O (PIO) Pair**

Global Buffer	Output Connections	Input Clock	Output Clock	Clock Enable
GBUF0	No (connect through PLB LUT)	Yes	Yes	Yes
GBUF1		Yes	Yes	No
GBUF2		Yes	Yes	Yes
GBUF3		Yes	Yes	No
GBUF4		Yes	Yes	Yes
GBUF5		Yes	Yes	No
GBUF6		Yes	Yes	Yes
GBUF7		Yes	Yes	No

Global Buffer Inputs

The iCE65 component has eight specialized GBIN/PIO pins that are optionally direct inputs to the global buffers, offering the best overall clock characteristics. As shown in Figure 15, each GBIN/PIO pin is a full-featured I/O pin but also provides a direct connection to its associated global buffer. The direct connection to the global buffer bypasses the iCEgate input-blocking latch and other PIO input logic. These special PIO pins are allocated two to an I/O Bank, a total of eight. These pins are labeled GBIN0 through GBIN7, as shown in Figure 14 and the pin locations for each GBIN input appear in Table 14.

***Table 14:* Global Buffer Input Ball/Pin Number by Package**

Global Buffer Input (GBIN)	I/O Bank	VQ100	CB132	`L04 CB196	`L08 CB196	CB284
GBIN0	0	90	A6	A7	A7	E10
GBIN1		89	A7	E7	E7	E11
GBIN2	1	63	G14	F10	F10	L18
GBIN3		62	F14	G12	G12	K18
GBIN4	2	34	P8	L7	N8	V12
GBIN5		33	P7	P5	M7	V11
GBIN6	3	15	H1	H1	H1	M5
GBIN7		13	G1	G1	H3	L5

Automatic Global Buffer Insertion, Manual Insertion

The iCEcube development software automatically assigns high-fanout signals to a global buffer. However, to manual insert a global buffer input/global buffer (GBIN/GBUF) combination, use the `SB_IO_GB` primitive. To insert just a global buffer (GBUF), use the `SB_GB` primitive.

Global Hi-Z Control

The global high-impedance control signal, GHIZ, connects to all I/O pins on the iCE65 device. This GHIZ signal is automatically asserted throughout the configuration process, forcing all user-I/O pins into their high-impedance state. Similarly, the PIO pins can be forced into their high-impedance state via the JTAG controller.

Global Reset Control

The global reset control signal connects to all PLB and PIO flip-flops on the iCE65 device. The global reset signal is automatically asserted throughout the configuration process, forcing all flip-flops to their defined wake-up state. For PLB flip-flops, the wake-up state is always reset, regardless of the PLB flip-flop primitive used in the application. See Table 3 for more information.

The PIO flip-flops are always reset during configuration, although the output flip-flop can be inverted before leaving the iCE65 device, as shown in Figure 11.

RAM

Each iCE65 device includes multiple high-speed synchronous RAM blocks (RAM4K), each 4Kbit in size. As shown in Table 16 a single iCE65 integrates between 16 to 96 such blocks. Each RAM4K block is generically a 256-word deep by 16-bit wide, two-port register file, as illustrated in Figure 17. The input and output connections, to and from a RAM4K block, feed into the programmable interconnect resources.

Figure 17: RAM4K Memory Block

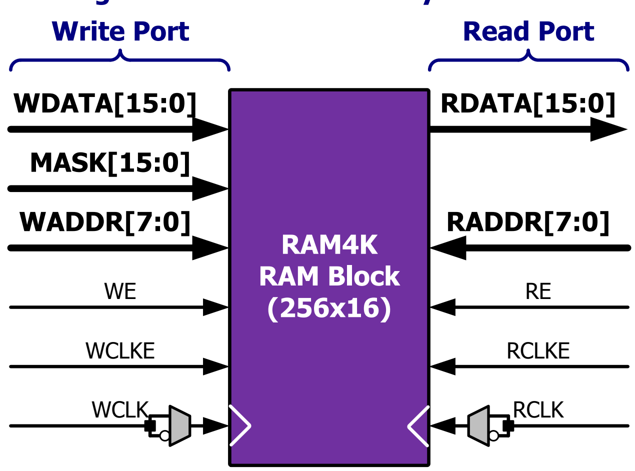


Table 16: RAM4K Blocks per Device

Device	RAM4K Blocks	Default Configuration	RAM Bits per Block	Block RAM Bits
iCE65L01	16	256 x 16	4K (4,096)	64K
iCE65L04	20			80K
iCE65L08	32			128K

Using programmable logic resources, a RAM4K block implements a variety of logic functions, each with configurable input and output data width.

- Random-access memory (RAM)
  - Single-port RAM with a common address, enable, and clock control lines
  - Two-port RAM with separate read and write control lines, address inputs, and enable

- Register file and scratchpad RAM
- First-In, First-Out (FIFO) memory for data buffering applications
- Circuit buffer
- A 256-deep by 16-wide ROM with registered outputs, contents loaded during configuration
  - Sixteen different 8-input look-up tables
  - Function or waveform tables such as sine, cosine, etc.
  - Correlators or pattern matching operations
- Counters, sequencers

As pictured in Figure 17, a RAM4K block has separate write and read ports, each with independent control signals. Table 17 lists the signals for both ports. Additionally, the write port has an active-Low bit-line write-enable control; optionally mask write operations on individual bits. By default, input and output data is 16 bits wide, although the data width is configurable using programmable logic and, if needed, multiple RAM4K blocks.

The WCLK and RCLK inputs optionally connect to one of the following clock sources.

- The output from any one of the eight Global Buffers, or
- A connection from the general-purpose interconnect fabric

The data contents of the RAM4K block are optionally pre-loaded during iCE65 device configuration. If the RAM4K blocks are not pre-loaded during configuration, then the resulting configuration bitstream image is smaller. However, if an uninitialized RAM4K block is used in the application, then the application must initialize the RAM contents to guarantee the data value.

See Table 56 for detailed timing information.

Signals

Table 17 lists the signal names, direction, and function of each connection to the RAM4K block. See also Figure 17.

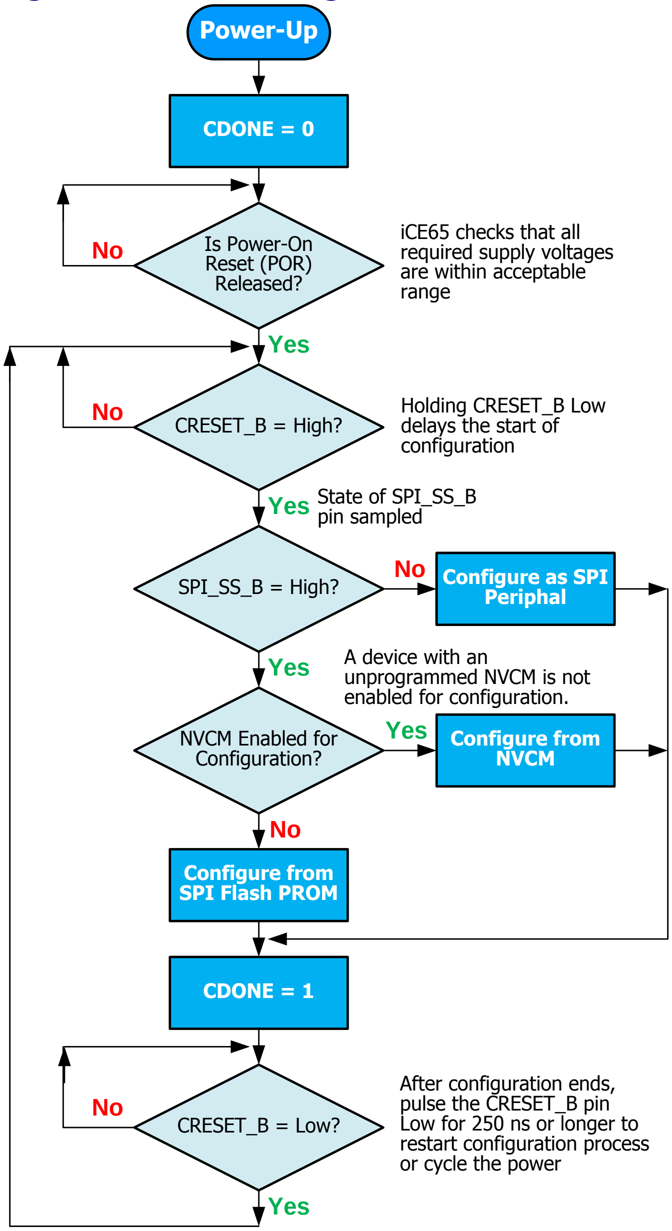
Table 17: RAM4K Block RAM Signals

Signal Name	Direction	Description
WDATA[15:0]	Input	Write Data input.
MASK[15:0]	Input	Masks write operations for individual data bit-lines. 0 = Write bit; 1 = Don't write bit
WADDR[7:0]	Input	Write Address input. Selects one of 256 possible RAM locations.
WE	Input	Write Enable input.
WCLKE	Input	Write Clock Enable input.
WCLK	Input	Write Clock input. Default rising-edge, but with falling-edge option.
RDATA[15:0]	Output	Read Data output.
RADDR[7:0]	Input	Read Address input. Selects one of 256 possible RAM locations.
RE	Input	Read Enable input.
RCLKE	Input	Read Clock Enable input.
RCLK	Input	Read Clock input. Default rising-edge, but with falling-edge option.

Write Operations

Figure 18 shows the logic involved in writing a data bit to a RAM location. Table 18 describes various write operations for a RAM4K block. By default, all RAM4K write operations are synchronized to the rising edge of WCLK although the clock is invertible as shown in Figure 18.

Figure 20: **Device Configuration Control Flow**



Configuration Image Size

Table 23 shows the number of memory bits required to configure an iCE65 device. Two values are provided for each device. The "Logic Only" value indicates the minimum configuration size, the number of bits required to configure only the logic fabric, leaving the RAM4K blocks uninitialized. The "Logic + RAM4K" column indicates the maximum configuration size, the number of bits to configure the logic fabric and to pre-initialize all the RAM4K blocks.

Figure 21: iCE65 Configuration Control Pins

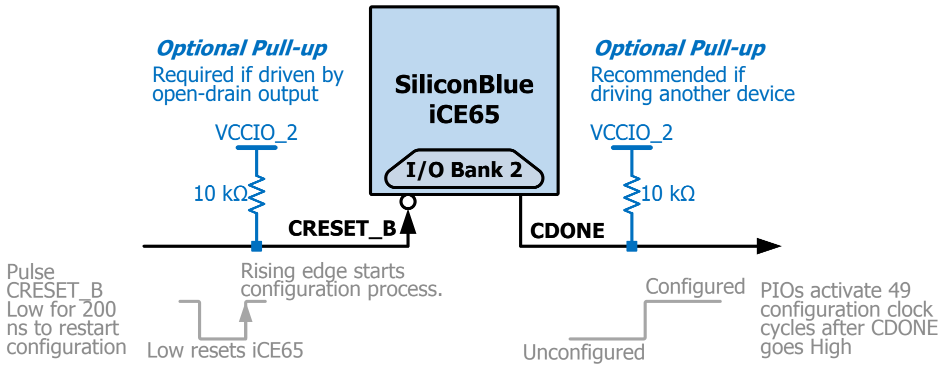


Figure 21 shows the two iCE65 configuration control pins, CRESET_B and CDONE. Table 23 lists the ball/pin numbers for the configuration control pins by package. When driven Low for at least 200 ns, the dedicated Configuration Reset input, CRESET_B, resets the iCE65 device. When CRESET_B returns High, the iCE65 FPGA restarts the configuration process from its power-on conditions (Cold Boot). The CRESET_B pin is a pure input with no internal pull-up resistor. If driven by open-drain driver or un-driven, then connect the CRESET_B pin to a 10 kΩ pull-up resistor connected to the VCCIO_2 supply.

Table 23: **Configuration Control Ball/Pin Numbers by Package**

Configuration Control Pins	CB81	QN84	VQ100	CB132	CB196	CB284
CRESET_B	J6	A21	44	L10	L10	R14
CDONE	H6	B16	43	M10	M10	T14

The iCE65 device signals the end of the configuration process by actively turning off the internal pull-down transistor on the Configuration Done output pin, CDONE. The pin has a permanent, weak internal pull-up resistor to the VCCIO_2 rail. If the iCE65 device drives other devices, then optionally connect the CDONE pin to a 10 kΩ pull-up resistor connected to the VCCIO_2 supply.

The PIO pins activate according to their configured function after 49 configuration clock cycles. The internal oscillator is the configuration clock source for the SPI Master Configuration Interface and when configuring from

* Note: only 14 of the 16 RAM4K Memory Blocks may be pre-initialized in the iCE65L01.

Nonvolatile Configuration Memory (NVCM). When using the SPI Peripheral Configuration Interface, the configuration clock source is the SPI_SCK clock input pin.

Internal Oscillator

During SPI Master or NVCM configuration mode, the controlling clock signal is generated from an internal oscillator. The oscillator starts operating at the Default frequency. During the configuration process, however, bit settings within the configuration bitstream can specify a higher-frequency mode in order to maximize SPI bandwidth and reduce overall configuration time. See Table 57: Internal Oscillator Frequency on page 105 for the specified oscillator frequency range.

Using the SPI Master Configuration Interface, internal oscillator controls all the interface timing and clocks the SPI serial Flash PROM via the SPI_SCK clock output pin.

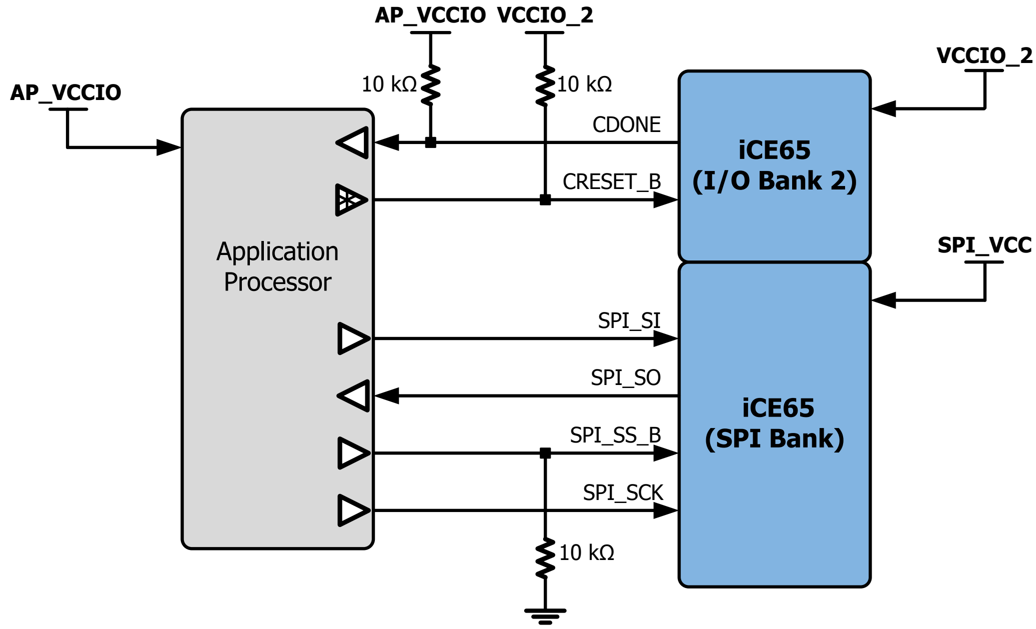
The oscillator output, which also supplies the SPI SCK clock output during the SPI Flash configuration process, has a 50% duty cycle.

Internal Device Reset

Figure 22 presents the various signals that internally reset the iCE65 internal logic.

- Power-On Reset (POR)
- CRESET_B Pin
- JTAG Interface

Figure 28: **iCE65 SPI Peripheral Configuration Interface**



The SPI control signals are defined in Table 25.

Table 29: **SPI Peripheral Configuration Interface Pins (SPI_SS_B Low when CRESET_B Released)**

Signal Name	Direction	iCE65 I/O Supply	Description
CDONE	AP ← iCE65	VCCIO_2	Configuration Done output from iCE65. Connect to a 10kΩ pull-up resistor to the application processor I/O voltage, AP_VCC.
CRESET_B	AP → iCE65		Configuration Reset input on iCE65. Typically driven by AP using an open-drain driver, which also requires a 10kΩ pull-up resistor to VCCIO_2.
SPI_VCC	Supply	SPI_VCC	SPI Flash PROM voltage supply input.
SPI_SI	AP → iCE65		SPI Serial Input to the iCE65 FPGA, driven by the application processor.
SPI_SO	AP ← iCE65		SPI Serial Output from CE65 device to the application processor. Not actually used during SPI peripheral mode configuration but required if the SPI interface is also used to program the NVCM.
SPI_SS_B	AP → iCE65		SPI Slave Select output from the application processor. Active Low. Optionally hold Low prior to configuration using a 10kΩ pull-down resistor to ground.
SPI_SCK	AP → iCE65		SPI Slave Clock output from the application processor.

After configuration, the SPI port pins are available to the user-application as additional PIO pins, supplied by the SPI_VCC input voltage, essentially providing a fifth "mini" I/O bank.

Enabling SPI Configuration Interface

The optional 10 kΩ pull-down resistor on the SPI_SS_B signal ensures that the iCE65 FPGA powers up in the SPI peripheral mode. Optionally, the application processor drives the SPI_SS_B pin Low when CRESET_B is released, forcing the iCE65 FPGA into SPI peripheral mode.

SPI Peripheral Configuration Process

Figure 29 illustrates the interface timing for the SPI peripheral mode and Figure 30 outlines the resulting configuration process. The actual timing specifications appear in Table 60. The application processor (AP) begins by driving the iCE65 CRESET_B pin Low, resetting the iCE65 FPGA. Similarly, the AP holds the iCE65's SPI_SS_B pin Low. The AP must hold the CRESET_B pin Low for at least 200 ns. Ultimately, the AP either releases the CRESET_B pin and allows it to float High via the 10 kΩ pull-up resistor to VCCIO_2 or drives CRESET_B High. The iCE65 FPGA enters SPI peripheral mode when the CRESET_B pin returns High while the SPI_SS_B pin is Low.

Table 31 describes how to maintain voltage compatibility for two interface scenarios. The easiest interface is when the Application Processor's (AP) I/O supply rail and the iCE65's SPI and VCCIO_2 bank supply rails all connect to the same voltage. The second scenario is when the AP's I/O supply voltage is greater than the iCE65's VCCIO_2 supply voltage.

Table 31: CRESET_B and CDONE Voltage Compatibility

Condition	CRESET_B Direct	CRESET_B Open-Drain	CRESET_B Pull-up	CDONE Pull-up	Requirement
VCCIO_AP = VCC_SPI **VCCIO_AP = VCCIO_2**	OK	OK with pull-up	Required if using open-drain output	Recommended	AP can directly drive CRESET_B High and Low although an open-drain output recommended is if multiple devices control CRESET_B. If using an open-drain driver, the CRESET_B input must include a 10 kΩ pull-up resistor to VCCIO_2. The 10 kΩ pull-up resistor to AP_VCCIO is also recommended.
AP_VCCIO > VCCIO_2	N/A	Required, requires pull-up	Required	Required	The AP must control CRESET_B with an open-drain output, which requires a 10 kΩ pull-up resistor to VCCIO_2. The 10 kΩ pull-up resistor to AP_VCCIO is required.

JTAG Boundary Scan Port

Overview

Each iCE65 device includes an IEEE 1149.1-compatible JTAG boundary-scan port. The port supports printed-circuit board (PCB) testing and debugging. It also provides an alternate means to configure the iCE65 device.

Signal Connections

The JTAG port connections are listed in Table 32.

Table 32: iCE65 JTAG Boundary Scan Signals

Signal Name	Direction	Description
TDI	Input	Test Data Input. Must be tied off to GND when unused. (no pull-up resistor)*
TMS	Input	Test Mode Select. Must be tied off to GND when unused. (no pull-up resistor)*
TCK	Input	Test Clock. Must be tied off to GND when unused. (no pull-up resistor)*
TDO	Output	Test Data Output.
TRST_B	Input	Test Reset, active Low. Must be Low during normal device operation. Must be High to enable JTAG operations.*

* Must be tied off to GND or VCCIO_1, else VCCIO_1 draws current.

Table 33 lists the ball/pin numbers for the JTAG interface by package code. The JTAG interface is available in select package types. The JTAG port is located in I/O Bank 1 along the right edge of the iCE65 device and powered by the VCCIO_1 supply inputs. Consequently, the JTAG interface uses the associated I/O standards for I/O Bank 1.

Table 33: JTAG Interface Ball/Pin Numbers by Package

JTAG Interface	VQ100	CB132	CB196	CB284
TDI	N/A	M12	M12	T16
TMS		P14	P14	V18
TCK		L12	L12	R16
TDO		N14	N14	U18
TRST_B		M14	M14	T18

Ball Function	Ball Number	Pin Type	Bank
PIO3	B1	PIO	3
PIO3	B2	PIO	3
PIO3	B3	PIO	3
PIO3	C1	PIO	3
PIO3	C2	PIO	3
PIO3	C3	PIO	3
GBIN7/PIO3	D1	GBIN	3
PIO3	D2	PIO	3
PIO3	D3	PIO	3
GBIN6/PIO3	E1	GBIN	3
PIO3	E2	PIO	3
PIO3	E3	PIO	3
PIO3	F2	PIO	3
PIO3	F3	PIO	3
PIO3	G1	PIO	3
PIO3	G2	PIO	3
PIO3	H1	PIO	3
PIO3	H2	PIO	3
VCCIO_3	F1	VCCIO	3
PIOS/SPI_SO	H7	SPI	SPI
PIOS/SPI_SI	J7	SPI	SPI
PIOS/SPI_SCK	J8	SPI	SPI
PIOS/SPI_SS_B	H8	SPI	SPI
SPI_VCC	H9	SPI	SPI
GND	A1	GND	GND
GND	A9	GND	GND
GND	J9	GND	GND
GND	J1	GND	GND
GND	E4	GND	GND
GND	E5	GND	GND
GND	F4	GND	GND
GND	F5	GND	GND
VCC	A5	VCC	VCC
VCC	J5	VCC	VCC
VPP_2V5	B9	VPP	VPP

Pinout Table

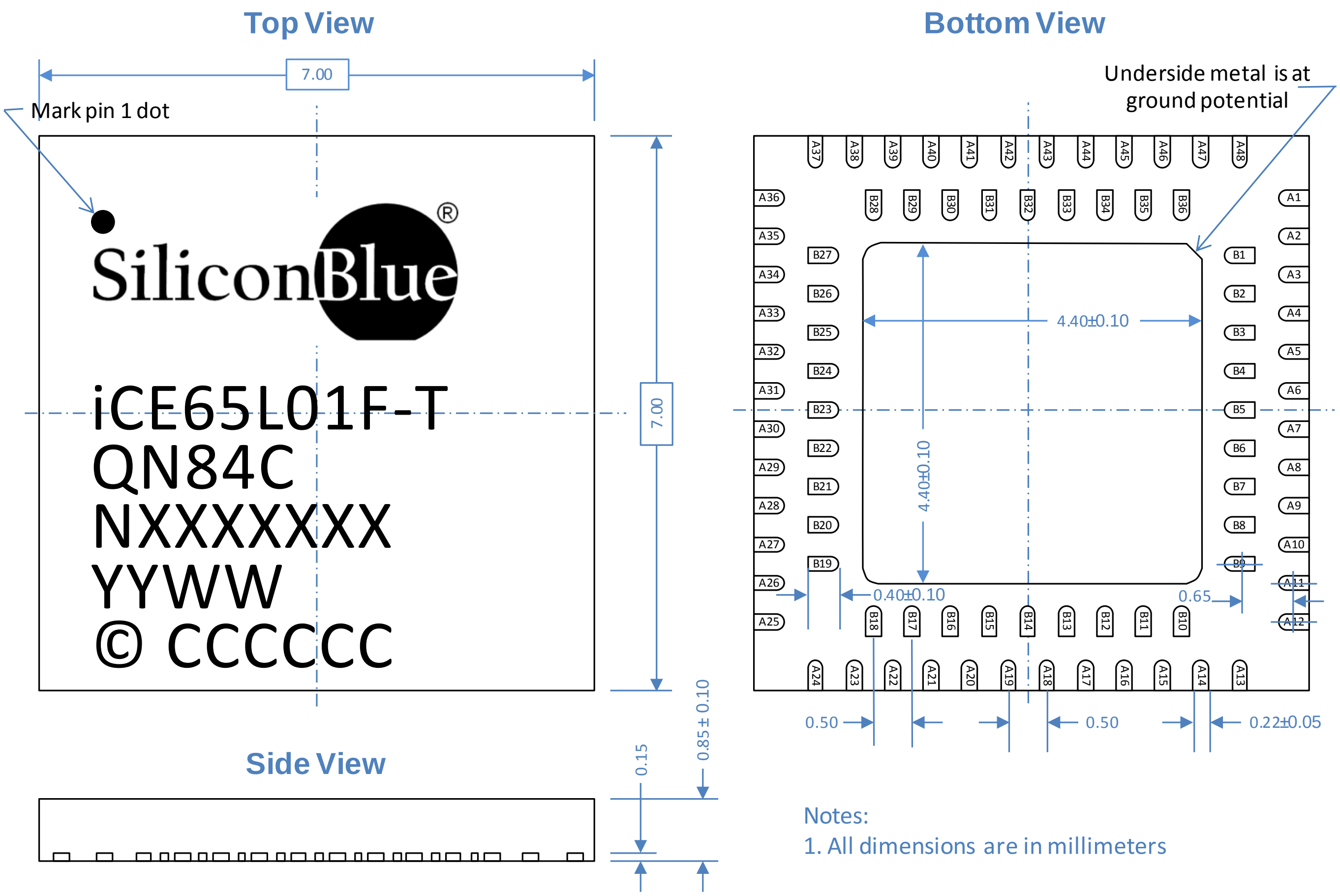
Table 38 provides a detailed pinout table for the QN84 package. Pins are generally arranged by I/O bank, then by ball function. The QN84 package has no JTAG pins.

Table 38: **iCE65 QN84 Chip-scale BGA Pinout Table**

Ball Function	Ball Number	Pin Type	Bank
GBIN0/PIO0	B32	GBIN	0
GBIN1/PIO0	A43	GBIN	0
PIO0	A38	PIO	0
PIO0	A39	PIO	0
PIO0	A40	PIO	0
PIO0	A41	PIO	0
PIO0	A44	PIO	0
PIO0	A45	PIO	0
PIO0	A46	PIO	0
PIO0	A47	PIO	0
PIO0	A48	PIO	0
PIO0	B29	PIO	0
PIO0	B30	PIO	0
PIO0	B31	PIO	0
PIO0	B34	PIO	0
PIO0	B35	PIO	0
PIO0	B36	PIO	0
VCCIO_0	A42	VCCIO	0
GBIN2/PIO1	B22	GBIN	1
GBIN3/PIO1	A29	GBIN	1
PIO1	A25	PIO	1
PIO1	A26	PIO	1
PIO1	A27	PIO	1
PIO1	A31	PIO	1
PIO1	A32	PIO	1
PIO1	A33	PIO	1
PIO1	A34	PIO	1
PIO1	A35	PIO	1
PIO1	B19	PIO	1
PIO1	B20	PIO	1
PIO1	B21	PIO	1
PIO1	B23	PIO	1
PIO1	B24	PIO	1
PIO1	B26	PIO	1
PIO1	B27	PIO	1
VCCIO_1	B25	VCCIO	1
CDONE	B16	CONFIG	2
CRESET_B	A21	CONFIG	2
GBIN4/PIO2	A14	GBIN	2
GBIN5/PIO2	A16	GBIN	2
PIO2	A13	PIO	2
PIO2	B12	PIO	2
PIO2	A19	PIO	2
PIO2	B10	PIO	2
PIO2	B11	PIO	2
PIO2	B13	PIO	2

Package Mechanical Drawing

Figure 35: QN84 Package Mechanical Drawing



Notes:
1. All dimensions are in millimeters

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65L01F	Part number
	-T	Power/Speed
3	QN84C	Package type
	ENG	Engineering
4	NXXXXXXX	Lot Number
5	YYWW	Date Code
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient * θ_{JA} (°C/W)	
0 LFM	200 LFM
45	44

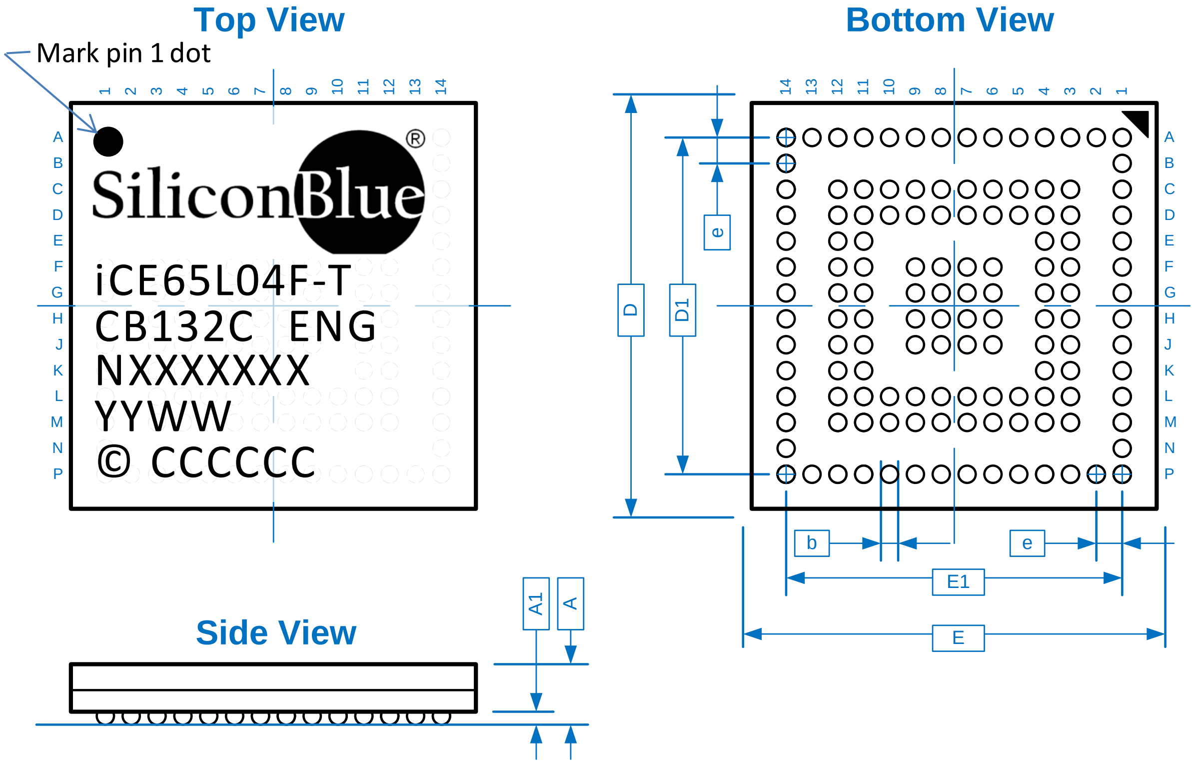
* With PCB thermal vias

Ball Function	Ball Number	Pin Type	Bank
PIO2	J11	PIO	2
PIO2	K3	PIO	2
PIO2	K4	PIO	2
PIO2	K11	PIO	2
PIO2	L2	PIO	2
PIO2	L3	PIO	2
PIO2	L4	PIO	2
PIO2	L5	PIO	2
PIO2	L10	PIO	2
PIO2	L11	PIO	2
PIO2/CBSEL0	H6	PIO	2
PIO2/CBSEL1	J6	PIO	2
VCCIO_2	K5	VCCIO	2
PIO3	C1	PIO	3
PIO3	B1	PIO	3
PIO3	D1	PIO	3
PIO3	E2	PIO	3
PIO3	C2	PIO	3
PIO3	D2	PIO	3
PIO3	C3	PIO	3
PIO3	C4	PIO	3
PIO3	E4	PIO	3
PIO3	D4	PIO	3
PIO3	F3	PIO	3
PIO3	G3	PIO	3
PIO3	G4	PIO	3
GBIN6/PIO3	F4	GBIN	3
GBIN7/PIO3	D3	GBIN	3
PIO3	E3	PIO	3
PIO3	F2	PIO	3
PIO3	G1	PIO	3
PIO3	H1	PIO	3
PIO3	J1	PIO	3
PIO3	H2	PIO	3
PIO3	H3	PIO	3
PIO3	J3	PIO	3
PIO3	J2	PIO	3
VCCIO_3	A1	VCCIO	3
VCCIO_3	G2	VCCIO	3
PIOS/SPI_SO	J8	SPI	SPI
PIOS/SPI_SI	K8	SPI	SPI
PIOS/SPI_SCK	K9	SPI	SPI
PIOS/SPI_SS_B	J9	SPI	SPI
SPI_VCC	J10	SPI	SPI
GND	B2	GND	GND
GND	B10	GND	GND
GND	E1	GND	GND
GND	F5	GND	GND
GND	F6	GND	GND
GND	G5	GND	GND
GND	G6	GND	GND
GND	G11	GND	GND

Package Mechanical Drawing

Figure 44: **CB132 Package Mechanical Drawing**

CB132: 8 x 8 mm, 132-ball, 0.5 mm ball-pitch, chip-scale ball grid array



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			14		Columns
Number of Ball Rows	Y			14		Rows
Number of Signal Balls		n		132		Balls
Body Size	X	E	7.90	8.00	8.10	mm
	Y	D	7.90	8.00	8.10	
Ball Pitch		e	—	0.50	—	
Ball Diameter		b	0.27	—	0.37	
Edge Ball Center to Center	X	E1	—	6.50	—	
	Y	D1	—	6.50	—	
Package Height		A	—	—	1.00	
Stand Off		A1	0.16	—	0.26	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65L04F	Part number
	-T	Power/Speed
3	CB132C	Package type
	ENG	Engineering
4	NXXXXXXX	Lot Number
5	YYWW	Date Code
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
42	34

Ball Function	Ball Number	Pin Type	Bank
PIO3/DP13A	H5	DPIO	3
PIO3/DP13B	G5	DPIO	3
PIO3/DP14A	L1	DPIO	3
PIO3/DP14B	L2	DPIO	3
PIO3/DP15A	M1	DPIO	3
PIO3/DP15B	M2	DPIO	3
PIO3/DP16A (◆)	***iCE65L04:*** K3 ***iCE65L08:*** K4	DPIO	3
PIO3/DP16B (◆)	***iCE65L08:*** K4 ***iCE65L08:*** K3	DPIO	3
PIO3/DP17A	N1	DPIO	3
PIO3/DP17B	N2	DPIO	3
VCCIO_3	E3	VCCIO	3
VCCIO_3	J6	VCCIO	3
VCCIO_3	K1	VCCIO	3
PIOS/SPI_SO	M11	SPI	SPI
PIOS/SPI_SI	P11	SPI	SPI
PIOS/SPI_SCK	P12	SPI	SPI
PIOS/SPI_SS_B	P13	SPI	SPI
SPI_VCC	L11	SPI	SPI
GND	A9	GND	GND
GND	B12	GND	GND
GND	C2	GND	GND
GND	F1	GND	GND
GND	F7	GND	GND
GND	G7	GND	GND
GND	G8	GND	GND
GND	G9	GND	GND
GND	H6	GND	GND
GND	H7	GND	GND
GND	H8	GND	GND
GND	J5	GND	GND
GND	J8	GND	GND
GND	J14	GND	GND
GND	K10	GND	GND
GND	L3	GND	GND
GND	P6	GND	GND
VCC	B7	VCC	VCC
VCC	F2	VCC	VCC
VCC	F8	VCC	VCC
VCC	G6	VCC	VCC
VCC	H9	VCC	VCC
VCC	J4	VCC	VCC
VCC	J7	VCC	VCC
VCC	K13	VCC	VCC
VCC	N7	VCC	VCC
VPP_2V5	A14	VPP	VPP
VPP_FAST	A13	VPP	VPP

iCE65L04 Pad Name	DiePlus VQ100	CB132	CB196	CB284	Pad	X (µm)	Y (µm)
PIO1_24	—	—	G11	F20	167	3,712.80	1,812.00
PIO1_25	—	—	F11	E20	168	3,610.80	1,847.00
PIO1_26	—	—	E10	D20	169	3,712.80	1,882.00
PIO1_27	—	—	E14	C20	170	3,610.80	1,917.00
GND	—	G8	G8	L12	171	3,712.80	1,952.00
GND	—	—	—	—	172	3,610.80	1,987.00
PIO1_28	—	—	F12	G22	173	3,712.80	2,022.00
PIO1_29	—	G12	D14	L16	174	3,610.80	2,057.00
PIO1_30	64	G11	E13	L15	175	3,712.80	2,092.00
PIO1_31	65	F12	C14	K16	176	3,610.80	2,127.00
VCC	—	—	K13	L20	177	3,712.80	2,162.00
VCC	—	—	—	—	178	3,610.80	2,197.00
PIO1_32	66	E14	E11	J18	179	3,712.80	2,232.00
PIO1_33	—	F11	C13	K15	180	3,610.80	2,267.00
VCCIO_1	67	F9	F9	K13	181	3,712.80	2,302.00
VCCIO_1	—	—	—	—	182	3,610.80	2,337.00
PIO1_34	68	E12	E12	J16	183	3,712.80	2,377.00
PIO1_35	69	D14	B14	H18	184	3,610.80	2,427.00
GND	70	G9	G9	L13	185	3,712.80	2,477.00
PIO1_36	71	E11	B13	J15	186	3,610.80	2,527.00
PIO1_37	72	D12	D12	H16	187	3,712.80	2,577.00
PIO1_38	73	C14	C12	G18	188	3,610.80	2,627.00
PIO1_39	74	B14	D11	F18	189	3,712.80	2,677.00
VPP_2V5	75	A14	A14	E18	190	3,610.80	2,739.68
VPP_FAST	76	A13	A13	E17	191	3,097.00	2,962.80
VCC	77	F8	F8	K12	192	2,997.00	2,860.80
VCC	77	F8	F8	K12	193	2,947.00	2,962.80
PIO0_00	78	A12	C11	E16	194	2,897.00	2,860.80
PIO0_01	—	C12	—	G16	195	2,847.00	2,962.80
PIO0_02	79	A11	A12	E15	196	2,797.00	2,860.80
PIO0_03	80	C11	B11	G15	197	2,747.00	2,962.80
PIO0_04	—	D11	—	H15	198	2,697.00	2,860.80
PIO0_05	81	A10	D10	E14	199	2,647.00	2,962.80
PIO0_06	82	C10	A11	G14	200	2,612.00	2,860.80
PIO0_07	83	D10	D9	H14	201	2,577.00	2,962.80
GND	84	A9	H6	E13	202	2,542.00	2,860.80
GND	—	—	—	—	203	2,507.00	2,962.80
PIO0_08	85	C9	C10	G13	204	2,472.00	2,860.80
PIO0_09	86	D9	A10	H13	205	2,437.00	2,962.80
PIO0_10	87	C8	B10	G12	206	2,402.00	2,860.80
PIO0_11	—	D8	E9	H12	207	2,367.00	2,962.80
PIO0_12	—	—	—	A18	208	2,332.00	2,860.80
PIO0_13	—	—	—	A17	209	2,297.00	2,962.80
PIO0_14	—	—	—	A16	210	2,262.00	2,860.80
PIO0_15	—	—	—	A15	211	2,227.00	2,962.80
VCCIO_0	88	A8	A8	E12	212	2,192.00	2,860.80
VCCIO_0	—	—	—	—	213	2,157.00	2,962.80

AC Timing Guidelines

The following examples provide some guidelines of device performance. The actual performance depends on the specific application and how it is physically implemented in the iCE65 FPGA using the Lattice iCEcube software. The following guidelines assume typical conditions (VCC = 1.0 V or 1.2 V as specified, temperature = 25 °C). Apply derating factors using the iCEcube timing analyzer to adjust to other operating regimes.

Programmable Logic Block (PLB) Timing

Table 54 provides timing information for the logic in a Programmable Logic Block (PLB), which includes the paths shown in Figure 55 and Figure 56.

Figure 55 PLB Sequential Timing Circuit

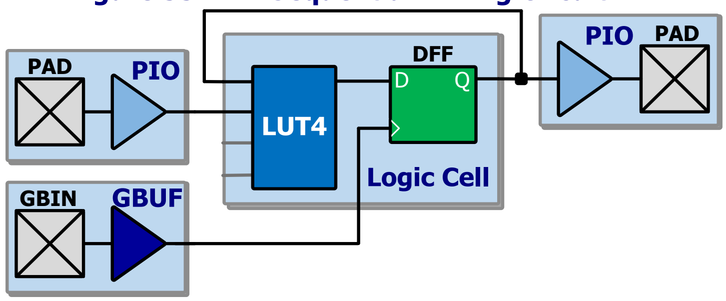


Figure 56 **PLB Combinational Timing Circuit**

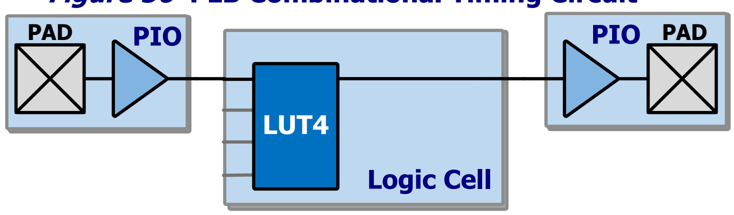


Table 54: **Typical Programmable Logic Block (PLB) Timing**

			Device: iCE65	L01	L04, L08			
			Power/Speed Grade	–T	–L		–T	
			Nominal VCC	1.2 V	1.0 V	1.2 V	1.2 V	
Symbol	**From**	**To**	**Description**	**Typ.**	**Typ.**	**Typ.**	**Typ.**	**Units**
		Sequential Logic Paths						
F_{TOGGLE}	GBIN input	GBIN input	Flip-flop toggle frequency. DFF flip-flop output fed back to LUT4 input with 4-input XOR, clocked on same clock edge.	256	224	256	256	MHz
t_{CKO}	DFF clock input	PIO output	Logic cell flip-flop (DFF) clock-to-output time, measured from the DFF CLK input to PIO output, including interconnect delay.	5.4	16.5	8.7	7.1	ns
t_{GBCKLC}	GBIN input	DFF clock input	Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to clock input on the logic cell DFF flip-flop.	2.2	7.3	3.8	2.7	ns
t_{SULI}	PIO input	GBIN input	Minimum setup time on PIO input, through LUT4, to DFF flip-flop D-input before active clock edge on the GBIN input, including interconnect delay.	1.0	4.0	2.1	1.2	ns
t_{HDLI}	GBIN input	PIO input	Minimum hold time on PIO input, through LUT4, to DFF flip-flop D-input after active clock edge on the GBIN input, including interconnect delay.	0	0	0	0	ns
		Combinational Logic Paths						
t_{LUT4IN}	PIO input	LUT4 input	Asynchronous delay from PIO input pad to adjacent PLB interconnect.	2.6	9.8	5.2	3.3	ns
t_{ILO}	LUT4 input	LUT4 output	Logic cell LUT4 combinational logic propagation delay, regardless of logic complexity from input to output.	0.6	1.9	1.0	0.6	ns
t_{LUT4IN}	LUT4 output	PIO output	Asynchronous delay from adjacent PLB interconnect to PIO output pad.	4.9	16.0	8.4	6.6	ns

Programmable Input/Output (PIO) Block

Table 55 provides timing information for the logic in a Programmable Logic Block (PLB), which includes the paths shown in Figure 57 and Figure 58. The timing shown is for the LVCMOS25 I/O standard in all I/O banks. The iCEcube development software reports timing adjustments for other I/O standards.

Figure 57: Programmable I/O (PIO) Pad-to-Pad Timing Circuit

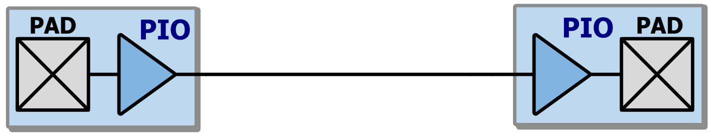


Figure 58: Programmable I/O (PIO) Sequential Timing Circuit

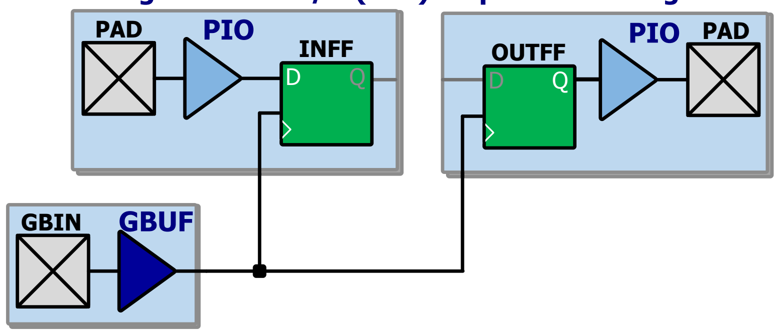


Table 55: Typical Programmable Input/Output (PIO) Timing (LVCMOS25)

Symbol	From	To	Description	L01	L04, L08			Units
			Device: iCE65	L01	L04, L08			
			Power/Speed Grad	–T	–L		–T	
			Nominal VCC	1.2 V	1.0 V	1.2 V	1.2 V	
				Typ.	Typ.	Typ.	Typ.	
		Synchronous Output Paths						
t_{OCKO}	OUTFF clock input	PIO output	Delay from clock input on OUTFF output flip-flop to PIO output pad.	4.7	13.8	7.3	5.6	ns
t_{GBCKIO}	GBIN input	OUTFF clock input	Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to clock input on the PIO OUTFF output flip-flop.	2.1	7.3	3.8	2.6	ns
		Synchronous Input Paths						
t_{SUPDIN}	PIO input	GBIN input	Setup time on PIO input pin to INFF input flip-flop before active clock edge on GBIN input, including interconnect delay.	0	0	0	0	ns
t_{HDPDIN}	GBIN input	PIO input	Hold time on PIO input to INFF input flip-flop after active clock edge on the GBIN input, including interconnect delay.	2.7	7.1	3.6	2.8	ns
		Pad to Pad						
t_{PADIN}	PIO input	Inter-connect	Asynchronous delay from PIO input pad to adjacent interconnect.	2.5	9.5	5.0	3.2	ns
t_{PADO}	Inter-connect	PIO output	Asynchronous delay from adjacent interconnect to PIO output pad including interconnect delay.	4.5	14.6	7.7	6.2	ns