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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	440
Number of Logic Elements/Cells	3520
Total RAM Bits	81920
Number of I/O	48
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	-
Supplier Device Package	63-WLCSP
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice65l04f-tcs63i

For best possible performance, the global buffer inputs (GBIN[7:-0]) connect directly to the their associated global buffers (GBUF[7:0]), bypassing the PIO logic and iCEgate circuitry as shown in Figure 7. Consequently, the direct GBIN-to-GBUF connection cannot be blocked by the iCEgate circuitry. However, it is possible to use iCEgate to block PIO-to-GBUF clock connections.

For additional information on using the iCEgate feature, please refer to the following application note.

AN002: Using iCEgate Blocking for Ultra-Low Power

Input Pull-Up Resistors on I/O Banks 0, 1, and 2

The PIO pins in I/O Banks 0, 1, and 2 have an optional input pull-up resistor. Pull-up resistors are not provided in iCE65L04 and iCE65L08 I/O Bank 3. During the iCE65 configuration process, the input pull-up resistor is unconditionally enabled and pulls the input to within a diode drop of the associated I/O bank supply voltage (VCCIO_#). This prevents any signals from floating on the circuit board during configuration.

After iCE65 configuration is complete, the input pull-up resistor is optional, defined by a configuration bit. The pull-up resistor is also useful to tie off unused PIO pins. The Lattice iCEcube development software defines all unused PIO pins in I/O Banks 0, 1 and 2 as inputs with the pull-up resistor turned on. The pull-up resistor value depends on the VCCIO voltage applied to the bank, as shown in Table 49.

Note: JTAG inputs TCK, TDI and TMS do not have the input pull-up resistor and must be tied off to GND when unused, else VCCIO_1 draws current.

No Input Pull-up Resistors on I/O Bank 3 of iCE65L04 and iCE65L08

The PIO pins in I/O Bank 3 do not have an internal pull-up resistor. To minimize power consumption, tie unused PIO pins in Bank 3 to a known logic level or drive them as a disabled high-impedance output.

Input Hysteresis

Inputs typically have about 50 mV of hysteresis, as indicated in Table 49.

Output and Output Enable Signal Path

As shown in Figure 7, a signal from programmable interconnect feeds the OUT signal on a Programmable I/O pad. This output connects either directly to the associated package pin or is held in an optional output flip-flop. Because all flip-flops are automatically reset after configuration, the output from the output flip-flop can be optionally inverted so that an active-Low output signal is held in the disabled (High) state immediately after configuration.

Similarly, each Programmable I/O pin has an output enable or three-state control called OE. When OE = High, the OUT output signal drives the associated pad, as described in Table 10. When OE = Low, the output driver is in the high-impedance (Hi-Z) state. The OE output enable control signal itself connects either directly to the output buffer or is held in an optional register. The output buffer is optionally permanently enabled or permanently disabled, either to unconditionally drive output signals, or to allow input-only signals.

Table 10: **PIO Output Operations (non-registered operation, no inversions)**

Operation	OUT Data Output	OE Enable	PAD
Three-State	X	0	Hi-Z
Drive Output Data	OUT	1*	OUT

X = don't care, 1* = High or unused, Hi-Z = high-impedance, three-stated, floating.

See Input and Output Register Control per PIO Pair for information about the registered input path.

Input and Output Register Control per PIO Pair

PIO pins are grouped into pairs for synchronous control. Registers within pairs of PIO pins share common input clock, output clock, and I/O clock enable control signals, as illustrated in Figure 11. The combinational logic paths are removed from the drawing for clarity.

The INCLK clock signal only controls the input flip-flops within the PIO pair.

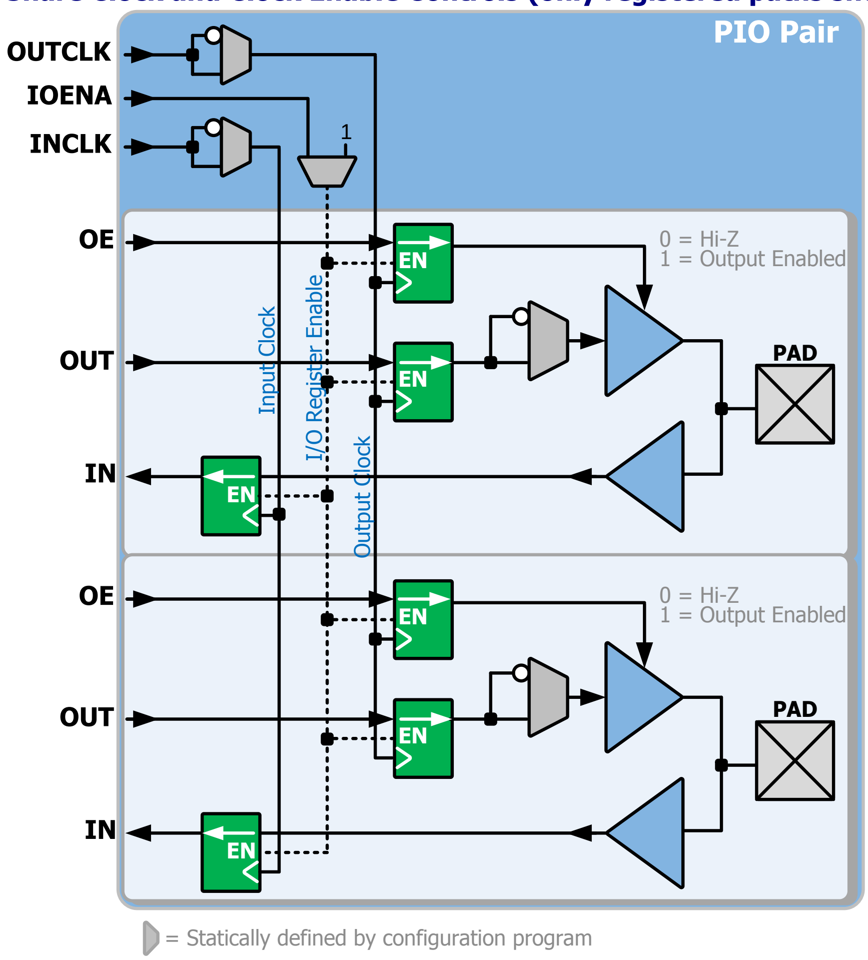
The OUTCLK clock signal controls the output flip-flops and the output-enable flip-flops within the PIO pair.

If desired in the iCE65 application, the INCLK and OUTCLK signals can be connected together.

The IOENA clock-enable input, if used, enables all registers in the PIO pair, as shown in Figure 11. By default, the registers are always enabled.

> ⚠ Before laying out your printed-circuit board, run the design through the iCEcube development software to verify that your selected pinout complies with these I/O register pairing requirements. See tables in "Die Cross Reference" starting on page 84.

***Figure 11:* PIO Pairs Share Clock and Clock Enable Controls (only registered paths shown for clarity)**



The pairing of PIO pairs is most evident in the tables in "Die Cross Reference" starting on page 84.

Table 12 and Table 13 list the connections between a specific global buffer and the inputs on a Programmable I/O (PIO) pair. Although there is no direct connection between a global buffer and a PIO output, such a connection is possible by first connecting through a PLB LUT4 function. Again, all global buffers optionally drive all clock inputs. However, even-numbered global buffers optionally drive the clock-enable input on a PIO pair.

The PIO clock enable connect is different between the iCE65L01/iCE65L04 and iCE65L08.

***Table 12:* iCE65L01 & iCE65L04: Global Buffer (GBUF) Connections to Programmable I/O (PIO) Pair**

Global Buffer	Output Connections	Input Clock	Output Clock	Clock Enable
GBUF0	No (connect through PLB LUT)	Yes	Yes	No
GBUF1		Yes	Yes	Yes
GBUF2		Yes	Yes	No
GBUF3		Yes	Yes	Yes
GBUF4		Yes	Yes	No
GBUF5		Yes	Yes	Yes
GBUF6		Yes	Yes	No
GBUF7		Yes	Yes	Yes

***Table 13:* iCE64L08: Global Buffer (GBUF) Connections to Programmable I/O (PIO) Pair**

Global Buffer	Output Connections	Input Clock	Output Clock	Clock Enable
GBUF0	No (connect through PLB LUT)	Yes	Yes	Yes
GBUF1		Yes	Yes	No
GBUF2		Yes	Yes	Yes
GBUF3		Yes	Yes	No
GBUF4		Yes	Yes	Yes
GBUF5		Yes	Yes	No
GBUF6		Yes	Yes	Yes
GBUF7		Yes	Yes	No

Global Buffer Inputs

The iCE65 component has eight specialized GBIN/PIO pins that are optionally direct inputs to the global buffers, offering the best overall clock characteristics. As shown in Figure 15, each GBIN/PIO pin is a full-featured I/O pin but also provides a direct connection to its associated global buffer. The direct connection to the global buffer bypasses the iCEgate input-blocking latch and other PIO input logic. These special PIO pins are allocated two to an I/O Bank, a total of eight. These pins are labeled GBIN0 through GBIN7, as shown in Figure 14 and the pin locations for each GBIN input appear in Table 14.

***Table 14:* Global Buffer Input Ball/Pin Number by Package**

Global Buffer Input (GBIN)	I/O Bank	VQ100	CB132	'L04 CB196	'L08 CB196	CB284
GBIN0	0	90	A6	A7	A7	E10
GBIN1		89	A7	E7	E7	E11
GBIN2	1	63	G14	F10	F10	L18
GBIN3		62	F14	G12	G12	K18
GBIN4	2	34	P8	L7	N8	V12
GBIN5		33	P7	P5	M7	V11
GBIN6	3	15	H1	H1	H1	M5
GBIN7		13	G1	G1	H3	L5

Automatic Global Buffer Insertion, Manual Insertion

The iCEcube development software automatically assigns high-fanout signals to a global buffer. However, to manual insert a global buffer input/global buffer (GBIN/GBUF) combination, use the `SB_IO_GB` primitive. To insert just a global buffer (GBUF), use the `SB_GB` primitive.

Global Hi-Z Control

The global high-impedance control signal, GHIZ, connects to all I/O pins on the iCE65 device. This GHIZ signal is automatically asserted throughout the configuration process, forcing all user-I/O pins into their high-impedance state. Similarly, the PIO pins can be forced into their high-impedance state via the JTAG controller.

Global Reset Control

The global reset control signal connects to all PLB and PIO flip-flops on the iCE65 device. The global reset signal is automatically asserted throughout the configuration process, forcing all flip-flops to their defined wake-up state. For PLB flip-flops, the wake-up state is always reset, regardless of the PLB flip-flop primitive used in the application. See Table 3 for more information.

The PIO flip-flops are always reset during configuration, although the output flip-flop can be inverted before leaving the iCE65 device, as shown in Figure 11.

RAM

Each iCE65 device includes multiple high-speed synchronous RAM blocks (RAM4K), each 4Kbit in size. As shown in Table 16 a single iCE65 integrates between 16 to 96 such blocks. Each RAM4K block is generically a 256-word deep by 16-bit wide, two-port register file, as illustrated in Figure 17. The input and output connections, to and from a RAM4K block, feed into the programmable interconnect resources.

Figure 17: RAM4K Memory Block

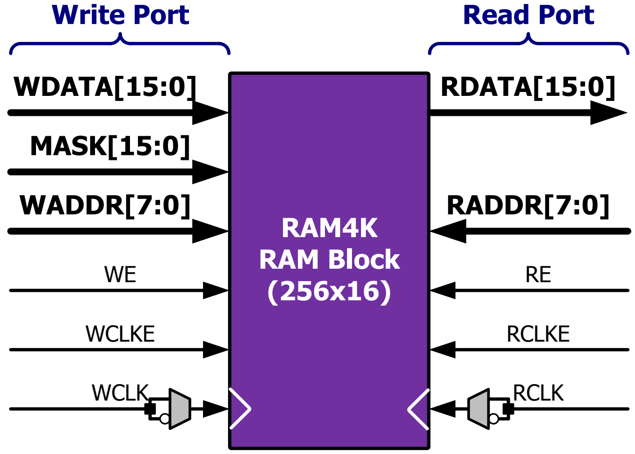


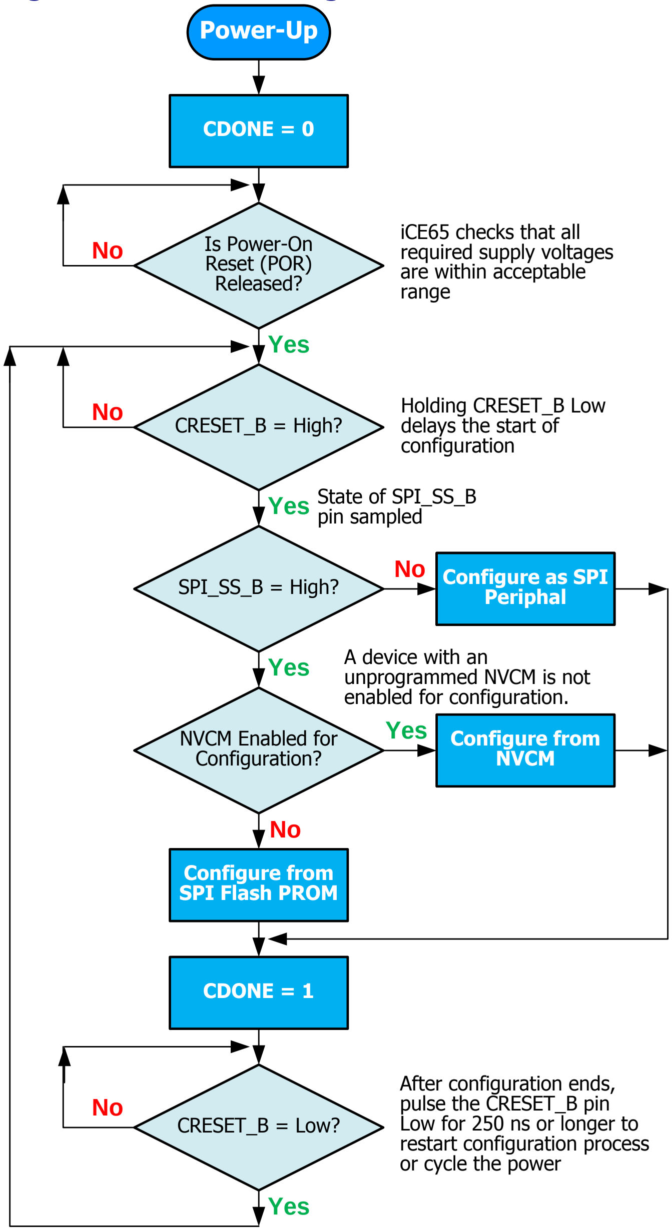
Table 16: RAM4K Blocks per Device

Device	RAM4K Blocks	Default Configuration	RAM Bits per Block	Block RAM Bits
iCE65L01	16	256 x 16	4K (4,096)	64K
iCE65L04	20			80K
iCE65L08	32			128K

Using programmable logic resources, a RAM4K block implements a variety of logic functions, each with configurable input and output data width.

- Random-access memory (RAM)
  - Single-port RAM with a common address, enable, and clock control lines
  - Two-port RAM with separate read and write control lines, address inputs, and enable

Figure 20: **Device Configuration Control Flow**



Configuration Image Size

Table 23 shows the number of memory bits required to configure an iCE65 device. Two values are provided for each device. The "Logic Only" value indicates the minimum configuration size, the number of bits required to configure only the logic fabric, leaving the RAM4K blocks uninitialized. The "Logic + RAM4K" column indicates the maximum configuration size, the number of bits to configure the logic fabric and to pre-initialize all the RAM4K blocks.

Figure 21: iCE65 Configuration Control Pins

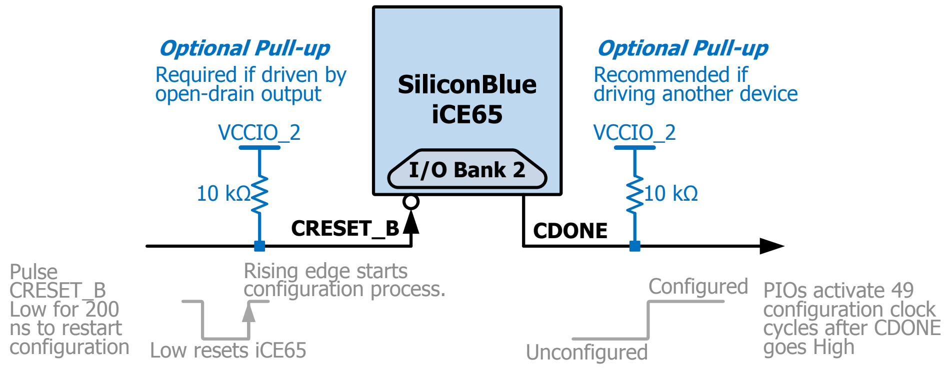


Figure 21 shows the two iCE65 configuration control pins, CRESET_B and CDONE. Table 23 lists the ball/pin numbers for the configuration control pins by package. When driven Low for at least 200 ns, the dedicated Configuration Reset input, CRESET_B, resets the iCE65 device. When CRESET_B returns High, the iCE65 FPGA restarts the configuration process from its power-on conditions (Cold Boot). The CRESET_B pin is a pure input with no internal pull-up resistor. If driven by open-drain driver or un-driven, then connect the CRESET_B pin to a 10 kΩ pull-up resistor connected to the VCCIO_2 supply.

***Table 23:* Configuration Control Ball/Pin Numbers by Package**

Configuration Control Pins	CB81	QN84	VQ100	CB132	CB196	CB284
CRESET_B	J6	A21	44	L10	L10	R14
CDONE	H6	B16	43	M10	M10	T14

The iCE65 device signals the end of the configuration process by actively turning off the internal pull-down transistor on the Configuration Done output pin, CDONE. The pin has a permanent, weak internal pull-up resistor to the VCCIO_2 rail. If the iCE65 device drives other devices, then optionally connect the CDONE pin to a 10 kΩ pull-up resistor connected to the VCCIO_2 supply.

The PIO pins activate according to their configured function after 49 configuration clock cycles. The internal oscillator is the configuration clock source for the SPI Master Configuration Interface and when configuring from

* Note: only 14 of the 16 RAM4K Memory Blocks may be pre-initialized in the iCE65L01.

Nonvolatile Configuration Memory (NVCM). When using the SPI Peripheral Configuration Interface, the configuration clock source is the SPI_SCK clock input pin.

Internal Oscillator

During SPI Master or NVCM configuration mode, the controlling clock signal is generated from an internal oscillator. The oscillator starts operating at the Default frequency. During the configuration process, however, bit settings within the configuration bitstream can specify a higher-frequency mode in order to maximize SPI bandwidth and reduce overall configuration time. See Table 57: Internal Oscillator Frequency on page 105 for the specified oscillator frequency range.

Using the SPI Master Configuration Interface, internal oscillator controls all the interface timing and clocks the SPI serial Flash PROM via the SPI_SCK clock output pin.

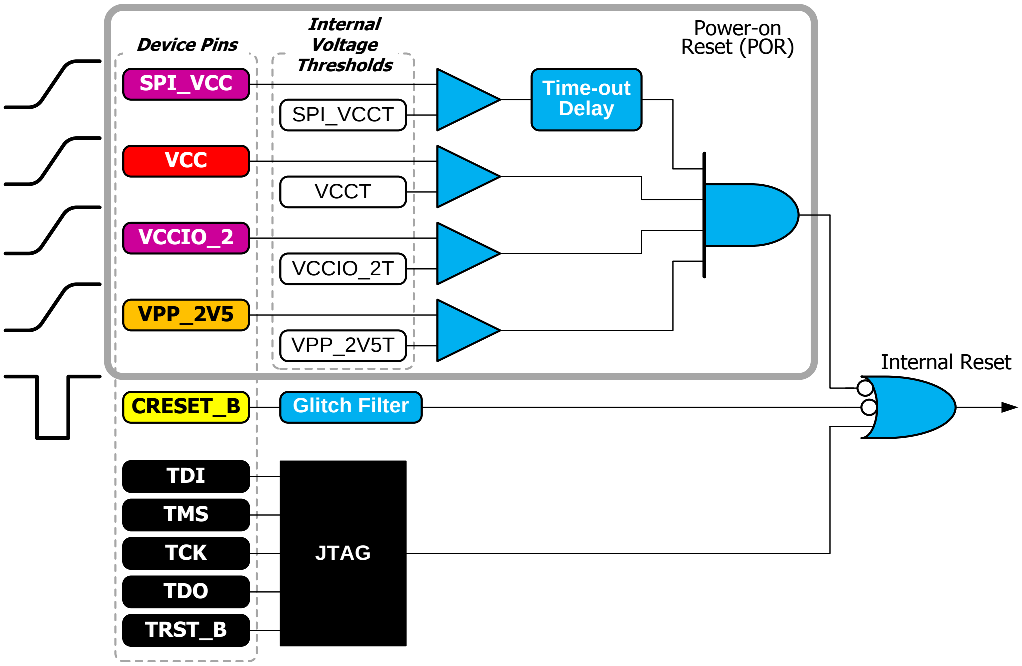
The oscillator output, which also supplies the SPI SCK clock output during the SPI Flash configuration process, has a 50% duty cycle.

Internal Device Reset

Figure 22 presents the various signals that internally reset the iCE65 internal logic.

- Power-On Reset (POR)
- CRESET_B Pin
- JTAG Interface

Figure 22: iCE65 Internal Reset Circuitry



Power-On Reset (POR)

The Power-on Reset (POR) circuit monitors specific voltage supply inputs and holds the device in reset until all the relevant supplies exceed the internal voltage thresholds. The SPI_VCC supply also has an additional time-out delay to allow an attached SPI serial PROM to power up properly. Table 24 shows the POR supply inputs. The Nonvolatile Configuration Memory (NVCM) requires that the VPP_2V5 supply be connected, even if the application does not use the NVCM.

***Table 24:* Power-on Reset (POR) Voltage Resources**

Supply Rail	iCE65 Production Devices
VCC	Yes
SPI_VCC	Yes
VCCIO_1	No
VCCIO_2	Yes
VPP_2V5	Yes

CRESET_B Pin

The CRESET_B pin resets the iCE65 internal logic when Low.

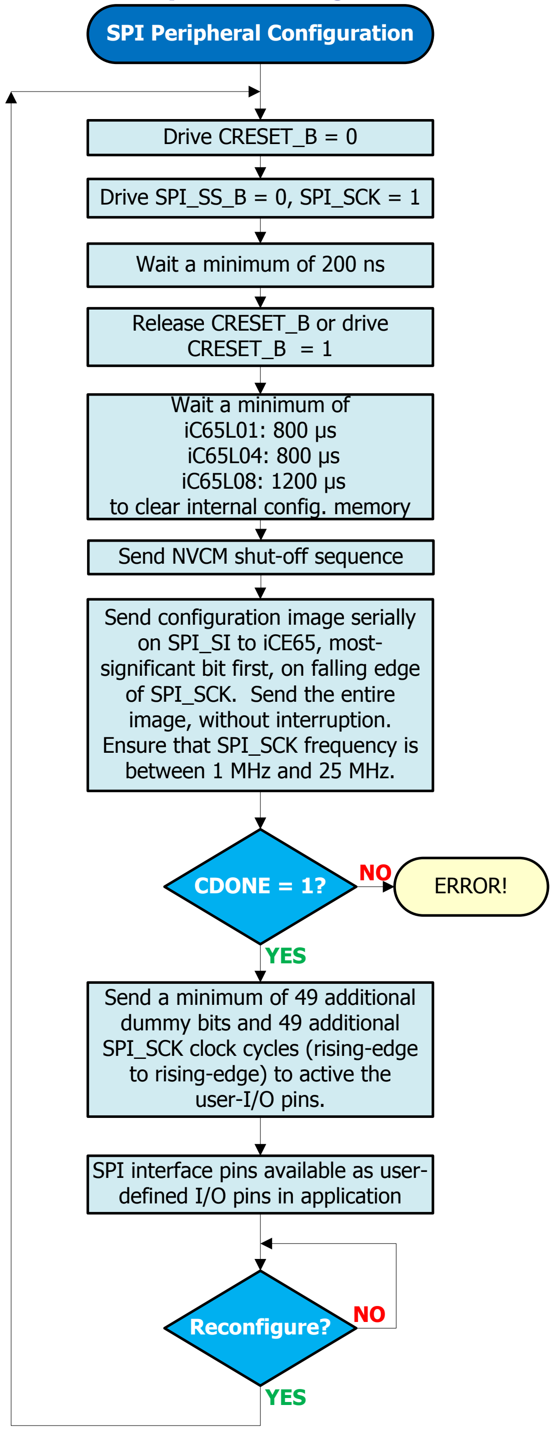
JTAG Interface

Specific command sequences also reset the iCE65 internal logic.

SPI Master Configuration Interface

All iCE65 devices, including those with NVCM, can be configured from an external, commodity SPI serial Flash PROM, as shown in Figure 23. The SPI configuration interface is essentially its own independent I/O bank, powered by the VCC_SPI supply input. Presently, most commercially-available SPI serial Flash PROMs require a 3.3V supply.

***Figure 30:* SPI Peripheral Configuration Process**



Voltage Compatibility

As shown in Figure 23, there are potentially three different supply voltages involved in the SPI Peripheral interface, described in Table 30.

***Table 30:* SPI Peripheral Mode Supply Voltages**

Supply Voltage	Description
AP_VCCIO	I/O supply to the Application Processor (AP)
VCC_SPI	Voltage supply for the iCE65 SPI interface.
VCCIO_2	Supply voltage for the iCE65 I/O Bank 2.

QN84 Quad Flat Pack No-Lead

The QN84 is a Quad Flat Pack No-Lead package with a 0.5 mm pad pitch.

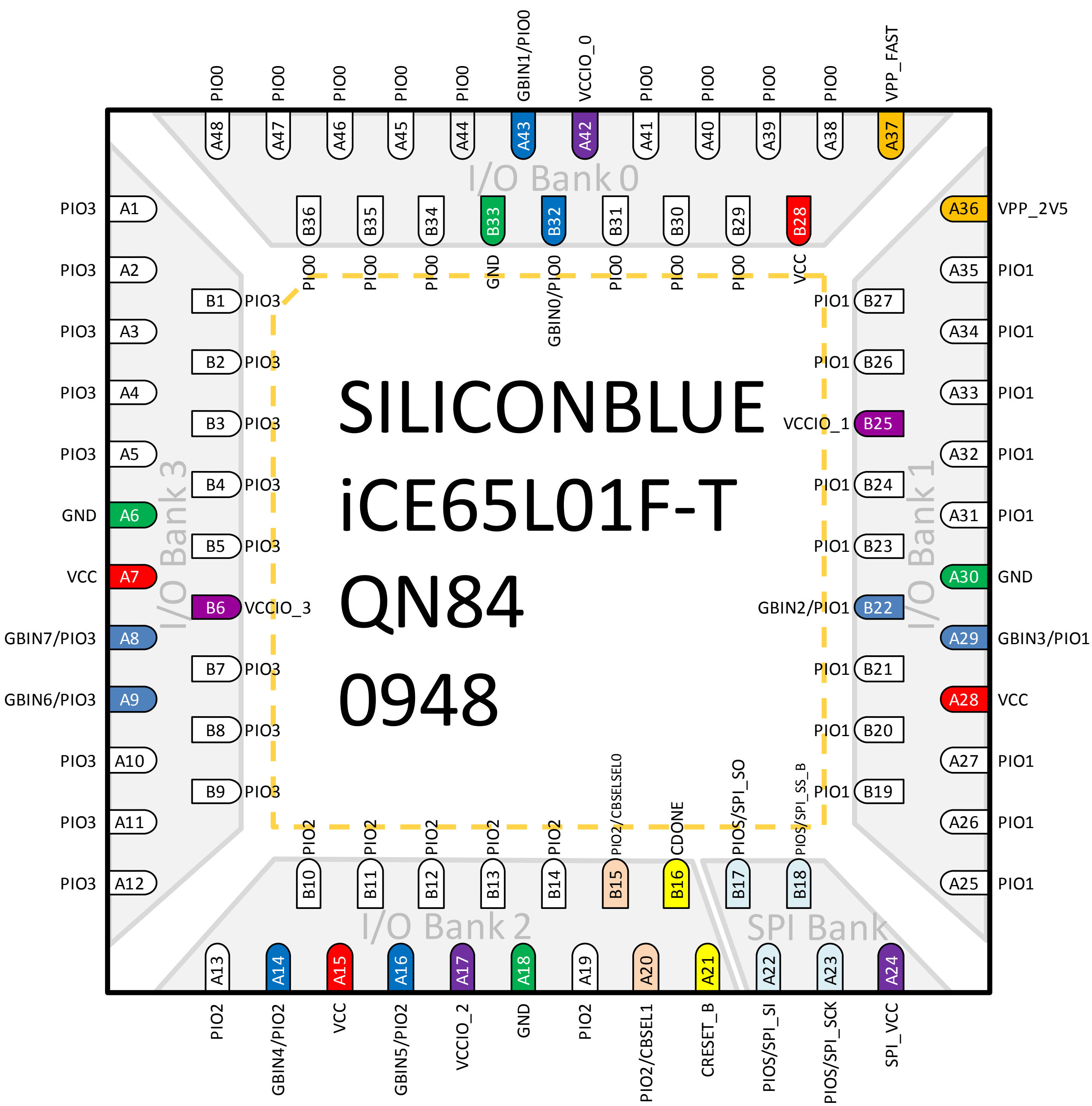
Footprint Diagram

Figure 34 shows the iCE65 footprint diagram for the QN84 package.

Also see Table 38 for a complete, detailed pinout for the QN84 package.

The signal pins are also grouped into the four I/O Banks and the SPI interface.

Figure 34: **iCE65 QN84 Quad Flat Pack No-Lead Footprint (Top View)**



Ball Function	Ball Number	Pin Type	Bank
PIO2	B14	PIO	2
PIO2/CBSEL0	B15	PIO	2
PIO2/CBSEL1	A20	PIO	2
VCCIO_2	A17	PIO	2
GBIN6/PIO3	A9	GBIN	3
GBIN7/PIO3	A8	GBIN	3
PIO3	A1	PIO	3
PIO3	A2	PIO	3
PIO3	A3	PIO	3
PIO3	A4	PIO	3
PIO3	A5	PIO	3
PIO3	A10	PIO	3
PIO3	A11	PIO	3
PIO3	A12	PIO	3
PIO3	B1	PIO	3
PIO3	B2	PIO	3
PIO3	B3	PIO	3
PIO3	B4	PIO	3
PIO3	B5	PIO	3
PIO3	B7	PIO	3
PIO3	B8	PIO	3
PIO3	B9	PIO	3
VCCIO_3	B6	VCCIO	3
PIOS/SPI_SO	B17	SPI	SPI
PIOS/SPI_SI	A22	SPI	SPI
PIOS/SPI_SCK	A23	SPI	SPI
PIOS/SPI_SS_B	B18	SPI	SPI
SPI_VCC	A24	SPI	SPI
GND	A6	GND	GND
GND	A18	GND	GND
GND	A30	GND	GND
GND	B33	GND	GND
VCC	A7	VCC	VCC
VCC	A15	VCC	VCC
VCC	A28	VCC	VCC
VCC	B28	VCC	VCC
VPP_2V5	A36	VPP	VPP
VPP_FAST	A37	VPP	VPP

Pin Function	Pin Number	Type	Bank
PIO2	28	PIO	2
PIO2	29	PIO	2
PIO2	30	PIO	2
PIO2	iCE65L01: 34 iCE65L04: 36	PIO	2
PIO2	37	PIO	2
PIO2	40	PIO	2
PIO2/CBSEL0	41	PIO	2
PIO2/CBSEL1	42	PIO	2
VCCIO_2	31	VCCIO	2
VCCIO_2	38	VCCIO	2
PIO3/DP00A	1	PIO/DPIO	3
PIO3/DP00B	2	PIO/DPIO	3
PIO3/DP01A	3	PIO/DPIO	3
PIO3/DP01B	4	PIO/DPIO	3
PIO3/DP02A	7	PIO/DPIO	3
PIO3/DP02B	8	PIO/DPIO	3
PIO3/DP03A	9	PIO/DPIO	3
PIO3/DP03B	10	PIO/DPIO	3
PIO3/DP04A	12	PIO/DPIO	3
GBIN7/PIO3/DP04B	13	GBIN/DPIO	3
GBIN6/PIO3/DP05A	15	GBIN/DPIO	3
PIO3/DP05B	16	PIO/DPIO	3
PIO3/DP06A	18	PIO/DPIO	3
PIO3/DP06B	19	PIO/DPIO	3
PIO3/DP07A	20	PIO/DPIO	3
PIO3/DP07B	21	PIO/DPIO	3
PIO3/DP08A	24	PIO/DPIO	3
PIO3/DP08B	25	PIO/DPIO	3
VCCIO_3	6	VCCIO	3
VCCIO_3	14	VCCIO	3
VCCIO_3	22	VCCIO	3
PIOS/SPI_SO	45	SPI	SPI
PIOS/SPI_SI	46	SPI	SPI
PIOS/SPI_SCK	48	SPI	SPI
PIOS/SPI_SS_B	49	SPI	SPI
SPI_VCC	50	SPI	SPI
GND	5	GND	GND
GND	17	GND	GND
GND	23	GND	GND
GND	32	GND	GND
GND	39	GND	GND
GND	47	GND	GND
GND	55	GND	GND
GND	70	GND	GND
GND	84	GND	GND
GND	98	GND	GND
VCC	11	VCC	VCC
VCC	35	VCC	VCC

Ball Function	Ball Number	Pin Type	Bank
GND	K2	GND	GND
GND	K10	GND	GND
VCC	B6	VCC	VCC
VCC	F1	VCC	VCC
VCC	F11	VCC	VCC
VCC	K6	VCC	VCC
VPP_2V5	C10	VPP	VPP
VPP_FAST	A9	VPP	VPP

Pinout Table

Table 41 provides a detailed pinout table for the CB132 package. Pins are generally arranged by I/O bank, then by ball function. The table also highlights the differential I/O pairs in I/O Bank 3.

***Table 41:* iCE65 CB132 Chip-scale BGA Pinout Table**

Ball Function	Ball Number	Pin Type	Bank
GBIN0/PIO0	iCE65L01: A7 iCE65L04/L08: A6	GBIN	0
GBIN1/PIO0	iCE65L01: A6 iCE65L04/08: A7	GBIN	0
PIO0	A1	PIO	0
PIO0	A2	PIO	0
iCE65L01: (NC) iCE65L04/L08: PIO0	A3	iCE65L01: (NC) iCE65L04: PIO0	0
PIO0	A4	PIO	0
PIO0	A5	PIO	0
PIO0	A10	PIO	0
iCE65L01: (NC) iCE65L04/L08: PIO0	A11	iCE65L01: (NC) iCE65L04: PIO0	0
PIO0	A12	PIO	0
PIO0	C10	PIO	0
PIO0	C11	PIO	0
PIO0	C12	PIO	0
PIO0	C4	PIO	0
PIO0	C5	PIO	0
PIO0	C6	PIO	0
PIO0	C7	PIO	0
PIO0	C8	PIO	0
PIO0	C9	PIO	0
PIO0	D5	PIO	0
PIO0	D6	PIO	0
PIO0	D7	PIO	0
PIO0	D8	PIO	0
PIO0	D9	PIO	0
PIO0	D10	PIO	0
PIO0	D11	PIO	0
VCCIO_0	A8	VCCIO	0
VCCIO_0	F6	VCCIO	0
GBIN2/PIO1	G14	GBIN	1
GBIN3/PIO1	F14	GBIN	1
PIO1	B14	PIO	1
PIO1	C14	PIO	1
PIO1	D12	PIO	1
PIO1	D14	PIO	1
PIO1	E11	PIO	1
PIO1	E12	PIO	1
PIO1	E14	PIO	1
PIO1	F11	PIO	1
PIO1	F12	PIO	1
PIO1	G11	PIO	1
PIO1	G12	PIO	1
PIO1	H11	PIO	1

Ball Function	Ball Number	Pin Type	Bank
PIO1	F14	PIO	1
PIO1	G10	PIO	1
PIO1	G11	PIO	1
PIO1	G13	PIO	1
PIO1	G14	PIO	1
PIO1	H10	PIO	1
PIO1	H11	PIO	1
PIO1	H12	PIO	1
PIO1	H13	PIO	1
PIO1	J10	PIO	1
PIO1	J11	PIO	1
PIO1	J12	PIO	1
PIO1	J13	PIO	1
PIO1	K11	PIO	1
PIO1	K12	PIO	1
PIO1	K14	PIO	1
PIO1	L13	PIO	1
PIO1	L14	PIO	1
PIO1	M13	PIO	1
TCK	L12	JTAG	1
TDI	M12	JTAG	1
TDO	N14	JTAG	1
TMS	P14	JTAG	1
TRST_B	M14	JTAG	1
VCCIO_1	F9	VCCIO	1
VCCIO_1	H14	VCCIO	1
CDONE	M10	CONFIG	2
CRESET_B	L10	CONFIG	2
GBIN4/PIO2 (◆)	***iCE65L04:*** L7 ***iCE65L08:*** N8	GBIN	2
GBIN5/PIO2 (◆)	***iCE65L04:*** P5 ***iCE65L08:*** M7	GBIN	2
PIO2	K5	PIO	2
PIO2	K6	PIO	2
PIO2	K7	PIO	2
PIO2	K8	PIO	2
PIO2	K9	PIO	2
PIO2	L4	PIO	2
PIO2	L5	PIO	2
PIO2	L6	PIO	2
PIO2	L8	PIO	2
PIO2	M3	PIO	2
PIO2	M4	PIO	2
PIO2	M6	PIO	2
PIO2 (◆)	***iCE65L04:*** M7 ***iCE65L08:*** P5	PIO	2
PIO2	M8	PIO	2
PIO2	M9	PIO	2
PIO2	N3	PIO	2
PIO2	N4	PIO	2
PIO2	N5	PIO	2
PIO2	N6	PIO	2

Die Cross Reference

The tables in this section list all the pads on a specific die type and provide a cross reference on how a specific pad connects to a ball or pin in each of the available package offerings. Similarly, the tables provide the pad coordinates for the die-based version of the product (DiePlus). These tables also provide a way to prototype with one package option and then later move to a different package or die.

As described in "Input and Output Register Control per PIO Pair" on page 16, PIO pairs share register control inputs. Similarly, as described in "Differential Inputs and Outputs" on page 12, a PIO pair can form a differential input or output. PIO pairs in I/O Bank 3 are optionally differential inputs or differential outputs. PIO pairs in all other I/O Banks are optionally differential outputs. In the tables, differential pairs are surrounded by a heavy blue box.

iCE65L04

Table 45 lists all the pads on the iCE65L04 die and how these pads connect to the balls or pins in the supported package styles. Most VCC, VCCIO, and GND pads are double-bonded inside the package although the table shows only a single connection.

For additional information on the iCE65L04 DiePlus product, please refer to the following data sheet.

DiePlus Advantage FPGA Known Good Die

Table 45: iCE65L04 Die Cross Reference

iCE65L04 Pad Name	VQ100	CB132	CB196	CB284	DiePlus Pad	X (µm)	Y (µm)
PIO3_00/DP00A	1	B1	C1	F5	1	129.40	2,687.75
PIO3_01/DP00B	2	C1	B1	G5	2	231.40	2,642.74
PIO3_02/DP01A	3	C3	D3	G7	3	129.40	2,597.75
PIO3_03/DP01B	4	D3	C3	H7	4	231.40	2,552.74
GND	5	F1	F1	K5	5	129.40	2,507.75
GND	—	—	—	—	6	231.40	2,462.74
VCCIO_3	6	E3	E3	J7	7	129.40	2,417.75
VCCIO_3	—	—	—	—	8	231.40	2,372.74
PIO3_04/DP02A	7	D4	D1	H8	9	129.40	2,327.75
PIO3_05/DP02B	8	E4	D2	J8	10	231.40	2,292.74
PIO3_06/DP03A	—	D1	E1	H5	11	129.40	2,257.75
PIO3_07/DP03B	—	E1	E2	J5	12	231.40	2,222.74
VCC	—	—	H9	D3	13	129.40	2,187.75
PIO3_08/DP04A	9	F4	D4	K8	14	231.40	2,152.74
PIO3_09/DP04B	10	F3	E4	K7	15	129.40	2,117.75
PIO3_10/DP05A	—	—	F3	E3	16	231.40	2,082.74
PIO3_11/DP05B	—	—	F4	F3	17	129.40	2,047.75
GND	—	H6	A9	M10	18	231.40	2,012.74
PIO3_12/DP06A	—	—	F5	G3	19	129.40	1,977.75
PIO3_13/DP06B	—	—	E5	H3	20	231.40	1,942.74
GND	—	—	A9	J3	21	129.40	1,907.75
GND	—	—	—	—	22	231.40	1,872.74
PIO3_14/DP07A	—	—	—	H1	23	129.40	1,837.75
PIO3_15/DP07B	—	—	—	J1	24	231.40	1,802.74
VCCIO_3	—	—	K1	K3	25	129.40	1,767.75
VCC	11	G6	G6	L10	26	231.40	1,732.74
PIO3_16/DP08A	—	—	—	K1	27	129.40	1,697.75
PIO3_17/DP08B	—	—	—	L1	28	231.40	1,662.74

iCE65L04	DiePlus						
Pad Name	VQ100	CB132	CB196	CB284	Pad	X (µm)	Y (µm)
PIO3_18/DP09A	12	—	G2	L3	29	129.40	1,627.75
GBIN7/PIO3_19/DP09B	13	G1	G1	L5	30	231.40	1,592.74
VCCIO_3	14	J6	J6	N10	31	129.40	1,557.75
VREF	N/A	N/A	N/A	M1	32	231.40	1,522.74
GND	—	—	A9	N1	33	129.40	1,487.75
GBIN6/PIO3_20/DP10A	15	H1	H1	M5	34	231.40	1,452.74
PIO3_21/DP10B	16	—	H2	M3	35	129.40	1,417.75
GND	17	H7	A9	M11	36	231.40	1,382.74
PIO3_22/DP11A	—	—	G3	N3	37	129.40	1,347.75
PIO3_23/DP11B	—	—	G4	P3	38	231.40	1,312.74
VCCIO_3	—	—	K1	R3	39	129.40	1,277.75
VCCIO_3	—	—	—	—	40	231.40	1,242.74
GND	—	—	A9	T3	41	129.40	1,207.75
GND	—	—	—	—	42	231.40	1,172.74
PIO3_24/DP12A	—	—	J1	U3	43	129.40	1,137.75
PIO3_25/DP12B	—	—	J2	V3	44	231.40	1,102.74
GND	—	—	A9	V1	45	129.40	1,067.75
PIO3_26/DP13A	—	—	H4	W3	46	231.40	1,032.74
PIO3_27/DP13B	—	—	H3	Y3	47	129.40	997.75
PIO3_28/DP14A	18	G3	K2	L7	48	231.40	962.74
PIO3_29/DP14B	19	G4	J3	L8	49	129.40	927.75
PIO3_30/DP15A	—	H3	H5	M7	50	231.40	892.74
PIO3_31/DP15B	—	H4	G5	M8	51	129.40	857.75
VCC	—	J4	F2	N8	52	231.40	822.74
PIO3_32/DP16A	20	J3	L1	N7	53	129.40	787.75
PIO3_33/DP16B	21	J1	L2	N5	54	231.40	752.74
VCCIO_3	22	K1	K1	P5	55	129.40	717.75
VCCIO_3	—	—	—	—	56	231.40	682.74
GND	23	L3	L3	R7	57	129.40	637.75
GND	—	—	—	—	58	231.40	592.74
PIO3_34/DP17A	—	K3	M1	P7	59	129.40	547.75
PIO3_35/DP17B	—	K4	M2	P8	60	231.40	502.74
PIO3_36/DP18A	24	L1	K3	R5	61	129.40	457.75
PIO3_37/DP18B	25	M1	K4	T5	62	231.40	412.74
PIO3_38/DP19A	—	N1	N1	U5	63	129.40	367.75
PIO3_39/DP19B	—	P1	N2	V5	64	231.40	322.74
PIO2_00	—	—	—	AB2	65	545.00	139.20
PIO2_01	—	P2	L4	V6	66	595.00	37.20
PIO2_02	—	M3	M3	T7	67	645.00	139.20
GND	—	—	C2	AB5	68	695.00	37.20
PIO2_03	26	L4	P1	R8	69	745.00	139.20
PIO2_04	27	P3	N3	V7	70	795.00	37.20
PIO2_05	28	M4	P2	T8	71	845.00	139.20
PIO2_06	29	L5	L5	R9	72	895.00	37.20
PIO2_07	30	P4	M4	V8	73	930.00	139.20

iCE65L04 Pad Name	DiePlus VQ100	CB132	CB196	CB284	Pad	X (µm)	Y (µm)
CRESET_B	44	L10	L10	R14	121	2,625.00	139.20
PIOS_00/SPI_SO	45	M11	M11	T15	122	2,690.00	37.20
PIOS_01/SPI_SI	46	P11	P11	V15	123	2,740.00	139.20
GND	47	—	P6	Y16	124	2,790.00	37.20
PIOS_02/SPI_SCK	48	P12	P12	V16	125	2,840.00	139.20
PIOS_03/SPI_SS_B	49	P13	P13	V17	126	2,890.00	37.20
SPI_VCC	50	L11	L11	R15	127	2,990.00	37.20
TDI	N/A	M12	M12	T16	128	3,610.80	342.00
TMS	N/A	P14	P14	V18	129	3,712.80	392.00
TCK	N/A	L12	L12	R16	130	3,610.80	442.00
TDO	N/A	N14	N14	U18	131	3,712.80	492.00
TRST_B	N/A	M14	M14	T18	132	3,610.80	542.00
PIO1_00	51	L14	K11	R18	133	3,712.80	592.00
PIO1_01	52	K12	L13	P16	134	3,610.80	642.00
PIO1_02	53	K11	K12	P15	135	3,712.80	692.00
PIO1_03	54	K14	M13	P18	136	3,610.80	727.00
GND	55	J14	J14	N18	137	3,712.80	762.00
GND	55	J14	J14	N18	138	3,610.80	797.00
PIO1_04	56	J12	J10	N16	139	3,712.80	832.00
PIO1_05	57	J11	L14	N15	140	3,610.80	867.00
VCCIO_1	58	H14	H14	M18	141	3,712.80	902.00
VCCIO_1	—	—	—	—	142	3,610.80	937.00
PIO1_06	59	H12	J11	M16	143	3,712.80	972.00
PIO1_07	60	H11	K14	M15	144	3,610.80	1,007.00
PIO1_08	—	—	H10	W20	145	3,712.80	1,042.00
PIO1_09	—	—	J13	V20	146	3,610.80	1,077.00
PIO1_10	—	—	J12	U20	147	3,712.80	1,112.00
VCC	61	H9	N7	M13	148	3,610.80	1,147.00
VCC	—	—	—	—	149	3,712.80	1,182.00
PIO1_11	—	—	H13	T22	150	3,610.80	1,217.00
PIO1_12	—	—	H12	R22	151	3,712.80	1,252.00
PIO1_13	—	—	—	P22	152	3,610.80	1,287.00
PIO1_14	—	—	—	N22	153	3,712.80	1,322.00
PIO1_15		—	G13	T20	154	3,610.80	1,357.00
PIO1_16	—	—	H11	R20	155	3,712.80	1,392.00
PIO1_17	—	—	G14	P20	156	3,610.80	1,427.00
GND	—	—	K10	N20	157	3,712.80	1,462.00
GND	—	—	—	—	158	3,610.80	1,497.00
PIO1_18	—	—	G10	M20	159	3,712.80	1,532.00
GBIN3/PIO1_19	62	F14	G12	K18	160	3,610.80	1,567.00
GBIN2/PIO1_20	63	G14	F10	L18	161	3,712.80	1,602.00
PIO1_21	—	—	F14	K20	162	3,610.80	1,637.00
VCCIO_1	—	—	H14	J20	163	3,712.80	1,672.00
VCCIO_1	—	—	—	—	164	3,610.80	1,707.00
PIO1_22	—	—	F13	H20	165	3,712.80	1,742.00
PIO1_23	—	—	D13	G20	166	3,610.80	1,777.00

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO2_28	—	Y13	132	2,062.5	139.5
GBIN5/PIO2_29	M7	V11	133	2,097.5	37.5
GBIN4/PIO2_30	N8	V12	134	2,132.5	139.5
GND	J8	Y12	135	2,167.5	37.5
GND	—	—	136	2,202.5	139.5
PIO2_31	P8	Y14	137	2,237.5	37.5
PIO2_32	—	AB15	138	2,272.5	139.5
PIO2_33	M8	V13	139	2,307.5	37.5
PIO2_34	—	AB16	140	2,342.5	139.5
PIO2_35	L8	Y15	141	2,377.5	37.5
PIO2_36	—	AB17	142	2,412.5	139.5
PIO2_37	N9	AB18	143	2,447.5	37.5
PIO2_38	—	AB19	144	2,482.5	139.5
PIO2_39	—	AB20	145	2,517.5	37.5
PIO2_40	—	AB21	146	2,552.5	139.5
PIO2_41	—	Y17	147	2,587.5	37.5
PIO2_42	—	AB22	148	2,622.5	139.5
PIO2_43	—	Y18	149	2,657.5	37.5
PIO2_44	P9	Y19	150	2,692.5	139.5
VCC	N7	N11	151	2,727.5	37.5
VCC	—	—	152	2,762.5	139.5
PIO2_45	M9	Y20	153	2,797.5	37.5
PIO2_46	K8	T11	154	2,832.5	139.5
VCCIO_2	J9	N13	155	2,867.5	37.5
VCCIO_2	—	—	156	2,902.5	139.5
PIO2_47	N11	R11	157	2,937.5	37.5
GND	J8	M12	158	2,972.5	139.5
GND	—	—	159	3,007.5	37.5
PIO2_48	N12	T12	160	3,042.5	139.5
PIO2_49	K9	R12	161	3,077.5	37.5
PIO2_50	N13	T13	162	3,112.5	139.5
PIO2_51/CBSEL0	L9	R13	163	3,147.5	37.5
PIO2_52/CBSEL1	P10	V14	164	3,182.5	139.5
CDONE	M10	T14	165	3,217.5	37.5
CRESET_B	L10	R14	166	3,260.0	139.5
PIOS_00/SPI_SO	M11	T15	167	3,320.0	37.5
PIOS_01/SPI_SI	P11	V15	168	3,370.0	139.5
GND	J8	Y16	169	3,420.0	37.5
GND	—	—	170	3,470.0	139.5
PIOS_02/SPI_SCK	P12	V16	171	3,520.0	37.5
PIOS_03/SPI_SS_B	P13	V17	172	3,570.0	139.5
VCC	—	—	173	3,620.0	37.5
VCC	—	—	174	3,670.0	139.5
SPI_VCC	L11	R15	175	3,720.0	37.5
SPI_VCC	—	—	176	3,770.0	139.5

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
GND	F7	E13	270	3,216.98	4,054.5
GND	—	—	271	3,166.98	4,156.5
PIO0_08	D9	E15	272	3,116.98	4,054.5
PIO0_09	C10	G14	273	3,064.48	4,156.5
PIO0_10	A10	A20	274	3,029.48	4,054.5
PIO0_11	B10	H13	275	2,994.48	4,156.5
PIO0_12	—	A19	276	2,959.48	4,054.5
PIO0_13	E9	G13	277	2,924.48	4,156.5
PIO0_14	—	C16	278	2,889.48	4,054.5
PIO0_15	—	E14	279	2,854.48	4,156.5
VCCIO_0	F6	E12	280	2,819.48	4,054.5
VCCIO_0	—	—	281	2,784.48	4,156.5
PIO0_16	—	A18	282	2,749.48	4,054.5
PIO0_17	—	A17	283	2,714.48	4,156.5
PIO0_18	C9	C15	284	2,679.48	4,054.5
PIO0_19	—	A16	285	2,644.48	4,156.5
PIO0_20	B9	C14	286	2,609.48	4,054.5
PIO0_21	—	H12	287	2,574.48	4,156.5
PIO0_22	D8	A15	288	2,539.48	4,054.5
PIO0_23	C8	H11	289	2,504.48	4,156.5
PIO0_24	E8	C13	290	2,469.48	4,054.5
PIO0_25	—	A14	291	2,434.48	4,156.5
GND	B12	C12	292	2,399.48	4,054.5
GND	—	—	293	2,364.48	4,156.5
PIO0_26	B8	A13	294	2,329.48	4,054.5
PIO0_27	D7	A12	295	2,294.48	4,156.5
PIO0_28	—	C11	296	2,259.48	4,054.5
GBIN1/PIO0_29	E7	E11	297	2,224.48	4,156.5
GBIN0/PIO0_30	A7	E10	298	2,189.48	4,054.5
PIO0_31	—	G12	299	2,154.48	4,156.5
VCCIO_0	A8	A8	300	2,119.48	4,054.5
VCCIO_0	—	—	301	2,084.48	4,156.5
PIO0_32	C7	A11	302	2,049.48	4,054.5
PIO0_33	—	G11	303	2,014.48	4,156.5
PIO0_34	E6	A10	304	1,979.48	4,054.5
PIO0_35	—	C10	305	1,944.48	4,156.5
VCC	B7	C8	306	1,909.48	4,054.5
VCC	—	—	307	1,874.48	4,156.5
PIO0_36	—	A9	308	1,839.48	4,054.5
PIO0_37	A6	A7	309	1,804.48	4,156.5
PIO0_38	B6	C9	310	1,769.48	4,054.5
PIO0_39	A5	A6	311	1,734.48	4,156.5
GND	G7	K11	312	1,699.48	4,054.5
GND	—	—	313	1,664.48	4,156.5
PIO0_40	D6	E9	314	1,629.48	4,054.5
PIO0_41	C6	G10	315	1,594.48	4,156.5

RAM4K Block

Table 56 provides timing information for the logic in a RAM4K block, which includes the paths shown in Figure 59.

Figure 59: RAM4K Timing Circuit

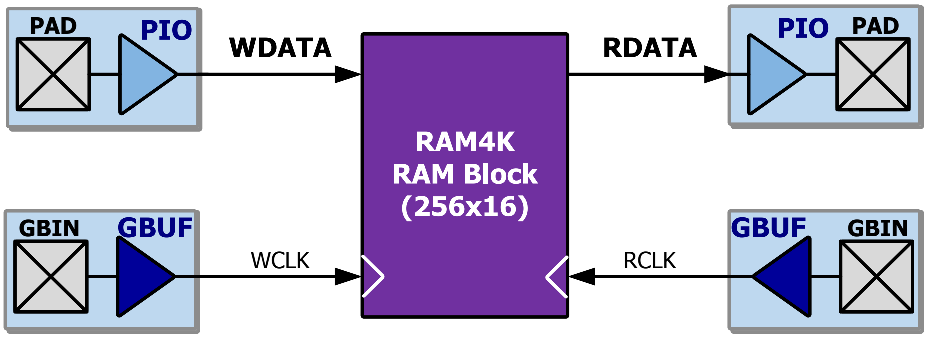


Table 56: Typical RAM4K Block Timing

Symbol	From	To	Description	L01	L04, L08			Units
			Device: iCE65	L01	L04, L08			
			Power/Speed Grade	–T	–L	–L	–T	
			Nominal VCC	1.2 V	1.0 V	1.2 V	1.2 V	
Symbol	From	To	Description	Typ.	Typ.	Typ.	Typ.	Units
	Write Setup/Hold Time							
t_{SUWD}	PIO input	GBIN input	Minimum write data setup time on PIO inputs before active clock edge on GBIN input, include interconnect delay.	0.6	3.1	1.7	0.8	ns
t_{HDWD}	GBIN input	PIO input	Minimum write data hold time on PIO inputs after active clock edge on GBIN input, including interconnect delay.	0	0	0	0	ns
	Read Clock-Output-Time							
t_{CKORD}	RCLK clock input	PIO output	Clock-to-output delay from RCLK input pin, through RAM4K RDATA output flip-flop to PIO output pad, including interconnect delay.	5.6	17.1	9.1	7.3	ns
t_{GBCKRM}	GBIN input	RCLK clock input	Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to the RCLK clock input.	2.1	7.3	3.8	2.6	ns
	Write and Read Clock Characteristics							
t_{RMWCKH}	WCLK RCLK	WCLK RCLK	Write clock High time	0.54	1.14	0.54	0.54	ns
t_{RMWCKL}			Write clock Low time	0.63	1.32	0.63	0.63	ns
t_{RMWCYC}			Write clock cycle time	1.27	2.64	1.27	1.27	ns
F_{WMAX}			Sustained write clock frequency	256	256	256	256	MHz