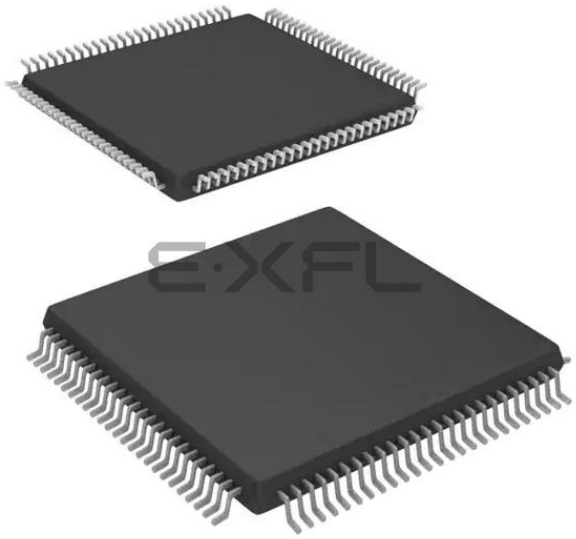

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	440
Number of Logic Elements/Cells	3520
Total RAM Bits	81920
Number of I/O	72
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice65l04f-tvq100i

Overview

The Lattice Semiconductor iCE65 programmable logic family is specifically designed to deliver the lowest static and dynamic power consumption of any comparable CPLD or FPGA device. iCE65 devices are designed for cost-sensitive, high-volume applications and provide on-chip, nonvolatile configuration memory (NVCM) to customize for a specific application. iCE65 devices can self-configure from a configuration image stored in an external commodity SPI serial Flash PROM or be downloaded from an external processor over an SPI-like serial port.

The three iCE65 components, highlighted in Table 1, deliver from approximately 1K to nearly 8K logic cells and flip-flops while consuming a fraction of the power of comparable programmable logic devices. Each iCE65 device includes between 16 to 32 RAM blocks, each with 4Kbits of storage, for on-chip data storage and data buffering.

As pictured in Figure 1, each iCE65 device consists of four primary architectural elements.

- An array of Programmable Logic Blocks (PLBs)
  - Each PLB contains eight Logic Cells (LCs); each Logic Cell consists of ...
    - A fast, four-input look-up table (LUT4) capable of implementing any combinational logic function of up to four inputs, regardless of complexity
    - A 'D'-type flip-flop with an optional clock-enable and set/reset control
    - Fast carry logic to accelerate arithmetic functions such as adders, subtracters, comparators, and counters.
  - Common clock input with polarity control, clock-enable input, and optional set/reset control input to the PLB is shared among all eight Logic Cells
- Two-port, 4Kbit RAM blocks (RAM4K)
  - 256x16 default configuration; selectable data width using programmable logic resources
  - Simultaneous read and write access; ideal for FIFO memory and data buffering applications
  - RAM contents pre-loadable during configuration
- Four I/O banks with independent supply voltage, each with multiple Programmable Input/Output (PIO) blocks
  - LVCMOS I/O standards and LVDS outputs supported in all banks
  - I/O Bank 3 supports additional SSTL, MDDR, LVDS, and SubLVDS I/O standards
- Programmable interconnections between the blocks
  - Flexible connections between all programmable logic functions
  - Eight dedicated low-skew, high-fanout clock distribution networks

Packaging Options

iCE65 components are available in a variety of package options to support specific application requirements. The available options, including the number of available user-programmable I/O pins (PIOs), are listed in Table 2. Fully-tested Known-Good Die (KGD) DiePlus™ are available for die stacking and highly space-conscious applications. All iCE65 devices are provided exclusively in Pb-free, RoHS-compliant packages.

Table 2: **iCE65 Family Packaging Options, Maximum I/O per Package**

Package	Package Body (mm)	Package Code	Ball/Lead Pitch (mm)	65L01	65L04	65L08
81-ball chip-scale BGA	5 x 5	CB81	0.5	63 *(0)*	—	—
84-pin quad flat no-lead package	7 x 7	QN84	0.5	67 *(0)*	—	—
100-pin very thin quad flat package	14 x 14	VQ100	0.5	72 *(0)* ⇔	72 *(9)*	—
121-ball chip-scale BGA	6 x 6	CB121	0.5	92 *(0)*	—	—
132-ball chip-scale BGA	8 x 8	CB132		93 *(0)* ⇨	95 *(11)* ⇨	95 *(12)*
196-ball chip-scale BGA	8 x 8	CB196		—	150 *(18)* ⇨	150 *(18)*
284-ball chip-scale BGA	12 x 12	CB284		—	176 *(20)* ⇔	222 *(25)*
Known Good Die	See DiePlus data sheet	DI	—	95 *(0)*	176 *(20)*	222 *(25)*

⇔ = Common footprint allows each density migration on the same printed circuit board. *(Differential input count)*.

The iCE65L04 and the iCE65L08 are both available in the CB196 package and have similar footprints but are not completely pin compatible. See "Pinout Differences between iCE65L04 and iCE65L08 in CB196 Package" on page 73 for more information.

When iCE65 components are supplied in the same package style, devices of different gate densities share a common footprint. The common footprint improves manufacturing flexibility. Different models of the same product can share a common circuit board. Feature-rich versions of the end application mount a larger iCE65 device on the circuit board. Low-end versions mount a smaller iCE65 device.

Programmable Logic Block (PLB)

Generally, a logic design for an iCE65 component is created using a high-level hardware description language such as Verilog or VHDL. The Lattice Semiconductor development software then synthesizes the high-level description into equivalent functions built using the programmable logic resources within each iCE65 device. Both sequential and combinational functions are constructed from an array of Programmable Logic Blocks (PLBs). Each PLB contains eight Logic Cells (LCs), as pictured in Figure 4, and share common control inputs, such as clocks, reset, and enable controls.

PLBs are connected to one another and other logic functions using the rich Programmable Interconnect resources.

Logic Cell (LC)

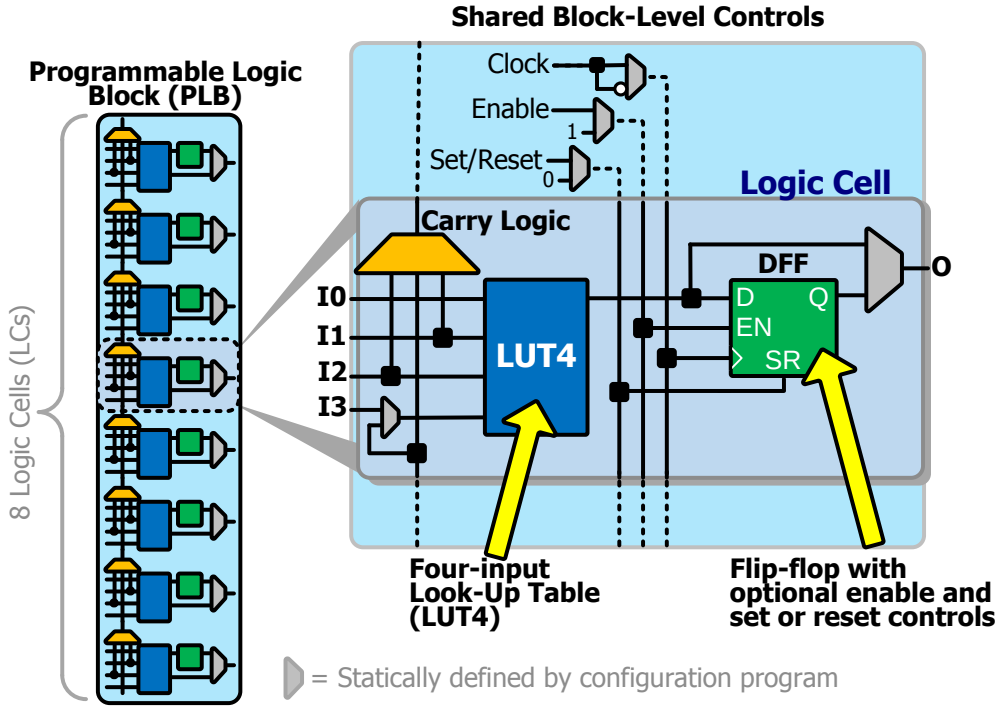
Each iCE65 device contains thousands of Logic Cells (LCs), as listed in Table 1. Each Logic Cell includes three primary logic elements, shown in Figure 4.

- A four-input Look-Up Table (LUT4) builds any combinational logic function, of any complexity, of up to four inputs. Similarly, the LUT4 element behaves as a 16x1 Read-Only Memory (ROM). Combine and cascade multiple LUT4s to create wider logic functions.

Figure 4: **Programmable Logic Block and Logic Cell**

- A 'D'-style Flip-Flop (DFF), with an optional clock-enable and reset control input, builds sequential logic functions. Each DFF also connects to a global reset signal that is automatically asserted immediately following device configuration.
- Carry Logic boosts the logic efficiency and performance of arithmetic functions, including adders, subtracters, comparators, binary counters and some wide, cascaded logic functions.

The output from a Logic Cell is available to all inputs to all eight Logic Cells within the Programmable Logic Block. Similarly, the Logic Cell output feeds into fabric to connect to other features on the iCE65 device.



Each flip-flop has an additional control that defines its set or reset behavior. As defined in the configuration image, the control defines whether the set or reset operation is synchronized to the active CLK clock edge or whether it is completely asynchronous.

- The SB_DFFR and SB_DFFS primitives are asynchronously controlled, solely by the SR input. If the SR input is High, then an SB_DFFR primitive is asynchronously reset and an SB_DFFS primitive is asynchronously set.
- The SB_DFFSR and SB_DFFRSS primitives are synchronously controlled by both the SR input and the clock input. If the SR input is High at a rising edge of the clock input, then an SB_DFFSR primitive is synchronously reset and an SB_DFFSS primitive is synchronously set.

The LUT4 output or the flip-flop output then connects to the programmable interconnect.

Because of the shared control signals, the design software can pack flip-flops with common control inputs into a single PLB block, as described by Table 4. There are eight total packing options.

Table 4: **Flip-flop Packing/Sharing within a PLB**

Group	Active Clock Edge	Clock Enable	Set or Reset Control (Sync. or Async)
1	↑	None (always enabled)	None
2	↓		
3	↑		PLB set/reset control
4	↓		
5	↑	Selective (controlled by PLB clock enable)	None
6	↓		
7	↑		PLB set/reset control
8	↓		

For detailed flip-flop internal timing, see Table 54.

Carry Logic

The dedicated Carry Logic within each Logic Cell primarily accelerates and improves the efficiency of arithmetic logic such as adders, accumulators, subtracters, incrementers, decrementers, counters, ALUs, and comparators. The Carry Logic also supports wide combinational logic functions.

$$COUT = I1 \bullet I2 + CIN \bullet I1 + CIN \bullet I2 \qquad \text{[Equation 1]}$$

Equation 1 and Figure 5 describe the Carry Logic structure within a Logic Cell. The Carry Logic shares inputs with the associated Look-Up Table (LUT4). The LUT4's I1 and I2 inputs directly feed the Carry Logic; inputs I0 and I3 do not. A signal cascades between Logic Cells within the Programmable Logic Block. The carry input from the previous adjacent Logic Cell optionally provides an alternate input to the LUT4 function, supplanting the I3 input.

Low-Power Disable

To save power and prevent unnecessary signal switching, the Carry Logic function within a Logic Cell is disabled if not used. The output of a Logic Cell's Carry Logic is forced High.

PLB Carry Input and Carry Output Connections

As shown in Figure 5, each Programmable Logic Block has a carry input signal that can be initialized High, Low, or come from the carry output signal from PLB immediately below.

Similarly, the Carry Logic output from the Programmable Logic Block connects to the PLB immediately above, which allows the Carry Logic to span across multiple PLBs in a column. As shown in Figure 6, the Carry Logic chain can be tapped mid-way through a chain or a PLB by feeding the value through a LUT4 function.

Adder Example

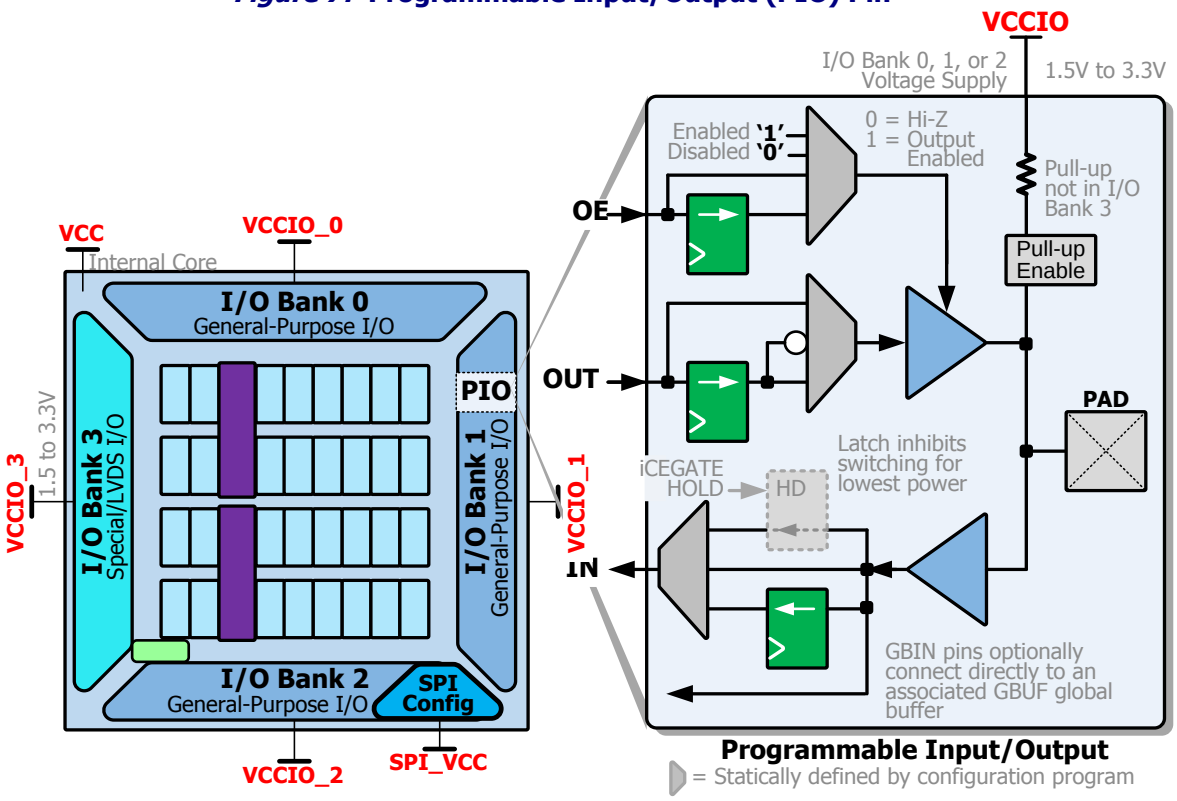
Figure 6 shows an example design that uses the Carry Logic. The example is a 2-bit adder, which can be expanded into an adder of arbitrary size. The LUT4 function within a Logic Cell is programmed to calculate the sum of the two input values and the carry input, `A[i] + B[i] + CARRY_IN[i-1] = SUM[i]`.

Programmable Input/Output Block (PIO)

Programmable Input/Output (PIO) blocks surround the periphery of the device and connect external components to the Programmable Logic Blocks (PLBs) and RAM4K blocks via programmable interconnect. Individual PIO pins are grouped into one of four I/O banks, as shown in Figure 7. I/O Bank 3 has additional capabilities, including LVDS differential I/O and the ability to interface to Mobile DDR memories.

Figure 7 also shows the logic within a PIO pin. When used in an application, a PIO pin becomes a signal input, an output, or a bidirectional I/O pin with a separate direction control input.

Figure 7: **Programmable Input/Output (PIO) Pin**



I/O Banks

PIO blocks are organized into four separate I/O banks, each with its own voltage supply input, as shown in Table 5. The voltage applied to the VCCIO pin on a bank defines the I/O standard used within the bank. Table 50 and Table 51 describe the I/O drive capabilities and switching thresholds by I/O standard. On iCE65L04 and iCE65L08 devices, I/O Bank 3, along the left edge of the die, is different than the others and supports specialized I/O standards.

I/O Bank Voltage Supply Inputs Support Different I/O Standards

Because each I/O bank has its own voltage supply, iCE65 components become the ideal bridging device between different interface standards. For example, the iCE65 device allows a 1.8V-only processor to interface cleanly with a 3.3V bus interface. The iCE65 device replaces external voltage translators.

Table 5: Supported Voltages by I/O Bank

Bank	Device Edge	Supply Input	3.3V	2.5V	1.8V	1.5V
0	Top	VCCIO_0	Yes	Yes	Yes	Outputs only
1	Right	VCCIO_1	Yes	Yes	Yes	Outputs only
2	Bottom	VCCIO_2	Yes	Yes	Yes	Outputs only
3	Left	VCCIO_3	Yes	Yes	Yes	iCE65L01: Outputs only iCE65L04/08: Yes
SPI	Bottom Right	SPI_VCC	Yes	Yes	Yes	No

For best possible performance, the global buffer inputs (GBIN[7:0]) connect directly to the their associated global buffers (GBUF[7:0]), bypassing the PIO logic and iCEgate circuitry as shown in Figure 7. Consequently, the direct GBIN-to-GBUF connection cannot be blocked by the iCEgate circuitry. However, it is possible to use iCEgate to block PIO-to-GBUF clock connections.

For additional information on using the iCEgate feature, please refer to the following application note.

AN002: Using iCEgate Blocking for Ultra-Low Power

Input Pull-Up Resistors on I/O Banks 0, 1, and 2

The PIO pins in I/O Banks 0, 1, and 2 have an optional input pull-up resistor. Pull-up resistors are not provided in iCE65L04 and iCE65L08 I/O Bank 3. During the iCE65 configuration process, the input pull-up resistor is unconditionally enabled and pulls the input to within a diode drop of the associated I/O bank supply voltage (VCCIO_#). This prevents any signals from floating on the circuit board during configuration.

After iCE65 configuration is complete, the input pull-up resistor is optional, defined by a configuration bit. The pull-up resistor is also useful to tie off unused PIO pins. The Lattice iCEcube development software defines all unused PIO pins in I/O Banks 0, 1 and 2 as inputs with the pull-up resistor turned on. The pull-up resistor value depends on the VCCIO voltage applied to the bank, as shown in Table 49.

Note: JTAG inputs TCK, TDI and TMS do not have the input pull-up resistor and must be tied off to GND when unused, else VCCIO_1 draws current.

No Input Pull-up Resistors on I/O Bank 3 of iCE65L04 and iCE65L08

The PIO pins in I/O Bank 3 do not have an internal pull-up resistor. To minimize power consumption, tie unused PIO pins in Bank 3 to a known logic level or drive them as a disabled high-impedance output.

Input Hysteresis

Inputs typically have about 50 mV of hysteresis, as indicated in Table 49.

Output and Output Enable Signal Path

As shown in Figure 7, a signal from programmable interconnect feeds the OUT signal on a Programmable I/O pad. This output connects either directly to the associated package pin or is held in an optional output flip-flop. Because all flip-flops are automatically reset after configuration, the output from the output flip-flop can be optionally inverted so that an active-Low output signal is held in the disabled (High) state immediately after configuration.

Similarly, each Programmable I/O pin has an output enable or three-state control called OE. When OE = High, the OUT output signal drives the associated pad, as described in Table 10. When OE = Low, the output driver is in the high-impedance (Hi-Z) state. The OE output enable control signal itself connects either directly to the output buffer or is held in an optional register. The output buffer is optionally permanently enabled or permanently disabled, either to unconditionally drive output signals, or to allow input-only signals.

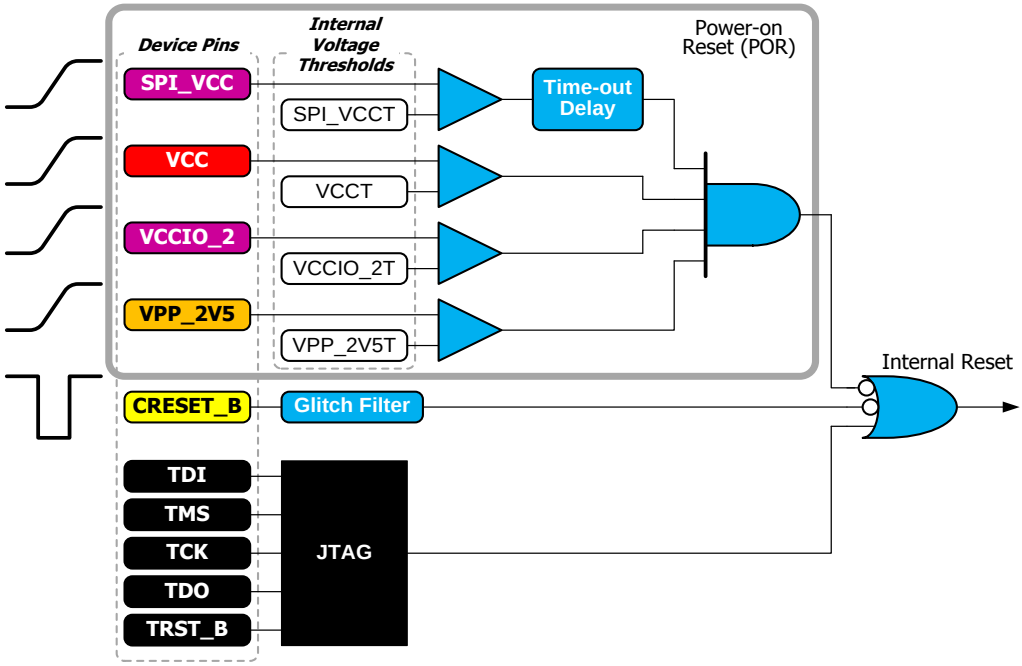
Table 10: **PIO Output Operations (non-registered operation, no inversions)**

Operation	OUT Data Output	OE Enable	PAD
Three-State	X	0	Hi-Z
Drive Output Data	OUT	1*	OUT

X = don't care, 1* = High or unused, Hi-Z = high-impedance, three-stated, floating.

See Input and Output Register Control per PIO Pair for information about the registered input path.

Figure 22: iCE65 Internal Reset Circuitry



Power-On Reset (POR)

The Power-on Reset (POR) circuit monitors specific voltage supply inputs and holds the device in reset until all the relevant supplies exceed the internal voltage thresholds. The SPI_VCC supply also has an additional time-out delay to allow an attached SPI serial PROM to power up properly. Table 24 shows the POR supply inputs. The Nonvolatile Configuration Memory (NVCM) requires that the VPP_2V5 supply be connected, even if the application does not use the NVCM.

***Table 24:* Power-on Reset (POR) Voltage Resources**

Supply Rail	iCE65 Production Devices
VCC	Yes
SPI_VCC	Yes
VCCIO_1	No
VCCIO_2	Yes
VPP_2V5	Yes

CRESET_B Pin

The CRESET_B pin resets the iCE65 internal logic when Low.

JTAG Interface

Specific command sequences also reset the iCE65 internal logic.

SPI Master Configuration Interface

All iCE65 devices, including those with NVCM, can be configured from an external, commodity SPI serial Flash PROM, as shown in Figure 23. The SPI configuration interface is essentially its own independent I/O bank, powered by the VCC_SPI supply input. Presently, most commercially-available SPI serial Flash PROMs require a 3.3V supply.

Pinout Table

Table 38 provides a detailed pinout table for the QN84 package. Pins are generally arranged by I/O bank, then by ball function. The QN84 package has no JTAG pins.

Table 38: **iCE65 QN84 Chip-scale BGA Pinout Table**

Ball Function	Ball Number	Pin Type	Bank
GBIN0/PIO0	B32	GBIN	0
GBIN1/PIO0	A43	GBIN	0
PIO0	A38	PIO	0
PIO0	A39	PIO	0
PIO0	A40	PIO	0
PIO0	A41	PIO	0
PIO0	A44	PIO	0
PIO0	A45	PIO	0
PIO0	A46	PIO	0
PIO0	A47	PIO	0
PIO0	A48	PIO	0
PIO0	B29	PIO	0
PIO0	B30	PIO	0
PIO0	B31	PIO	0
PIO0	B34	PIO	0
PIO0	B35	PIO	0
PIO0	B36	PIO	0
VCCIO_0	A42	VCCIO	0
GBIN2/PIO1	B22	GBIN	1
GBIN3/PIO1	A29	GBIN	1
PIO1	A25	PIO	1
PIO1	A26	PIO	1
PIO1	A27	PIO	1
PIO1	A31	PIO	1
PIO1	A32	PIO	1
PIO1	A33	PIO	1
PIO1	A34	PIO	1
PIO1	A35	PIO	1
PIO1	B19	PIO	1
PIO1	B20	PIO	1
PIO1	B21	PIO	1
PIO1	B23	PIO	1
PIO1	B24	PIO	1
PIO1	B26	PIO	1
PIO1	B27	PIO	1
VCCIO_1	B25	VCCIO	1
CDONE	B16	CONFIG	2
CRESET_B	A21	CONFIG	2
GBIN4/PIO2	A14	GBIN	2
GBIN5/PIO2	A16	GBIN	2
PIO2	A13	PIO	2
PIO2	B12	PIO	2
PIO2	A19	PIO	2
PIO2	B10	PIO	2
PIO2	B11	PIO	2
PIO2	B13	PIO	2

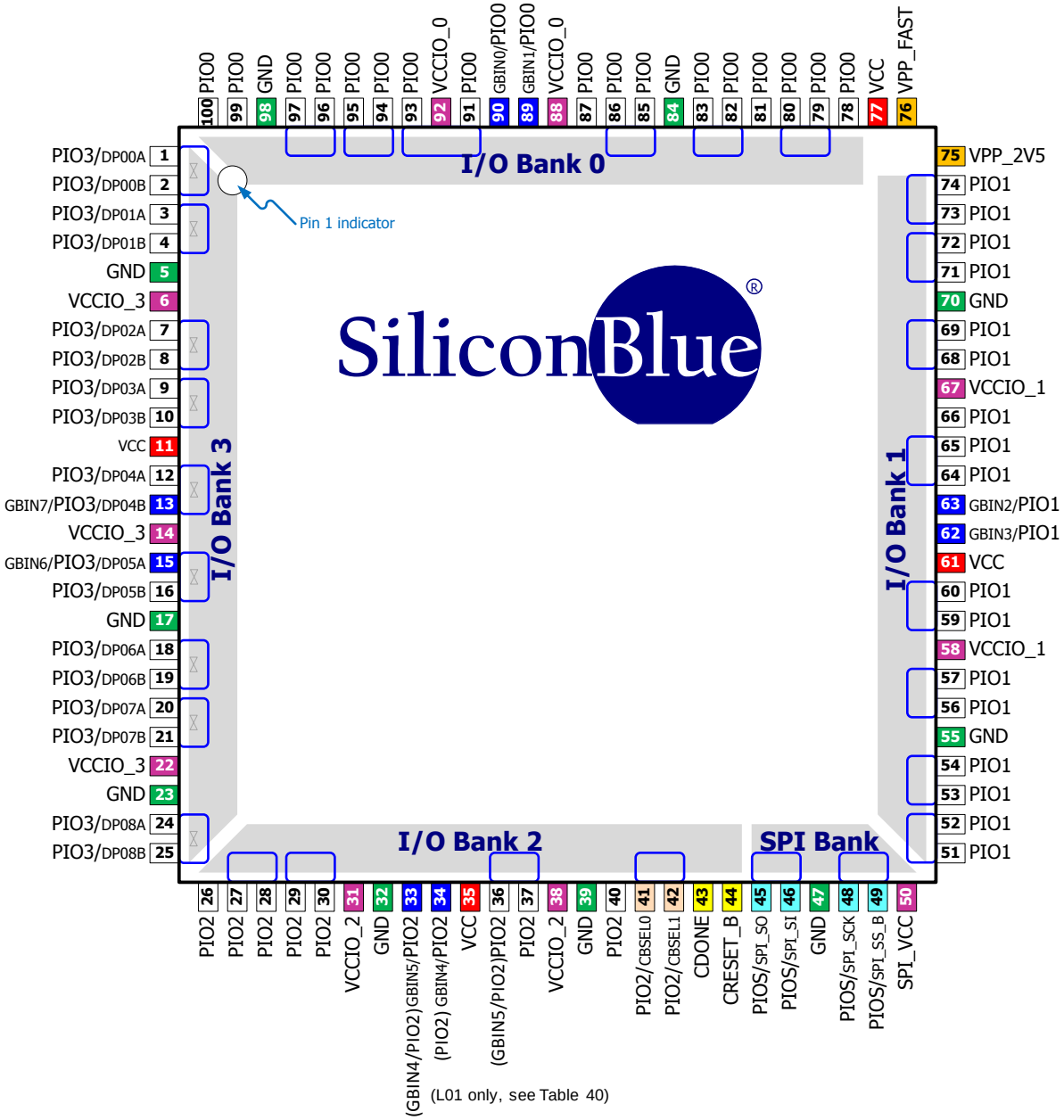
VQ100 Very-thin Quad Flat Package

The VQ100 package is a very-thin quad-flat package with 0.5 mm lead pitch. The iCE65L01 and iCE65L04 devices are available in this package.

Footprint Diagram

Figure 36 shows the footprint diagram for the 100-lead very-thin quad-flat package (VQ100). See Table 40 for a complete, detailed pinout for the 100-lead very-thin quad-flat package. The signal pins are also grouped into the four I/O Banks and the SPI interface.

Figure 36: iCE65 VQ100 Footprint (Top View)



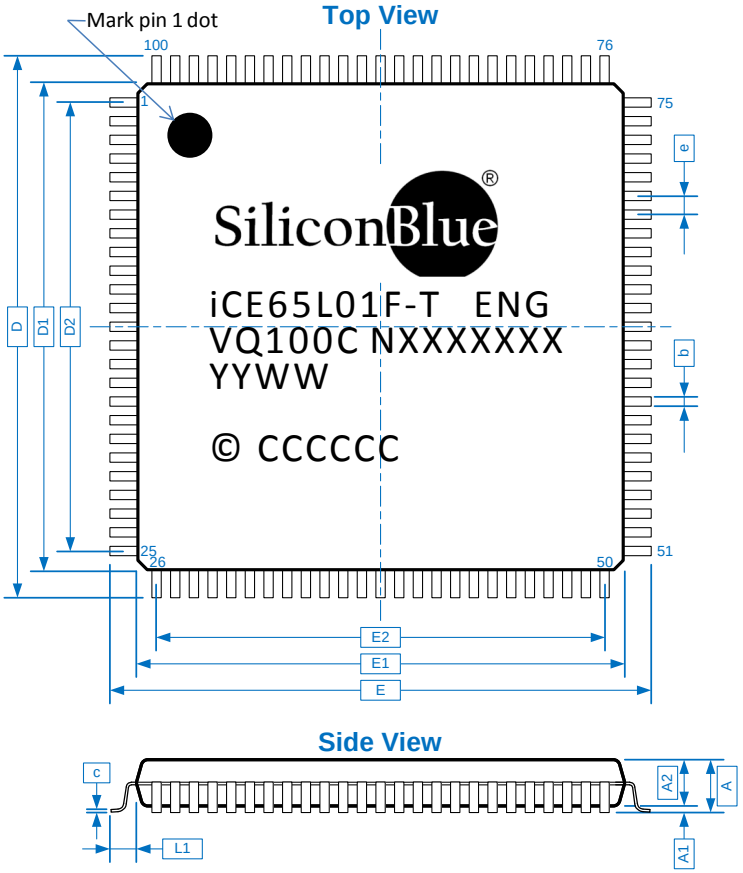
Pinout Table

Table 39 provides a detailed pinout table for the VQ100 package. Pins are generally arranged by I/O bank, then by pin function. The table also highlights the differential I/O pairs in I/O Bank 3. The VQ100 package has no JTAG pins.

Pin Function	Pin Number	Type	Bank
VCC	61	VCC	VCC
VCC	77	VCC	VCC
VPP_2V5	75	VPP	VPP
VPP_FAST	76	VPP	VPP

Package Mechanical Drawing

Figure 37: VQ100 Package Mechanical Drawing: Standard Device Marking



Description		Symbol	Min.	Nominal	Max.	Units
Leads per Edge	X			25		Leads
	Y			25		
Number of Signal Leads		n		100		
Maximum Size (lead tip to lead tip)	X	E	—	16.0	—	mm
	Y	D	—	16.0	—	
Body Size	X	E1	—	14.0	—	
	Y	D1	—	14.0	—	
Edge Pin Center to Center	X	E2	—	12.0	—	
	Y	D2	—	12.0	—	
Lead Pitch		e	—	0.50	—	
Lead Width		b	0.17	0.20	0.27	
Total Package Height		A	—	1.20	—	
Stand Off		A1	0.05	—	0.15	
Body Thickness		A2	0.95	1.00	1.05	
Lead Length		L1	—	1.00	—	
Lead Thickness		c	0.09	—	0.20	
Coplanarity			—	0.08	—	

Top Marking Format

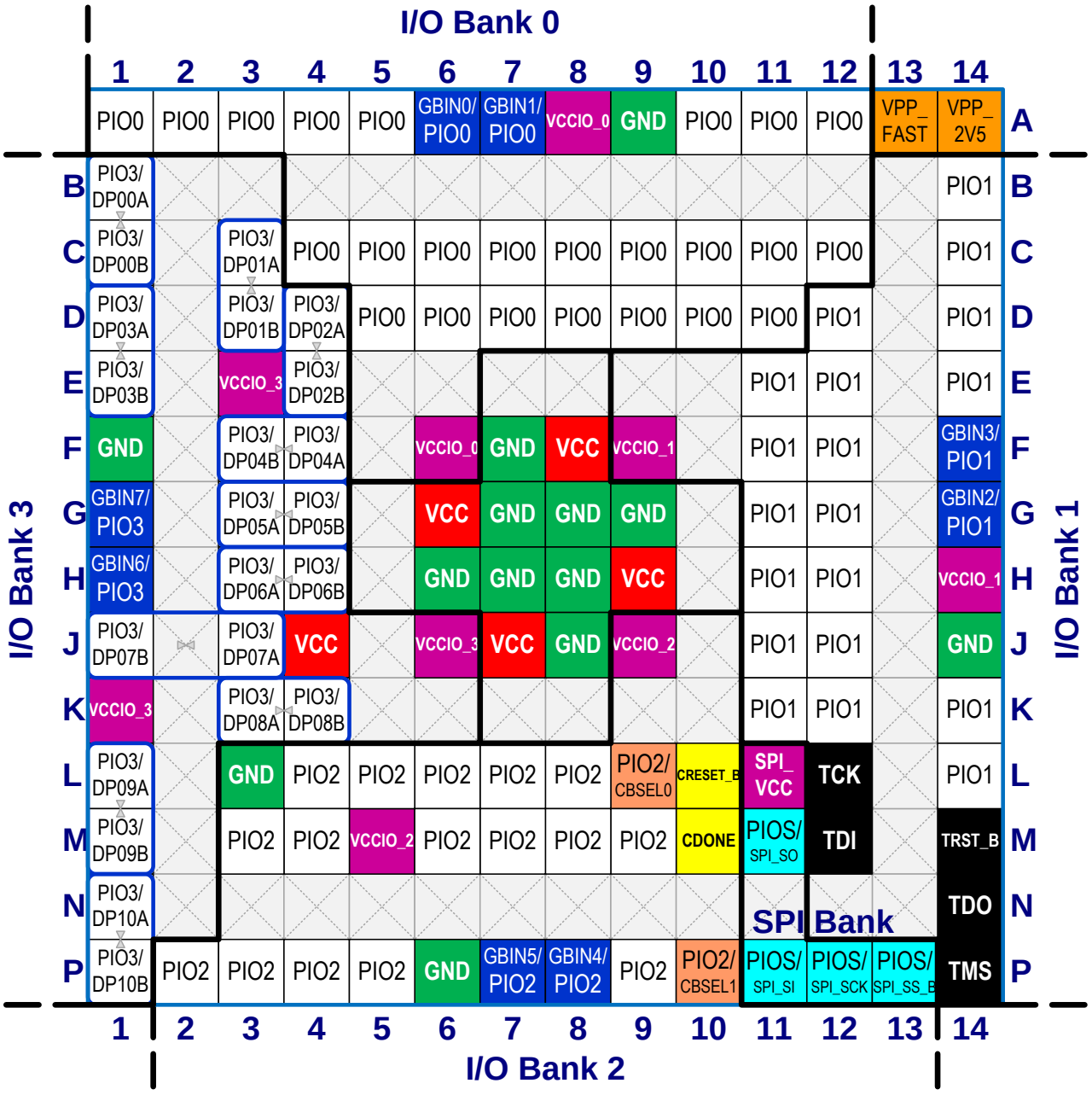
Line	Content	Description
1	Logo	Logo
2	iCE65L01F	Part number
	-T	Power/Speed
	ENG	Engineering
3	VQ100C NXXXXXXX	Package type and Lot number
4	YYWW	Date Code
5	N/A	Blank
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θJA (°C/W)	
0 LFM	200 LFM
38	32

Ball Function	Ball Number	Pin Type	Bank
PIO2	J11	PIO	2
PIO2	K3	PIO	2
PIO2	K4	PIO	2
PIO2	K11	PIO	2
PIO2	L2	PIO	2
PIO2	L3	PIO	2
PIO2	L4	PIO	2
PIO2	L5	PIO	2
PIO2	L10	PIO	2
PIO2	L11	PIO	2
PIO2/CBSEL0	H6	PIO	2
PIO2/CBSEL1	J6	PIO	2
VCCIO_2	K5	VCCIO	2
PIO3	C1	PIO	3
PIO3	B1	PIO	3
PIO3	D1	PIO	3
PIO3	E2	PIO	3
PIO3	C2	PIO	3
PIO3	D2	PIO	3
PIO3	C3	PIO	3
PIO3	C4	PIO	3
PIO3	E4	PIO	3
PIO3	D4	PIO	3
PIO3	F3	PIO	3
PIO3	G3	PIO	3
PIO3	G4	PIO	3
GBIN6/PIO3	F4	GBIN	3
GBIN7/PIO3	D3	GBIN	3
PIO3	E3	PIO	3
PIO3	F2	PIO	3
PIO3	G1	PIO	3
PIO3	H1	PIO	3
PIO3	J1	PIO	3
PIO3	H2	PIO	3
PIO3	H3	PIO	3
PIO3	J3	PIO	3
PIO3	J2	PIO	3
VCCIO_3	A1	VCCIO	3
VCCIO_3	G2	VCCIO	3
PIOS/SPI_SO	J8	SPI	SPI
PIOS/SPI_SI	K8	SPI	SPI
PIOS/SPI_SCK	K9	SPI	SPI
PIOS/SPI_SS_B	J9	SPI	SPI
SPI_VCC	J10	SPI	SPI
GND	B2	GND	GND
GND	B10	GND	GND
GND	E1	GND	GND
GND	F5	GND	GND
GND	F6	GND	GND
GND	G5	GND	GND
GND	G6	GND	GND
GND	G11	GND	GND

Figure 42: **iCE65L04 CB132 Chip-Scale BGA Footprint (Top View)**



Ball Function	Ball Number	Pin Type	Bank
L01/L04: GBIN7/PIO3 L08: GBIN7/DP05B	G1	GBIN	3
L01/L04: PIO3/DP05A L08: PIO3/DP05A	G3	DPIO	3
L01/L04: PIO3/DP05B L08: PIO3/DP11B	G4	DPIO	3
L01/L04: PIO3/DP06A L08: PIO3/DP06B	H3	DPIO	3
L01/L04: PIO3/DP06B L08: PIO3/DP11A	H4	DPIO	3
PIO3/DP07A	J3	DPIO	3
PIO3/DP07B	J1	DPIO	3
PIO3/DP08A	K3	DPIO	3
PIO3/DP08B	K4	DPIO	3
PIO3/DP09A	L1	DPIO	3
PIO3/DP09B	M1	DPIO	3
PIO3/DP10A	N1	DPIO	3
PIO3/DP10B	P1	DPIO	3
VCCIO_3	E3	VCCIO	3
VCCIO_3	J6	VCCIO	3
VCCIO_3	K1	VCCIO	3
PIOS/SPI_SO	M11	SPI	SPI
PIOS/SPI_SI	P11	SPI	SPI
PIOS/SPI_SCK	P12	SPI	SPI
PIOS/SPI_SS_B	P13	SPI	SPI
SPI_VCC	L11	SPI	SPI
GND	A9	GND	GND
GND	F1	GND	GND
GND	F7	GND	GND
GND	G7	GND	GND
GND	G8	GND	GND
GND	G9	GND	GND
GND	H6	GND	GND
GND	H7	GND	GND
GND	H8	GND	GND
GND	J8	GND	GND
GND	J14	GND	GND
GND	L3	GND	GND
GND	P6	GND	GND
VCC	F8	VCC	VCC
VCC	G6	VCC	VCC
VCC	H9	VCC	VCC
VCC	J4	VCC	VCC
VCC	J7	VCC	VCC
VPP_2V5	A14	VPP	VPP
VPP_FAST	A13	VPP	VPP

CB196 Chip-Scale Ball-Grid Array

The CB196 package is a chip-scale, fully-populated, ball-grid array with 0.5 mm ball pitch.

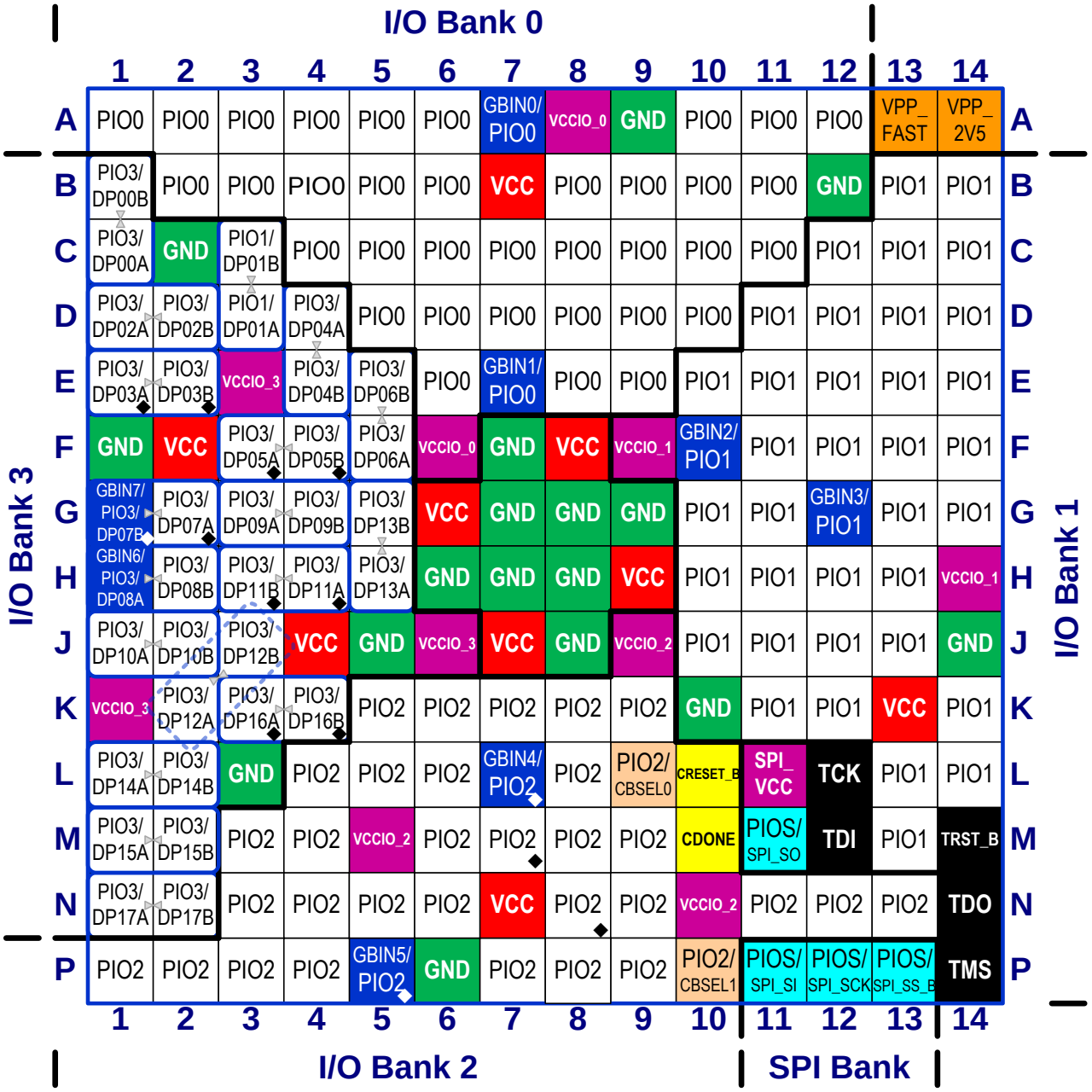
Footprint Diagram

Figure 45 shows the iCE65L04 chip-scale BGA footprint for the 8 x 8 mm CB196 package. The footprint for the iCE65L08 is different than the iCE64L04 footprint, as shown in Figure 46. The pinout differences are highlighted by warning diamonds (◆) in the footprint diagrams and summarized in Table 43.

> Although both the iCE65L04 and iCE65L08 are both available in the CB196 package and ***almost*** completely pin compatible, there are differences as shown in Table 43.

Figure 31 shows the conventions used in the diagram. Also see Table 42 for a complete, detailed pinout for the 196-ball chip-scale BGA packages. The signal pins are also grouped into the four I/O Banks and the SPI interface.

Figure 45: **iCE65L04 CB196 Chip-Scale BGA Footprint (Top View)**



Ball Function	Ball Number	Pin Type	Bank
PIO2 (◆)	***iCE65L04:*** N8 ***iCE65L08:*** L7	PIO	2
PIO2	N9	PIO	2
PIO2	N11	PIO	2
PIO2	N12	PIO	2
PIO2	N13	PIO	2
PIO2	P1	PIO	2
PIO2	P2	PIO	2
PIO2	P3	PIO	2
PIO2	P4	PIO	2
PIO2	P7	PIO	2
PIO2	P8	PIO	2
PIO2	P9	PIO	2
PIO2/CBSEL0	L9	PIO	2
PIO2/CBSEL1	P10	PIO	2
VCCIO_2	J9	VCCIO	2
VCCIO_2	M5	VCCIO	2
VCCIO_2	N10	VCCIO	2
PIO3/DP00A	C1	DPIO	3
PIO3/DP00B	B1	DPIO	3
PIO3/DP01A	D3	DPIO	3
PIO3/DP01B	C3	DPIO	3
PIO3/DP02A	D1	DPIO	3
PIO3/DP02B	D2	DPIO	3
PIO3/DP03A (◆)	***iCE65L04:*** E1 ***iCE65L08:*** E2	DPIO	3
PIO3/DP03B (◆)	***iCE65L04:*** E2 ***iCE65L04:*** E1	DPIO	3
PIO3/DP04A	D4	DPIO	3
PIO3/DP04B	E4	DPIO	3
PIO3/DP05A (◆)	***iCE65L04:*** F3 ***iCE65L08:*** F4	DPIO	3
PIO3/DP05B (◆)	***iCE65L04:*** F4 ***iCE65L08:*** F3	DPIO	3
PIO3/DP06A	F5	DPIO	3
PIO3/DP06B	E5	DPIO	3
PIO3/DP07A (◆)	***iCE65L04:*** G2 ***iCE65L08:*** H4	DPIO	3
GBIN7/PIO3/DP07B (◆)	***iCE65L04:*** G1 ***iCE65L08:*** H3	GBIN	3
GBIN6/PIO3/DP08A	H1	GBIN	3
PIO3/DP08B	H2	DPIO	3
PIO3/DP09A	G3	DPIO	3
PIO3/DP09B	G4	DPIO	3
PIO3/DP10A	J1	DPIO	3
PIO3/DP10B	J2	DPIO	3
PIO3/DP11A (◆)	***iCE65L04:*** H4 ***iCE65L08:*** G1	DPIO	3
PIO3/DP11B (◆)	***iCE65L04:*** H3 ***iCE65L08:*** G2	DPIO	3
PIO3/DP12A	K2	DPIO	3
PIO3/DP12B	J3	DPIO	3

Ball Function	Ball Number iCE65L04 iCE65L08	Pin Type by Device iCE65L04	Pin Type by Device iCE65L08	Bank	CB132 Ball Equivalent
PIO0	E15	PIO	PIO	0	A11
PIO0	E16	PIO	PIO	0	A12
PIO0	G8	PIO	PIO	0	C4
PIO0	G9	PIO	PIO	0	C5
PIO0	G10	PIO	PIO	0	C6
PIO0	G11	PIO	PIO	0	C7
PIO0	G12	PIO	PIO	0	C8
PIO0	G13	PIO	PIO	0	C9
PIO0	G14	PIO	PIO	0	C10
PIO0	G15	PIO	PIO	0	C11
PIO0	G16	PIO	PIO	0	C12
PIO0	H9	PIO	PIO	0	D5
PIO0	H10	PIO	PIO	0	D6
PIO0	H11	PIO	PIO	0	D7
PIO0	H12	PIO	PIO	0	D8
PIO0	H13	PIO	PIO	0	D9
PIO0	H14	PIO	PIO	0	D10
PIO0	H15	PIO	PIO	0	D11
VCCIO_0	A8	VCCIO	VCCIO	0	—
VCCIO_0	A21	VCCIO	VCCIO	0	—
VCCIO_0	E12	VCCIO	VCCIO	0	A8
VCCIO_0	K10	VCCIO	VCCIO	0	F6
GBIN2/PIO1	L18	GBIN	GBIN	1	G14
GBIN3/PIO1	K18	GBIN	GBIN	1	F14
PIO1 (●)	A22	N.C.	PIO	1	—
PIO1 (●)	AA22	N.C.	PIO	1	—
PIO1 (●)	B22	N.C.	PIO	1	—
PIO1	C20	PIO	PIO	1	—
PIO1 (●)	C22	N.C.	PIO	1	—
PIO1	D20	PIO	PIO	1	—
PIO1 (●)	D22	N.C.	PIO	1	—
PIO1	E20	PIO	PIO	1	—
PIO1 (●)	E22	N.C.	PIO	1	—
PIO1	F18	PIO	PIO	1	B14
PIO1	F20	PIO	PIO	1	—
PIO1 (●)	F22	N.C.	PIO	1	—
PIO1	G18	PIO	PIO	1	C14
PIO1	G20	PIO	PIO	1	—
PIO1	G22	PIO	PIO	1	—
PIO1	H16	PIO	PIO	1	D12
PIO1	H18	PIO	PIO	1	D14
PIO1	H20	PIO	PIO	1	—
PIO1	J15	PIO	PIO	1	E11
PIO1	J16	PIO	PIO	1	E12
PIO1	J18	PIO	PIO	1	E14
PIO1 (●)	J22	N.C.	PIO	1	—
PIO1	K15	PIO	PIO	1	F11
PIO1	K16	PIO	PIO	1	F12
PIO1	K20	PIO	PIO	1	—
PIO1 (●)	K22	N.C.	PIO	1	—

iCE65L04 Pad Name	DiePlus VQ100	CB132	CB196	CB284	Pad	X (µm)	Y (µm)
PIO3_18/DP09A	12	—	G2	L3	29	129.40	1,627.75
GBIN7/PIO3_19/DP09B	13	G1	G1	L5	30	231.40	1,592.74
VCCIO_3	14	J6	J6	N10	31	129.40	1,557.75
VREF	N/A	N/A	N/A	M1	32	231.40	1,522.74
GND	—	—	A9	N1	33	129.40	1,487.75
GBIN6/PIO3_20/DP10A	15	H1	H1	M5	34	231.40	1,452.74
PIO3_21/DP10B	16	—	H2	M3	35	129.40	1,417.75
GND	17	H7	A9	M11	36	231.40	1,382.74
PIO3_22/DP11A	—	—	G3	N3	37	129.40	1,347.75
PIO3_23/DP11B	—	—	G4	P3	38	231.40	1,312.74
VCCIO_3	—	—	K1	R3	39	129.40	1,277.75
VCCIO_3	—	—	—	—	40	231.40	1,242.74
GND	—	—	A9	T3	41	129.40	1,207.75
GND	—	—	—	—	42	231.40	1,172.74
PIO3_24/DP12A	—	—	J1	U3	43	129.40	1,137.75
PIO3_25/DP12B	—	—	J2	V3	44	231.40	1,102.74
GND	—	—	A9	V1	45	129.40	1,067.75
PIO3_26/DP13A	—	—	H4	W3	46	231.40	1,032.74
PIO3_27/DP13B	—	—	H3	Y3	47	129.40	997.75
PIO3_28/DP14A	18	G3	K2	L7	48	231.40	962.74
PIO3_29/DP14B	19	G4	J3	L8	49	129.40	927.75
PIO3_30/DP15A	—	H3	H5	M7	50	231.40	892.74
PIO3_31/DP15B	—	H4	G5	M8	51	129.40	857.75
VCC	—	J4	F2	N8	52	231.40	822.74
PIO3_32/DP16A	20	J3	L1	N7	53	129.40	787.75
PIO3_33/DP16B	21	J1	L2	N5	54	231.40	752.74
VCCIO_3	22	K1	K1	P5	55	129.40	717.75
VCCIO_3	—	—	—	—	56	231.40	682.74
GND	23	L3	L3	R7	57	129.40	637.75
GND	—	—	—	—	58	231.40	592.74
PIO3_34/DP17A	—	K3	M1	P7	59	129.40	547.75
PIO3_35/DP17B	—	K4	M2	P8	60	231.40	502.74
PIO3_36/DP18A	24	L1	K3	R5	61	129.40	457.75
PIO3_37/DP18B	25	M1	K4	T5	62	231.40	412.74
PIO3_38/DP19A	—	N1	N1	U5	63	129.40	367.75
PIO3_39/DP19B	—	P1	N2	V5	64	231.40	322.74
PIO2_00	—	—	—	AB2	65	545.00	139.20
PIO2_01	—	P2	L4	V6	66	595.00	37.20
PIO2_02	—	M3	M3	T7	67	645.00	139.20
GND	—	—	C2	AB5	68	695.00	37.20
PIO2_03	26	L4	P1	R8	69	745.00	139.20
PIO2_04	27	P3	N3	V7	70	795.00	37.20
PIO2_05	28	M4	P2	T8	71	845.00	139.20
PIO2_06	29	L5	L5	R9	72	895.00	37.20
PIO2_07	30	P4	M4	V8	73	930.00	139.20

iCE65L04 Pad Name	DiePlus VQ100	CB132	CB196	CB284	Pad	X (µm)	Y (µm)
PIO2_08	—	L6	P3	R10	74	965.00	37.20
VCCIO_2	31	M5	M5	T9	75	1,000.00	139.20
PIO2_09	—	P5	K5	V9	76	1,035.00	37.20
PIO2_10	—	M6	N4	T10	77	1,070.00	139.20
GND	32	P6	H7	V10	78	1,105.00	37.20
PIO2_11	—	—	P4	Y4	79	1,140.00	139.20
PIO2_12	—	—	L6	Y5	80	1,175.00	37.20
PIO2_13	—	—	—	AB6	81	1,210.00	139.20
PIO2_14	—	—	—	AB7	82	1,245.00	37.20
PIO2_15	—	—	—	AB8	83	1,280.00	139.20
PIO2_16	—	—	—	AB9	84	1,315.00	37.20
PIO2_17	—	—	—	AB10	85	1,350.00	139.20
PIO2_18	—	—	—	AB11	86	1,385.00	37.20
GND	—	J8	H8	N12	87	1,420.00	139.20
PIO2_19	—	—	K6	Y6	88	1,455.00	37.20
PIO2_20	—	—	N5	Y7	89	1,490.00	139.20
VCC	—	—	J4	Y8	90	1,525.00	37.20
PIO2_21	—	—	M6	Y9	91	1,560.00	139.20
PIO2_22	—	—	N6	Y10	92	1,595.00	37.20
GBIN5/PIO2_23	33	P7	P5	V11	93	1,630.00	139.20
GBIN4/PIO2_24	34	P8	L7	V12	94	1,665.00	37.20
PIO2_25	—	—	—	AB12	95	1,700.00	139.20
VCCIO_2	—	—	J9	Y11	96	1,735.00	37.20
PIO2_26	—	—	—	AB13	97	1,770.00	139.20
PIO2_27	—	—	K7	AB14	98	1,805.00	37.20
GND	—	—	J5	Y12	99	1,840.00	139.20
PIO2_28	—	—	K9	AB15	100	1,875.00	37.20
PIO2_29	—	—	M7	Y13	101	1,910.00	139.20
PIO2_30	—	—	K8	Y14	102	1,945.00	37.20
PIO2_31	—	—	P7	Y15	103	1,980.00	139.20
PIO2_32	—	—	L8	Y17	104	2,015.00	37.20
PIO2_33	—	—	P8	Y18	105	2,050.00	139.20
PIO2_34	—	—	N8	Y19	106	2,085.00	37.20
PIO2_35	—	—	M8	Y20	107	2,120.00	139.20
VCC	35	J7	J7	N11	108	2,155.00	37.20
VCC	—	—	—	—	109	2,190.00	139.20
PIO2_36	36	P9	P9	V13	110	2,225.00	37.20
PIO2_37	37	M7	N9	T11	111	2,260.00	139.20
VCCIO_2	38	J9	N10	N13	112	2,295.00	37.20
PIO2_38	—	L7	M9	R11	113	2,330.00	139.20
GND	39	H8	J8	M12	114	2,365.00	37.20
PIO2_39	—	M8	N12	T12	115	2,400.00	139.20
PIO2_40	—	L8	N11	R12	116	2,435.00	37.20
PIO2_41	40	M9	N13	T13	117	2,470.00	139.20
PIO2_42/CBSEL0	41	L9	L9	R13	118	2,505.00	37.20
PIO2_43/CBSEL1	42	P10	P10	V14	119	2,540.00	139.20
CDONE	43	M10	M10	T14	120	2,575.00	37.20

Programmable Input/Output (PIO) Block

Table 55 provides timing information for the logic in a Programmable Logic Block (PLB), which includes the paths shown in Figure 57 and Figure 58. The timing shown is for the LVCMOS25 I/O standard in all I/O banks. The iCEcube development software reports timing adjustments for other I/O standards.

Figure 57: **Programmable I/O (PIO) Pad-to-Pad Timing Circuit**

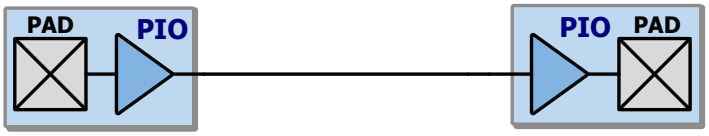


Figure 58: **Programmable I/O (PIO) Sequential Timing Circuit**

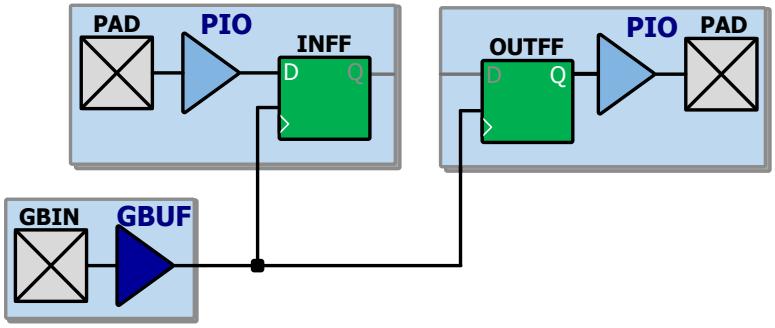


Table 55: **Typical Programmable Input/Output (PIO) Timing (LVCMOS25)**

Symbol	From	To	Device: iCE65	L01	L04, L08			Units
			Power/Speed Grad	–T	–L		–T	
			Nominal VCC	1.2 V	1.0 V	1.2 V	1.2 V	
			Description	Typ.	Typ.	Typ.	Typ.	
		Synchronous Output Paths						
t_{OCKO}	OUTFF clock input	PIO output	Delay from clock input on OUTFF output flip-flop to PIO output pad.	4.7	13.8	7.3	5.6	ns
t_{GBCKIO}	GBIN input	OUTFF clock input	Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to clock input on the PIO OUTFF output flip-flop.	2.1	7.3	3.8	2.6	ns
		Synchronous Input Paths						
t_{SUPDIN}	PIO input	GBIN input	Setup time on PIO input pin to INFF input flip-flop before active clock edge on GBIN input, including interconnect delay.	0	0	0	0	ns
t_{HDPDIN}	GBIN input	PIO input	Hold time on PIO input to INFF input flip-flop after active clock edge on the GBIN input, including interconnect delay.	2.7	7.1	3.6	2.8	ns
		Pad to Pad						
t_{PADIN}	PIO input	Inter-connect	Asynchronous delay from PIO input pad to adjacent interconnect.	2.5	9.5	5.0	3.2	ns
t_{PADO}	Inter-connect	PIO output	Asynchronous delay from adjacent interconnect to PIO output pad including interconnect delay.	4.5	14.6	7.7	6.2	ns

		minimum temperature to –40°C in Figure 2 and Table 48. Added NVCM programming temperature to Table 48.
1.3	17-DEC-2008	Added footprint and pinout information for the CS110 Wafer-Level Chip-Scale Ball Grid Array. Clarified that the CB196 footprint shown is for the iCE65L04; the iCE65L08 footprint for the CB196 package is similar but different. Added updated information on Differential Inputs and Outputs, including support for SubLVDS. Updated Electrical Characteristics and AC Timing Guidelines sections. Added support for the LVCMOS15 I/O standard. Corrected the diagram showing the direct differential clock input, Figure 16. Updated the number of I/Os by package in Table 34. Updated company address. Other minor updates throughout.
1.2	11-OCT-2008	Updated I/O Bank 3 characteristics in Table 7 and Table 51. Corrected label in Figure 14. Added JTAG configuration to Table 20. Added pull-up resistor information in Table 22 and Figure 21. Added "Internal Device Reset" section. Updated internal oscillator performance in and Table 57. Updated configuration timing in Table 58 based on new oscillator timing. Completely reorganized the "Package and Pinout Information" section. Added information on CS63 and CB196 packages. Updated information on VPP_2V5 signal in Table 36. Reduced package height for CB132 and CB284 packages to 1.0 mm. Added "Differential Inputs" and "Differential Outputs" sections.
1.1	4-SEPT-2008	Updated package roadmap (Table 2) and updated ordering codes (Figure 2). Updated Figure 7. Updated Figure 24. Added CS63 package footprint (Figure 36), pinout (Table 39) and Package.
1.0	31-MAY-2008	Initial public release.