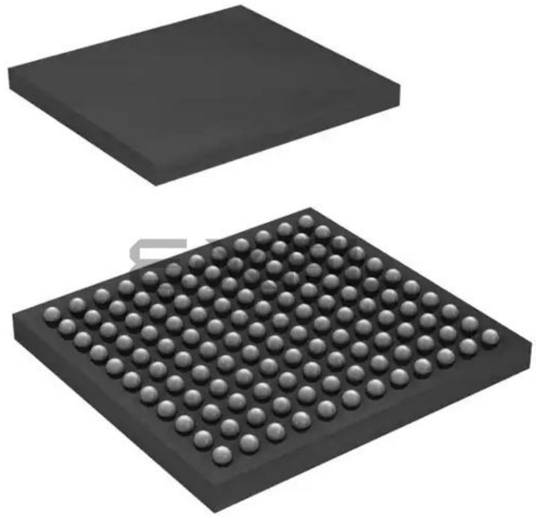

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

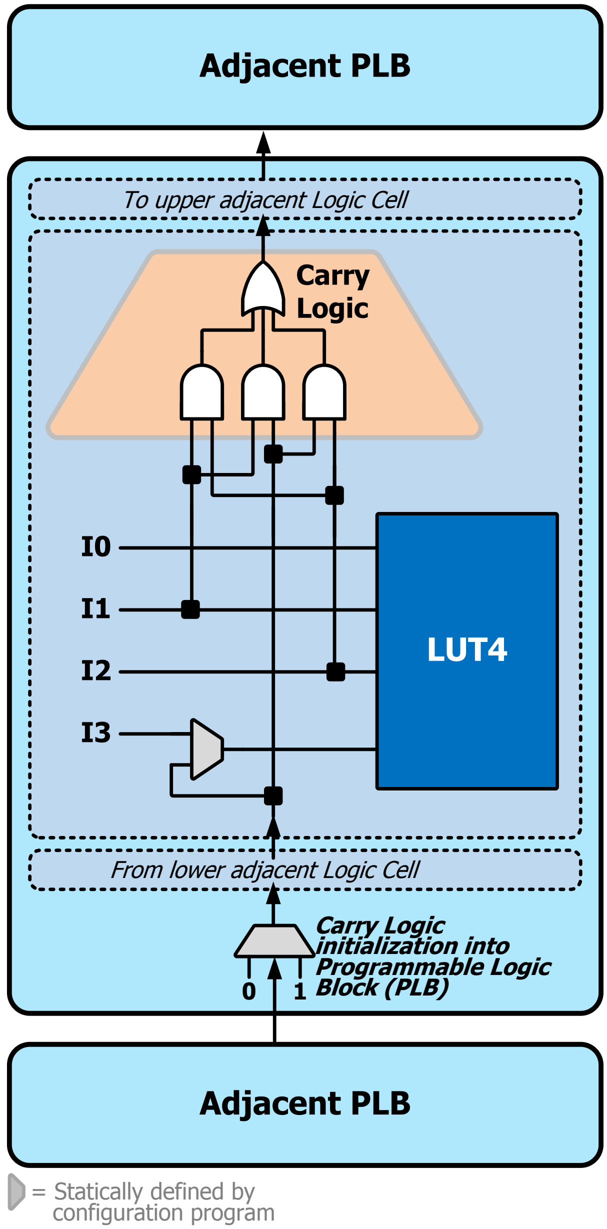
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	960
Number of Logic Elements/Cells	7680
Total RAM Bits	131072
Number of I/O	95
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	132-VFBGA, CSPBGA
Supplier Device Package	132-CSBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice65l08f-lcb132i

The Carry Logic generates the carry value to feed the next bit in the adder. The calculated carry value replaces the I3 input to the next LUT4 in the upper Logic Cell.

If required by the application, the carry output from the final stage of the adder is available by passing it through the final LUT4.

***Figure 5:* Carry Logic Structure within a Logic Cell and between PLBs**



If not connected to an external SPI PROM, the four pins associated with the SPI Master Configuration Interface can be used as PIO pins, supplied by the SPI_VCC input, essentially forming a fifth "mini" I/O bank. If using an SPI Flash PROM, then connect SPI_VCC to 3.3V.

I/O Banks 0, 1, 2, SPI and Bank 3 of iCE65L01

Table 6 highlights the available I/O standards when using an iCE65 device, indicating the drive current options, and in which bank(s) the standard is supported. I/O Banks 0, 1, 2 and SPI interface support the same standards. I/O Bank 3 has additional capabilities in iCE65L04 and iCE65L08, including support for MDDR memory standards and LVDS differential I/O.

***Table 6:* I/O Standards for I/O Banks 0, 1, 2, SPI Interface Bank, and Bank 3 of iCE65L01**

I/O Standard	Supply Voltage	Drive Current (mA)	Attribute Name
5V Input Tolerance	3.3V	N/A	N/A
LVCMOS33	3.3V	±11	SB_LVCMOS
LVCMOS25	2.5V	±8	
LVCMOS18	1.8V	±5	
LVCMOS15 outputs	1.5V	±4	

IBIS Models for I/O Banks 0, 1, 2 and the SPI Bank

The IBIS (I/O Buffer Information Specification) file that describes the output buffers used in I/O Banks 0, 1, 2, SPI Bank and Bank 3 of iCE65L01 is available from the following link.

- IBIS Models for I/O Banks 0, 1, 2, SPI Bank and Bank 3 of iCE65L01

I/O Bank 3 of iCE65L04 and iCE65L08

I/O Bank 3, located along the left edge of the die, has additional special I/O capabilities to support memory components and differential I/O signaling (LVDS). Table 7 lists the various I/O standards supported by I/O Bank 3. The SSTL2 and SSTL18 I/O standards require the VREF voltage reference input pin which is only available on the CB284 package. Also see Table 51 for electrical characteristics.

***Table 7:* I/O Standards for I/O Bank 3 Only of iCE65L04 and iCE65L08**

I/O Standard	Supply Voltage	VREF Pin (CB284 or DiePlus) Required?	Target Drive Current (mA)	Attribute Name
LVCMOS33	3.3V	No	±8	SB_LVCMOS33_8
LVCMOS25	2.5V	No	±16	SB_LVCMOS25_16
			±12	SB_LVCMOS25_12
			±8	SB_LVCMOS25_8
			±4	SB_LVCMOS25_4
LVCMOS18	1.8V	No	±10	SB_LVCMOS18_10
			±8	SB_LVCMOS18_8
			±4	SB_LVCMOS18_4
			±2	SB_LVCMOS18_2
LVCMOS15	1.5V	No	±4	SB_LVCMOS15_4
			±2	SB_LVCMOS15_2
SSTL2_II	2.5V	Yes	±16.2	SB_SSTL2_CLASS_2
SSTL2_I			±8.1	SB_SSTL2_CLASS_1
SSTL18_II	1.8V	Yes	±13.4	SB_SSTL18_FULL
SSTL18_I			±6.7	SB_SSTL18_HALF
MDDR	1.8V	No	±10	SB_MDDR10
			±8	SB_MDDR8
			±4	SB_MDDR4
			±2	SB_MDDR2
LVDS	2.5V	No	N/A	SB_LVDS_INPUT

Automatic Global Buffer Insertion, Manual Insertion

The iCEcube development software automatically assigns high-fanout signals to a global buffer. However, to manual insert a global buffer input/global buffer (GBIN/GBUF) combination, use the `SB_IO_GB` primitive. To insert just a global buffer (GBUF), use the `SB_GB` primitive.

Global Hi-Z Control

The global high-impedance control signal, GHIZ, connects to all I/O pins on the iCE65 device. This GHIZ signal is automatically asserted throughout the configuration process, forcing all user-I/O pins into their high-impedance state. Similarly, the PIO pins can be forced into their high-impedance state via the JTAG controller.

Global Reset Control

The global reset control signal connects to all PLB and PIO flip-flops on the iCE65 device. The global reset signal is automatically asserted throughout the configuration process, forcing all flip-flops to their defined wake-up state. For PLB flip-flops, the wake-up state is always reset, regardless of the PLB flip-flop primitive used in the application. See Table 3 for more information.

The PIO flip-flops are always reset during configuration, although the output flip-flop can be inverted before leaving the iCE65 device, as shown in Figure 11.

RAM

Each iCE65 device includes multiple high-speed synchronous RAM blocks (RAM4K), each 4Kbit in size. As shown in Table 16 a single iCE65 integrates between 16 to 96 such blocks. Each RAM4K block is generically a 256-word deep by 16-bit wide, two-port register file, as illustrated in Figure 17. The input and output connections, to and from a RAM4K block, feed into the programmable interconnect resources.

Figure 17: RAM4K Memory Block

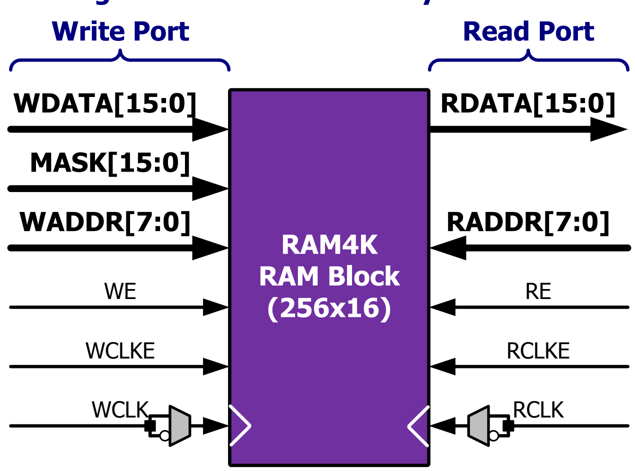


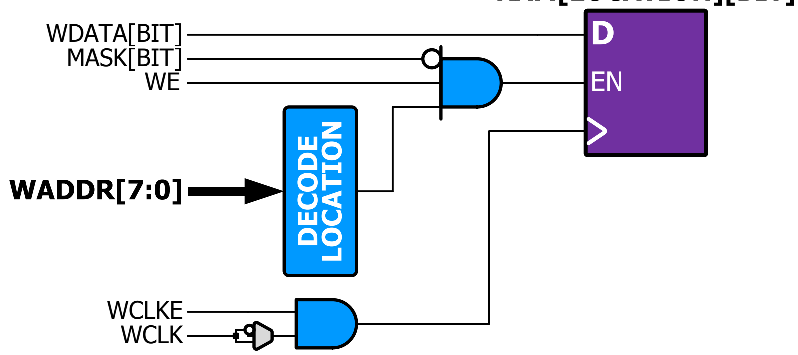
Table 16: RAM4K Blocks per Device

Device	RAM4K Blocks	Default Configuration	RAM Bits per Block	Block RAM Bits
iCE65L01	16	256 x 16	4K (4,096)	64K
iCE65L04	20			80K
iCE65L08	32			128K

Using programmable logic resources, a RAM4K block implements a variety of logic functions, each with configurable input and output data width.

- Random-access memory (RAM)
  - Single-port RAM with a common address, enable, and clock control lines
  - Two-port RAM with separate read and write control lines, address inputs, and enable

Figure 18: RAM4K Bit Write Logic



When the WCLKE signal is Low, the clock to the RAM4K block is disabled, keeping the RAM in its lowest power mode.

Table 18: RAM4K Write Operations

Operation	WDATA[15:0] Data	MASK[15:0] Mask Bit	WADDR[7:0] Address	WE Write Enable	WCLKE Clock Enable	WCLK Clock	RAM Location
Disabled	X	X	X	X	X	0	No change
Disabled					0	X	No change
Disabled	X	X	X	0	X	X	No change
Write Data	WDATA[i]	MASK[i] = 0	WADDR	1	1	↑	RAM[WADDR][i] = WDATA[i]
Masked Write	X	MASK[i] = 1	WADDR	1	1	↑	RAM[WADDR][i] = No change

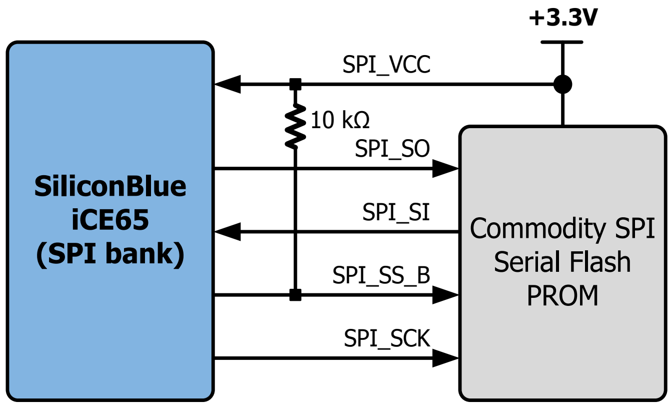
To write data into the RAM4K block, perform the following operations.

- Supply a valid address on the WADDR[7:0] address input port
- Supply valid data on the WDATA[15:0] data input port
- To write or mask selected data bits, set the associated MASK input port accordingly. For example, write operations on data bit D[i] are controlled by the associated MASK[i] input.
  - MASK[i] = 0: Write operations are enabled for data line WDATA[i]
  - MASK[i] = 1: Mask write operations are disabled for data line WDATA[i]
- Enable the RAM4K write port (WE = 1)
- Enable the RAM4K write clock (WCLKE = 1)
- Apply a rising clock edge on WCLK (assuming that the clock is not inverted)

Read Operations

Figure 19 shows the logic involved in reading a location from RAM. Table 19 describes various read operations for a RAM4K block. By default, all RAM4K read operations are synchronized to the rising edge of RCLK although the clock is invertible as shown in Figure 19.

Figure 23: **iCE65 SPI Master Configuration Interface**



The SPI configuration interface is used primarily during development before mass production, where the configuration is then permanently programmed in the NVCM configuration memory. However, the SPI interface can also be the primary configuration interface allowing easy in-system upgrades and support for multiple configuration images.

The SPI control signals are defined in Table 25. Table 26 lists the SPI interface ball or pins numbers by package.

Table 25: **SPI Master Configuration Interface Pins (SPI_SS_B High before Configuration)**

Signal Name	Direction	Description
SPI_VCC	Supply	SPI Flash PROM voltage supply input.
SPI_SO	Output	SPI Serial Output from the iCE65 device.
SPI_SI	Input	SPI Serial Input to the iCE65 device, driven by the select SPI serial Flash PROM.
SPI_SS_B	Output	SPI Slave Select output from the iCE65 device. Active Low.
SPI_SCK	Output	SPI Slave Clock output from the iCE65 device.

After configuration, the SPI port pins are available to the user-application as additional PIO pins, supplied by the SPI_VCC input voltage, essentially providing a fifth "mini" I/O bank.

Table 26: **SPI Interface Ball/Pin Numbers by Package**

SPI Interface	VQ100	CB132	CB196	CB284
SPI_VCC	50	L11	L11	R15
PIOS/SPI_SO	45	M11	M11	T15
PIOS/SPI_SI	46	P11	P11	V15
PIOS/SPI_SS_B	49	P13	P13	V17
PIOS/SPI_SCK	48	P12	P12	V16

SPI PROM Requirements

The iCE65 mobileFPGA SPI Flash configuration interface supports a variety of SPI Flash memory vendors and product families. However, Lattice Semiconductor does not specifically test, qualify, or otherwise endorse any specific SPI Flash vendor or product family. The iCE65 SPI interface supports SPI PROMs that they meet the following requirements.

- The PROM must operate at 3.3V or 2.5V in order to trigger the iCE65 FPGA's power-on reset circuit.
- The PROM must support the `0x0B` Fast Read command, using a 24-bit start address and has 8 dummy bits before the PROM provides first data (see Figure 25: SPI Fast Read Command).
- The PROM must have enough bits to program the iCE65 device (see Table 27: Smallest SPI PROM Size (bits), by Device, by Number of Images).
- The PROM must support data operations at the upper frequency range for the selected iCE65 internal oscillator frequency (see Table 57). The oscillator frequency is selectable when creating the FPGA bitstream image.

- For lowest possible power consumption after configuration, the PROM should also support the `0xB9` Deep Power Down command and the `0xAB` Release from Deep Power-down Command (see Figure 24 and Figure 26). The low-power mode is optional.
- The PROM must be ready to accept commands 10 µs after meeting its power-on conditions. In the PROM data sheet, this may be specified as t_{VSL} or t_{VCSL}. It is possible to use slower PROMs by holding the CRESET_B input Low until the PROM is ready, then releasing CRESET_B, either under program control or using an external power-on reset circuit.

The Lattice iCEman65 development board and associated programming software uses an ST Micro/Numonyx M25Pxx SPI serial Flash PROM.

SPI PROM Size Requirements

Table 27 lists the minimum SPI PROM size required to configure an iCE65 device. Larger PROM sizes are allowed, but not required unless the end application uses the additional space. SPI serial PROM sizes are specified in bits. For each device size, the table shows the required minimum PROM size for "Logic Only" (no BRAM initialization) and "Logic + RAM4K" (RAM4K blocks pre-initialized). Furthermore, the table shows the PROM size for varying numbers of configuration images. Most applications will use a single image. Applications that use the Cold Boot or Warm Boot features may use more than one image.

Table 27: Smallest SPI PROM Size (bits), by Device, by Number of Images

	1 Image		2 Images		3 Images		4 Images	
Device	Logic Only	Logic + RAM4K	Logic Only	Logic + RAM4K	Logic Only	Logic + RAM4K	Logic Only	Logic + RAM4K
iCE65L01	256K	256K	512K	512K	1M	1M	1M	1M
iCE65L04	512K	1M	1M	2M	2M	2M	2M	4M
iCE65L08	1M	2M	2M	4M	4M	4M	4M	8M

Enabling SPI Configuration Interface

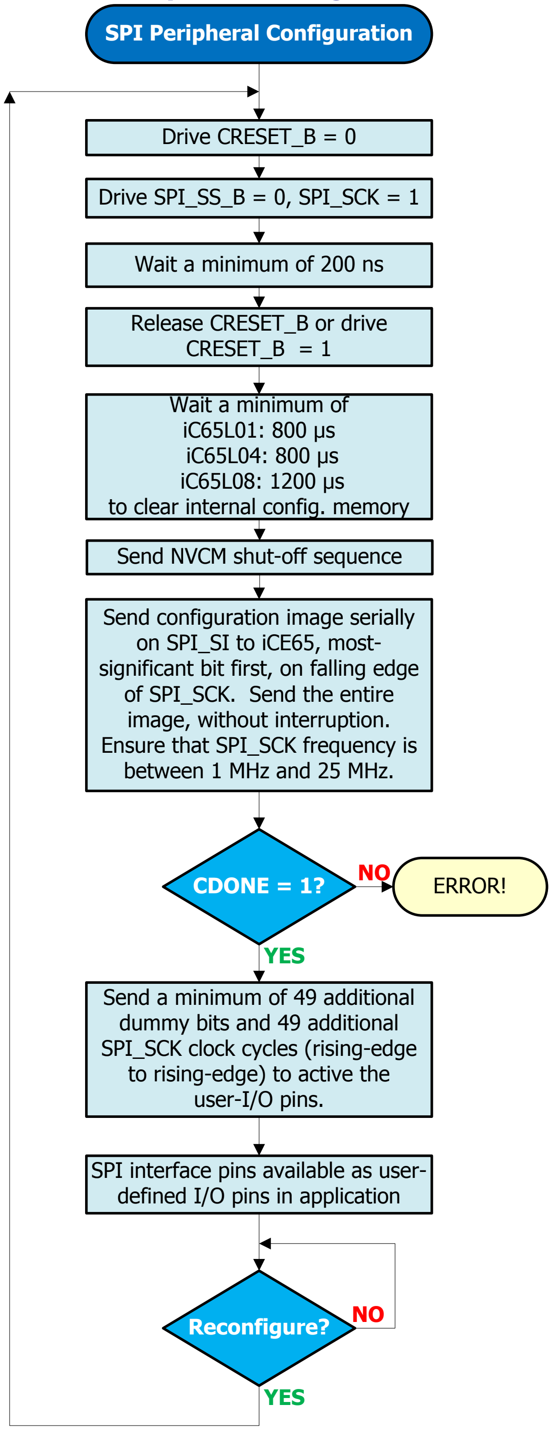
To enable the SPI configuration mode, the SPI_SS_B pin must be allowed to float High. The SPI_SS_B pin has an internal pull-up resistor. If SPI_SS_B is Low, then the iCE65 component defaults to the SPI Slave configuration mode.

SPI Master Configuration Process

The iCE65 SPI Master Configuration Interface supports a variety of modern, high-density, low-cost SPI serial Flash PROMs. Most modern SPI PROMs include a power-saving Deep Power-down mode. The iCE65 component exploits this mode for additional system power savings.

The iCE65 SPI interface starts by driving SPI_SS_B Low, and then sends a Release from Power-down command to the SPI PROM, hexadecimal command code `0xAB`. Figure 24 provides an example waveform. This initial command wakes up the SPI PROM if it is already in Deep Power-down mode. If the PROM is not in Deep Power-down mode, the extra command has no adverse affect other than that it requires a few additional microseconds during the configuration process. The iCE65 device transmits data on the SPI_SO output, on the falling edge of the SPI_SCK output. The SPI PROM does not provide any data to the iCE65 device's SPI_SI input. After sending the last command bit, the iCE65 device de-asserts SPI_SS_B High, completing the command. The iCE65 device then waits a minimum of 10 µS before sending the next SPI PROM command.

Figure 30: SPI Peripheral Configuration Process



Voltage Compatibility

As shown in Figure 23, there are potentially three different supply voltages involved in the SPI Peripheral interface, described in Table 30.

Table 30: SPI Peripheral Mode Supply Voltages

Supply Voltage	Description
AP_VCCIO	I/O supply to the Application Processor (AP)
VCC_SPI	Voltage supply for the iCE65 SPI interface.
VCCIO_2	Supply voltage for the iCE65 I/O Bank 2.

Table 31 describes how to maintain voltage compatibility for two interface scenarios. The easiest interface is when the Application Processor's (AP) I/O supply rail and the iCE65's SPI and VCCIO_2 bank supply rails all connect to the same voltage. The second scenario is when the AP's I/O supply voltage is greater than the iCE65's VCCIO_2 supply voltage.

***Table 31:* CRESET_B and CDONE Voltage Compatibility**

Condition	CRESET_B			CDONE Pull-up	Requirement
	Direct	**Open-Drain**	**Pull-up**		
VCCIO_AP = VCC_SPI **VCCIO_AP = VCCIO_2**	OK	OK with pull-up	Required if using open-drain output	Recommended	AP can directly drive CRESET_B High and Low although an open-drain output recommended is if multiple devices control CRESET_B. If using an open-drain driver, the CRESET_B input must include a 10 kΩ pull-up resistor to VCCIO_2. The 10 kΩ pull-up resistor to AP_VCCIO is also recommended.
AP_VCCIO > VCCIO_2	N/A	Required, requires pull-up	Required	Required	The AP must control CRESET_B with an open-drain output, which requires a 10 kΩ pull-up resistor to VCCIO_2. The 10 kΩ pull-up resistor to AP_VCCIO is required.

JTAG Boundary Scan Port

Overview

Each iCE65 device includes an IEEE 1149.1-compatible JTAG boundary-scan port. The port supports printed-circuit board (PCB) testing and debugging. It also provides an alternate means to configure the iCE65 device.

Signal Connections

The JTAG port connections are listed in Table 32.

***Table 32:* iCE65 JTAG Boundary Scan Signals**

Signal Name	Direction	Description
TDI	Input	Test Data Input. Must be tied off to GND when unused. (no pull-up resistor)*
TMS	Input	Test Mode Select. Must be tied off to GND when unused. (no pull-up resistor)*
TCK	Input	Test Clock. Must be tied off to GND when unused. (no pull-up resistor)*
TDO	Output	Test Data Output.
TRST_B	Input	Test Reset, active Low. Must be Low during normal device operation. Must be High to enable JTAG operations.*

* Must be tied off to GND or VCCIO_1, else VCCIO_1 draws current.

Table 33 lists the ball/pin numbers for the JTAG interface by package code. The JTAG interface is available in select package types. The JTAG port is located in I/O Bank 1 along the right edge of the iCE65 device and powered by the VCCIO_1 supply inputs. Consequently, the JTAG interface uses the associated I/O standards for I/O Bank 1.

***Table 33:* JTAG Interface Ball/Pin Numbers by Package**

JTAG Interface	VQ100	CB132	CB196	CB284
TDI	N/A	M12	M12	T16
TMS		P14	P14	V18
TCK		L12	L12	R16
TDO		N14	N14	U18
TRST_B		M14	M14	T18

Supported JTAG Commands

The JTAG interface supports the IEEE 1149.1 mandatory instructions, including EXTEST, SAMPLE/PRELOAD, and BYPASS.

Package and Pinout Information

Maximum User I/O Pins by Package and by I/O Bank

Table 34 lists the maximum number of user-programmable I/O pins by package, with additional detail showing user I/O pins by I/O bank. In some cases, a smaller iCE65 device is packaged in a larger package with unconnected (N.C.) pins or balls, resulting in fewer overall I/O pins. See Table 35 for device-specific I/O counts by package.

Table 34: **User I/O by Package, by I/O Bank**

	CB81	QN84	VQ100	CB132	CB196	CB284
Package Leads	81	84	100	132	196	284
Package Body (mm)	5 x 5	7 x 7	14 x 14	8 x 8	8 x 8	12 x 12
Ball Array (balls)	9 x 9	N/A	N/A	14 x 14	14 x 14	22 x 22
Ball/Lead Pitch (mm)	0.5	0.5	0.5	0.5	0.5	0.5
Maximum user I/O, all I/O banks	63	67	72	95	150	222
PIO Pins in Bank 0	17	17	19	26	37	60
PIO Pins in Bank 1	16	17	19	21	38	55
PIO Pins in Bank 2	12	11	12	20	35	53
PIO Pins in Bank 3	18	18	18	24	36	50
PIO Pins in SPI Interface	4	4	4	4	4	4

Printed Circuit Board Layout Information

For information on how to use the iCE65 packages on a printed circuit board (PCB) design, consult the following application note.

- AN010: iCE65 Printed Circuit Board (PCB Layout) Guidelines

Maximum User I/O by Device and Package

Table 35 lists the maximum available user I/O by device and by and package type. Not all devices are available in all packages. Similarly, smaller iCE65 devices may have unconnected balls in some packages. Devices sharing a common package have similar footprints.

Table 35: **Maximum User I/O by Device and Package**

Package	Device		
	iCE65L01	**iCE65L04**	**iCE65L08**
CB81	63	—	—
QN84	67	—	—
VQ100	72	72	
CB132	93	95	—
CB196	—	150	150
CB284	—	176	222

Pinout Table

Table 38 provides a detailed pinout table for the QN84 package. Pins are generally arranged by I/O bank, then by ball function. The QN84 package has no JTAG pins.

Table 38: **iCE65 QN84 Chip-scale BGA Pinout Table**

Ball Function	Ball Number	Pin Type	Bank
GBIN0/PIO0	B32	GBIN	0
GBIN1/PIO0	A43	GBIN	0
PIO0	A38	PIO	0
PIO0	A39	PIO	0
PIO0	A40	PIO	0
PIO0	A41	PIO	0
PIO0	A44	PIO	0
PIO0	A45	PIO	0
PIO0	A46	PIO	0
PIO0	A47	PIO	0
PIO0	A48	PIO	0
PIO0	B29	PIO	0
PIO0	B30	PIO	0
PIO0	B31	PIO	0
PIO0	B34	PIO	0
PIO0	B35	PIO	0
PIO0	B36	PIO	0
VCCIO_0	A42	VCCIO	0
GBIN2/PIO1	B22	GBIN	1
GBIN3/PIO1	A29	GBIN	1
PIO1	A25	PIO	1
PIO1	A26	PIO	1
PIO1	A27	PIO	1
PIO1	A31	PIO	1
PIO1	A32	PIO	1
PIO1	A33	PIO	1
PIO1	A34	PIO	1
PIO1	A35	PIO	1
PIO1	B19	PIO	1
PIO1	B20	PIO	1
PIO1	B21	PIO	1
PIO1	B23	PIO	1
PIO1	B24	PIO	1
PIO1	B26	PIO	1
PIO1	B27	PIO	1
VCCIO_1	B25	VCCIO	1
CDONE	B16	CONFIG	2
CRESET_B	A21	CONFIG	2
GBIN4/PIO2	A14	GBIN	2
GBIN5/PIO2	A16	GBIN	2
PIO2	A13	PIO	2
PIO2	B12	PIO	2
PIO2	A19	PIO	2
PIO2	B10	PIO	2
PIO2	B11	PIO	2
PIO2	B13	PIO	2

Figure 43: **iCE65L08 CB132 Chip-Scale BGA Footprint (Top View)**

I/O Bank 0

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	PIO0	PIO0	PIO0	PIO0	PIO0	GBIN0/ PIO0	GBIN1/ PIO0	VCCIO_0	GND	PIO0	PIO0	PIO0	VPP_ FAST	VPP_ 2V5	A
B	PIO3/ DP00A													PIO1	B
C	PIO3/ DP00B		PIO3/ DP01A	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0		PIO1	C
D	PIO3/ DP03A		PIO3/ DP01B	PIO3/ DP02A	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0	PIO0	PIO1		PIO1	D
E	PIO3/ DP03B		VCCIO_3	PIO3/ DP02B							PIO1	PIO1		PIO1	E
F	GND		PIO3/ DP04B	PIO3/ DP04A		VCCIO_0	GND	VCC	VCCIO_1		PIO1	PIO1		GBIN3/ PIO1	F
G	GBIN7/ DP05B		PIO3/ DP05A	PIO3/ DP11B		VCC	GND	GND	GND		PIO1	PIO1		GBIN2/ PIO1	G
H	GBIN6/ DP06A		PIO3/ DP06B	PIO3/ DP11A		GND	GND	GND	VCC		PIO1	PIO1		VCCIO_1	H
J	PIO3/ DP07B		PIO3/ DP07A	VCC		VCCIO_3	VCC	GND	VCCIO_2		PIO1	PIO1		GND	J
K	VCCIO_3		PIO3/ DP08A	PIO3/ DP08B							PIO1	PIO1		PIO1	K
L	PIO3/ DP09A		GND	PIO2	PIO2	PIO2	PIO2	PIO2	PIO2/ CBSEL0	CRESET_B	SPI_ VCC	TCK		PIO1	L
M	PIO3/ DP09B		PIO2	PIO2	VCCIO_2	PIO2	PIO2	PIO2	PIO2	CDONE	PIOS/ SPI_SO	TDI		TRST_B	M
N	PIO3/ DP10A													TDO	N
P	PIO3/ DP10B	PIO2	PIO2	PIO2	PIO2	GND	GBIN5/ PIO2	GBIN4/ PIO2	PIO2	PIO2/ CBSEL1	PIOS/ SPI_SI	PIOS/ SPI_SCK	PIOS/ SPI_SS_B	TMS	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

I/O Bank 3 (left) · I/O Bank 1 (right) · SPI Bank

I/O Bank 2

Pinout Table

Table 41 provides a detailed pinout table for the CB132 package. Pins are generally arranged by I/O bank, then by ball function. The table also highlights the differential I/O pairs in I/O Bank 3.

Table 41: iCE65 CB132 Chip-scale BGA Pinout Table

Ball Function	Ball Number	Pin Type	Bank
GBIN0/PIO0	iCE65L01: A7 iCE65L04/L08: A6	GBIN	0
GBIN1/PIO0	iCE65L01: A6 iCE65L04/08: A7	GBIN	0
PIO0	A1	PIO	0
PIO0	A2	PIO	0
iCE65L01: (NC) iCE65L04/L08: PIO0	A3	iCE65L01: (NC) iCE65L04: PIO0	0
PIO0	A4	PIO	0
PIO0	A5	PIO	0
PIO0	A10	PIO	0
iCE65L01: (NC) iCE65L04/L08: PIO0	A11	iCE65L01: (NC) iCE65L04: PIO0	0
PIO0	A12	PIO	0
PIO0	C10	PIO	0
PIO0	C11	PIO	0
PIO0	C12	PIO	0
PIO0	C4	PIO	0
PIO0	C5	PIO	0
PIO0	C6	PIO	0
PIO0	C7	PIO	0
PIO0	C8	PIO	0
PIO0	C9	PIO	0
PIO0	D5	PIO	0
PIO0	D6	PIO	0
PIO0	D7	PIO	0
PIO0	D8	PIO	0
PIO0	D9	PIO	0
PIO0	D10	PIO	0
PIO0	D11	PIO	0
VCCIO_0	A8	VCCIO	0
VCCIO_0	F6	VCCIO	0
GBIN2/PIO1	G14	GBIN	1
GBIN3/PIO1	F14	GBIN	1
PIO1	B14	PIO	1
PIO1	C14	PIO	1
PIO1	D12	PIO	1
PIO1	D14	PIO	1
PIO1	E11	PIO	1
PIO1	E12	PIO	1
PIO1	E14	PIO	1
PIO1	F11	PIO	1
PIO1	F12	PIO	1
PIO1	G11	PIO	1
PIO1	G12	PIO	1
PIO1	H11	PIO	1

Pinout Table

Table 44 provides a detailed pinout table for the two chip-scale BGA packages. Pins are generally arranged by I/O bank, then by ball function. The balls with a black circle (●) are unconnected balls (N.C.) for the iCE65L04 in the CB284 package. The CB132 package fits within the CB284 package footprint as shown in Figure 48. The right-most column shows which CB132 ball corresponds to the CB284.

The table also highlights the differential I/O pairs in I/O Bank 3.

Table 44: iCE65 CB284 Chip-scale BGA Pinout Table (with CB132 cross reference)

Ball Function	Ball Number iCE65L04 iCE65L08	Pin Type by Device iCE65L04	Pin Type by Device iCE65L08	Bank	CB132 Ball Equivalent
GBIN0/PIO0	E10	GBIN	GBIN	0	A6
GBIN1/PIO0	E11	GBIN	GBIN	0	A7
PIO0 (●)	A1	N.C.	PIO	0	—
PIO0 (●)	A2	N.C.	PIO	0	—
PIO0 (●)	A3	N.C.	PIO	0	—
PIO0 (●)	A4	N.C.	PIO	0	—
PIO0	A5	PIO	PIO	0	—
PIO0	A6	PIO	PIO	0	—
PIO0	A7	PIO	PIO	0	—
PIO0 (●)	A9	N.C.	PIO	0	—
PIO0 (●)	A10	N.C.	PIO	0	—
PIO0 (●)	A11	N.C.	PIO	0	—
PIO0 (●)	A12	N.C.	PIO	0	—
PIO0 (●)	A13	N.C.	PIO	0	—
PIO0	A15	PIO	PIO	0	—
PIO0	A16	PIO	PIO	0	—
PIO0	A17	PIO	PIO	0	—
PIO0	A18	PIO	PIO	0	—
PIO0 (●)	A14	N.C.	PIO	0	—
PIO0 (●)	A19	N.C.	PIO	0	—
PIO0 (●)	A20	N.C.	PIO	0	—
PIO0	C3	PIO	PIO	0	—
PIO0	C4	PIO	PIO	0	—
PIO0	C5	PIO	PIO	0	—
PIO0	C6	PIO	PIO	0	—
PIO0	C7	PIO	PIO	0	—
PIO0	C9	PIO	PIO	0	—
PIO0	C10	PIO	PIO	0	—
PIO0	C11	PIO	PIO	0	—
PIO0	C13	PIO	PIO	0	—
PIO0	C14	PIO	PIO	0	—
PIO0	C15	PIO	PIO	0	—
PIO0	C16	PIO	PIO	0	—
PIO0	C17	PIO	PIO	0	—
PIO0	C18	PIO	PIO	0	—
PIO0	C19	PIO	PIO	0	—
PIO0	E5	PIO	PIO	0	A1
PIO0	E6	PIO	PIO	0	A2
PIO0	E7	PIO	PIO	0	A3
PIO0	E8	PIO	PIO	0	A4
PIO0	E9	PIO	PIO	0	A5
PIO0	E14	PIO	PIO	0	A10

Ball Function	Ball Number	Pin Type by Device		Bank	CB132 Ball Equivalent
	iCE65L04 iCE65L08	iCE65L04	iCE65L08		
PIO1	L15	PIO	PIO	1	G11
PIO1	L16	PIO	PIO	1	G12
PIO1 (●)	L22	N.C.	PIO	1	—
PIO1	M15	PIO	PIO	1	H11
PIO1	M16	PIO	PIO	1	H12
PIO1	M20	PIO	PIO	1	—
PIO1 (●)	M22	N.C.	PIO	1	—
PIO1	N15	PIO	PIO	1	J11
PIO1	N16	PIO	PIO	1	J12
PIO1	N22	PIO	PIO	1	—
PIO1	P15	PIO	PIO	1	K11
PIO1	P16	PIO	PIO	1	K12
PIO1	P18	PIO	PIO	1	K14
PIO1	P20	PIO	PIO	1	—
PIO1	P22	PIO	PIO	1	—
PIO1	R18	PIO	PIO	1	L14
PIO1	R20	PIO	PIO	1	—
PIO1	R22	PIO	PIO	1	—
PIO1	T20	PIO	PIO	1	—
PIO1	T22	PIO	PIO	1	—
PIO1	U20	PIO	PIO	1	—
PIO1 (●)	U22	N.C.	PIO	1	—
PIO1	V20	PIO	PIO	1	—
PIO1 (●)	V22	N.C.	PIO	1	—
PIO1	W20	PIO	PIO	1	—
PIO1 (●)	W22	N.C.	PIO	1	—
PIO1 (●)	Y22	N.C.	PIO	1	—
TCK	R16	JTAG	JTAG	1	L12
TDI	T16	JTAG	JTAG	1	M12
TDO	U18	JTAG	JTAG	1	N14
TMS	V18	JTAG	JTAG	1	P14
TRST_B	T18	JTAG	JTAG	1	M14
VCCIO_1	H22	VCCIO	VCCIO	1	—
VCCIO_1	J20	VCCIO	VCCIO	1	—
VCCIO_1	K13	VCCIO	VCCIO	1	F9
VCCIO_1	M18	VCCIO	VCCIO	1	H14
CDONE	T14	CONFIG	CONFIG	2	M10
CRESET_B	R14	CONFIG	CONFIG	2	L10
GBIN4/PIO2	V12	GBIN	GBIN	2	P7
GBIN5/PIO2	V11	GBIN	GBIN	2	P8
PIO2	R8	PIO	PIO	2	L4
PIO2	R9	PIO	PIO	2	L5
PIO2	R10	PIO	PIO	2	L6
PIO2	R11	PIO	PIO	2	L7
PIO2	R12	PIO	PIO	2	L8
PIO2	T7	PIO	PIO	2	M3
PIO2	T8	PIO	PIO	2	M4
PIO2	T10	PIO	PIO	2	M6
PIO2	T11	PIO	PIO	2	M7
PIO2	T12	PIO	PIO	2	M8

Ball Function	Ball Number iCE65L04 iCE65L08	Pin Type by Device iCE65L04	iCE65L08	Bank	CB132 Ball Equivalent
VCCIO_3	J7	VCCIO	VCCIO	3	E3
VCCIO_3	K3	VCCIO	VCCIO	3	—
VCCIO_3	N10	VCCIO	VCCIO	3	J6
VCCIO_3	P5	VCCIO	VCCIO	3	K1
VCCIO_3	R3	VCCIO	VCCIO	3	—
VREF	M1	VREF	VREF	3	—
PIOS/SPI_SO	T15	SPI	SPI	SPI	M11
PIOS/SPI_SI	V15	SPI	SPI	SPI	P11
PIOS/SPI_SCK	V16	SPI	SPI	SPI	P12
PIOS/SPI_SS_B	V17	SPI	SPI	SPI	P13
SPI_VCC	R15	SPI	SPI	SPI	L11
GND	C12	GND	GND	GND	—
GND	E13	GND	GND	GND	A9
GND	J3	GND	GND	GND	—
GND	K5	GND	GND	GND	F1
GND	K11	GND	GND	GND	F7
GND	L11	GND	GND	GND	G7
GND	L12	GND	GND	GND	G8
GND	L13	GND	GND	GND	G9
GND	M10	GND	GND	GND	H6
GND	M11	GND	GND	GND	H7
GND	M12	GND	GND	GND	H8
GND	N1	GND	GND	GND	—
GND	N12	GND	GND	GND	J8
GND	N18	GND	GND	GND	J14
GND	N20	GND	GND	GND	—
GND	R7	GND	GND	GND	L3
GND	T3	GND	GND	GND	—
GND	V1	GND	GND	GND	—
GND	V10	GND	GND	GND	P6
GND	Y12	GND	GND	GND	—
GND	Y16	GND	GND	GND	—
GND	AB5	GND	GND	GND	—
GND	G1	GND	GND	GND	—
GND	R1	GND	GND	GND	—
VCC	C8	VCC	VCC	VCC	—
VCC	D3	VCC	VCC	VCC	—
VCC	K12	VCC	VCC	VCC	F8
VCC	L10	VCC	VCC	VCC	G6
VCC	L20	VCC	VCC	VCC	—
VCC	M13	VCC	VCC	VCC	H9
VCC	N8	VCC	VCC	VCC	J4
VCC	N11	VCC	VCC	VCC	J7
VCC	Y8	VCC	VCC	VCC	—
VPP_2V5	E18	VPP	VPP	VPP	A14
VPP_FAST	E17	VPP	VPP	VPP	A13

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO2_28	—	Y13	132	2,062.5	139.5
GBIN5/PIO2_29	M7	V11	133	2,097.5	37.5
GBIN4/PIO2_30	N8	V12	134	2,132.5	139.5
GND	J8	Y12	135	2,167.5	37.5
GND	—	—	136	2,202.5	139.5
PIO2_31	P8	Y14	137	2,237.5	37.5
PIO2_32	—	AB15	138	2,272.5	139.5
PIO2_33	M8	V13	139	2,307.5	37.5
PIO2_34	—	AB16	140	2,342.5	139.5
PIO2_35	L8	Y15	141	2,377.5	37.5
PIO2_36	—	AB17	142	2,412.5	139.5
PIO2_37	N9	AB18	143	2,447.5	37.5
PIO2_38	—	AB19	144	2,482.5	139.5
PIO2_39	—	AB20	145	2,517.5	37.5
PIO2_40	—	AB21	146	2,552.5	139.5
PIO2_41	—	Y17	147	2,587.5	37.5
PIO2_42	—	AB22	148	2,622.5	139.5
PIO2_43	—	Y18	149	2,657.5	37.5
PIO2_44	P9	Y19	150	2,692.5	139.5
VCC	N7	N11	151	2,727.5	37.5
VCC	—	—	152	2,762.5	139.5
PIO2_45	M9	Y20	153	2,797.5	37.5
PIO2_46	K8	T11	154	2,832.5	139.5
VCCIO_2	J9	N13	155	2,867.5	37.5
VCCIO_2	—	—	156	2,902.5	139.5
PIO2_47	N11	R11	157	2,937.5	37.5
GND	J8	M12	158	2,972.5	139.5
GND	—	—	159	3,007.5	37.5
PIO2_48	N12	T12	160	3,042.5	139.5
PIO2_49	K9	R12	161	3,077.5	37.5
PIO2_50	N13	T13	162	3,112.5	139.5
PIO2_51/CBSEL0	L9	R13	163	3,147.5	37.5
PIO2_52/CBSEL1	P10	V14	164	3,182.5	139.5
CDONE	M10	T14	165	3,217.5	37.5
CRESET_B	L10	R14	166	3,260.0	139.5
PIOS_00/SPI_SO	M11	T15	167	3,320.0	37.5
PIOS_01/SPI_SI	P11	V15	168	3,370.0	139.5
GND	J8	Y16	169	3,420.0	37.5
GND	—	—	170	3,470.0	139.5
PIOS_02/SPI_SCK	P12	V16	171	3,520.0	37.5
PIOS_03/SPI_SS_B	P13	V17	172	3,570.0	139.5
VCC	—	—	173	3,620.0	37.5
VCC	—	—	174	3,670.0	139.5
SPI_VCC	L11	R15	175	3,720.0	37.5
SPI_VCC	—	—	176	3,770.0	139.5

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
TDI	M12	T16	177	4,470.5	634.615
TMS	P14	V18	178	4,572.5	684.615
TCK	L12	R16	179	4,470.5	734.615
TDO	N14	U18	180	4,572.5	784.615
TRST_B	M14	T18	181	4,470.5	834.615
PIO1_00	M13	R18	182	4,572.5	884.615
PIO1_01	K11	P16	183	4,470.5	934.615
PIO1_02	L13	P15	184	4,572.5	984.615
PIO1_03	L14	P18	185	4,470.5	1,034.615
GND	G9	N18	186	4,572.5	1,084.615
GND	—	—	187	4,470.5	1,134.615
PIO1_04	J11	N16	188	4,572.5	1,184.615
PIO1_05	K12	N15	189	4,470.5	1,234.62
VCCIO_1	F9	M18	190	4,572.5	1,287.115
VCCIO_1	—	—	191	4,470.5	1,322.115
PIO1_06	J12	M15	192	4,572.5	1,357.115
PIO1_07	K14	M16	193	4,470.5	1,392.115
PIO1_08	—	T20	194	4,572.5	1,427.115
PIO1_09	—	W20	195	4,470.5	1,462.115
PIO1_10	—	V20	196	4,572.5	1,497.115
VCC	H9	M13	197	4,470.5	1,532.115
VCC	—	—	198	4,572.5	1,567.115
PIO1_11	—	R20	199	4,470.5	1,602.115
PIO1_12	—	Y22	200	4,572.5	1,637.115
PIO1_13	—	AA22	201	4,470.5	1,672.115
PIO1_14	—	U20	202	4,572.5	1,707.115
PIO1_15	J13	W22	203	4,470.5	1,742.115
PIO1_16	H11	P20	204	4,572.5	1,777.115
PIO1_17	J10	V22	205	4,470.5	1,812.115
PIO1_18	H12	U22	206	4,572.5	1,847.115
GND	K10	N20	207	4,470.5	1,882.115
GND	—	—	208	4,572.5	1,917.110
PIO1_19	H13	T22	209	4,470.5	1,952.115
PIO1_20	—	M20	210	4,572.5	1,987.115
PIO1_21	H10	R22	211	4,470.5	2,022.115
PIO1_22	—	P22	212	4,572.5	2,057.115
VCCIO_1	F9	J20	213	4,470.5	2,092.115
VCCIO_1	—	—	214	4,572.5	2,127.115
PIO1_23	G10	M22	215	4,470.5	2,162.115
PIO1_24	G11	N22	216	4,572.5	2,197.115
PIO1_25	—	K22	217	4,470.5	2,232.115
PIO1_26	—	L22	218	4,572.5	2,267.115
GBIN3/PIO1_27	G12	K18	219	4,470.5	2,302.11
GBIN2/PIO1_28	F10	L18	220	4,572.5	2,337.115
PIO1_29	—	J22	221	4,470.5	2,372.115

I/O Banks 0, 1, 2 and SPI Bank Characteristic Curves

Figure 52: **Typical LVCMOS Output Low Characteristics (I/O Banks 0, 1, 2, and SPI)**

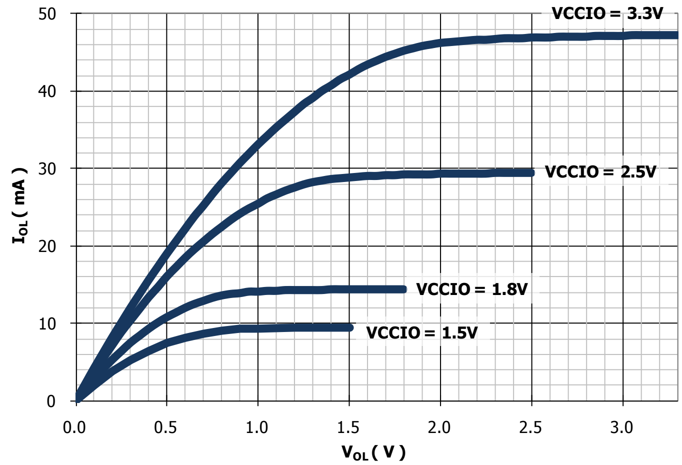


Figure 53: **Typical LVCMOS Output High Characteristics (I/O Banks 0, 1, 2, and SPI)**

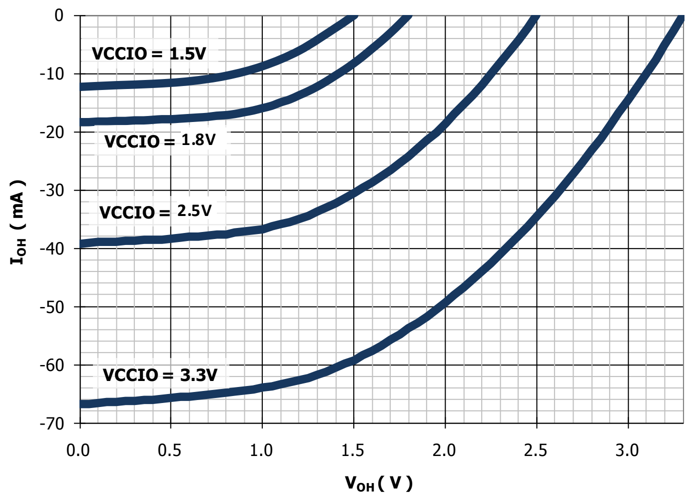
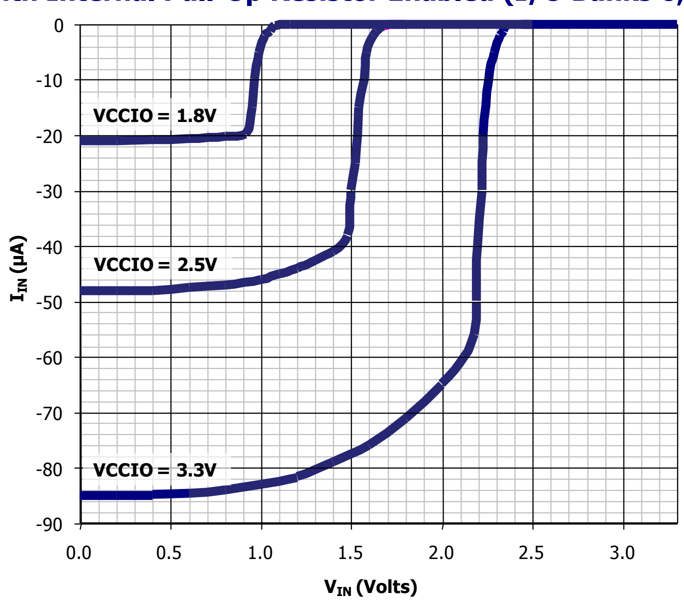


Figure 54: **Input with Internal Pull-Up Resistor Enabled (I/O Banks 0, 1, 2, and SPI)**



RAM4K Block

Table 56 provides timing information for the logic in a RAM4K block, which includes the paths shown in Figure 59.

Figure 59: RAM4K Timing Circuit

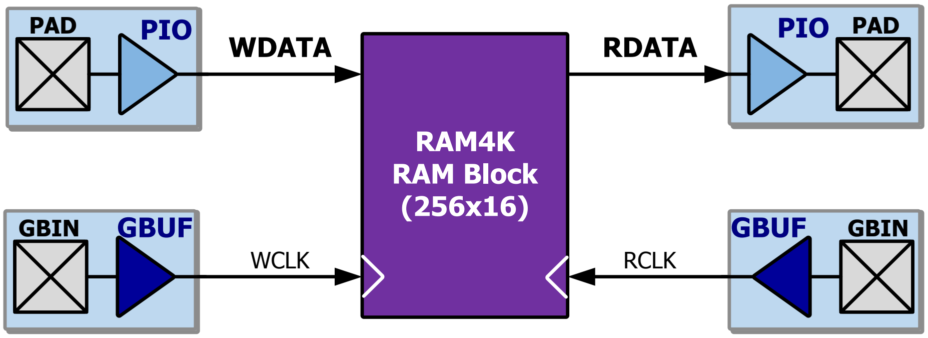


Table 56: Typical RAM4K Block Timing

			Device: iCE65	L01	L04, L08			
			Power/Speed Grade	–T	–L	–L	–T	
			Nominal VCC	1.2 V	1.0 V	1.2 V	1.2 V	
Symbol	**From**	**To**	**Description**	**Typ.**	**Typ.**	**Typ.**	**Typ.**	**Units**
Write Setup/Hold Time								
t_{SUWD}	PIO input	GBIN input	Minimum write data setup time on PIO inputs before active clock edge on GBIN input, include interconnect delay.	0.6	3.1	1.7	0.8	ns
t_{HDWD}	GBIN input	PIO input	Minimum write data hold time on PIO inputs after active clock edge on GBIN input, including interconnect delay.	0	0	0	0	ns
Read Clock-Output-Time								
t_{CKORD}	RCLK clock input	PIO output	Clock-to-output delay from RCLK input pin, through RAM4K RDATA output flip-flop to PIO output pad, including interconnect delay.	5.6	17.1	9.1	7.3	ns
t_{GBCKRM}	GBIN input	RCLK clock input	Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to the RCLK clock input.	2.1	7.3	3.8	2.6	ns
Write and Read Clock Characteristics								
t_{RMWCKH}	WCLK RCLK	WCLK RCLK	Write clock High time	0.54	1.14	0.54	0.54	ns
t_{RMWCKL}			Write clock Low time	0.63	1.32	0.63	0.63	ns
t_{RMWCYC}			Write clock cycle time	1.27	2.64	1.27	1.27	ns
F_{WMAX}			Sustained write clock frequency	256	256	256	256	MHz

Notes