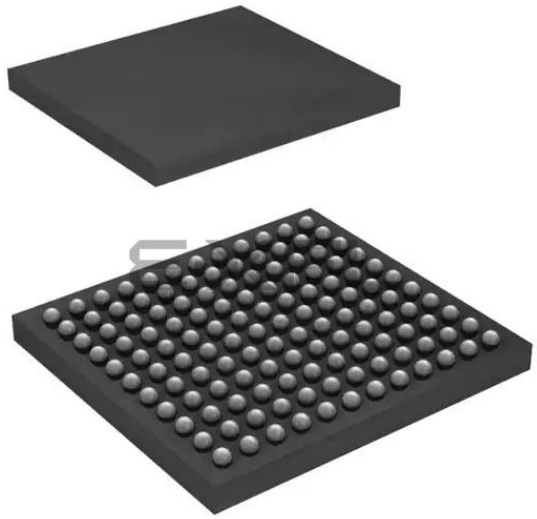
Lattice Semiconductor Corporation - ICE65L08F-TCB132C Datasheet



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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	960
Number of Logic Elements/Cells	7680
Total RAM Bits	131072
Number of I/O	95
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	132-VFBGA, CSPBGA
Supplier Device Package	132-CSBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice65l08f-tcb132c

Overview

The Lattice Semiconductor iCE65 programmable logic family is specifically designed to deliver the lowest static and dynamic power consumption of any comparable CPLD or FPGA device. iCE65 devices are designed for cost-sensitive, high-volume applications and provide on-chip, nonvolatile configuration memory (NVCM) to customize for a specific application. iCE65 devices can self-configure from a configuration image stored in an external commodity SPI serial Flash PROM or be downloaded from an external processor over an SPI-like serial port.

The three iCE65 components, highlighted in Table 1, deliver from approximately 1K to nearly 8K logic cells and flip-flops while consuming a fraction of the power of comparable programmable logic devices. Each iCE65 device includes between 16 to 32 RAM blocks, each with 4Kbits of storage, for on-chip data storage and data buffering.

As pictured in Figure 1, each iCE65 device consists of four primary architectural elements.

- An array of Programmable Logic Blocks (PLBs)
  - Each PLB contains eight Logic Cells (LCs); each Logic Cell consists of ...
    - A fast, four-input look-up table (LUT4) capable of implementing any combinational logic function of up to four inputs, regardless of complexity
    - A 'D'-type flip-flop with an optional clock-enable and set/reset control
    - Fast carry logic to accelerate arithmetic functions such as adders, subtracters, comparators, and counters.
  - Common clock input with polarity control, clock-enable input, and optional set/reset control input to the PLB is shared among all eight Logic Cells
- Two-port, 4Kbit RAM blocks (RAM4K)
  - 256x16 default configuration; selectable data width using programmable logic resources
  - Simultaneous read and write access; ideal for FIFO memory and data buffering applications
  - RAM contents pre-loadable during configuration
- Four I/O banks with independent supply voltage, each with multiple Programmable Input/Output (PIO) blocks
  - LVCMOS I/O standards and LVDS outputs supported in all banks
  - I/O Bank 3 supports additional SSTL, MDDR, LVDS, and SubLVDS I/O standards
- Programmable interconnections between the blocks
  - Flexible connections between all programmable logic functions
  - Eight dedicated low-skew, high-fanout clock distribution networks

Packaging Options

iCE65 components are available in a variety of package options to support specific application requirements. The available options, including the number of available user-programmable I/O pins (PIOs), are listed in Table 2. Fully-tested Known-Good Die (KGD) DiePlus™ are available for die stacking and highly space-conscious applications. All iCE65 devices are provided exclusively in Pb-free, RoHS-compliant packages.

Table 2: **iCE65 Family Packaging Options, Maximum I/O per Package**

Package	Package Body (mm)	Package Code	Ball/Lead Pitch (mm)	65L01	65L04	65L08
81-ball chip-scale BGA	5 x 5	CB81	0.5	63 *(0)*	—	—
84-pin quad flat no-lead package	7 x 7	QN84	0.5	67 *(0)*	—	—
100-pin very thin quad flat package	14 x 14	VQ100	0.5	72 *(0)* ⟺	72 *(9)*	—
121-ball chip-scale BGA	6 x 6	CB121	0.5	92 *(0)*	—	—
132-ball chip-scale BGA	8 x 8	CB132		93 *(0)* ⇔	95 *(11)* ⇔	95 *(12)*
196-ball chip-scale BGA	8 x 8	CB196		—	150 *(18)* ⇔	150 *(18)*
284-ball chip-scale BGA	12 x 12	CB284		—	176 *(20)* ⟺	222 *(25)*
Known Good Die	See DiePlus data sheet	DI	—	95 *(0)*	176 *(20)*	222 *(25)*

⟺ = Common footprint allows each density migration on the same printed circuit board. *(Differential input count)*.

The iCE65L04 and the iCE65L08 are both available in the CB196 package and have similar footprints but are not completely pin compatible. See "Pinout Differences between iCE65L04 and iCE65L08 in CB196 Package" on page 73 for more information.

When iCE65 components are supplied in the same package style, devices of different gate densities share a common footprint. The common footprint improves manufacturing flexibility. Different models of the same product can share a common circuit board. Feature-rich versions of the end application mount a larger iCE65 device on the circuit board. Low-end versions mount a smaller iCE65 device.

Implementing Subtracters, Decrementers

As mentioned earlier, the Carry Logic generates a High output whenever the sum of `I1 + I2 + CARRY_IN` generates a carry. The Carry Logic does not specifically have a subtract mode. To implement a subtract function or decrement function, logically invert either the I1 or I2 input and invert the initial carry input. This performs a 2s complement subtract operation.

Figure 6: Two-bit Adder Example

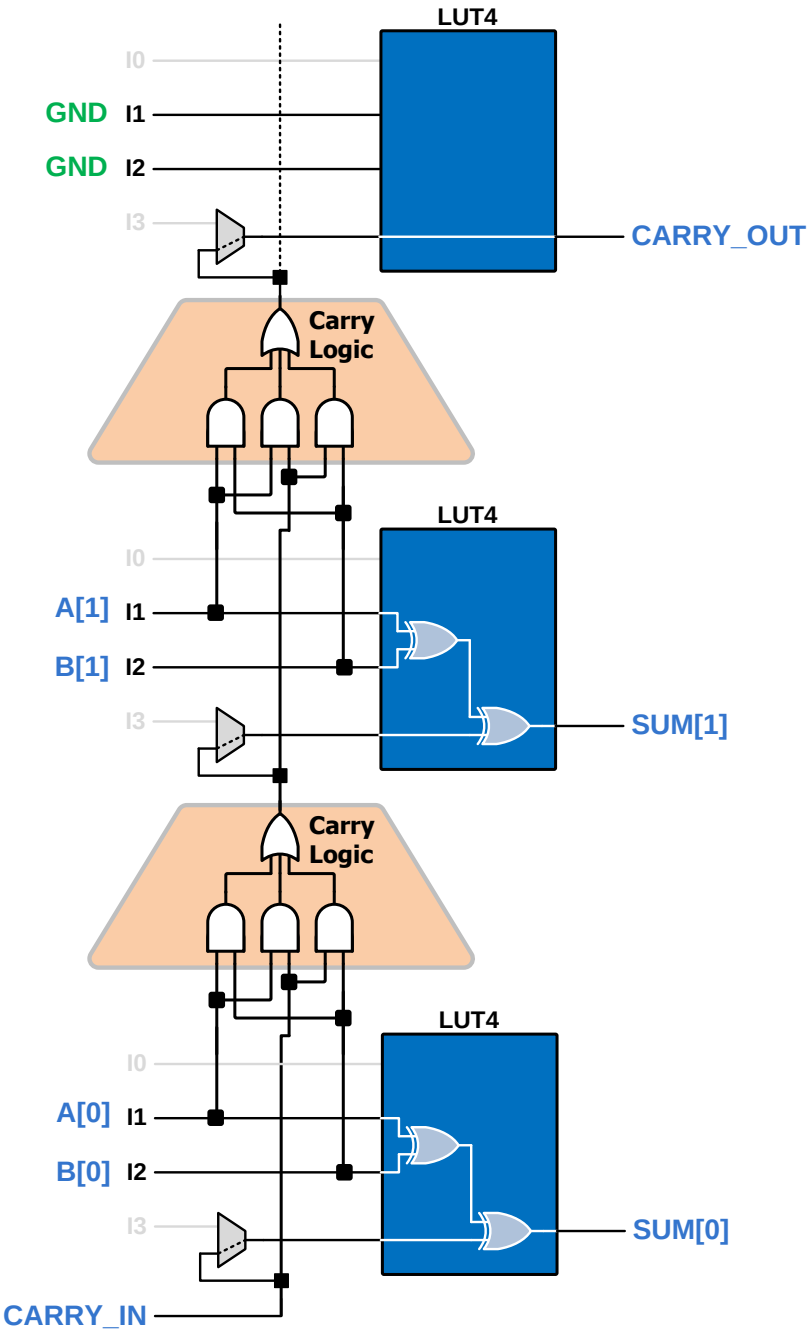
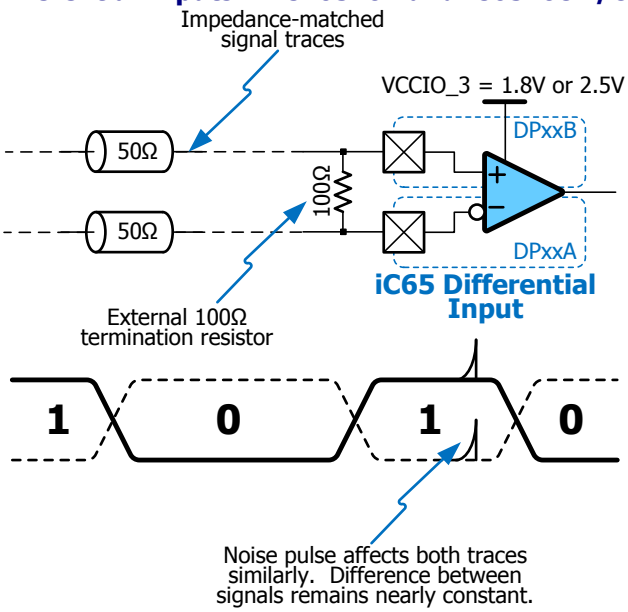


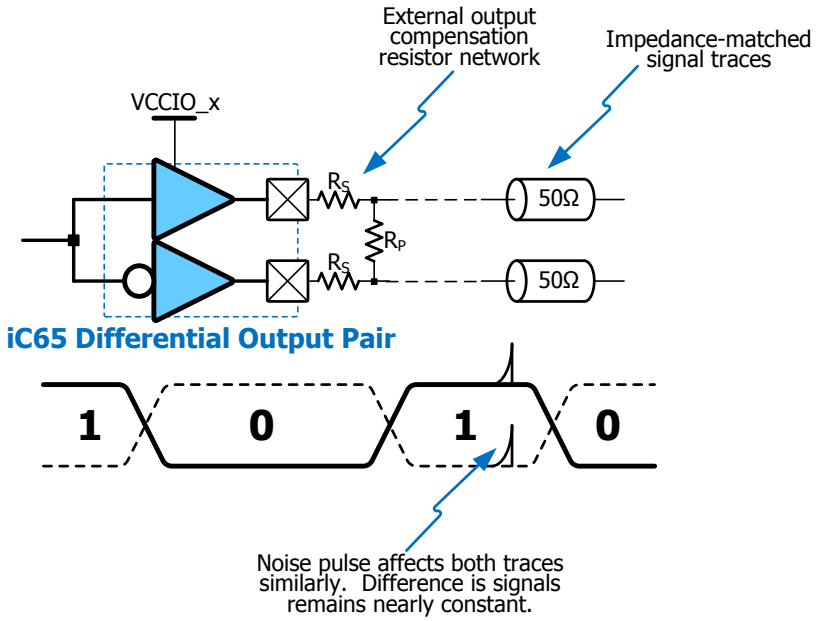
Figure 8: **Differential Inputs in iCE65L04 and iC65L08 I/O Bank 3**



Differential Outputs in Any Bank

Differential outputs are built using a pair of single-ended PIO pins as shown in Figure 9. Each differential I/O pair requires a three-resistor termination network to adjust output characteristic to match those for the specific differential I/O standard. The output characteristics depend on the values of the parallel resistors (RP) and series resistor (RS). Differential outputs must be located in the same I/O tile.

Figure 9: Differential Output Pair



For electrical characteristics, see "Differential Outputs" on page 100.

The PIO pins that make up a differential output pair are indicated with a blue bounding box in the in the tables in "Die Cross Reference" starting on page 84.

Figure 21: iCE65 Configuration Control Pins

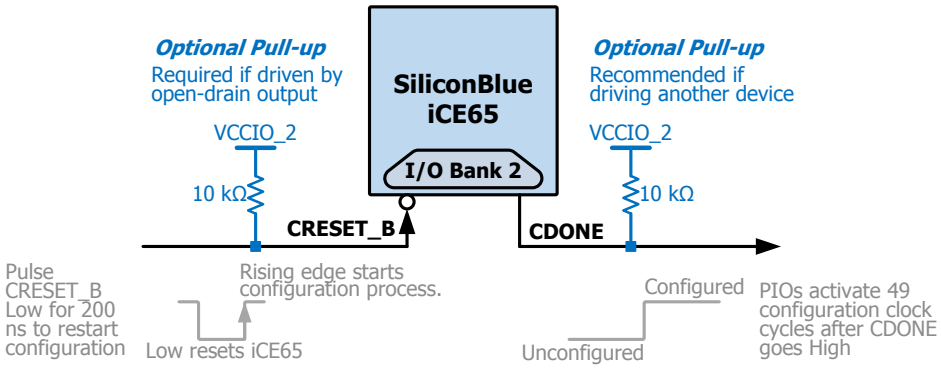


Figure 21 shows the two iCE65 configuration control pins, CRESET_B and CDONE. Table 23 lists the ball/pin numbers for the configuration control pins by package. When driven Low for at least 200 ns, the dedicated Configuration Reset input, CRESET_B, resets the iCE65 device. When CRESET_B returns High, the iCE65 FPGA restarts the configuration process from its power-on conditions (Cold Boot). The CRESET_B pin is a pure input with no internal pull-up resistor. If driven by open-drain driver or un-driven, then connect the CRESET_B pin to a 10 kΩ pull-up resistor connected to the VCCIO_2 supply.

***Table 23:* Configuration Control Ball/Pin Numbers by Package**

Configuration Control Pins	CB81	QN84	VQ100	CB132	CB196	CB284
CRESET_B	J6	A21	44	L10	L10	R14
CDONE	H6	B16	43	M10	M10	T14

The iCE65 device signals the end of the configuration process by actively turning off the internal pull-down transistor on the Configuration Done output pin, CDONE. The pin has a permanent, weak internal pull-up resistor to the VCCIO_2 rail. If the iCE65 device drives other devices, then optionally connect the CDONE pin to a 10 kΩ pull-up resistor connected to the VCCIO_2 supply.

The PIO pins activate according to their configured function after 49 configuration clock cycles. The internal oscillator is the configuration clock source for the SPI Master Configuration Interface and when configuring from

* Note: only 14 of the 16 RAM4K Memory Blocks may be pre-initialized in the iCE65L01.

Nonvolatile Configuration Memory (NVCM). When using the SPI Peripheral Configuration Interface, the configuration clock source is the SPI_SCK clock input pin.

Internal Oscillator

During SPI Master or NVCM configuration mode, the controlling clock signal is generated from an internal oscillator. The oscillator starts operating at the Default frequency. During the configuration process, however, bit settings within the configuration bitstream can specify a higher-frequency mode in order to maximize SPI bandwidth and reduce overall configuration time. See Table 57: Internal Oscillator Frequency on page 105 for the specified oscillator frequency range.

Using the SPI Master Configuration Interface, internal oscillator controls all the interface timing and clocks the SPI serial Flash PROM via the SPI_SCK clock output pin.

The oscillator output, which also supplies the SPI SCK clock output during the SPI Flash configuration process, has a 50% duty cycle.

Internal Device Reset

Figure 22 presents the various signals that internally reset the iCE65 internal logic.

- Power-On Reset (POR)
- CRESET_B Pin
- JTAG Interface

- For lowest possible power consumption after configuration, the PROM should also support the 0xB9 Deep Power Down command and the 0xAB Release from Deep Power-down Command (see Figure 24 and Figure 26). The low-power mode is optional.
- The PROM must be ready to accept commands 10 µs after meeting its power-on conditions. In the PROM data sheet, this may be specified as t_{VSL} or t_{VCSL}. It is possible to use slower PROMs by holding the CRESET_B input Low until the PROM is ready, then releasing CRESET_B, either under program control or using an external power-on reset circuit.

The Lattice iCEman65 development board and associated programming software uses an ST Micro/Numonyx M25Pxx SPI serial Flash PROM.

SPI PROM Size Requirements

Table 27 lists the minimum SPI PROM size required to configure an iCE65 device. Larger PROM sizes are allowed, but not required unless the end application uses the additional space. SPI serial PROM sizes are specified in bits. For each device size, the table shows the required minimum PROM size for "Logic Only" (no BRAM initialization) and "Logic + RAM4K" (RAM4K blocks pre-initialized). Furthermore, the table shows the PROM size for varying numbers of configuration images. Most applications will use a single image. Applications that use the Cold Boot or Warm Boot features may use more than one image.

Table 27: Smallest SPI PROM Size (bits), by Device, by Number of Images

Device	1 Image		2 Images		3 Images		4 Images	
	Logic Only	**Logic + RAM4K**	**Logic Only**	**Logic + RAM4K**	**Logic Only**	**Logic + RAM4K**	**Logic Only**	**Logic + RAM4K**
iCE65L01	256K	256K	512K	512K	1M	1M	1M	1M
iCE65L04	512K	1M	1M	2M	2M	2M	2M	4M
iCE65L08	1M	2M	2M	4M	4M	4M	4M	8M

Enabling SPI Configuration Interface

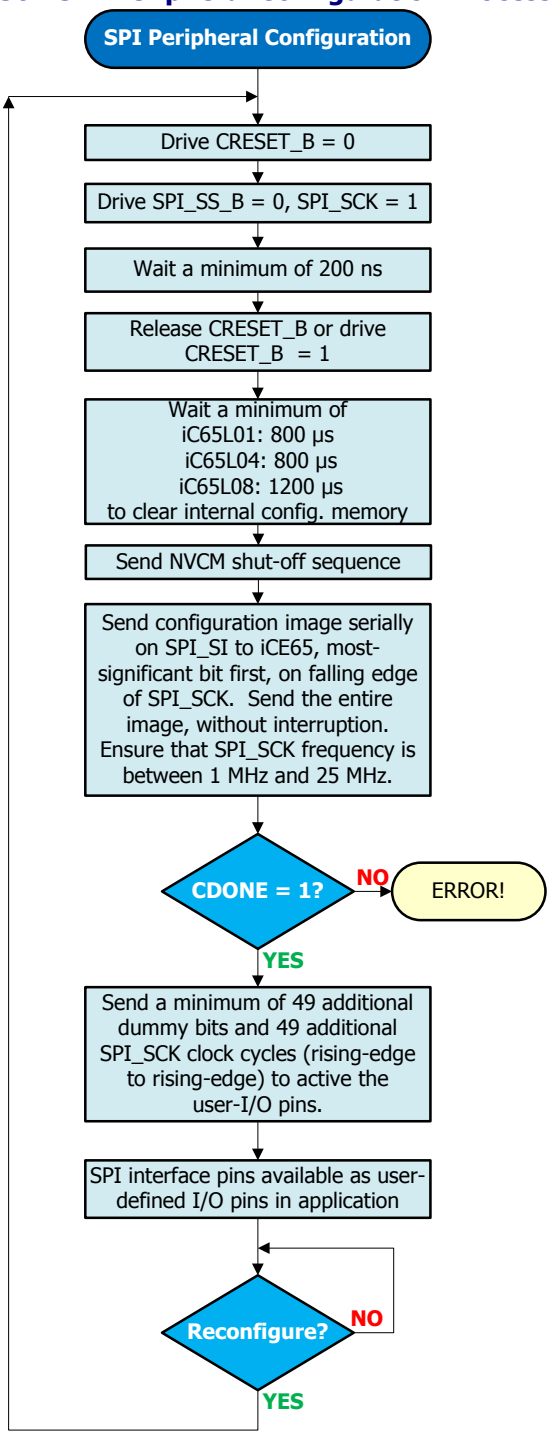
To enable the SPI configuration mode, the SPI_SS_B pin must be allowed to float High. The SPI_SS_B pin has an internal pull-up resistor. If SPI_SS_B is Low, then the iCE65 component defaults to the SPI Slave configuration mode.

SPI Master Configuration Process

The iCE65 SPI Master Configuration Interface supports a variety of modern, high-density, low-cost SPI serial Flash PROMs. Most modern SPI PROMs include a power-saving Deep Power-down mode. The iCE65 component exploits this mode for additional system power savings.

The iCE65 SPI interface starts by driving SPI_SS_B Low, and then sends a Release from Power-down command to the SPI PROM, hexadecimal command code 0xAB. Figure 24 provides an example waveform. This initial command wakes up the SPI PROM if it is already in Deep Power-down mode. If the PROM is not in Deep Power-down mode, the extra command has no adverse affect other than that it requires a few additional microseconds during the configuration process. The iCE65 device transmits data on the SPI_SO output, on the falling edge of the SPI_SCK output. The SPI PROM does not provide any data to the iCE65 device's SPI_SI input. After sending the last command bit, the iCE65 device de-asserts SPI_SS_B High, completing the command. The iCE65 device then waits a minimum of 10 µS before sending the next SPI PROM command.

Figure 30: **SPI Peripheral Configuration Process**



Voltage Compatibility

As shown in Figure 23, there are potentially three different supply voltages involved in the SPI Peripheral interface, described in Table 30.

Table 30: **SPI Peripheral Mode Supply Voltages**

Supply Voltage	Description
AP_VCCIO	I/O supply to the Application Processor (AP)
VCC_SPI	Voltage supply for the iCE65 SPI interface.
VCCIO_2	Supply voltage for the iCE65 I/O Bank 2.

Table 31 describes how to maintain voltage compatibility for two interface scenarios. The easiest interface is when the Application Processor's (AP) I/O supply rail and the iCE65's SPI and VCCIO_2 bank supply rails all connect to the same voltage. The second scenario is when the AP's I/O supply voltage is greater than the iCE65's VCCIO_2 supply voltage.

***Table 31:* CRESET_B and CDONE Voltage Compatibility**

Condition	CRESET_B			CDONE Pull-up	Requirement
	Direct	**Open-Drain**	**Pull-up**		
VCCIO_AP = VCC_SPI **VCCIO_AP = VCCIO_2**	OK	OK with pull-up	Required if using open-drain output	Recommended	AP can directly drive CRESET_B High and Low although an open-drain output recommended is if multiple devices control CRESET_B. If using an open-drain driver, the CRESET_B input must include a 10 kΩ pull-up resistor to VCCIO_2. The 10 kΩ pull-up resistor to AP_VCCIO is also recommended.
AP_VCCIO > VCCIO_2	N/A	Required, requires pull-up	Required	Required	The AP must control CRESET_B with an open-drain output, which requires a 10 kΩ pull-up resistor to VCCIO_2. The 10 kΩ pull-up resistor to AP_VCCIO is required.

JTAG Boundary Scan Port

Overview

Each iCE65 device includes an IEEE 1149.1-compatible JTAG boundary-scan port. The port supports printed-circuit board (PCB) testing and debugging. It also provides an alternate means to configure the iCE65 device.

Signal Connections

The JTAG port connections are listed in Table 32.

***Table 32:* iCE65 JTAG Boundary Scan Signals**

Signal Name	Direction	Description
TDI	Input	Test Data Input. Must be tied off to GND when unused. (no pull-up resistor)*
TMS	Input	Test Mode Select. Must be tied off to GND when unused. (no pull-up resistor)*
TCK	Input	Test Clock. Must be tied off to GND when unused. (no pull-up resistor)*
TDO	Output	Test Data Output.
TRST_B	Input	Test Reset, active Low. Must be Low during normal device operation. Must be High to enable JTAG operations.*

* Must be tied off to GND or VCCIO_1, else VCCIO_1 draws current.

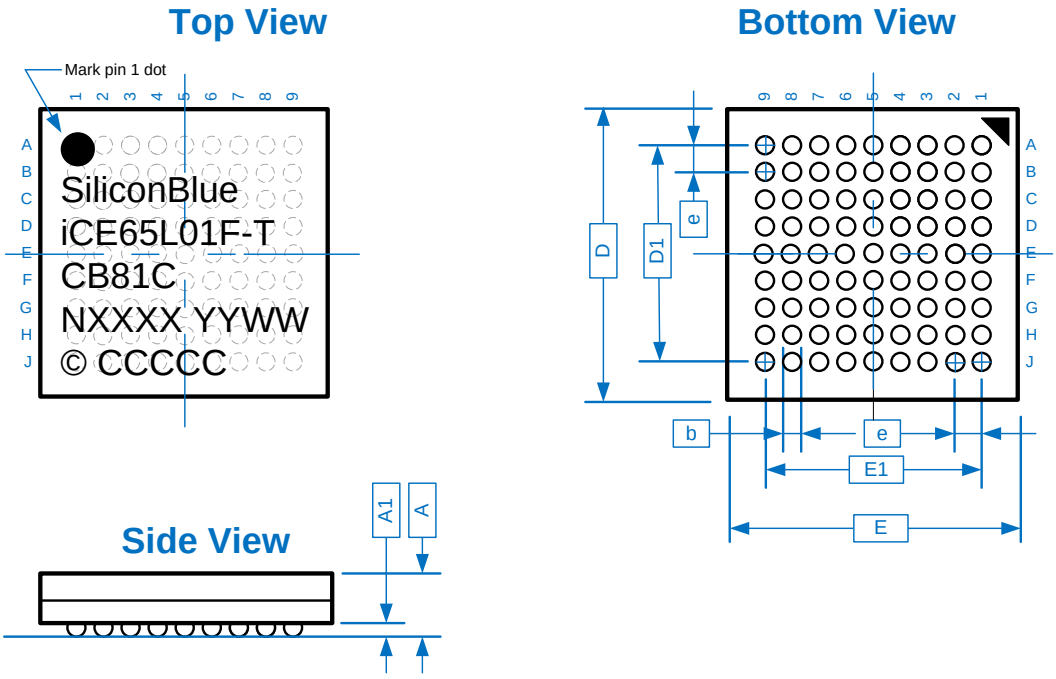
Table 33 lists the ball/pin numbers for the JTAG interface by package code. The JTAG interface is available in select package types. The JTAG port is located in I/O Bank 1 along the right edge of the iCE65 device and powered by the VCCIO_1 supply inputs. Consequently, the JTAG interface uses the associated I/O standards for I/O Bank 1.

***Table 33:* JTAG Interface Ball/Pin Numbers by Package**

JTAG Interface	VQ100	CB132	CB196	CB284
TDI	N/A	M12	M12	T16
TMS		P14	P14	V18
TCK		L12	L12	R16
TDO		N14	N14	U18
TRST_B		M14	M14	T18

***Figure 33:* CB81 Package Mechanical Drawing**

CB81: 5 x 5 mm, 81-ball, 0.5 mm ball-pitch, chip-scale ball grid array



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			9		Columns
Number of Ball Rows	Y			9		Rows
Number of Signal Balls		n		81		Balls
Body Size	X	E	4.90	5.00	5.10	mm
	Y	D	4.90	5.00	5.10	
Ball Pitch		e	—	0.50	—	
Ball Diameter		b	0.2	—	0.3	
Edge Ball Center to Center	X	E1	—	4.00	—	
	Y	D1	—	4.00	—	
Package Height		A	—	—	1.00	
Stand Off		A1	0.15	—	0.25	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65P01F	Part number
	-T	Power/Speed
3	CB81C	Package type
	ENG	Engineering
4	NXXXX	Lot Number
5	YYWW	Date Code
6	© CCCCCC	Country

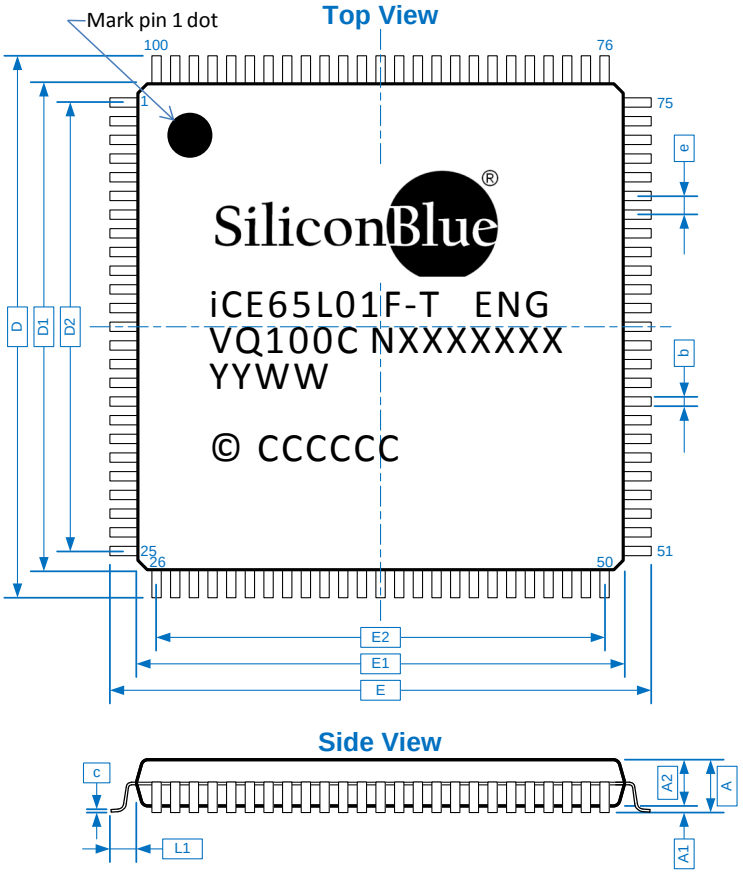
Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
67	57

Pin Function	Pin Number	Type	Bank
VCC	61	VCC	VCC
VCC	77	VCC	VCC
VPP_2V5	75	VPP	VPP
VPP_FAST	76	VPP	VPP

Package Mechanical Drawing

Figure 37: VQ100 Package Mechanical Drawing: Standard Device Marking



Description		Symbol	Min.	Nominal	Max.	Units
Leads per Edge	X			25		Leads
	Y			25		
Number of Signal Leads		n		100		
Maximum Size (lead tip to lead tip)	X	E	—	16.0	—	mm
	Y	D	—	16.0	—	
Body Size	X	E1	—	14.0	—	
	Y	D1	—	14.0	—	
Edge Pin Center to Center	X	E2	—	12.0	—	
	Y	D2	—	12.0	—	
Lead Pitch		e	—	0.50	—	
Lead Width		b	0.17	0.20	0.27	
Total Package Height		A	—	1.20	—	
Stand Off		A1	0.05	—	0.15	
Body Thickness		A2	0.95	1.00	1.05	
Lead Length		L1	—	1.00	—	
Lead Thickness		c	0.09	—	0.20	
Coplanarity			—	0.08	—	

Top Marking Format

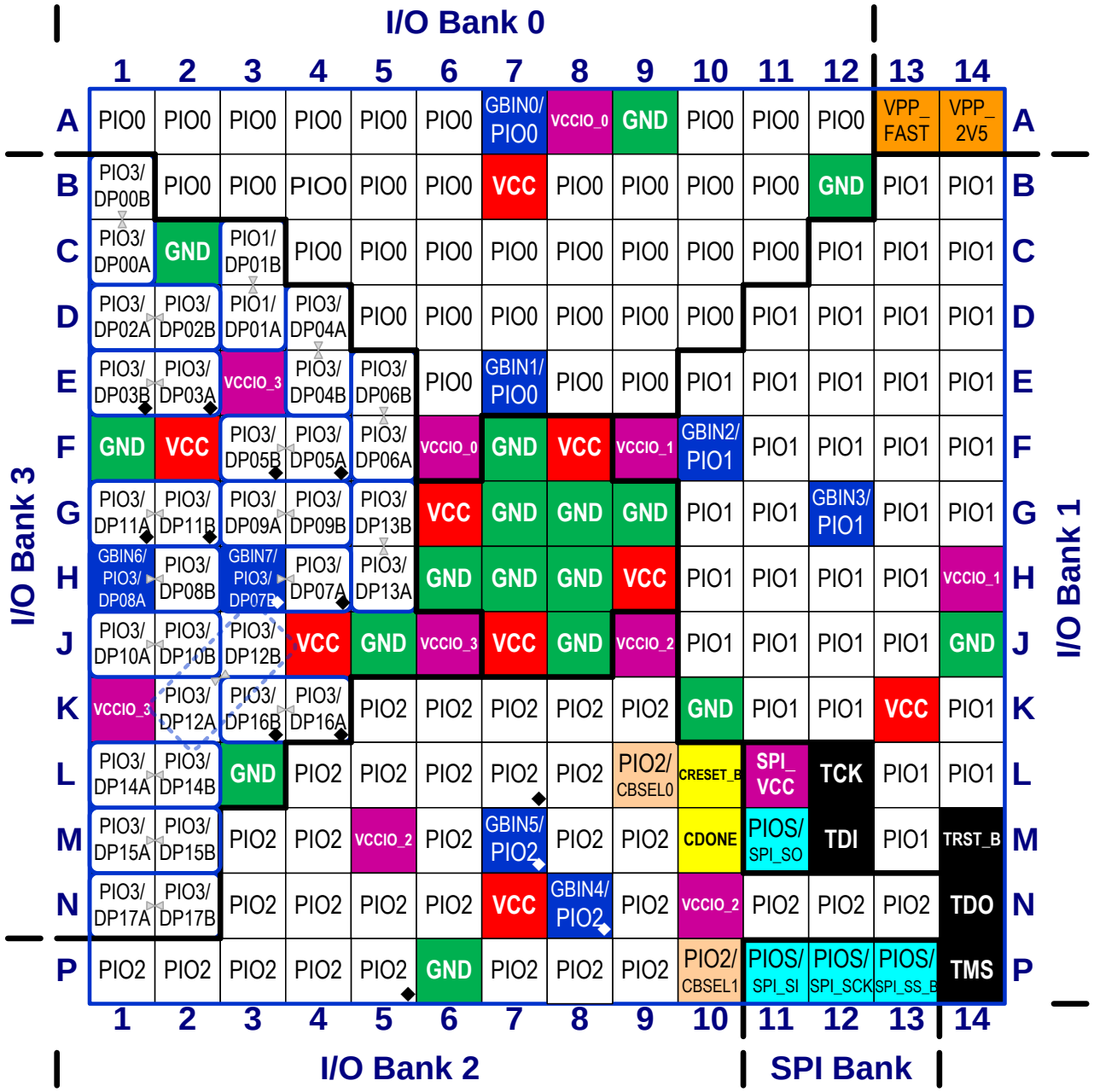
Line	Content	Description
1	Logo	Logo
2	iCE65L01F	Part number
	-T	Power/Speed
	ENG	Engineering
3	VQ100C NXXXXXXX	Package type and Lot number
4	YYWW	Date Code
5	N/A	Blank
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θJA (°C/W)	
0 LFM	200 LFM
38	32

Ball Function	Ball Number	Pin Type	Bank
L01/L04: GBIN7/PIO3 L08: GBIN7/DP05B	G1	GBIN	3
L01/L04: PIO3/DP05A L08: PIO3/DP05A	G3	DPIO	3
L01/L04: PIO3/DP05B L08: PIO3/DP11B	G4	DPIO	3
L01/L04: PIO3/DP06A L08: PIO3/DP06B	H3	DPIO	3
L01/L04: PIO3/DP06B L08: PIO3/DP11A	H4	DPIO	3
PIO3/DP07A	J3	DPIO	3
PIO3/DP07B	J1	DPIO	3
PIO3/DP08A	K3	DPIO	3
PIO3/DP08B	K4	DPIO	3
PIO3/DP09A	L1	DPIO	3
PIO3/DP09B	M1	DPIO	3
PIO3/DP10A	N1	DPIO	3
PIO3/DP10B	P1	DPIO	3
VCCIO_3	E3	VCCIO	3
VCCIO_3	J6	VCCIO	3
VCCIO_3	K1	VCCIO	3
PIOS/SPI_SO	M11	SPI	SPI
PIOS/SPI_SI	P11	SPI	SPI
PIOS/SPI_SCK	P12	SPI	SPI
PIOS/SPI_SS_B	P13	SPI	SPI
SPI_VCC	L11	SPI	SPI
GND	A9	GND	GND
GND	F1	GND	GND
GND	F7	GND	GND
GND	G7	GND	GND
GND	G8	GND	GND
GND	G9	GND	GND
GND	H6	GND	GND
GND	H7	GND	GND
GND	H8	GND	GND
GND	J8	GND	GND
GND	J14	GND	GND
GND	L3	GND	GND
GND	P6	GND	GND
VCC	F8	VCC	VCC
VCC	G6	VCC	VCC
VCC	H9	VCC	VCC
VCC	J4	VCC	VCC
VCC	J7	VCC	VCC
VPP_2V5	A14	VPP	VPP
VPP_FAST	A13	VPP	VPP

Figure 46: **iCE65L08 CB196 Chip-Scale BGA Footprint (Top View)**



Pinout Table

Table 42 provides a detailed pinout table for the iCE65L04 in the CB196 chip-scale BGA package. Pins are generally arranged by I/O bank, then by ball function. The pinout for the iCE65L08 is different than the iCE64L04 pinout.

Although both the iCE65L04 and iCE65L08 are both available in the CB196 package and *almost* completely pin compatible, there are differences as shown in Table 43.

Table 42: **iCE65L04 CB196 Chip-scale BGA Pinout Table**

Ball Function	Ball Number	Pin Type	Bank
GBIN0/PIO0	A7	GBIN	0
GBIN1/PIO0	E7	GBIN	0
PIO0	A1	PIO	0
PIO0	A2	PIO	0
PIO0	A3	PIO	0
PIO0	A4	PIO	0

Ball Function	Ball Number iCE65L04 iCE65L08	Pin Type by Device iCE65L04	Pin Type by Device iCE65L08	Bank	CB132 Ball Equivalent
PIO2	T13	PIO	PIO	2	M9
PIO2	V6	PIO	PIO	2	P2
PIO2	V7	PIO	PIO	2	P3
PIO2	V8	PIO	PIO	2	P4
PIO2	V9	PIO	PIO	2	P5
PIO2	V13	PIO	PIO	2	P9
PIO2	Y4	PIO	PIO	2	—
PIO2	Y5	PIO	PIO	2	—
PIO2	Y6	PIO	PIO	2	—
PIO2	Y7	PIO	PIO	2	—
PIO2	Y9	PIO	PIO	2	—
PIO2	Y10	PIO	PIO	2	—
PIO2	Y13	PIO	PIO	2	—
PIO2	Y14	PIO	PIO	2	—
PIO2	Y15	PIO	PIO	2	—
PIO2	Y17	PIO	PIO	2	—
PIO2	Y18	PIO	PIO	2	—
PIO2	Y19	PIO	PIO	2	—
PIO2	Y20	PIO	PIO	2	—
PIO2	AB2	PIO	PIO	2	—
PIO2 (●)	AB3	N.C.	PIO	2	—
PIO2 (●)	AB4	N.C.	PIO	2	—
PIO2	AB6	PIO	PIO	2	—
PIO2	AB7	PIO	PIO	2	—
PIO2	AB8	PIO	PIO	2	—
PIO2	AB9	PIO	PIO	2	—
PIO2	AB10	PIO	PIO	2	—
PIO2	AB11	PIO	PIO	2	—
PIO2	AB12	PIO	PIO	2	—
PIO2	AB13	PIO	PIO	2	—
PIO2	AB14	PIO	PIO	2	—
PIO2	AB15	PIO	PIO	2	—
PIO2 (●)	AB16	N.C.	PIO	2	—
PIO2 (●)	AB17	N.C.	PIO	2	—
PIO2 (●)	AB18	N.C.	PIO	2	—
PIO2 (●)	AB19	N.C.	PIO	2	—
PIO2 (●)	AB20	N.C.	PIO	2	—
PIO2 (●)	AB21	N.C.	PIO	2	—
PIO2 (●)	AB22	N.C.	PIO	2	—
PIO2/CBSEL0	R13	PIO	PIO	2	L9
PIO2/CBSEL1	V14	PIO	PIO	2	P10
VCCIO_2	N13	VCCIO	VCCIO	2	J9
VCCIO_2	T9	VCCIO	VCCIO	2	M5
VCCIO_2	Y11	VCCIO	VCCIO	2	—
PIO3/DP00A	F5	DPIO	DPIO	3	B1
PIO3/DP00B	G5	DPIO	DPIO	3	C1
PIO3/DP01A	G7	DPIO	DPIO	3	C3
PIO3/DP01B	H7	DPIO	DPIO	3	D3
PIO3/DP02A	H8	DPIO	DPIO	3	D4
PIO3/DP02B	J8	DPIO	DPIO	3	E4

Ball Function	Ball Number iCE65L04 iCE65L08	Pin Type by Device iCE65L04	Pin Type by Device iCE65L08	Bank	CB132 Ball Equivalent
PIO3/DP03A	H5	DPIO	DPIO	3	D1
PIO3/DP03B	J5	DPIO	DPIO	3	E1
PIO3/DP04A	K8	DPIO	DPIO	3	F4
PIO3/DP04B	K7	DPIO	DPIO	3	F3
PIO3/DP05A	E3	DPIO	DPIO	3	—
PIO3/DP05B	F3	DPIO	DPIO	3	—
PIO3/DP06A	G3	DPIO	DPIO	3	—
PIO3/DP06B	H3	DPIO	DPIO	3	—
PIO3/DP07A (●)	B1	N.C.	DPIO	3	—
PIO3/DP07B (●)	C1	N.C.	DPIO	3	—
PIO3/DP08A (●)	D1	N.C.	DPIO	3	—
PIO3/DP08B (●)	E1	N.C.	DPIO	3	—
PIO3/DP09A	H1	DPIO	DPIO	3	—
PIO3/DP09B	J1	DPIO	DPIO	3	—
PIO3/DP10A	K1	DPIO	DPIO	3	—
PIO3/DP10B	L1	DPIO	DPIO	3	—
PIO3/DP11A	L3	DPIO	DPIO	3	—
GBIN7/PIO3/DP11B	L5	GBIN	GBIN	3	G1
PIO3/DP12A (●)	T1	N.C.	DPIO	3	—
PIO3/DP12B (●)	U1	N.C.	DPIO	3	—
PIO3/DP13A (●)	W1	N.C.	DPIO	3	—
PIO3/DP13B (●)	Y1	N.C.	DPIO	3	—
PIO3/DP14A (●)	AA1	N.C.	DPIO	3	—
PIO3/DP14B (●)	AB1	N.C.	DPIO	3	—
GBIN6/PIO3/DP15A	M5	GBIN	GBIN	3	H1
PIO3/DP15B	M3	DPIO	DPIO	3	—
PIO3/DP16A	N3	DPIO	DPIO	3	—
PIO3/DP16B	P3	DPIO	DPIO	3	—
PIO3/DP17A	U3	DPIO	DPIO	3	—
PIO3/DP17B	V3	DPIO	DPIO	3	—
PIO3/DP18A	W3	DPIO	DPIO	3	—
PIO3/DP18B	Y3	DPIO	DPIO	3	—
PIO3/DP19A	L7	DPIO	DPIO	3	G3
PIO3/DP19B	L8	DPIO	DPIO	3	G4
PIO3/DP20A	M7	DPIO	DPIO	3	H3
PIO3/DP20B	M8	DPIO	DPIO	3	H4
PIO3/DP21A	N7	DPIO	DPIO	3	J3
PIO3/DP21B	N5	DPIO	DPIO	3	J1
PIO3/DP22A	P7	DPIO	DPIO	3	K3
PIO3/DP22B	P8	DPIO	DPIO	3	K4
PIO3/DP23A	R5	DPIO	DPIO	3	L1
PIO3/DP23B	T5	DPIO	DPIO	3	M1
PIO3/DP24A	U5	DPIO	DPIO	3	N1
PIO3/DP24B	V5	DPIO	DPIO	3	P1
VCCIO_3	F1	VCCIO	VCCIO	3	—
VCCIO_3	P1	VCCIO	VCCIO	3	—

iCE65L04 Pad Name	DiePlus VQ100	CB132	CB196	CB284	Pad	X (µm)	Y (µm)
PIO1_24	—	—	G11	F20	167	3,712.80	1,812.00
PIO1_25	—	—	F11	E20	168	3,610.80	1,847.00
PIO1_26	—	—	E10	D20	169	3,712.80	1,882.00
PIO1_27	—	—	E14	C20	170	3,610.80	1,917.00
GND	—	G8	G8	L12	171	3,712.80	1,952.00
GND	—	—	—	—	172	3,610.80	1,987.00
PIO1_28	—	—	F12	G22	173	3,712.80	2,022.00
PIO1_29	—	G12	D14	L16	174	3,610.80	2,057.00
PIO1_30	64	G11	E13	L15	175	3,712.80	2,092.00
PIO1_31	65	F12	C14	K16	176	3,610.80	2,127.00
VCC	—	—	K13	L20	177	3,712.80	2,162.00
VCC	—	—	—	—	178	3,610.80	2,197.00
PIO1_32	66	E14	E11	J18	179	3,712.80	2,232.00
PIO1_33	—	F11	C13	K15	180	3,610.80	2,267.00
VCCIO_1	67	F9	F9	K13	181	3,712.80	2,302.00
VCCIO_1	—	—	—	—	182	3,610.80	2,337.00
PIO1_34	68	E12	E12	J16	183	3,712.80	2,377.00
PIO1_35	69	D14	B14	H18	184	3,610.80	2,427.00
GND	70	G9	G9	L13	185	3,712.80	2,477.00
PIO1_36	71	E11	B13	J15	186	3,610.80	2,527.00
PIO1_37	72	D12	D12	H16	187	3,712.80	2,577.00
PIO1_38	73	C14	C12	G18	188	3,610.80	2,627.00
PIO1_39	74	B14	D11	F18	189	3,712.80	2,677.00
VPP_2V5	75	A14	A14	E18	190	3,610.80	2,739.68
VPP_FAST	76	A13	A13	E17	191	3,097.00	2,962.80
VCC	77	F8	F8	K12	192	2,997.00	2,860.80
VCC	77	F8	F8	K12	193	2,947.00	2,962.80
PIO0_00	78	A12	C11	E16	194	2,897.00	2,860.80
PIO0_01	—	C12	—	G16	195	2,847.00	2,962.80
PIO0_02	79	A11	A12	E15	196	2,797.00	2,860.80
PIO0_03	80	C11	B11	G15	197	2,747.00	2,962.80
PIO0_04	—	D11	—	H15	198	2,697.00	2,860.80
PIO0_05	81	A10	D10	E14	199	2,647.00	2,962.80
PIO0_06	82	C10	A11	G14	200	2,612.00	2,860.80
PIO0_07	83	D10	D9	H14	201	2,577.00	2,962.80
GND	84	A9	H6	E13	202	2,542.00	2,860.80
GND	—	—	—	—	203	2,507.00	2,962.80
PIO0_08	85	C9	C10	G13	204	2,472.00	2,860.80
PIO0_09	86	D9	A10	H13	205	2,437.00	2,962.80
PIO0_10	87	C8	B10	G12	206	2,402.00	2,860.80
PIO0_11	—	D8	E9	H12	207	2,367.00	2,962.80
PIO0_12	—	—	—	A18	208	2,332.00	2,860.80
PIO0_13	—	—	—	A17	209	2,297.00	2,962.80
PIO0_14	—	—	—	A16	210	2,262.00	2,860.80
PIO0_15	—	—	—	A15	211	2,227.00	2,962.80
VCCIO_0	88	A8	A8	E12	212	2,192.00	2,860.80
VCCIO_0	—	—	—	—	213	2,157.00	2,962.80

iCE65L08

Table 46 lists all the pads on the iCE65L08 die and how these pads connect to the balls or pins in the supported package styles. Most VCC, VCCIO, and GND pads are double-bonded inside the package although the table shows only a single connection.

For additional information on the iCE65L08 DiePlus product, please refer to the following data sheet.

- DiePlusAdvantage FPGA Known Good Die

Table 46: iCE65L08 Die Cross Reference

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO3_00/DP00A	—	B1	1	129.735	3,882.665
PIO3_01/DP00B	—	C1	2	231.735	3,837.665
PIO3_02/DP01A	C1	F5	3	129.735	3,792.665
PIO3_03/DP01B	B1	G5	4	231.735	3,747.665
GND	C2	K5	5	129.735	3,702.665
GND	—	—	6	231.735	3,657.665
VCCIO_3	E3	J7	7	129.735	3,612.665
VCCIO_3	—	—	8	231.735	3,567.665
PIO3_04/DP02A	D3	E3	9	129.735	3,512.665
PIO3_05/DP02B	C3	F3	10	231.735	3,477.665
PIO3_06/DP03A	D1	G3	11	129.735	3,442.665
PIO3_07/DP03B	D2	H3	12	231.735	3,407.665
VCC	F2	D3	13	129.735	3,372.665
VCC	—	—	14	231.735	3,337.665
PIO3_08/DP04A	D4	D1	15	129.735	3,302.665
PIO3_09/DP04B	E4	E1	16	231.735	3,267.665
PIO3_10/DP05A	—	H1	17	129.735	3,232.665
PIO3_11/DP05B	—	J1	18	231.735	3,197.665
GND	F1	M10	19	129.735	3,162.665
GND	—	—	20	231.735	3,127.665
PIO3_12/DP06A	E2	H5	21	129.735	3,092.665
PIO3_13/DP06B	E1	J5	22	231.735	3,057.665
GND	L3	J3	23	129.735	3,022.665
GND	—	—	24	231.735	2,987.665
PIO3_14/DP07A	F5	K1	25	129.735	2,952.665
PIO3_15/DP07B	E5	L1	26	231.735	2,917.665
VCCIO_3	E3	K3	27	129.735	2,882.665
VCCIO_3	—	—	28	231.735	2,847.665
VCC	G6	L10	29	129.735	2,812.665
VCC	—	—	30	231.735	2,777.665
PIO3_16/DP08A	F4	G7	31	129.735	2,742.665
PIO3_17/DP08B	F3	H7	32	231.735	2,707.665
VCCIO_3	K1	F1	33	129.735	2,672.665
VCCIO_3	—	—	34	231.735	2,637.665
GND	—	G1	35	129.735	2,602.665
GND	—	—	36	231.735	2,567.665
PIO3_18/DP09A	G3	K8	37	129.735	2,532.665
PIO3_19/DP09B	G4	K7	38	231.735	2,497.665

I/O Characteristics

Table 49: PIO Pin Electrical Characteristics

Symbol	Description		Conditions	Minimum	Nominal	Maximum	Units
I_I	Input pin leakage current	I/O Bank 0, 1, 2	V_{IN} = $VCCIO_{max}$ to 0 V			±10	µA
		I/O Bank 3	V_{IN} = $VCCIO_{max}$				
I_{OZ}	Three-state I/O pin (Hi-Z) leakage current		V_O = $VCCIO_{max}$ to 0 V			±10	µA
C_{PIO}	PIO pin input capacitance				6		pF
C_{GBIN}	GBIN global buffer pin input capacitance				6		pF
R_{PULLUP}	Internal PIO pull-up resistance during configuration		VCCIO = 3.3V		40		kΩ
			VCCIO = 2.5V		50		kΩ
			VCCIO = 1.8V		90		kΩ
			VCCIO = 1.5V				kΩ
			VCCIO = 1.2V				kΩ
V_{HYST}	Input hysteresis		VCCIO = 1.5V to 3.3V		50		mV

NOTE: All characteristics are characterized and may or may not be tested on each pin on each device.

Single-ended I/O Characteristics

Table 50: I/O Characteristics (I/O Banks 0, 1, 2 and SPI only) (I/O Bank 3 iCE65L01 only)

I/O Standard	Nominal I/O Bank Supply Voltage	Input Voltage (V)		Output Voltage (V)		Output Current at Voltage (mA)	
		V_{IL}	V_{IH}	V_{OL}	V_{OH}	I_{OL}	I_{OH}
LVCMOS33	3.3V	0.80	2.00	0.4	2.40	8	8
LVCMOS25	2.5V	0.70	1.70	0.4	2.00	6	6
LVCMOS18	1.8V	35% VCCIO	65% VCCIO	0.4	1.40	4	4
LVCMOS15	1.5V	Not supported Use I/O Bank 3		0.4	1.20	2	2

Table 51: I/O Characteristics (I/O Bank 3 and iCE65L04/08 only)

I/O Standard	Supply Voltage	Input Voltage (V)		Output Voltage (V)		I/O Attribute Name	mA at Voltage
		Max. V_{IL}	Min. V_{IH}	Max. V_{OL}	Min. V_{OH}		I_{OL}, I_{OH}
LVCMOS33	3.3V	0.80	2.20	0.4	2.40	SL_LVCMOS33_8	±8
LVCMOS25	2.5V	0.70	1.70	0.4	2.00	SB_LVCMOS25_16	±16
						SB_LVCMOS25_12	±12
						SB_LVCMOS25_8 *	±8
						SB_LVCMOS25_4	±4
LVCMOS18	1.8V	35% VCCIO	65% VCCIO	0.4	VCCIO–0.45	SB_LVCMOS18_10	±10
						SB_LVCMOS18_8	±8
						SB_LVCMOS18_4 *	±4
						SB_LVCMOS18_2	±2
LVCMOS15	1.5V	35% VCCIO	65% VCCIO	25% VCCIO	75% VCCIO	SB_LVCMOS15_4	±4
						SB_LVCMOS15_2 *	±2
MDDR	1.8V	35% VCCIO	65% VCCIO	0.4	VCCIO–0.45	SB_MDDR10	±10
						SB_MDDR8	±8
						SB_MDDR4 *	±4
						SB_MDDR2	±2
SSTL2 (Class 2)	2.5V	VREF–0.180	VREF+0.180	0.35	VTT+0.430	SB_SSTL2_CLASS_2	±16.2
SSTL2 (Class 1)				0.54		SB_SSTL2_CLASS_1	±8.1
SSTL18 (Full)	1.8V	VREF–0.125	VREF+0.125	0.28	VTT+0.280	SB_SSTL18_FULL	±13.4
SSTL18 (Half)				VTT–0.475	VTT+0.475	SB_SSTL18_HALF	±6.7

NOTES:
SSTL2 and SSTL18 I/O standards require the VREF input pin, which is only available on the CB284 package and die-based products.

RAM4K Block

Table 56 provides timing information for the logic in a RAM4K block, which includes the paths shown in Figure 59.

Figure 59: RAM4K Timing Circuit

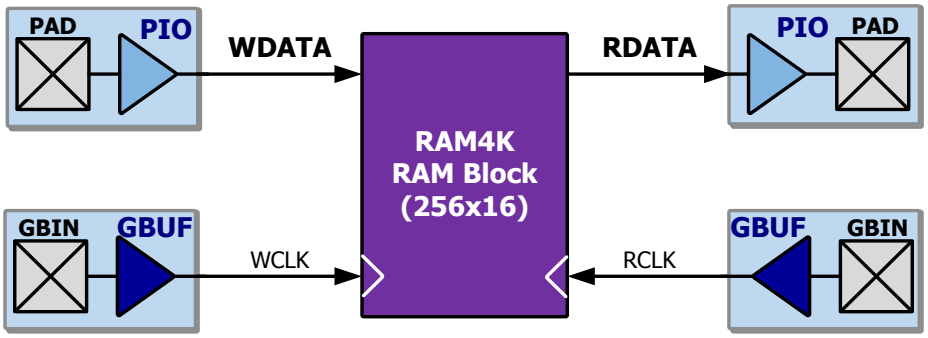


Table 56: Typical RAM4K Block Timing

Symbol	From	To	Device: iCE65 / Description	L01	L04, L08			Units
			Power/Speed Grade	–T	–L	–L	–T	
			Nominal VCC	1.2 V	1.0 V	1.2 V	1.2 V	
			Description	Typ.	Typ.	Typ.	Typ.	
Write Setup/Hold Time								
t_{SUWD}	PIO input	GBIN input	Minimum write data setup time on PIO inputs before active clock edge on GBIN input, include interconnect delay.	0.6	3.1	1.7	0.8	ns
t_{HDWD}	GBIN input	PIO input	Minimum write data hold time on PIO inputs after active clock edge on GBIN input, including interconnect delay.	0	0	0	0	ns
Read Clock-Output-Time								
t_{CKORD}	RCLK clock input	PIO output	Clock-to-output delay from RCLK input pin, through RAM4K RDATA output flip-flop to PIO output pad, including interconnect delay.	5.6	17.1	9.1	7.3	ns
t_{GBCKRM}	GBIN input	RCLK clock input	Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to the RCLK clock input.	2.1	7.3	3.8	2.6	ns
Write and Read Clock Characteristics								
t_{RMWCKH}	WCLK RCLK	WCLK RCLK	Write clock High time	0.54	1.14	0.54	0.54	ns
t_{RMWCKL}			Write clock Low time	0.63	1.32	0.63	0.63	ns
t_{RMWCYC}			Write clock cycle time	1.27	2.64	1.27	1.27	ns
F_{WMAX}			Sustained write clock frequency	256	256	256	256	MHz

Notes

		minimum temperature to –40°C in Figure 2 and Table 48. Added NVCM programming temperature to Table 48.
1.3	17-DEC-2008	Added footprint and pinout information for the CS110 Wafer-Level Chip-Scale Ball Grid Array. Clarified that the CB196 footprint shown is for the iCE65L04; the iCE65L08 footprint for the CB196 package is similar but different. Added updated information on Differential Inputs and Outputs, including support for SubLVDS. Updated Electrical Characteristics and AC Timing Guidelines sections. Added support for the LVCMOS15 I/O standard. Corrected the diagram showing the direct differential clock input, Figure 16. Updated the number of I/Os by package in Table 34. Updated company address. Other minor updates throughout.
1.2	11-OCT-2008	Updated I/O Bank 3 characteristics in Table 7 and Table 51. Corrected label in Figure 14. Added JTAG configuration to Table 20. Added pull-up resistor information in Table 22 and Figure 21. Added "Internal Device Reset" section. Updated internal oscillator performance in and Table 57. Updated configuration timing in Table 58 based on new oscillator timing. Completely reorganized the "Package and Pinout Information" section. Added information on CS63 and CB196 packages. Updated information on VPP_2V5 signal in Table 36. Reduced package height for CB132 and CB284 packages to 1.0 mm. Added "Differential Inputs" and "Differential Outputs" sections.
1.1	4-SEPT-2008	Updated package roadmap (Table 2) and updated ordering codes (Figure 2). Updated Figure 7. Updated Figure 24. Added CS63 package footprint (Figure 36), pinout (Table 39) and Package.
1.0	31-MAY-2008	Initial public release.