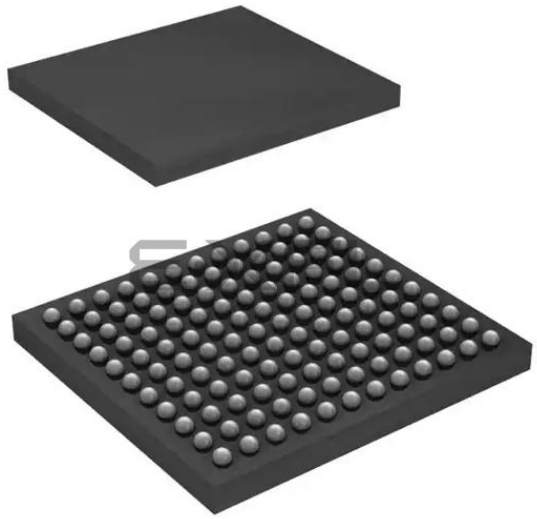
Lattice Semiconductor Corporation - ICE65L08F-TCB132I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

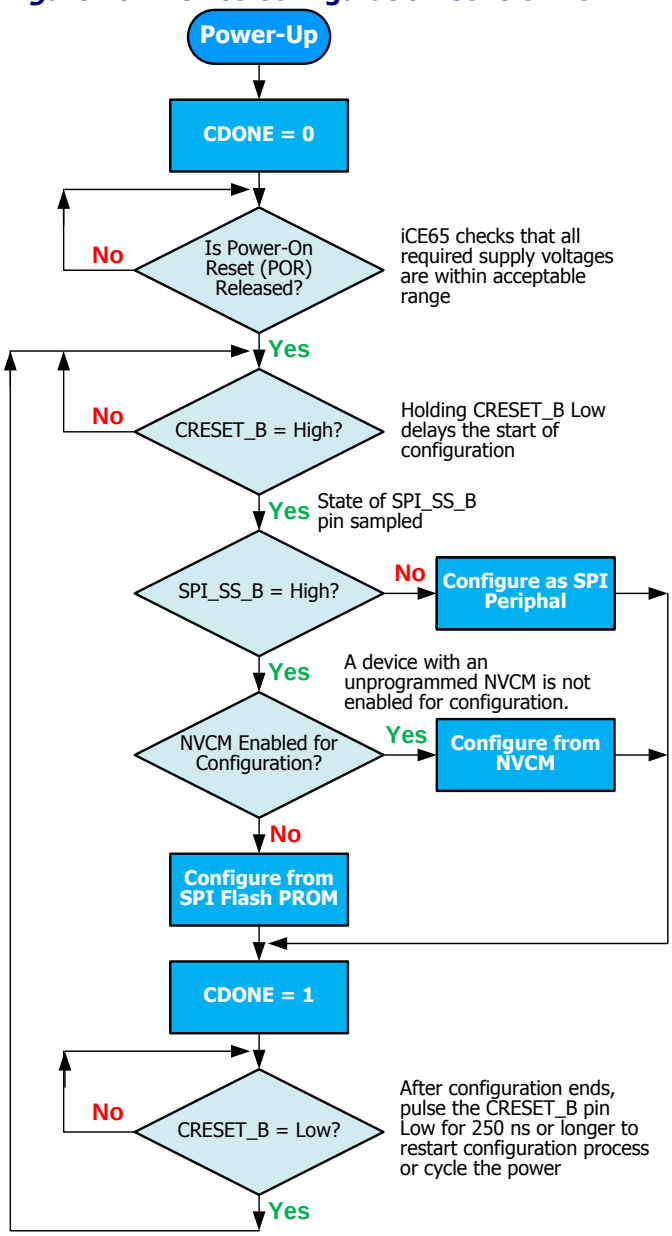
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	960
Number of Logic Elements/Cells	7680
Total RAM Bits	131072
Number of I/O	95
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	132-VFBGA, CSPBGA
Supplier Device Package	132-CSBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice65l08f-tcb132i

Figure 20: **Device Configuration Control Flow**



Configuration Image Size

Table 23 shows the number of memory bits required to configure an iCE65 device. Two values are provided for each device. The "Logic Only" value indicates the minimum configuration size, the number of bits required to configure only the logic fabric, leaving the RAM4K blocks uninitialized. The "Logic + RAM4K" column indicates the maximum configuration size, the number of bits to configure the logic fabric and to pre-initialize all the RAM4K blocks.

Table 21: **iCE65 Configuration Image Size (Kbits)**

Device	MINIMUM Logic Only (RAM4K not initialized)	MAXIUM Logic + RAM4K (RAM4K pre-initialized)
iCE65L01	181 Kbits	245 Kbits*
iCE65L04	453 Kbits	533 Kbits
iCE65L08	929 Kbits	1,057 Kbits

* Note: only 14 of the 16 RAM4K Memory Blocks may be pre-initialized in the iCE65L01.

Nonvolatile Configuration Memory (NVCM)

All standard iCE65 devices have an internal, nonvolatile configuration memory (NVCM). The NVCM is large enough to program a complete iCE65 device, including initializing all RAM4K block locations (MAXIMUM column in Table 23. The NVCM memory also has very high programming yield due to extensive error checking and correction (ECC) circuitry.

The NVCM is ideal for cost-sensitive, high-volume production applications, saving the cost and board space associated with an external configuration PROM. Furthermore, the NVCM provides exceptional design security, protecting critical intellectual property (IP). The NVCM contents are entirely contained within the iCE65 device and are not readable once protected by the one-time programmable Security bits. Furthermore, there is no observable difference between a programmed or un-programmed memory cell using optical or electron microscopy.

The NVCM memory has a programming interface similar to a 25-series SPI serial Flash PROM. Consequently, it can be programmed using standard device programmers before or after circuit board assembly or programmed in-system from a microprocessor or other intelligent controller. NVCM programming requires VCCIO_1, Bank 1 voltage to be applied on power-up, at the same time as other voltage supplies.

Configuration Control Signals

The iCE65 configuration process is self-timed and controlled by a few internal signals and device I/O pins, as described in Table 22.

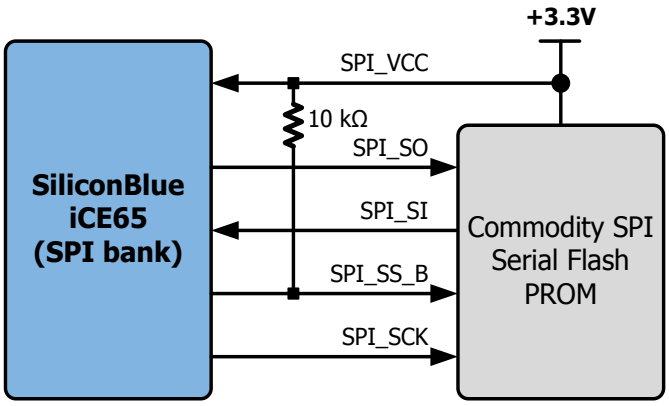
Table 22: **iCE65 Configuration Control Signals**

Signal Name	Direction	Description
POR	Internal control	Internal Power-On Reset (POR) circuit.
OSC	Internal control	Internal configuration oscillator.
CRESET_B	Input	Configuration Reset input. Active-Low. No internal pull-up resistor.
CDONE	Open-drain Output	Configuration Done output. Permanent, weak pull-up resistor to VCCIO_2.

The Power-On Reset circuit, POR, automatically resets the iCE65 component to a known state during power-up (cold boot). The POR circuit monitors the relevant voltage supply inputs, as shown in Figure 22. Once all supplies exceed their minimum thresholds, the configuration controller can start the configuration process.

The configuration controller begins configuring the iCE65 device, clocked by the Internal Oscillator, OSC. The OSC oscillator continues controlling configuration unless the iCE65 device is configured using the SPI Peripheral Configuration Interface.

Figure 23: **iCE65 SPI Master Configuration Interface**



The SPI configuration interface is used primarily during development before mass production, where the configuration is then permanently programmed in the NVCM configuration memory. However, the SPI interface can also be the primary configuration interface allowing easy in-system upgrades and support for multiple configuration images.

The SPI control signals are defined in Table 25. Table 26 lists the SPI interface ball or pins numbers by package.

Table 25: **SPI Master Configuration Interface Pins (SPI_SS_B High before Configuration)**

Signal Name	Direction	Description
SPI_VCC	Supply	SPI Flash PROM voltage supply input.
SPI_SO	Output	SPI Serial Output from the iCE65 device.
SPI_SI	Input	SPI Serial Input to the iCE65 device, driven by the select SPI serial Flash PROM.
SPI_SS_B	Output	SPI Slave Select output from the iCE65 device. Active Low.
SPI_SCK	Output	SPI Slave Clock output from the iCE65 device.

After configuration, the SPI port pins are available to the user-application as additional PIO pins, supplied by the SPI_VCC input voltage, essentially providing a fifth "mini" I/O bank.

Table 26: **SPI Interface Ball/Pin Numbers by Package**

SPI Interface	VQ100	CB132	CB196	CB284
SPI_VCC	50	L11	L11	R15
PIOS/SPI_SO	45	M11	M11	T15
PIOS/SPI_SI	46	P11	P11	V15
PIOS/SPI_SS_B	49	P13	P13	V17
PIOS/SPI_SCK	48	P12	P12	V16

SPI PROM Requirements

The iCE65 mobileFPGA SPI Flash configuration interface supports a variety of SPI Flash memory vendors and product families. However, Lattice Semiconductor does not specifically test, qualify, or otherwise endorse any specific SPI Flash vendor or product family. The iCE65 SPI interface supports SPI PROMs that they meet the following requirements.

- The PROM must operate at 3.3V or 2.5V in order to trigger the iCE65 FPGA's power-on reset circuit.
- The PROM must support the `0x0B` Fast Read command, using a 24-bit start address and has 8 dummy bits before the PROM provides first data (see Figure 25: SPI Fast Read Command).
- The PROM must have enough bits to program the iCE65 device (see Table 27: Smallest SPI PROM Size (bits), by Device, by Number of Images).
- The PROM must support data operations at the upper frequency range for the selected iCE65 internal oscillator frequency (see Table 57). The oscillator frequency is selectable when creating the FPGA bitstream image.

- For lowest possible power consumption after configuration, the PROM should also support the 0xB9 Deep Power Down command and the 0xAB Release from Deep Power-down Command (see Figure 24 and Figure 26). The low-power mode is optional.
- The PROM must be ready to accept commands 10 µs after meeting its power-on conditions. In the PROM data sheet, this may be specified as t_{VSL} or t_{VCSL}. It is possible to use slower PROMs by holding the CRESET_B input Low until the PROM is ready, then releasing CRESET_B, either under program control or using an external power-on reset circuit.

The Lattice iCEman65 development board and associated programming software uses an ST Micro/Numonyx M25Pxx SPI serial Flash PROM.

SPI PROM Size Requirements

Table 27 lists the minimum SPI PROM size required to configure an iCE65 device. Larger PROM sizes are allowed, but not required unless the end application uses the additional space. SPI serial PROM sizes are specified in bits. For each device size, the table shows the required minimum PROM size for "Logic Only" (no BRAM initialization) and "Logic + RAM4K" (RAM4K blocks pre-initialized). Furthermore, the table shows the PROM size for varying numbers of configuration images. Most applications will use a single image. Applications that use the Cold Boot or Warm Boot features may use more than one image.

Table 27: Smallest SPI PROM Size (bits), by Device, by Number of Images

Device	1 Image		2 Images		3 Images		4 Images	
	Logic Only	**Logic + RAM4K**	**Logic Only**	**Logic + RAM4K**	**Logic Only**	**Logic + RAM4K**	**Logic Only**	**Logic + RAM4K**
iCE65L01	256K	256K	512K	512K	1M	1M	1M	1M
iCE65L04	512K	1M	1M	2M	2M	2M	2M	4M
iCE65L08	1M	2M	2M	4M	4M	4M	4M	8M

Enabling SPI Configuration Interface

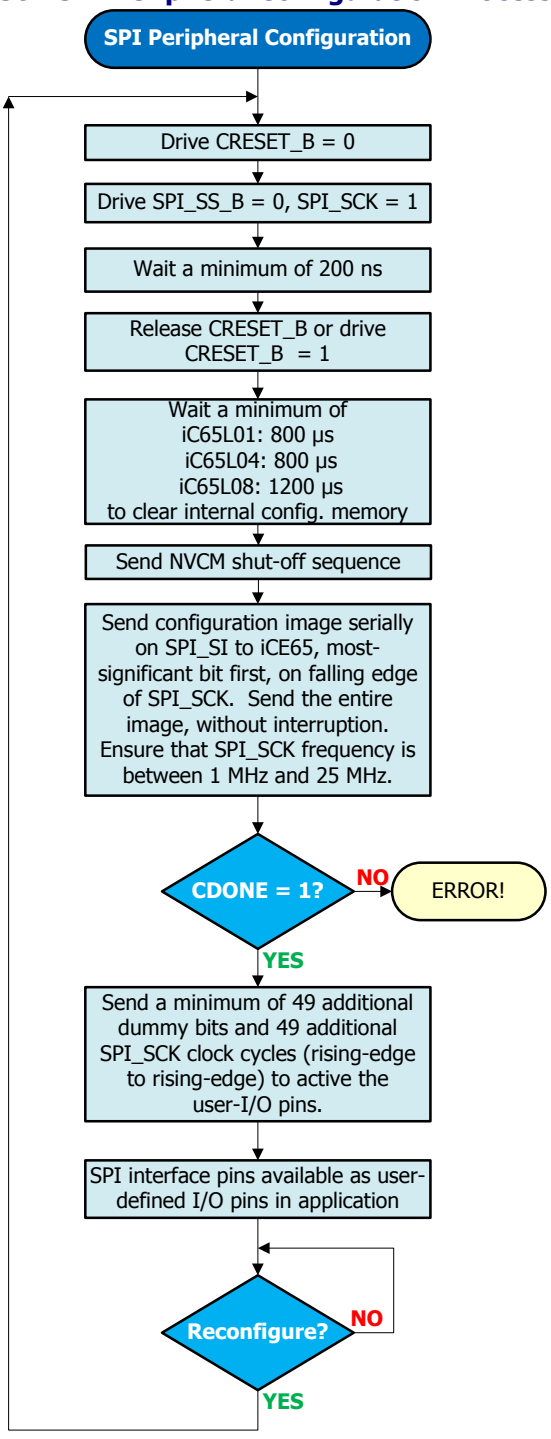
To enable the SPI configuration mode, the SPI_SS_B pin must be allowed to float High. The SPI_SS_B pin has an internal pull-up resistor. If SPI_SS_B is Low, then the iCE65 component defaults to the SPI Slave configuration mode.

SPI Master Configuration Process

The iCE65 SPI Master Configuration Interface supports a variety of modern, high-density, low-cost SPI serial Flash PROMs. Most modern SPI PROMs include a power-saving Deep Power-down mode. The iCE65 component exploits this mode for additional system power savings.

The iCE65 SPI interface starts by driving SPI_SS_B Low, and then sends a Release from Power-down command to the SPI PROM, hexadecimal command code 0xAB. Figure 24 provides an example waveform. This initial command wakes up the SPI PROM if it is already in Deep Power-down mode. If the PROM is not in Deep Power-down mode, the extra command has no adverse affect other than that it requires a few additional microseconds during the configuration process. The iCE65 device transmits data on the SPI_SO output, on the falling edge of the SPI_SCK output. The SPI PROM does not provide any data to the iCE65 device's SPI_SI input. After sending the last command bit, the iCE65 device de-asserts SPI_SS_B High, completing the command. The iCE65 device then waits a minimum of 10 µS before sending the next SPI PROM command.

Figure 30: **SPI Peripheral Configuration Process**



Voltage Compatibility

As shown in Figure 23, there are potentially three different supply voltages involved in the SPI Peripheral interface, described in Table 30.

Table 30: **SPI Peripheral Mode Supply Voltages**

Supply Voltage	Description
AP_VCCIO	I/O supply to the Application Processor (AP)
VCC_SPI	Voltage supply for the iCE65 SPI interface.
VCCIO_2	Supply voltage for the iCE65 I/O Bank 2.

QN84 Quad Flat Pack No-Lead

The QN84 is a Quad Flat Pack No-Lead package with a 0.5 mm pad pitch.

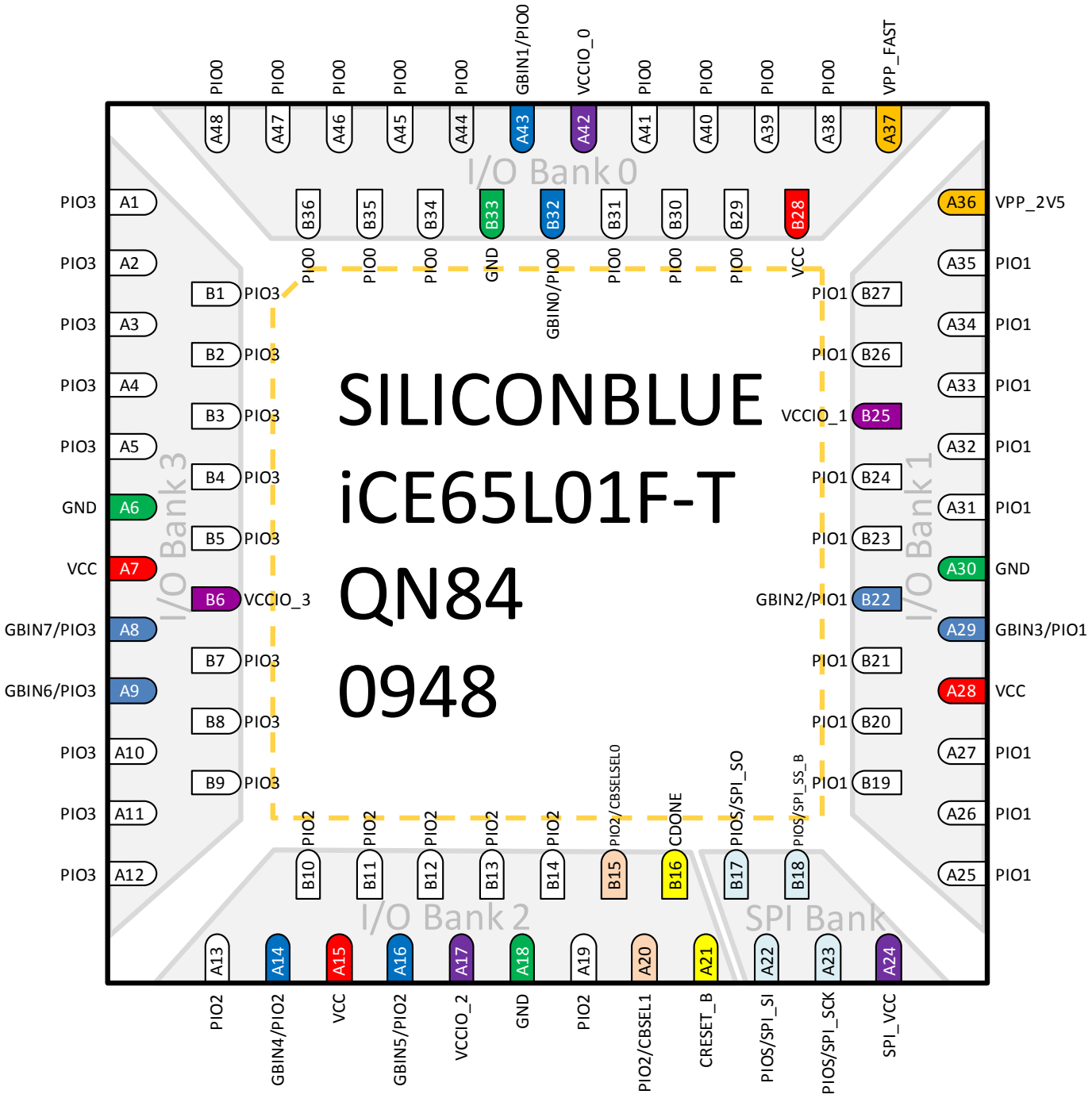
Footprint Diagram

Figure 34 shows the iCE65 footprint diagram for the QN84 package.

Also see Table 38 for a complete, detailed pinout for the QN84 package.

The signal pins are also grouped into the four I/O Banks and the SPI interface.

Figure 34: **iCE65 QN84 Quad Flat Pack No-Lead Footprint (Top View)**



Pinout Table

Table 38 provides a detailed pinout table for the QN84 package. Pins are generally arranged by I/O bank, then by ball function. The QN84 package has no JTAG pins.

Table 38: **iCE65 QN84 Chip-scale BGA Pinout Table**

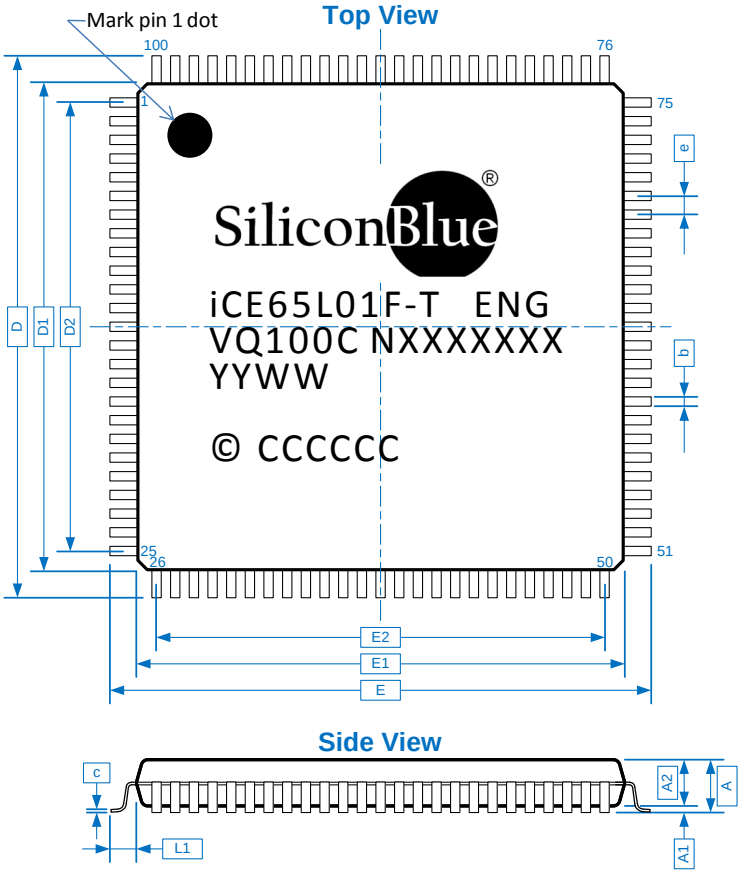
Ball Function	Ball Number	Pin Type	Bank
GBIN0/PIO0	B32	GBIN	0
GBIN1/PIO0	A43	GBIN	0
PIO0	A38	PIO	0
PIO0	A39	PIO	0
PIO0	A40	PIO	0
PIO0	A41	PIO	0
PIO0	A44	PIO	0
PIO0	A45	PIO	0
PIO0	A46	PIO	0
PIO0	A47	PIO	0
PIO0	A48	PIO	0
PIO0	B29	PIO	0
PIO0	B30	PIO	0
PIO0	B31	PIO	0
PIO0	B34	PIO	0
PIO0	B35	PIO	0
PIO0	B36	PIO	0
VCCIO_0	A42	VCCIO	0
GBIN2/PIO1	B22	GBIN	1
GBIN3/PIO1	A29	GBIN	1
PIO1	A25	PIO	1
PIO1	A26	PIO	1
PIO1	A27	PIO	1
PIO1	A31	PIO	1
PIO1	A32	PIO	1
PIO1	A33	PIO	1
PIO1	A34	PIO	1
PIO1	A35	PIO	1
PIO1	B19	PIO	1
PIO1	B20	PIO	1
PIO1	B21	PIO	1
PIO1	B23	PIO	1
PIO1	B24	PIO	1
PIO1	B26	PIO	1
PIO1	B27	PIO	1
VCCIO_1	B25	VCCIO	1
CDONE	B16	CONFIG	2
CRESET_B	A21	CONFIG	2
GBIN4/PIO2	A14	GBIN	2
GBIN5/PIO2	A16	GBIN	2
PIO2	A13	PIO	2
PIO2	B12	PIO	2
PIO2	A19	PIO	2
PIO2	B10	PIO	2
PIO2	B11	PIO	2
PIO2	B13	PIO	2

Pin Function	Pin Number	Type	Bank
PIO2	28	PIO	2
PIO2	29	PIO	2
PIO2	30	PIO	2
PIO2	iCE65L01: 34 iCE65L04: 36	PIO	2
PIO2	37	PIO	2
PIO2	40	PIO	2
PIO2/CBSEL0	41	PIO	2
PIO2/CBSEL1	42	PIO	2
VCCIO_2	31	VCCIO	2
VCCIO_2	38	VCCIO	2
PIO3/DP00A	1	PIO/DPIO	3
PIO3/DP00B	2	PIO/DPIO	3
PIO3/DP01A	3	PIO/DPIO	3
PIO3/DP01B	4	PIO/DPIO	3
PIO3/DP02A	7	PIO/DPIO	3
PIO3/DP02B	8	PIO/DPIO	3
PIO3/DP03A	9	PIO/DPIO	3
PIO3/DP03B	10	PIO/DPIO	3
PIO3/DP04A	12	PIO/DPIO	3
GBIN7/PIO3/DP04B	13	GBIN/DPIO	3
GBIN6/PIO3/DP05A	15	GBIN/DPIO	3
PIO3/DP05B	16	PIO/DPIO	3
PIO3/DP06A	18	PIO/DPIO	3
PIO3/DP06B	19	PIO/DPIO	3
PIO3/DP07A	20	PIO/DPIO	3
PIO3/DP07B	21	PIO/DPIO	3
PIO3/DP08A	24	PIO/DPIO	3
PIO3/DP08B	25	PIO/DPIO	3
VCCIO_3	6	VCCIO	3
VCCIO_3	14	VCCIO	3
VCCIO_3	22	VCCIO	3
PIOS/SPI_SO	45	SPI	SPI
PIOS/SPI_SI	46	SPI	SPI
PIOS/SPI_SCK	48	SPI	SPI
PIOS/SPI_SS_B	49	SPI	SPI
SPI_VCC	50	SPI	SPI
GND	5	GND	GND
GND	17	GND	GND
GND	23	GND	GND
GND	32	GND	GND
GND	39	GND	GND
GND	47	GND	GND
GND	55	GND	GND
GND	70	GND	GND
GND	84	GND	GND
GND	98	GND	GND
VCC	11	VCC	VCC
VCC	35	VCC	VCC

Pin Function	Pin Number	Type	Bank
VCC	61	VCC	VCC
VCC	77	VCC	VCC
VPP_2V5	75	VPP	VPP
VPP_FAST	76	VPP	VPP

Package Mechanical Drawing

Figure 37: VQ100 Package Mechanical Drawing: Standard Device Marking



Description		Symbol	Min.	Nominal	Max.	Units
Leads per Edge	X			25		Leads
	Y			25		
Number of Signal Leads		n		100		
Maximum Size (lead tip to lead tip)	X	E	—	16.0	—	mm
	Y	D	—	16.0	—	
Body Size	X	E1	—	14.0	—	
	Y	D1	—	14.0	—	
Edge Pin Center to Center	X	E2	—	12.0	—	
	Y	D2	—	12.0	—	
Lead Pitch		e	—	0.50	—	
Lead Width		b	0.17	0.20	0.27	
Total Package Height		A	—	1.20	—	
Stand Off		A1	0.05	—	0.15	
Body Thickness		A2	0.95	1.00	1.05	
Lead Length		L1	—	1.00	—	
Lead Thickness		c	0.09	—	0.20	
Coplanarity			—	0.08	—	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65L01F	Part number
	-T	Power/Speed
	ENG	Engineering
3	VQ100C NXXXXXXX	Package type and Lot number
4	YYWW	Date Code
5	N/A	Blank
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θJA (°C/W)	
0 LFM	200 LFM
38	32

Ball Function	Ball Number	Pin Type	Bank
PIO0	A5	PIO	0
PIO0	A6	PIO	0
PIO0	A8	PIO	0
PIO0	A10	PIO	0
PIO0	B3	PIO	0
PIO0	B4	PIO	0
PIO0	B5	PIO	0
PIO0	B8	PIO	0
PIO0	B9	PIO	0
PIO0	C5	PIO	0
PIO0	C7	PIO	0
PIO0	C8	PIO	0
PIO0	C9	PIO	0
PIO0	D5	PIO	0
PIO0	D7	PIO	0
PIO0	E5	PIO	0
PIO0	E6	PIO	0
PIO0	E7	PIO	0
PIO0	F7	PIO	0
VCCIO_0	B7	VCCIO	0
GBIN2/PIO1	F9	GBIN	1
GBIN3/PIO1	F8	GBIN	1
PIO1	A11	PIO	1
PIO1	B11	PIO	1
PIO1	C11	PIO	1
PIO1	D8	PIO	1
PIO1	D9	PIO	1
PIO1	D10	PIO	1
PIO1	D11	PIO	1
PIO1	E8	PIO	1
PIO1	E9	PIO	1
PIO1	E11	PIO	1
PIO1	F10	PIO	1
PIO1	G7	PIO	1
PIO1	G8	PIO	1
PIO1	G9	PIO	1
PIO1	G10	PIO	1
PIO1	H7	PIO	1
PIO1	H8	PIO	1
PIO1	H9	PIO	1
PIO1	H10	PIO	1
VCCIO_1	E10	VCCIO	1
CDONE	J7	CONFIG	2
CRESET_B	K7	CONFIG	2
GBIN4/PIO2	L8	GBIN	2
GBIN5/PIO2	L9	GBIN	2
PIO2	H4	PIO	2
PIO2	H5	PIO	2
PIO2	H11	PIO	2
PIO2	J4	PIO	2
PIO2	J5	PIO	2

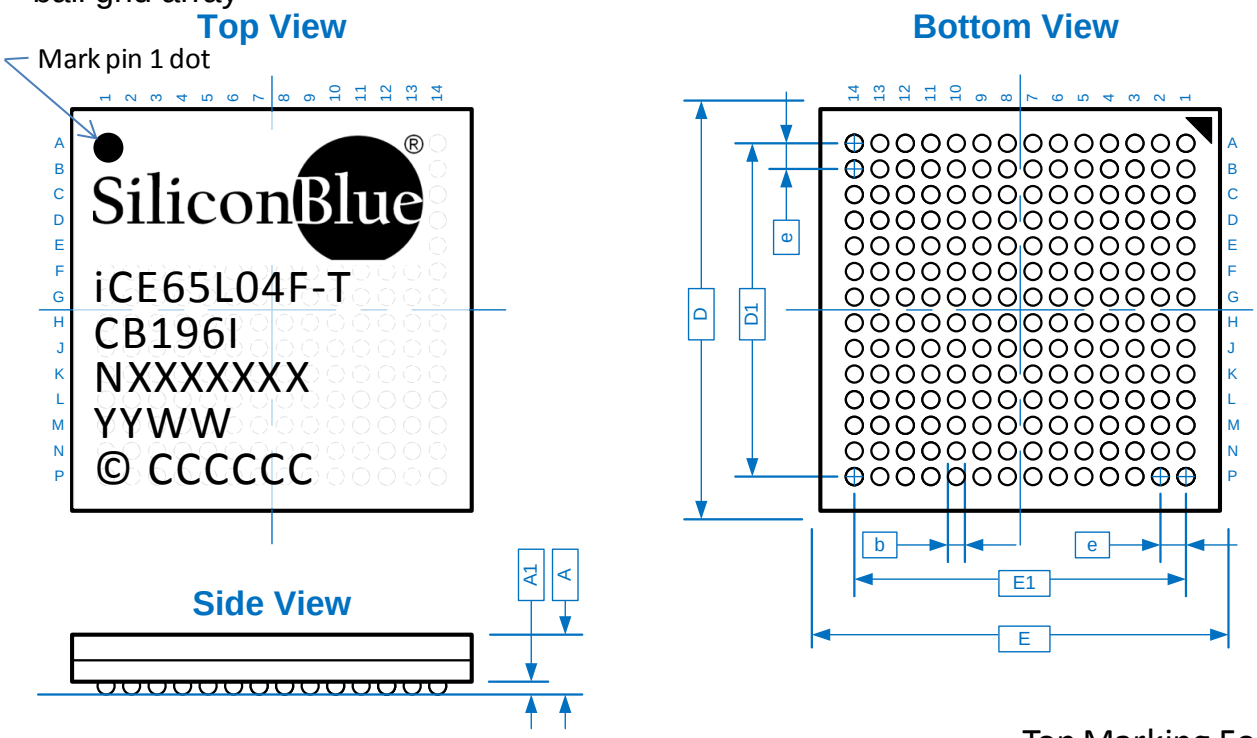
Ball Function	Ball Number	Pin Type	Bank
PIO1	H12	PIO	1
PIO1	J11	PIO	1
PIO1	J12	PIO	1
PIO1	K11	PIO	1
PIO1	K12	PIO	1
PIO1	K14	PIO	1
PIO1	L14	PIO	1
TCK	L12	JTAG	1
TDI	M12	JTAG	1
TDO	N14	JTAG	1
TMS	P14	JTAG	1
TRST_B	M14	JTAG	1
VCCIO_1	F9	VCCIO	1
VCCIO_1	H14	VCCIO	1
CDONE	M10	CONFIG	2
CRESET_B	L10	CONFIG	2
GBIN4/PIO2	P8	GBIN	2
GBIN5/PIO2	P7	GBIN	2
PIO2	L4	PIO	2
PIO2	L5	PIO	2
PIO2	L6	PIO	2
PIO2	L7	PIO	2
PIO2	L8	PIO	2
PIO2	M3	PIO	2
PIO2	M4	PIO	2
PIO2	M6	PIO	2
PIO2	M7	PIO	2
PIO2	M8	PIO	2
PIO2	M9	PIO	2
PIO2	P2	PIO	2
PIO2	P3	PIO	2
PIO2	P4	PIO	2
PIO2	P5	PIO	2
PIO2	P9	PIO	2
PIO2/CBSEL0	L9	PIO	2
PIO2/CBSEL1	P10	PIO	2
VCCIO_2	J9	PIO	2
VCCIO_2	M5	PIO	2
PIO3/DP00A	B1	DPIO	3
PIO3/DP00B	C1	DPIO	3
PIO3/DP01A	C3	DPIO	3
PIO3/DP01B	D3	DPIO	3
PIO3/DP02A	D4	DPIO	3
PIO3/DP02B	E4	DPIO	3
PIO3/DP03A	D1	DPIO	3
PIO3/DP03B	E1	DPIO	3
PIO3/DP04A	F4	DPIO	3
PIO3/DP04B	F3	DPIO	3
L01/L04: GBIN6/PIO3 L08: GBIN6/DP06A	H1	GBIN	3

Ball Function	Ball Number	Pin Type	Bank
L01/L04: GBIN7/PIO3 L08: GBIN7/DP05B	G1	GBIN	3
L01/L04: PIO3/DP05A L08: PIO3/DP05A	G3	DPIO	3
L01/L04: PIO3/DP05B L08: PIO3/DP11B	G4	DPIO	3
L01/L04: PIO3/DP06A L08: PIO3/DP06B	H3	DPIO	3
L01/L04: PIO3/DP06B L08: PIO3/DP11A	H4	DPIO	3
PIO3/DP07A	J3	DPIO	3
PIO3/DP07B	J1	DPIO	3
PIO3/DP08A	K3	DPIO	3
PIO3/DP08B	K4	DPIO	3
PIO3/DP09A	L1	DPIO	3
PIO3/DP09B	M1	DPIO	3
PIO3/DP10A	N1	DPIO	3
PIO3/DP10B	P1	DPIO	3
VCCIO_3	E3	VCCIO	3
VCCIO_3	J6	VCCIO	3
VCCIO_3	K1	VCCIO	3
PIOS/SPI_SO	M11	SPI	SPI
PIOS/SPI_SI	P11	SPI	SPI
PIOS/SPI_SCK	P12	SPI	SPI
PIOS/SPI_SS_B	P13	SPI	SPI
SPI_VCC	L11	SPI	SPI
GND	A9	GND	GND
GND	F1	GND	GND
GND	F7	GND	GND
GND	G7	GND	GND
GND	G8	GND	GND
GND	G9	GND	GND
GND	H6	GND	GND
GND	H7	GND	GND
GND	H8	GND	GND
GND	J8	GND	GND
GND	J14	GND	GND
GND	L3	GND	GND
GND	P6	GND	GND
VCC	F8	VCC	VCC
VCC	G6	VCC	VCC
VCC	H9	VCC	VCC
VCC	J4	VCC	VCC
VCC	J7	VCC	VCC
VPP_2V5	A14	VPP	VPP
VPP_FAST	A13	VPP	VPP

Package Mechanical Drawing

Figure 47:
(a) iCE65L04 CB196 Package Mechanical Drawing

CB196: 8 x8 mm, 196-ball, 0.5 mm ball-pitch, fully-populated, chip-scale ball grid array



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			14		Columns
Number of Ball Rows	Y			14		Rows
Number of Signal Balls		n		196		Balls
Body Size	X	E	7.90	8.00	8.10	mm
	Y	D	7.90	8.00	8.10	
Ball Pitch		e	—	0.50	—	
Ball Diameter		b	0.27	—	0.37	
Edge Ball Center to Center	X	E1	—	6.50	—	
	Y	D1	—	6.50	—	
Package Height		A	—	—	1.00	
Stand Off		A1	0.16	—	0.26	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65L04F	Part number
	-T	Power/Speed
3	CB196I	Package type
	ENG	Engineering
4	NXXXXXXX	Lot Number
5	YYWW	Date Code
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
42	34

Pinout Table

Table 44 provides a detailed pinout table for the two chip-scale BGA packages. Pins are generally arranged by I/O bank, then by ball function. The balls with a black circle (●) are unconnected balls (N.C.) for the iCE65L04 in the CB284 package. The CB132 package fits within the CB284 package footprint as shown in Figure 48. The right-most column shows which CB132 ball corresponds to the CB284.

The table also highlights the differential I/O pairs in I/O Bank 3.

Table 44: iCE65 CB284 Chip-scale BGA Pinout Table (with CB132 cross reference)

Ball Function	Ball Number	Pin Type by Device		Bank	CB132 Ball Equivalent
	iCE65L04 iCE65L08	iCE65L04	iCE65L08		
GBIN0/PIO0	E10	GBIN	GBIN	0	A6
GBIN1/PIO0	E11	GBIN	GBIN	0	A7
PIO0 (●)	A1	N.C.	PIO	0	—
PIO0 (●)	A2	N.C.	PIO	0	—
PIO0 (●)	A3	N.C.	PIO	0	—
PIO0 (●)	A4	N.C.	PIO	0	—
PIO0	A5	PIO	PIO	0	—
PIO0	A6	PIO	PIO	0	—
PIO0	A7	PIO	PIO	0	—
PIO0 (●)	A9	N.C.	PIO	0	—
PIO0 (●)	A10	N.C.	PIO	0	—
PIO0 (●)	A11	N.C.	PIO	0	—
PIO0 (●)	A12	N.C.	PIO	0	—
PIO0 (●)	A13	N.C.	PIO	0	—
PIO0	A15	PIO	PIO	0	—
PIO0	A16	PIO	PIO	0	—
PIO0	A17	PIO	PIO	0	—
PIO0	A18	PIO	PIO	0	—
PIO0 (●)	A14	N.C.	PIO	0	—
PIO0 (●)	A19	N.C.	PIO	0	—
PIO0 (●)	A20	N.C.	PIO	0	—
PIO0	C3	PIO	PIO	0	—
PIO0	C4	PIO	PIO	0	—
PIO0	C5	PIO	PIO	0	—
PIO0	C6	PIO	PIO	0	—
PIO0	C7	PIO	PIO	0	—
PIO0	C9	PIO	PIO	0	—
PIO0	C10	PIO	PIO	0	—
PIO0	C11	PIO	PIO	0	—
PIO0	C13	PIO	PIO	0	—
PIO0	C14	PIO	PIO	0	—
PIO0	C15	PIO	PIO	0	—
PIO0	C16	PIO	PIO	0	—
PIO0	C17	PIO	PIO	0	—
PIO0	C18	PIO	PIO	0	—
PIO0	C19	PIO	PIO	0	—
PIO0	E5	PIO	PIO	0	A1
PIO0	E6	PIO	PIO	0	A2
PIO0	E7	PIO	PIO	0	A3
PIO0	E8	PIO	PIO	0	A4
PIO0	E9	PIO	PIO	0	A5
PIO0	E14	PIO	PIO	0	A10

Ball Function	Ball Number iCE65L04 iCE65L08	Pin Type by Device iCE65L04	Pin Type by Device iCE65L08	Bank	CB132 Ball Equivalent
VCCIO_3	J7	VCCIO	VCCIO	3	E3
VCCIO_3	K3	VCCIO	VCCIO	3	—
VCCIO_3	N10	VCCIO	VCCIO	3	J6
VCCIO_3	P5	VCCIO	VCCIO	3	K1
VCCIO_3	R3	VCCIO	VCCIO	3	—
VREF	M1	VREF	VREF	3	—
PIOS/SPI_SO	T15	SPI	SPI	SPI	M11
PIOS/SPI_SI	V15	SPI	SPI	SPI	P11
PIOS/SPI_SCK	V16	SPI	SPI	SPI	P12
PIOS/SPI_SS_B	V17	SPI	SPI	SPI	P13
SPI_VCC	R15	SPI	SPI	SPI	L11
GND	C12	GND	GND	GND	—
GND	E13	GND	GND	GND	A9
GND	J3	GND	GND	GND	—
GND	K5	GND	GND	GND	F1
GND	K11	GND	GND	GND	F7
GND	L11	GND	GND	GND	G7
GND	L12	GND	GND	GND	G8
GND	L13	GND	GND	GND	G9
GND	M10	GND	GND	GND	H6
GND	M11	GND	GND	GND	H7
GND	M12	GND	GND	GND	H8
GND	N1	GND	GND	GND	—
GND	N12	GND	GND	GND	J8
GND	N18	GND	GND	GND	J14
GND	N20	GND	GND	GND	—
GND	R7	GND	GND	GND	L3
GND	T3	GND	GND	GND	—
GND	V1	GND	GND	GND	—
GND	V10	GND	GND	GND	P6
GND	Y12	GND	GND	GND	—
GND	Y16	GND	GND	GND	—
GND	AB5	GND	GND	GND	—
GND	G1	GND	GND	GND	—
GND	R1	GND	GND	GND	—
VCC	C8	VCC	VCC	VCC	—
VCC	D3	VCC	VCC	VCC	—
VCC	K12	VCC	VCC	VCC	F8
VCC	L10	VCC	VCC	VCC	G6
VCC	L20	VCC	VCC	VCC	—
VCC	M13	VCC	VCC	VCC	H9
VCC	N8	VCC	VCC	VCC	J4
VCC	N11	VCC	VCC	VCC	J7
VCC	Y8	VCC	VCC	VCC	—
VPP_2V5	E18	VPP	VPP	VPP	A14
VPP_FAST	E17	VPP	VPP	VPP	A13

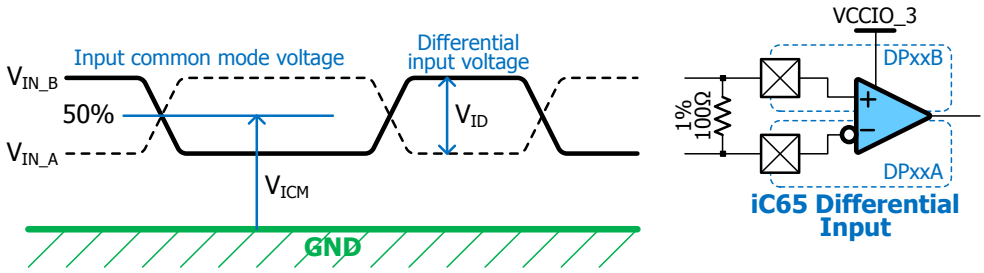
iCE65L04 Pad Name	DiePlus VQ100	CB132	CB196	CB284	Pad	X (µm)	Y (µm)
CRESET_B	44	L10	L10	R14	121	2,625.00	139.20
PIOS_00/SPI_SO	45	M11	M11	T15	122	2,690.00	37.20
PIOS_01/SPI_SI	46	P11	P11	V15	123	2,740.00	139.20
GND	47	—	P6	Y16	124	2,790.00	37.20
PIOS_02/SPI_SCK	48	P12	P12	V16	125	2,840.00	139.20
PIOS_03/SPI_SS_B	49	P13	P13	V17	126	2,890.00	37.20
SPI_VCC	50	L11	L11	R15	127	2,990.00	37.20
TDI	N/A	M12	M12	T16	128	3,610.80	342.00
TMS	N/A	P14	P14	V18	129	3,712.80	392.00
TCK	N/A	L12	L12	R16	130	3,610.80	442.00
TDO	N/A	N14	N14	U18	131	3,712.80	492.00
TRST_B	N/A	M14	M14	T18	132	3,610.80	542.00
PIO1_00	51	L14	K11	R18	133	3,712.80	592.00
PIO1_01	52	K12	L13	P16	134	3,610.80	642.00
PIO1_02	53	K11	K12	P15	135	3,712.80	692.00
PIO1_03	54	K14	M13	P18	136	3,610.80	727.00
GND	55	J14	J14	N18	137	3,712.80	762.00
GND	55	J14	J14	N18	138	3,610.80	797.00
PIO1_04	56	J12	J10	N16	139	3,712.80	832.00
PIO1_05	57	J11	L14	N15	140	3,610.80	867.00
VCCIO_1	58	H14	H14	M18	141	3,712.80	902.00
VCCIO_1	—	—	—	—	142	3,610.80	937.00
PIO1_06	59	H12	J11	M16	143	3,712.80	972.00
PIO1_07	60	H11	K14	M15	144	3,610.80	1,007.00
PIO1_08	—	—	H10	W20	145	3,712.80	1,042.00
PIO1_09	—	—	J13	V20	146	3,610.80	1,077.00
PIO1_10	—	—	J12	U20	147	3,712.80	1,112.00
VCC	61	H9	N7	M13	148	3,610.80	1,147.00
VCC	—	—	—	—	149	3,712.80	1,182.00
PIO1_11	—	—	H13	T22	150	3,610.80	1,217.00
PIO1_12	—	—	H12	R22	151	3,712.80	1,252.00
PIO1_13	—	—	—	P22	152	3,610.80	1,287.00
PIO1_14	—	—	—	N22	153	3,712.80	1,322.00
PIO1_15		—	G13	T20	154	3,610.80	1,357.00
PIO1_16	—	—	H11	R20	155	3,712.80	1,392.00
PIO1_17	—	—	G14	P20	156	3,610.80	1,427.00
GND	—	—	K10	N20	157	3,712.80	1,462.00
GND	—	—	—	—	158	3,610.80	1,497.00
PIO1_18	—	—	G10	M20	159	3,712.80	1,532.00
GBIN3/PIO1_19	62	F14	G12	K18	160	3,610.80	1,567.00
GBIN2/PIO1_20	63	G14	F10	L18	161	3,712.80	1,602.00
PIO1_21	—	—	F14	K20	162	3,610.80	1,637.00
VCCIO_1	—	—	H14	J20	163	3,712.80	1,672.00
VCCIO_1	—	—	—	—	164	3,610.80	1,707.00
PIO1_22	—	—	F13	H20	165	3,712.80	1,742.00
PIO1_23	—	—	D13	G20	166	3,610.80	1,777.00

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO3_20/DP10A	—	H8	39	129.735	2,462.665
PIO3_21/DP10B	—	J8	40	231.735	2,427.665
PIO3_22/DP11A	G1	T1	41	129.735	2,392.665
PIO3_23/DP11B	G2	U1	42	231.735	2,357.665
VCCIO_3	K1	N10	43	129.735	2,322.665
VCCIO_3	—	—	44	231.735	2,287.665
VREF	N/A	M1	45	129.735	2,252.665
VREF	N/A	—	46	231.735	2,217.665
GND	J5	N1	47	129.735	2,182.665
GND	—	—	48	231.735	2,147.665
VCCIO_3	J6	P1	49	129.735	2,112.665
VCCIO_3	—	—	50	231.735	2,077.665
GND	H6	R1	51	129.735	2,042.665
GND	—	—	52	231.735	2,007.665
PIO3_24/DP12A	H4	L3	53	129.735	1,972.665
GBIN7/PIO3_25/DP12B	H3	L5	54	231.735	1,937.665
GND	H7	V1	55	129.735	1,902.665
GBIN6/PIO3_26/DP13A	H1	M5	56	231.735	1,867.665
PIO3_27/DP13B	H2	M3	57	129.735	1,832.665
PIO3_28/DP14A	—	N7	58	231.735	1,798.665
PIO3_29/DP14B	—	N5	59	129.735	1,762.665
PIO3_30/DP15A	J1	N3	60	231.735	1,727.665
PIO3_31/DP15B	J2	P3	61	129.735	1,692.665
GND	J5	M11	62	231.735	1,657.665
GND	—	—	63	129.735	1,622.665
PIO3_32/DP16A	H5	W1	64	231.735	1,587.665
PIO3_33/DP16B	G5	Y1	65	129.735	1,552.665
VCCIO_3	J6	R3	66	231.735	1,517.665
VCCIO_3	—	—	67	129.735	1,482.665
GND	J5	T3	68	231.735	1,447.665
GND	—	—	69	129.735	1,412.665
PIO3_34/DP17A	K2	AA1	70	231.735	1,377.665
PIO3_35/DP17B	J3	AB1	71	129.735	1,342.665
PIO3_36/DP18A	—	L7	72	231.735	1,307.665
PIO3_37/DP18B	—	L8	73	129.735	1,272.665
PIO3_38/DP19A	—	M7	74	231.735	1,237.665
PIO3_39/DP19B	—	M8	75	129.735	1,202.665
PIO3_40/DP20A	L1	P7	76	231.735	1,167.665
PIO3_41/DP20B	L2	P8	77	129.735	1,132.665
VCC	J4	N8	78	231.735	1,097.665
VCC	—	—	79	129.735	1,062.665
PIO3_42/DP21A	K4	R5	80	231.735	1,027.665
PIO3_43/DP21B	K3	T5	81	129.735	992.665
VCCIO_3	K1	P5	82	231.735	957.665
VCCIO_3	—	—	83	129.735	912.665
GND	L3	R7	84	231.735	867.665
GND	—	—	85	129.735	822.67

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
GND	F7	E13	270	3,216.98	4,054.5
GND	—	—	271	3,166.98	4,156.5
PIO0_08	D9	E15	272	3,116.98	4,054.5
PIO0_09	C10	G14	273	3,064.48	4,156.5
PIO0_10	A10	A20	274	3,029.48	4,054.5
PIO0_11	B10	H13	275	2,994.48	4,156.5
PIO0_12	—	A19	276	2,959.48	4,054.5
PIO0_13	E9	G13	277	2,924.48	4,156.5
PIO0_14	—	C16	278	2,889.48	4,054.5
PIO0_15	—	E14	279	2,854.48	4,156.5
VCCIO_0	F6	E12	280	2,819.48	4,054.5
VCCIO_0	—	—	281	2,784.48	4,156.5
PIO0_16	—	A18	282	2,749.48	4,054.5
PIO0_17	—	A17	283	2,714.48	4,156.5
PIO0_18	C9	C15	284	2,679.48	4,054.5
PIO0_19	—	A16	285	2,644.48	4,156.5
PIO0_20	B9	C14	286	2,609.48	4,054.5
PIO0_21	—	H12	287	2,574.48	4,156.5
PIO0_22	D8	A15	288	2,539.48	4,054.5
PIO0_23	C8	H11	289	2,504.48	4,156.5
PIO0_24	E8	C13	290	2,469.48	4,054.5
PIO0_25	—	A14	291	2,434.48	4,156.5
GND	B12	C12	292	2,399.48	4,054.5
GND	—	—	293	2,364.48	4,156.5
PIO0_26	B8	A13	294	2,329.48	4,054.5
PIO0_27	D7	A12	295	2,294.48	4,156.5
PIO0_28	—	C11	296	2,259.48	4,054.5
GBIN1/PIO0_29	E7	E11	297	2,224.48	4,156.5
GBIN0/PIO0_30	A7	E10	298	2,189.48	4,054.5
PIO0_31	—	G12	299	2,154.48	4,156.5
VCCIO_0	A8	A8	300	2,119.48	4,054.5
VCCIO_0	—	—	301	2,084.48	4,156.5
PIO0_32	C7	A11	302	2,049.48	4,054.5
PIO0_33	—	G11	303	2,014.48	4,156.5
PIO0_34	E6	A10	304	1,979.48	4,054.5
PIO0_35	—	C10	305	1,944.48	4,156.5
VCC	B7	C8	306	1,909.48	4,054.5
VCC	—	—	307	1,874.48	4,156.5
PIO0_36	—	A9	308	1,839.48	4,054.5
PIO0_37	A6	A7	309	1,804.48	4,156.5
PIO0_38	B6	C9	310	1,769.48	4,054.5
PIO0_39	A5	A6	311	1,734.48	4,156.5
GND	G7	K11	312	1,699.48	4,054.5
GND	—	—	313	1,664.48	4,156.5
PIO0_40	D6	E9	314	1,629.48	4,054.5
PIO0_41	C6	G10	315	1,594.48	4,156.5

Differential Inputs

Figure 50: Differential Input Specifications



Input common mode voltage: $$V_{ICM} = \frac{VCCIO\_3}{2} \pm \Delta V_{ICM}$$

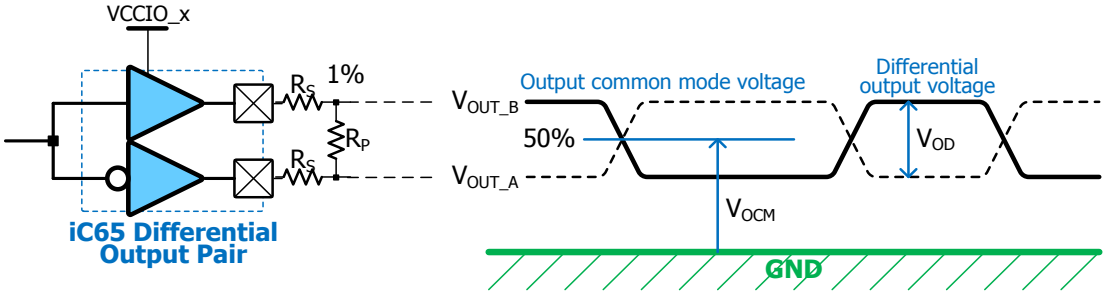
Differential input voltage: $$V_{ID} = |V_{IN\_B} - V_{IN\_A}|$$

Table 52: **Recommended Operating Conditions for Differential Inputs**

I/O Standard	VCCIO_3 (V)			V_{ID} (mV)			V_{ICM} (V)		
	Min	**Nom**	**Max**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
LVDS	2.38	2.50	2.63	250	350	450	$\frac{VCCIO\_3}{2} - 0.30$	$\frac{VCCIO\_3}{2}$	$\frac{VCCIO\_3}{2} + 0.30$
SubLVDS	1.71	1.80	1.89	100	150	200	$\frac{VCCIO\_3}{2} - 0.25$	$\frac{VCCIO\_3}{2}$	$\frac{VCCIO\_3}{2} + 0.25$

Differential Outputs

Figure 51: Differential Output Specifications



Output common mode voltage: $$V_{OCM} = \frac{VCCIO\_x}{2} \pm \Delta V_{OCM}$$

Differential output voltage: $$V_{OD} = |V_{OUT\_B} - V_{OUT\_A}|$$

Table 53: **Recommended Operating Conditions for Differential Outputs**

I/O Standard	VCCIO_x (V)			Ω		V_{OD} (mV)			V_{OCM} (V)		
	Min	**Nom**	**Max**	**R_S**	**R_P**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
LVDS	2.38	2.50	2.63	150	140	300	350	400	$\frac{VCCIO}{2} - 0.15$	$\frac{VCCIO}{2}$	$\frac{VCCIO}{2} + 0.15$
SubLVDS	1.71	1.80	1.89	270	120	100	150	200	$\frac{VCCIO}{2} - 0.10$	$\frac{VCCIO}{2}$	$\frac{VCCIO}{2} + 0.10$

Table 60 provides various timing specifications for the SPI peripheral mode interface.

Table 60: SPI Peripheral Mode Timing

Symbol	From	To	Description		All Grades Min.	All Grades Max.	Units
t_{CR_SCK}	CRESET_B	SPI_SCK	Minimum time from a rising edge on CRESET_B until the first SPI write operation, first SPI_SCK. During this time, the iCE65 FPGA is clearing its internal configuration memory	iC65L01	800	—	µs
				iC65L04	800		
				iC65L08	1200		
$t_{SUSPISI}$	SPI_SI	SPI_SCK	Setup time on SPI_SI before the rising SPI_SCK clock edge		12	—	ns
$t_{HDSPISI}$	SPI_SCK	SPI_SI	Hold time on SPI_SI after the rising SPI_SCK clock edge		12	—	ns
$t_{SPISCKH}$	SPI_SCK	SPI_SCK	SPI_SCK clock High time		20	—	ns
$t_{SPISCKL}$	SPI_SCK	SPI_SCK	SPI_SCK clock Low time		20	—	ns
$t_{SPISCKCYC}$	SPI_SCK	SPI_SCK	SPI_SCK clock period*		40	1,000	ns
F_{SPI_SCK}	SPI_SCK	SPI_SCK	Sustained SPI_SCK clock frequency*		1	25	MHz

* = Applies after sending the synchronization pattern.

Power Consumption Characteristics

Core Power

Table 61 shows the power consumed on the internal VCC supply rail when the device is filled with 16-bit binary counters, measured with a 32.768 kHz and at 32.0 MHz. Low power (-L) at 1.0 V operation and high-performance (-T) version at 1.2V operation is provided.

***Table 61:* VCC Power Consumption for Device Filled with 16-Bit Binary Counters**

Symbol	Description	Grade	VCC	iCE65L01 Typical	iCE65L01 Max.	iCE65L04 Typical	iCE65L04 Max.	iCE65L08 Typical	iCE65L08 Max.	Units
I_{CC0K}	f =0,	-L	1.0V	12		26		54		µA
		-T	1.2V	19		43		90		
I_{CC32K}	f ≤ 32.768 kHz	-L	1.0V	15		31		62		µA
		-T	1.2V	23		50		100		
I_{CC32M}	f = 32.0 MHz	-L	1.0V	3		7		14		mA
		-T	1.2V	4		8		17		

I/O Power

Table 62 provides the static current by I/O bank. The typical current for I/O Banks 0, 1, 2 and the SPI bank is not measurable within the accuracy of the test environment. The PIOs in I/O Bank 3 use different circuitry and dissipate a small amount of static current.

Table 62: I/O Bank Static Current (f = 0 MHz)

Symbol	Description		Typical	Max	Units
I_{CCO_0}	I/O Bank 0	Static current consumption per I/O bank. f = 0 MHz. No PIO pull-up resistors enabled. All inputs grounded. All outputs driving Low.	« 1		µA
I_{CCO_1}	I/O Bank 1		« 1		µA
I_{CCO_2}	I/O Bank 2		« 1		µA
I_{CCO_3}	I/O Bank 3		iCE65L01: « 1 iCE65L04/08: 1.2		µA
I_{CCO_SPI}	SPI Bank		« 1		µA

NOTE: The typical static current for I/O Banks 0, 1, 2, and the SPI bank is less than the accuracy of the device tester.

Power Estimator

To estimate the power consumption for a specific application, please download and use the iCE65 Power Estimator Spreadsheet our use the power estimator built into the iCEcube software.

- iCE65 Power Estimator Spreadsheet